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Isolated Loop Powered Thermocouple Transmitter

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Design Resources

TIDA-00189	Tool Folder
TIDA-00165	Tool Folder
TIDA-00095	Tool Folder
TIPD109	Tool Folder
TIDA-00018	Tool Folder
DAC161P997	Product Folder
MSP430F5172I	Product Folder
TPS71733	Product Folder
SN74LVC125A	Product Folder
TPS60402	Product Folder
ADS1220	Product Folder
TPS7A1601	Product Folder

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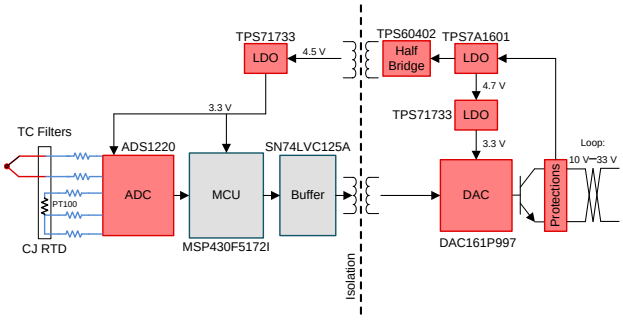
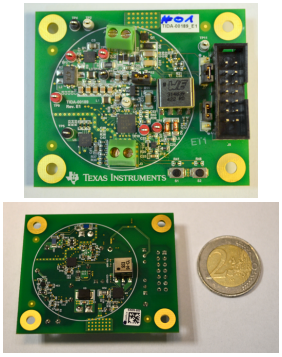
Design Features

- Sensor input compatible with k-Type Thermocouple probes
- Temperature range of the Thermocouple: -200°C to +1375°C
- Operating temperature of the circuit: -40°C to +85°C
- Implements Cold Junction compensation (RTD based)
- Front End accuracy < 0.5°C (-200°C to +270°C) and < 0.15% (270°C to +1375°C)
- 4mA to 20mA current loop output signal
- Output resolution: 0.76µA
- Input power supply range: 10V to 33V DC
- Design to meet IEC 61000-4-5

Featured Applications

- Process Control
- Sensors and Field Transmitters
- Factory Automation
- Portable Instruments





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1 Introduction

Factory automation and Industrial Process Control require monitoring and maintaining process variables at the appropriate levels in order to take decisions and drive actions. A sensor transmitter (highlighted by a dashed line in Figure 1) is either continuously or periodically measuring vital parameters such as temperature and transmitting them from Field Level to the Control Level (to PLC for example).

This specific design focuses on the main challenges of sensing in industrial environments such as conditioning low signal levels in the presence of high noise and high-surge voltage.

A fully isolated power supply and an isolated signal path have been implemented in order to eliminate the effect of ground potential differences (Functional Isolation). The main difference between this design and the RTD Temperature Transmitter for 2-Wire, 4 to 20-mA Current Loop Systems (TIDA-00095) is the use of a Thermocouple front end instead of and RTD and the Isolation barrier. This also complements Temperature Sensor Interface Module PLC (TIDA-00018) and Precision Thermocouple Measurement (TIPD109).

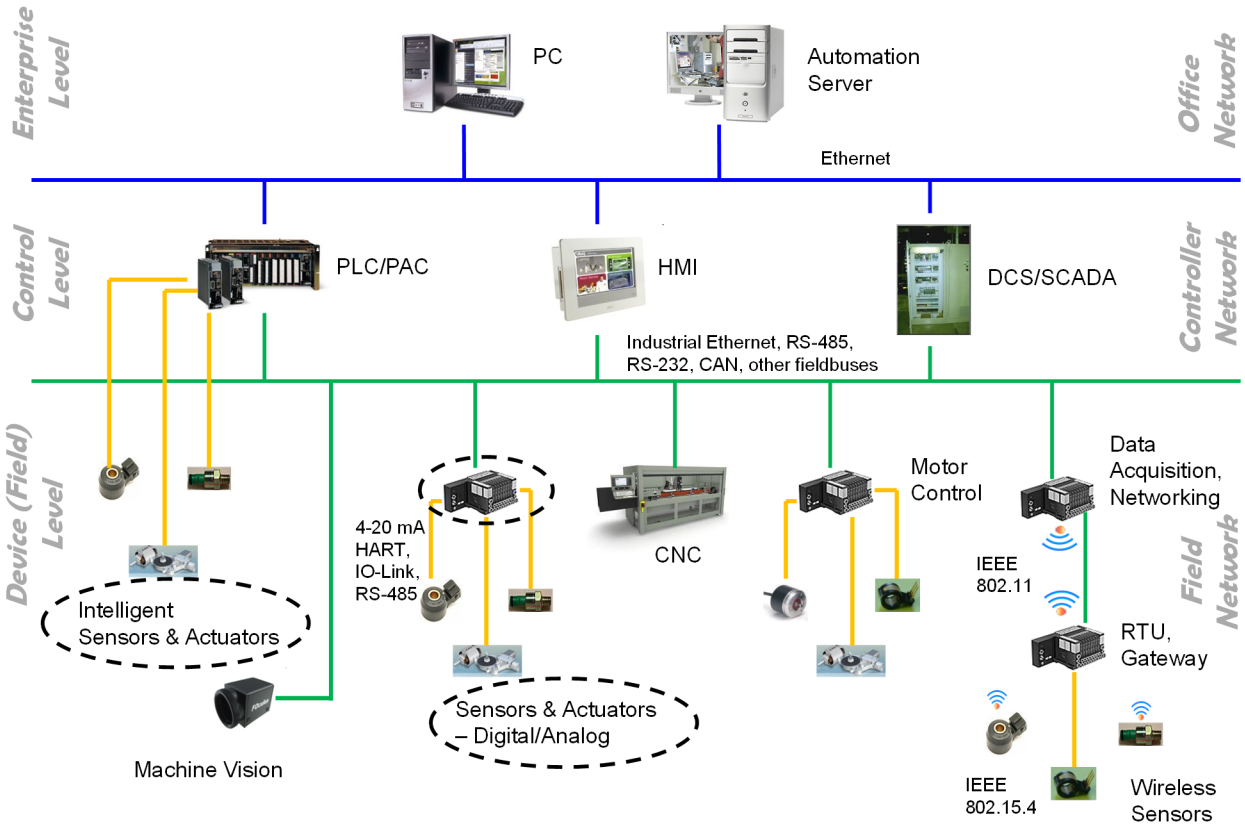


Figure 1. Factory Automation and Process Control Ecosystem

2 Key System Specifications

Parameters	Specifications and Features
Sensor Type	K-type Thermocouple
Temperature Range	-200°C to +1375°C
Output Signal	2-wire 4 to 20mA current loop according to NAMUR NE43
Measurement Type	Thermocouple with RTD based Cold Junction Compensation (pt100)
Power Supply Voltage Range on Loop Interface Terminals	10V to 33V DC
Supply Current Consumption	>3.3mA (To power all the functional blocks of transmitter)
Maximum Load (Including Wiring Resistance)	(Loop Supply Voltage – 10V)/24mA
Error Output Currents	Low: 3.375 mA (typical) High: 21.75 mA (typical)
Reverse Polarity Protection	Yes, on Loop Input
Galvanic Isolation Rating	Functional Isolation
Output Current Resolution	0.76μA
Power Supply Influence on Output	0.3μA
Front End Accuracy- Typical (Excluding sensor errors, at Cold Junction temperature of 25°C, before calibration)	Better than 0.5°C (-200°C to +270°C temperature range) and <0.15% (270°C to +1375°C temperature range)
Front End Accuracy -Maximum (Excluding sensor errors, at Cold Junction temperature of 85°C, before calibration)	Better than 1.2°C (-200°C to +270°C temperature range) and <0.3% (270°C to +1375°C temperature range)
Calibration	Offset and gain calibration for ADC and DAC
Thermocouple Temperature Linearization	–200°C to 1375°C look-up table with 1°C resolution implemented in the MSP430 Firmware to resolve non-linearity
RTD Temperature Linearization	–40°C to 85°C look-up table with 1°C resolution implemented in the MSP430 Firmware to resolve non-linearity
Surge Transient Immunity	Designed to meet IEC 61000-4-5: ±1KV line-line (DM)
Operating Temperature	-40°C to +85°C (temperature of the board including the Cold Junction)
Interface Connector(s)	Two pin TH Terminal Block, 6A, 3.5mm for loop interface Two pin TH Terminal Block, 6A, 3.5mm for sensor interface
Form Factor (diameter)	4cm diameter, circular area for the main electronics

3 System Description

The **Isolated Loop Powered Thermocouple Transmitter** reference design is a system solution providing precision K-type thermocouple measurements for 4 to 20-mA isolated current-loop applications. This design is intended as an evaluation module for users to fast prototype and develop end-products for process-control and factory-automation. Potential challenges with thermocouples as a temperature sensor include tiny voltage outputs, low sensitivity and nonlinearity; in addition, because in industrial environments ground potential differences higher than 100V are common, thermocouple and signal conditioning circuitry must be galvanically isolated. The design files include design considerations, block diagrams, schematics, Bill of Materials (BOM), layer plots, Altium files, Gerber Files, and MSP430 Firmware.

4 Block Diagram

This Reference Design (see block diagram in Figure 2) includes:

- Integrated analog front end
- Isolated power converter
- Isolated data path
- MCU
- Current output DAC

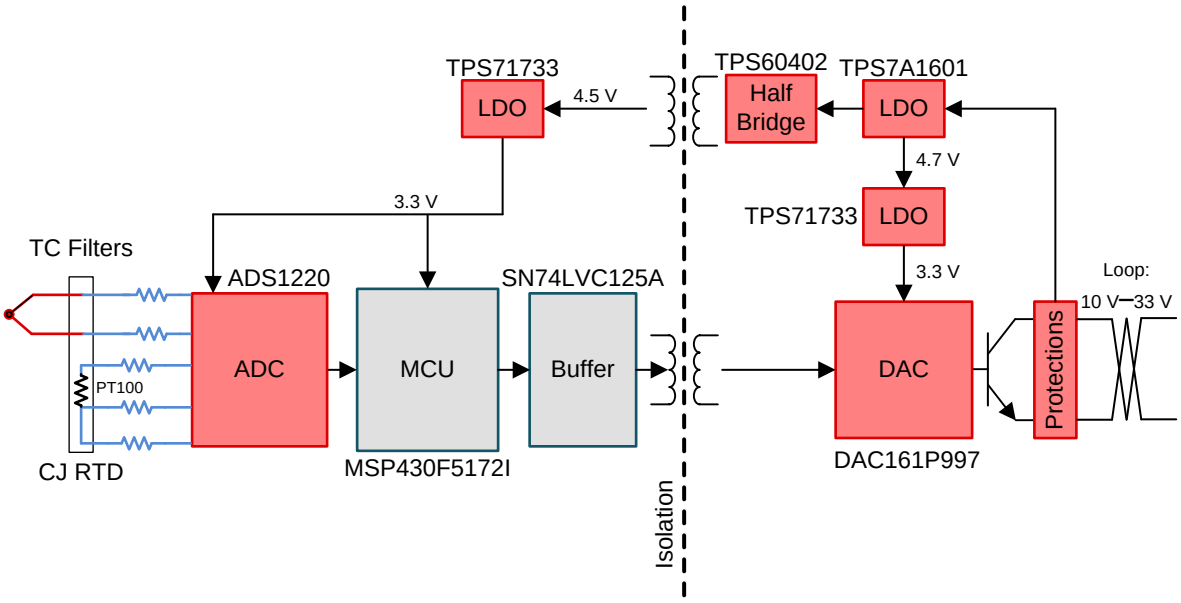


Figure 2. Block Diagram

The front end circuit biases a k-type Thermocouple, filters out of bandwidth noise, reads the generated signal, amplifies it and then converts this signal into a 24-bit digital value. Manufacturers typically provide a look up table of the thermoelectric voltage in Millivolts; the temperature can be determinate by using a lookup table implemented in the Firmware running on the MCU. To generate a meaningful Temperature measure, the system also monitors the temperature of the parasitic junction at the point where the sensor is connected on the PCB (cold junction). This design uses an RTD (pt100) as an auxiliary cold junction sensor mounted really close to the thermocouple connector. The firmware running on the processor uses this reference temperature to determine the voltage error at the Thermocouple output (again based on the previously mentioned look up tables) and translate it into temperature. The final result is the measured absolute temperature at the Thermocouple far end. The processor is also taking care of full system calibration routine and data transmission. The digital value of this absolute temperature is then transferred across the functional isolation barrier to the 4-20mA interface. The DAC translate the temperature information into and analog current signal for robust data transmission over a cable in a noisy industrial environment (standard 4-20mA transmission). The signal path isolation uses a single wire interface (SWIF) and is implemented by driving a simple transformer. This solution optimizes the power consumption and cost of the system. The Temperature transmitter is a 2 wires system so it is completely powered by the 4-20mA loop itself. As a result the power supply circuit has to convert the loop voltage to the right voltage to all the blocks before and after the isolation barrier. An isolated half bridge configuration has been implemented to provide this function and to guarantee sufficient efficiency also at very small power ranges (few 10s of mW).

5 System Theory

5.1 Thermocouple Fundamentals – "Back to Basics"

A simple metal bar produces a voltage when there is temperature difference between the two ends, see Figure 3. The electrons at the hot end are more thermally agitated than the electrons at the cooler end. These more thermally agitated electrons on the hot end begin to diffuse towards the cooler end. This redistribution of electrons creates a negative charge at cooler end and equal positive charge at the hot end. This produces an electrostatic voltage between the two ends. The open circuit voltage thus produced is called as " ***Seebeck Voltage*** " and this phenomenon is called as " **Seebeck Effect"** as it was first discovered by German scientist Thomas Johann Seebeck in 1821. Direct measurement of Seebeck voltage of a single metal bar is impossible. Another similar metal bar will also produce the same Seebeck voltage cancelling each other and results in 0V at the measuring point. But a single wire does not form as thermocouple. A thermocouple is formed when two dissimilar metals are bonded together electrically to form two junctions as shown in Figure 4.

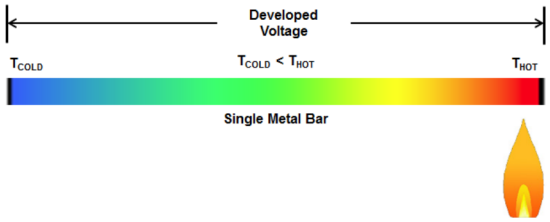


Figure 3. Voltage Developed Due to Temperature Gradient

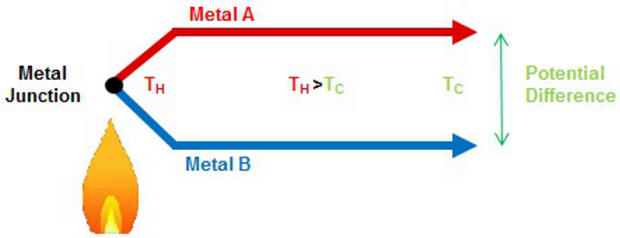


Figure 4. Thermocouple

The magnitude and direction of open circuit voltage developed between the two ends is proportional to the temperature difference.

$$\Delta V = S \times (T_{HOT} - T_{COLD})$$

Where, S is the **Seebeck coefficient** or **thermoelectric sensitivity.** When designing with thermocouples, it is important to understand that thermocouples are bipolar, which means they can produce a positive or a negative voltage depending on whether or not the measured temperature is higher or lower than the system temperature, respectively.

The most misunderstood and very important point about the thermocouple is that virtually no voltage is developed at the junction. Junction is basically an electrical bond between two metals just to complete the circuit so that current flow can take place. Voltage is developed across each wire as temperature changes. The voltage difference is observed at the measuring end because two dissimilar metals have different Seebeck coefficients.

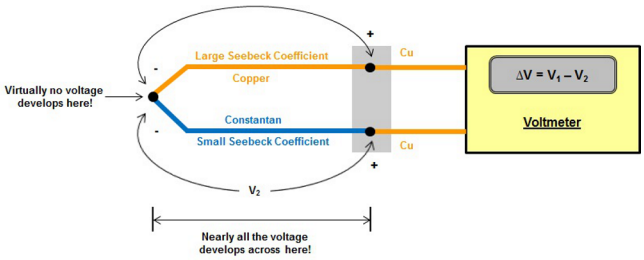


Figure 5. Thermocouple and Developed Voltage

Depending on the required temperature range, vibration resistance, chemical resistance, response time, installation and equipment requirements, the user may choose the appropriate thermocouple. Thermocouples are available in different combinations of metals and/or calibrations as given in Table 1.

Table 1. Types of Thermocouple

Type	Type E	Type K	Type J	Type R	Type S	Type T
Junction Material	Nickel -10% Chromium Vs Constantan	Nickel -10% Chromium Vs Nickel -5% Aluminum Silicon	Iron Constantan	Platinum -13% Rhodium Vs Platinum (-)	Platinum -10% Rhodium Vs Platinum (-)	Copper Constantan
Seebeck Coefficient @20°C	62µV/C°	40µV/°C	62µV/C°	7µV/C°	7µV/C°	40µV/C°
Temperature Range	-100°C to 1000°C	0°C to 1370°C	0°C to 760°C	0°C to 1450°C	0°C to 1750°C	-160°C to 400°C
General Application	Cryogenic use; non-magnetic use	General Purpose	Higher Sensitivity	High resistance to oxidation and corrosion, calibration purposes	Standard for calibration for the melting point of gold	Often used in differential measurements

5.2 Thermocouple Sensitivity and Linearity

Each thermocouple sensor has its own sensitivity (µV/C°), a temperature range, and a non-linear voltage curve over that temperature range depending on its metals and/or calibration type. Thermocouple voltage curves are non-linear over their operating temperature ranges, as can be seen in Figure 6.

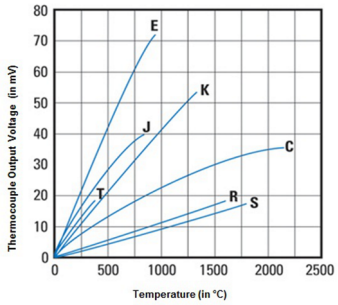
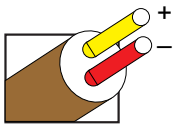


Figure 6. Thermocouple Output as Function of Temperature

This is then valid also for the K-Type used in this design.

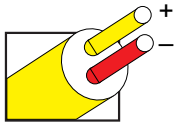
The sensitivity values of a K-type is between 39μV/°C and 41μV/°C, depending on the temperature range. As shown in Figure 7, the non-linearity can be expressed using a simple **look up table** provided by the sensor manufacturer.

MAXIMUM TEMPERATURE RANGE
Thermocouple Grade
– 328 to 2282°F
– 200 to 1250°C
Extension Grade
32 to 392°F
0 to 200°C
LIMITS OF ERROR
(whichever is greater)
Standard:2.2°C or 0.75% Above 0°C
2.2°C or 2.0% Below 0°C
Special:1.1°C or 0.4%
COMMENTS, BARE WIRE ENVIRONMENT:
Clean Oxidizing and Inert; Limited Use in Vacuum or Reducing; Wide Temperature Range; Most Popular Calibration
TEMPERATURE IN DEGREES °C
REFERENCE JUNCTION AT 0°C



Thermocouple Grade

Nickel-Chromium vs. Nickel-Aluminum



Extension Grade

Revised Thermocouple Reference Tables

TYPE K
Reference Tables
N.I.S.T. Monograph 175
Revised to ITS-90

Thermoelectric Voltage in Millivolts

°C	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	°C
												250
												260
												270
-260	-6.458	-6.457	-6.456	-6.455	-6.453	-6.452	-6.450	-6.448	-6.446	-6.444	-6.441	-260
-250	-6.441	-6.438	-6.435	-6.432	-6.429	-6.425	-6.421	-6.417	-6.413	-6.408	-6.404	-250
-240	-6.404	-6.399	-6.393	-6.388	-6.382	-6.377	-6.370	-6.364	-6.358	-6.351	-6.344	-240
-230	-6.344	-6.337	-6.329	-6.322	-6.314	-6.306	-6.297	-6.289	-6.280	-6.271	-6.262	-230
-220	-6.262	-6.252	-6.243	-6.233	-6.223	-6.213	-6.202	-6.192	-6.181	-6.170	-6.158	-220
-210	-6.158	-6.147	-6.135	-6.123	-6.111	-6.099	-6.087	-6.074	-6.061	-6.048	-6.035	-210
-200	-6.035	-6.021	-6.007	-5.994	-5.980	-5.965	-5.951	-5.936	-5.922	-5.907	-5.891	-200
-190	-5.891	-5.876	-5.861	-5.845	-5.829	-5.813	-5.797	-5.780	-5.763	-5.747	-5.730	-190
-180	-5.730	-5.713	-5.695	-5.678	-5.660	-5.642	-5.624	-5.606	-5.588	-5.569	-5.550	-180
-170	-5.550	-5.531	-5.512	-5.493	-5.474	-5.454	-5.435	-5.415	-5.395	-5.374	-5.354	-170
-160	-5.354	-5.333	-5.313	-5.292	-5.271	-5.250	-5.228	-5.207	-5.185	-5.163	-5.141	-160
-150	-5.141	-5.119	-5.097	-5.074	-5.052	-5.029	-5.006	-4.983	-4.960	-4.936	-4.913	-150

°C	0	1	2	3	4	5	6	7	8	9	10	°C
250	10.153	10.194	10.235	10.276	10.316	10.357	10.398	10.439	10.480	10.520	10.561	250
260	10.561	10.602	10.643	10.684	10.725	10.766	10.807	10.848	10.889	10.930	10.971	260
270	10.971	11.012	11.053	11.094	11.135	11.176	11.217	11.259	11.300	11.341	11.382	270
280	11.382	11.423	11.465	11.506	11.547	11.588	11.630	11.671	11.712	11.753	11.795	280
290	11.795	11.836	11.877	11.919	11.960	12.001	12.043	12.084	12.126	12.167	12.209	290
300	12.209	12.250	12.291	12.333	12.374	12.416	12.457	12.499	12.540	12.582	12.624	300
310	12.624	12.665	12.707	12.748	12.790	12.831	12.873	12.915	12.956	12.998	13.040	310
320	13.040	13.081	13.123	13.165	13.206	13.248	13.290	13.331	13.373	13.415	13.457	320
330	13.457	13.498	13.540	13.582	13.624	13.665	13.707	13.749	13.791	13.833	13.874	330
340	13.874	13.916	13.958	14.000	14.042	14.084	14.126	14.167	14.209	14.251	14.293	340
350	14.293	14.335	14.377	14.419	14.461	14.503	14.545	14.587	14.629	14.671	14.713	350
360	14.713	14.755	14.797	14.839	14.881	14.923	14.965	15.007	15.049	15.091	15.133	360
370	15.133	15.175	15.217	15.259	15.301	15.343	15.385	15.427	15.469	15.511	15.554	370
380	15.554	15.596	15.638	15.680	15.722	15.764	15.806	15.849	15.891	15.933	15.975	380
390	15.975	16.017	16.059	16.102	16.144	16.186	16.228	16.270	16.313	16.355	16.397	390

Figure 7. Look Up Table for a K-Type Thermocouple

Another way to express the relation between temperature and voltage is **the complete polynomial formula** . Direct Polynomials provide the thermoelectric voltage (μV) from a known temperature (°C); Inverse Polynomials provide the temperature (°C) from a known thermoelectric voltage (μV). See Figure 8.

NOTE: Considering the manufacturing limitations of the Type K thermocouple (mainly related to the purity of materials), the initial error of the Thermocouple sensor (tolerance class 1) is typically **smaller than 1.5°C between -200°C and 375°C and then better than 0.4% up to 1375°C (maximum thermocouple temperature range).**

Type K Thermocouples - coefficients α_0, α_1 and α_i, of reference equations giving the thermoelectric voltage, *E*, as a function of temperature, t_{90} for the indicated temperature ranges. The equation below 0°C is of the form:

$$E = \sum_{i=0}^{n} c_i (t_{90})^i$$

the equation above 0°C is of the form:

$$E = \sum_{i=0}^{n} c_i (t_{90})^i + \alpha_0 e^{\alpha_1 (t_{90} - 126.9686)^2}$$

where *e* is the natural logarithm constant, *E* is in microvolts and t_{90} is in degrees Celsius.

Temperature Range:	Coefficients
-270 to 0°C	c_0 = 0.000 000 000 0 .... c_1 = 3.945 012 802 5 x 10^{1} c_2 = 2.362 237 359 8 x 10^{-2} c_3 = -3.285 890 678 4 x 10^{-4} c_4 = -4.990 482 877 7 x 10^{-6} c_5 = -6.750 905 917 3 x 10^{-8} c_6 = -5.741 032 742 8 x 10^{-10} c_7 = -3.108 887 289 4 x 10^{-12} c_8 = -1.045 160 936 5 x 10^{-14} c_9 = -1.988 926 687 8 x 10^{-17} c_{10} = -1.632 269 748 6 x 10^{-20}
0 to 1372°C	c_0 = -1.760 041 368 6 x 10^{1} c_1 = 3.892 120 497 5 x 10^{1} c_2 = 1.855 877 003 2 x 10^{-2} c_3 = -9.945 759 287 4 x 10^{-5} c_4 = 3.184 094 571 9 x 10^{-7} c_5 = -5.607 284 488 9 x 10^{-10} c_6 = 5.607 505 905 9 x 10^{-13} c_7 = -3.202 072 000 3 x 10^{-16} c_8 = 9.715 114 715 2 x 10^{-20} c_9 = -1.210 472 127 5 x 10^{-23} α_0 = 1.185 976 x 10^{2} α_1 = -1.183 432 x 10^{-4}

Type K Thermocouples - coefficients of approximate inverse functions giving temperature, t_{90}, as a function of the thermoelectric voltage, *E*, in selected temperature and voltage ranges. The functions are of the form:

$$t_{90} = c_o + c_1 E + c_2 E^2 \quad c_i E^i$$

where *E* is in microvolts and t_{90} is in degrees Celsius.

Temperature Range:	-200 to 0°C	0 to 500°C	500 to 1,372°C
Voltage Range:	-5891 to 0 ∝V	0 to 20,644 ∝V	20,644 to 54,886 ∝V
c_0 = c_1 = c_2 = c_3 = c_4 = c_5 = c_6 = c_7 = c_8 = c_9 =	0.000 000 0 .... 2.517 346 2 x 10^{-2} -1.166 287 8 x 10^{-6} -1.083 363 8 x 10^{-9} -8.977 354 0 x 10^{-13} -3.734 237 7 x 10^{-16} -8.663 264 3 x 10^{-20} -1.045 059 8 x 10^{-23} -5.192 057 7 x 10^{-28}	0.000 000 .... 2.508 355 x 10^{-2} 7.860 106 x 10^{-8} -2.503 131 x 10^{-10} 8.315 270 x 10^{-14} -1.228 034 x 10^{-17} 9.804 036 x 10^{-22} -4.413 030 x 10^{-26} 1.057 734 x 10^{-30} -1.052 755 x 10^{-35}	-1.318 058 x 10^{2} 4.830 222 x 10^{-2} -1.646 031 x 10^{-6} 5.464 731 x 10^{-11} -9.650 715 x 10^{-16} 8.802 193 x 10^{-21} -3.110 810 x 10^{-26}
Error Range:	0.04°C to -0.02°C	0.04°C to -0.05°C	0.06°C to -0.05°C

Adapted from NIST Monograph 175, *Temperature-Electromotive Force Reference Functions and Tables for the Letter-Designated Thermocouple Types Based on the ITS-90,* by G.W. Burns, M.G. Scroger, G.F. Strouse, M.C. Croarkin, and W.F. Guthrie, 1993. Not copyrightable in the United States.

Figure 8. Direct Polynomials and Inverse Polynomials for a K-Type Thermocouple

5.3 Cold Junction Compensation (CJC)

Thermocouple measures the temperature difference between hot and cold junctions. They do not measure the absolute temperature at one junction as illustrated in Figure 9. The cold junction sometimes also referred to as reference junction.

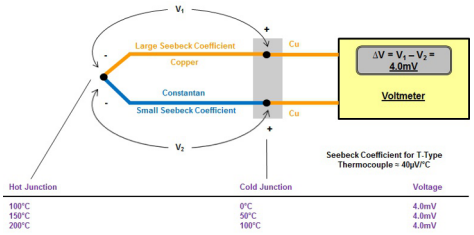


Figure 9. Simplified View of Cold Junction Compensation

The voltmeter measures the same voltage for all three example cases where 100°C temperature difference between hot and cold junctions always generates 4.0mV. Connecting voltmeter in order to measure the thermocouple output creates one more junction J2. This junction also creates a small voltage and the difference between the two voltages is what is measured by the voltmeter. Figure 10 shows a unique case of T-Type thermocouple just for simplicity where copper-to-copper connection does not form another junction. But when thermocouples other than T-Type are employed, two parasitic or unwanted

thermocouples are created with leads at the meter connection. In the PCB, these unwanted thermocouples are one of the biggest concerns, each dissimilar metal connection creates a new thermocouple as one proceeds from measuring end to wire connector, to solder, to copper PCB trace, to IC pin, to bonding wire and to chip/die contact. However, if the signal is differential, and each of the thermocouple pairs are at the same temperature, then the thermocouple voltages will cancel and have no net effect on the measurement. Therefore, the net voltage error added by these connections is zero.

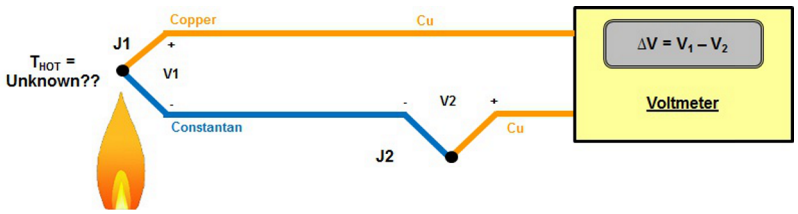


Figure 10. Unwanted Thermocouple Junction

Let's find out what is required to know the temperature (T_{HOT}) of measuring junction J1.

$$T_{HOT} = (\Delta V/S) + T_{COLD}$$

From the above equation, it is evident that to find out the temperature of hot junction of a thermocouple requires the temperature of the cold junction to be known. Classically, cold junction of a thermocouple is kept in an ice bath as shown in Figure 11 to keep it at a known reference temperature of 0°C (another reason it is called as cold junction). In reality, it is impractical and inconvenient in most applications to provide a true ice point reference. The National Institute of Standards and Technology (NIST) thermocouple reference tables also assumes that the cold junction at 0°C.

For example, if a T-Type thermocouple produces an open circuit voltage of 3.4mV with its cold junction reference temperature maintained at 0°C. What would be the temperature of its hot junction? Assume, Seebeck coefficient of T-Type thermocouple is 40µV/°C.

$$T_{HOT} = (3.4mV/(40\mu V/°C)) + 0°C = 85°C$$

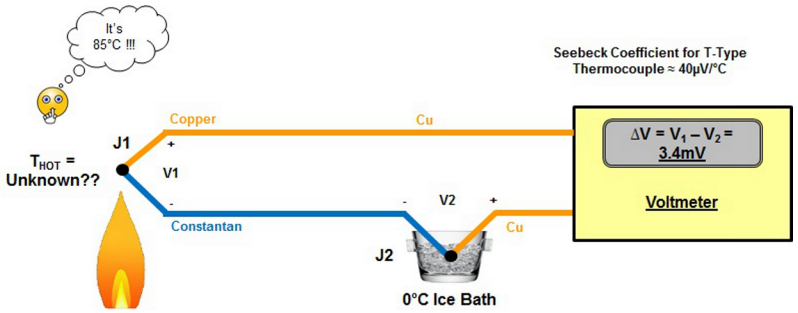


Figure 11. Measuring Absolute Temperature Using 0°C Ice Bath

Due to this fact in order to determine the correct absolute temperature at the measuring junction, it is necessary to know the cold junction reference temperature. An additional measurement becomes mandatory to know the cold junction reference temperature. The more practical and logical approach is to use some other type of direct-reading temperature sensor means capable of absolute, not relative measurement like RTD, Thermistor or Sensor IC to measure the temperature at the reference junction and then use it to compute the temperature at measuring junction of thermocouple. This technique is called **Cold Junction Compensation (CJC)**. In this design, an RTD is used for the compensation.

5.4 RTD Overview

A resistance temperature detector (RTD) is a sensing element made of a metal with predictable resistance characteristics over temperature. The temperature of an RTD is therefore calculated by measuring the resistance. RTD sensors offer wide temperature ranges, good linearity, excellent long-term stability and repeatability which make RTD sensors suitable for many precision applications.

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC, which converts the voltage into a digital output code that can be used to calculate the RTD resistance. A much simplified circuit for RTD measurement application is shown in Figure 12.

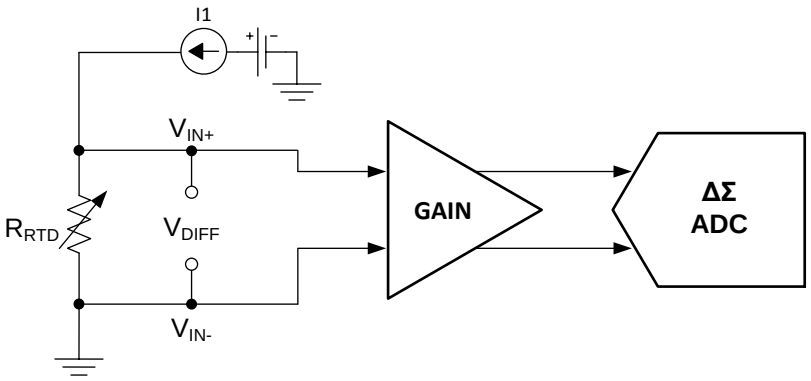


Figure 12. Simplified RTD Application Circuit

The basic principal for RTD operation is that all the metals have positive change in resistance with increase in temperature. Metals having high resistivity, high melting point and high corrosion resistance are generally preferred for making RTDs and allow using less amount of material to achieve high nominal resistance value. By far, platinum is the best material for RTDs because of its high resistivity and long term stability. It follows a very linear resistance-temperature relationship compared to other metals. As a noble metal (chemically inert), platinum is less susceptible to contamination and becomes one of the leading choice for temperature measurement application. The PT100 RTD has an impedance of 100Ω at 0°C and approximately 0.385Ω of resistance change per 1°C change in temperature. This impedance results in 18.52Ω at –200°C and 390.481Ω at 850°C. However, Higher-valued RTDs such as PT200, PT500 or PT1000 can be used for increased sensitivity and resolution at small extra cost.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long term stability. A Class-A RTD has less than 0.5°C of error at 100°C without calibration and the long-term stability makes accurate infrequent calibration possible. Table 2 displays the tolerance, initial accuracy, and resulting error at 100°C for the five main classes of RTDs.

Table 2. RTD Class Tolerance Information

Tolerance Class (DIN-IEC 60751)	Tolerance Values (°C)	Resistance at 0°C (Ω)	Error at 100°C (°C)
AAA[1]	± (0.03 + 0.0005 × T)	100 ± 0.012	± 0.08
AA	± (0.01 + 0.0017 × T)	100 ± 0.04	± 0.27
A	± (0.15 + 0.002 × T)	100 ± 0.06	± 0.35
B	± (0.3 + 0.005 × T)	100 ± 0.12	± 0.8
C	± (0.6 + 0.01 × T)	100 ± 0.24	± 1.6

(1) AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

The relationship between the resistance and temperature of platinum RTD is defined by a non-linear mathematical model known as Callendar-Van Dusen (CVD) equations. The coefficients in the Callendar-Van Dusen equations are defined by the IEC-60751 standard.

For T > 0°C, the CVD equation is a second-order polynomial as:

$$RTD\ (T) = R_0 \times [1 + A(T) + B(T)^2]$$

For T < 0°C, the CVD equation expands to a fourth-order polynomial as:

$$RTD\ (T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3\ (T - 100)]$$

Linear approximation model is:

$$RTD\ (T) = R_0 \times [1 + \alpha(T)]$$

Where:

T = Temperature of RTD element in °C

RTD (T) = resistance of RTD element as a function of temperature

R_0 is the resistance of the RTD element at 0°C

α = Sensitivity of RTD element = 0.00385Ω/Ω/°C

$A = 3.9083 \times 10^{-3}\ °C^{-1}$

$B = -5.7750 \times 10^{-7}\ °C^{-2}$

$C = -4.1830 \times 10^{-12}\ °C^{-4}$

The behavior of resistance for PT100 RTD from –200°C to 850°C is shown in Figure 13.

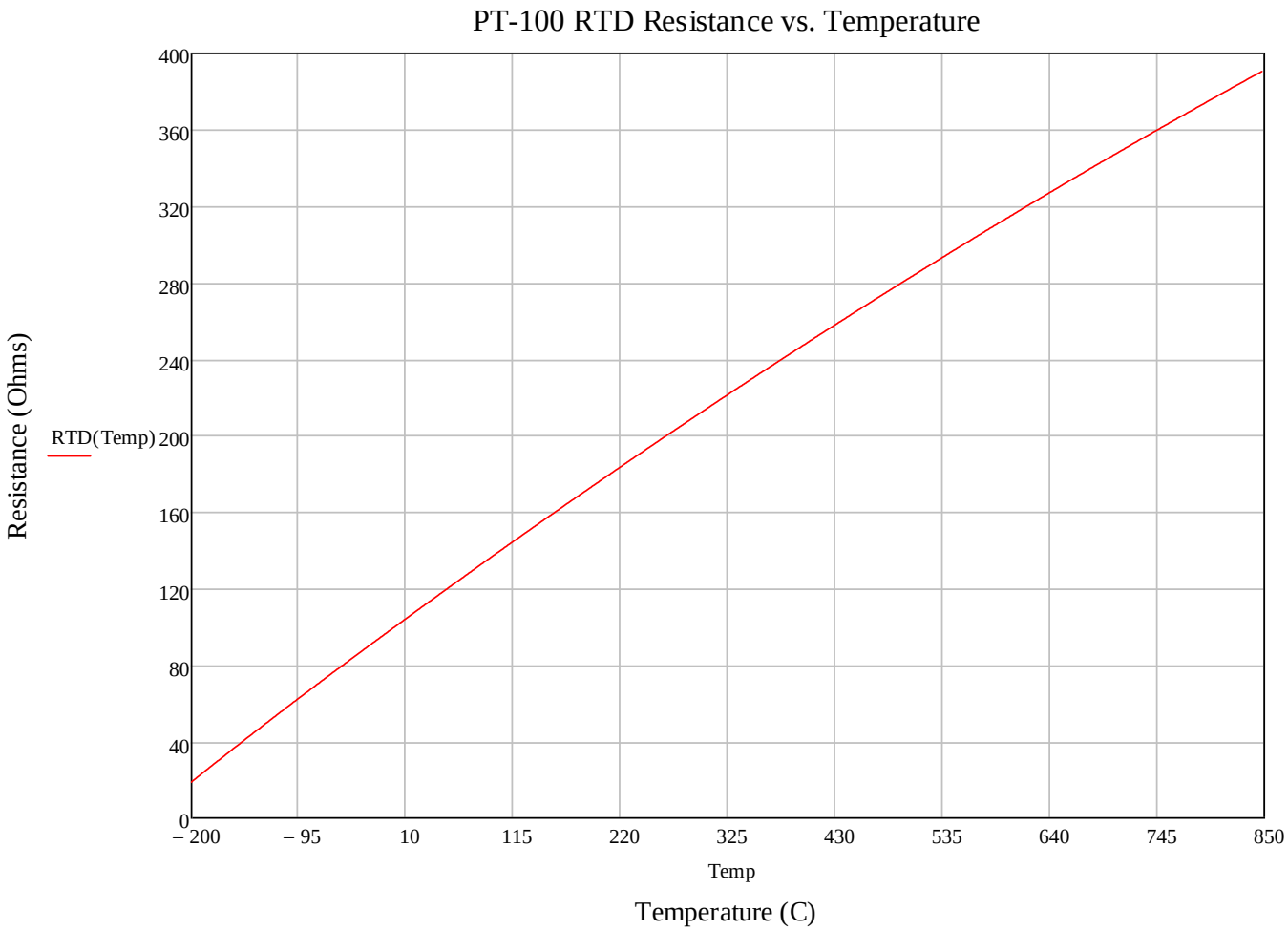


Figure 13. RTD Resistance and Linear Fit Line Versus Temperature

The change in RTD resistance is piecewise linear over small temperature ranges. An end point curve fitting shows RTDs have second-order non-linearity of approximately 0.375% as shown in Figure 14. So, it is necessary to implement digital linearization technique to correct this non-linearity error. Table 3 compares three digital linearization techniques.

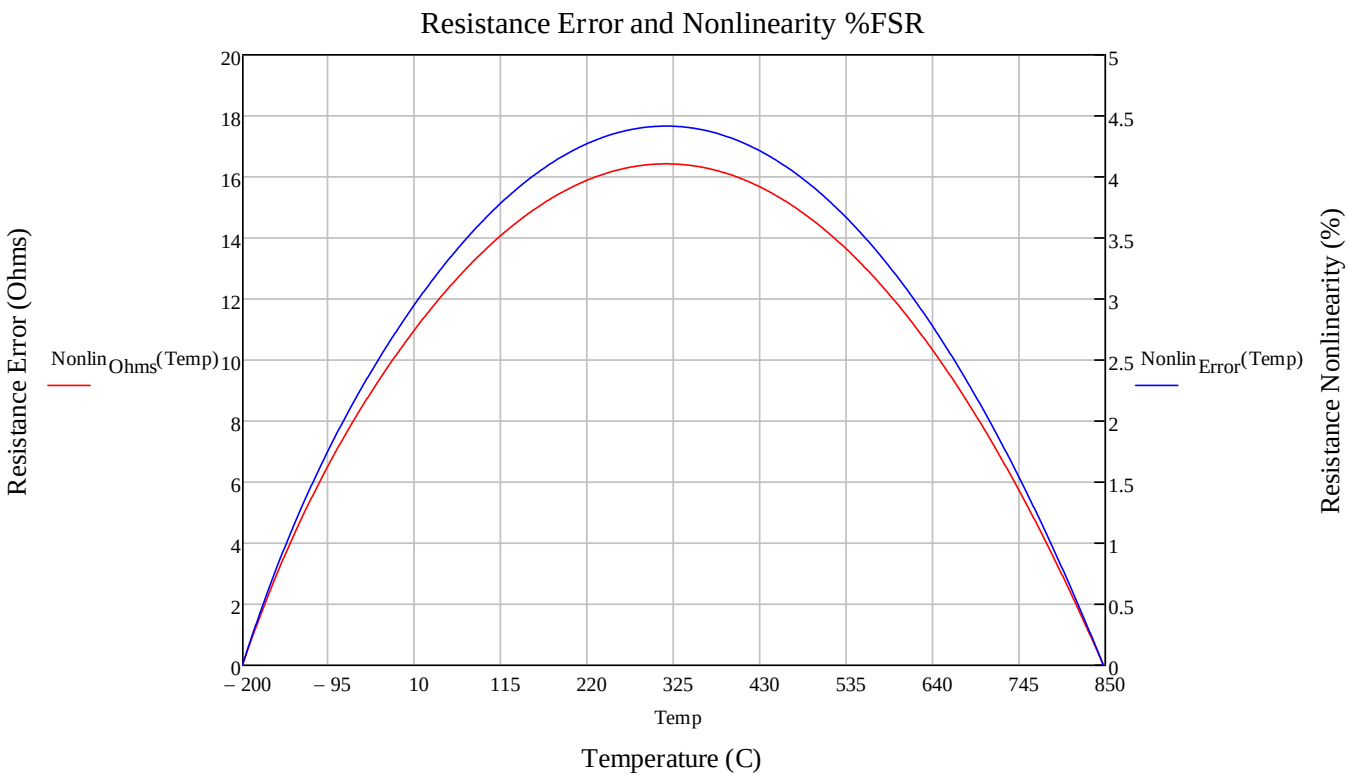


Figure 14. PT100 RTD Non-Linearity from –200°C to 850°C

Table 3. Comparison of Linear Approximation Methods

Method	Advantage	Disadvantage	Other Remarks
Simple Linear Approximation	Easy to implement Fast execution Accurate over small temperature ranges Smaller code size	Least accurate over wide temperature range	Simple method when memory size is limited and temperature range is smaller
Piecewise Linear Approximation	Accuracy depends on the entries in the look-up table Fast execution	High accuracy more entries in look-up table bigger code size	Most practical method implement by most of the embedded systems
Callendar-Van Dusen Equation	Most accurate	Extremely processor Intensive Time consuming Requires square root and power functions on the processor	Not practical in most applications

In this reference design, a look-up table for the PT100 RTD with a resolution of 1°C is used for linear interpolation. The RTD value is computed after offset and gain calibration. Then, this RTD value is used in linear interpolation of the line segment involving two surrounding points in the PT100 RTD look-up table. If additional accuracy is desired, a table with more points with less than 1°C or more accurate curve fit can be stored as a look-up reference table.

5.5 Galvanic Isolation Basic Principle

In various applications multiple grounds are used to lower the impedance of the path between the circuit and the actual ground or simply because it's impossible to have an ideal connection between the respective grounds of two circuits that have to exchange signals; this, however, creates ground loops as shown in Figure 15.

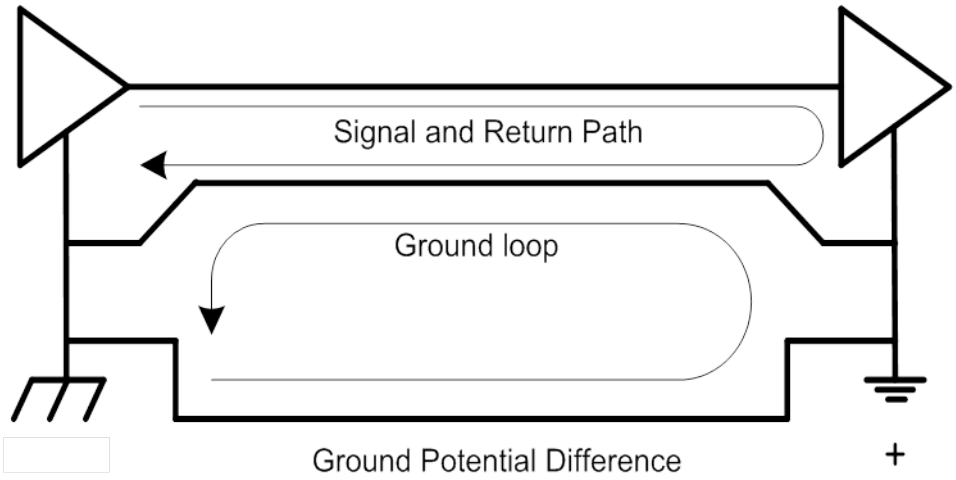


Figure 15. Ground Loops in Presence of Different Ground Potentials

Multiple ground paths may lead to unintended equalization current and can create big common mode differences in the transmission. There are multitudinous options to break these loops but except for galvanic isolation, all solutions are only suitable up to a couple of volts potential difference. Considering that in industrial environments ground potential differences higher than 100V are common, thermocouple and signal conditioning circuitry must be galvanically isolated (Functional isolation) as explained in Figure 16.

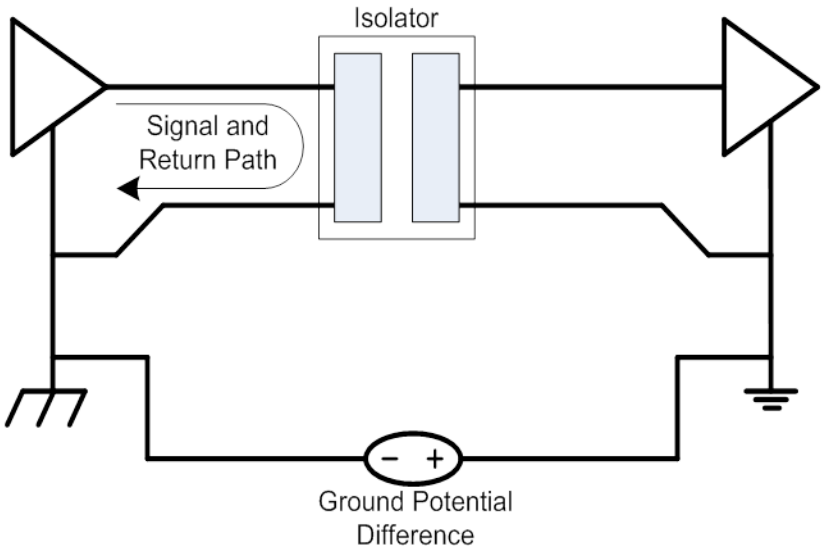


Figure 16. Galvanic Isolation Breaks Ground Loops

Galvanic isolation makes the input, which is referenced to the first ground, independent from the ground of the receiver. As a result the common mode rejection is significantly enhanced. This implies that also the power line has to cross an isolation barrier.

Referring to Figure 17, Circuit 1 and Circuit 2 exchange signals, but no current (electrons) pass from Circuit 1 to Circuit 2. In this case the two circuits are defined galvanically isolated.

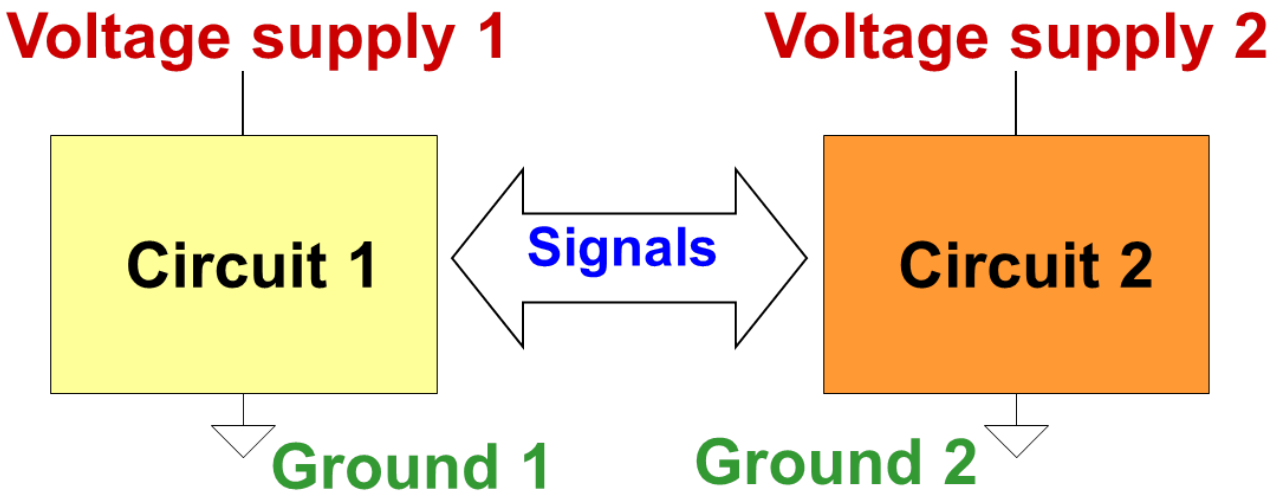


Figure 17. Definition of Galvanic Isolation

5.6 The 4 to 20mA Current Loop – At a Glance

A typical current loop system basically consists of four components, as shown in Figure 18:

1. Sensor (in this case, RTD temperature sensor)
2. **4mA to 20mA Current Loop Sensor Transmitter**
3. Loop Power Supply
4. Loop Receiver

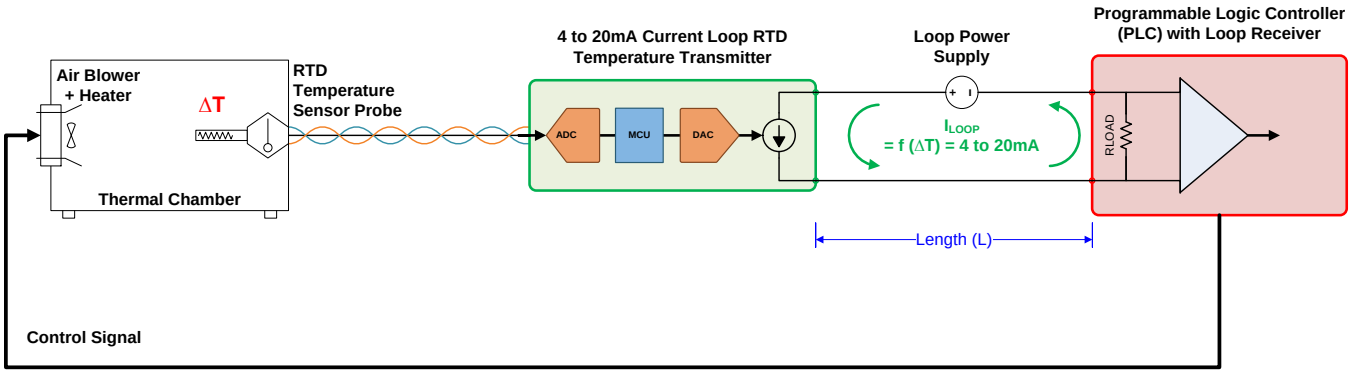


Figure 18. Typical Block Diagram of a Current Loop System

The sensor converts a physical parameter (in this case, temperature) to an equivalent voltage output. By regulating the current supplied by loop power supply, the transmitter converts sensor's output to a proportional 4 to 20mA dc current, where zero-value process variable, that is -200°C, is represented by 4mA and the full scale process variable, that is +1375°C, is represented by 20mA. That means, a 16mA span is available to represent the entire measurement information range. The current returns back to the power supply after flowing through a precision load resistor of loop receiver. As no system can measure the current directly, the receiver first converts 4 to 20mA loop current into a voltage which is easily measured by analog input module of Programmable Logic Controller (PLC) system and processed further.

Choosing current over voltage as an information carrier is mostly preferred due to the following facts:

1. Current loops have inherent immunity against noise.
2. Transmitting current signal over long distances does produce the voltage drop (also known as voltage loss or loop drop) across the loop due to wiring resistance. But, the magnitude of signaling is not affected as long as the loop power supply is high enough to compensate for these losses and still meeting the compliance voltage requirement at transmitter for its proper operation. The basic circuit theory shows that current is the same along the line which means same amount of current supplied by loop power supply always returns back to the source.
3. The residual 4mA current as zero-point allows easy detection of wire-break condition. It also allows the transmitter to be powered up if the current requirement is within 4mA. Current will exceed 20mA for short circuit condition. Thus, current loops are self-monitoring.
4. Minimizes the cost and simplifies the installation as signal current and transmitter power supply current share the same pair of conductors.
5. Ensures safer operation in hazardous areas by limiting the energy available for ignition. Lower current and voltage level also ensure the personnel safety.

The complete loop power supply voltage doesn't appear across the transmitter as all the devices in a 2-wire loop powered system are connected in series. So, it is important to ensure that loop power supply is large enough to supply minimum voltage at transmitter at maximum expected loop current having taken care of other drops in the loop. For detailed calculations of minimum loop power supply voltage, refer to Section 16.

6 Component Selection

6.1 ADC Selection: ADS1220

The ADC selected for this application is ADS1220 that is a low-power, low-noise, 24-bit, delta-sigma ADC for small-signal sensors. High integration and small package size of ADS1220 enables the use in space sensitive applications. ADS1220 has exact numbers of pins required for connecting with one thermocouple sensor and one RTD for cold junction compensation.

Some of the highlighted features of ADS1220 (see Figure 19) are:

- Low current consumption ≈ 415µA (in normal mode)
- Programmable gain: 1V/V to 128V/V
- Programmable data rates up to 2000SPS
- 50Hz and 60Hz line frequency rejection at 20SPS
- Low noise PGA: 90nVRMS at 20SPS
- Dual matched programmable current sources for sensor excitation: 10µA to 1.5mA
- Two differential or four single ended inputs
- Highly flexible input multiplexer
- Two burn-out current sources for sensor open circuit detection
- Internal offset calibration by shorting PGA inputs using register setting
- SPI compatible interface
- 3.5mm × 3.5mm 16-pin QFN package

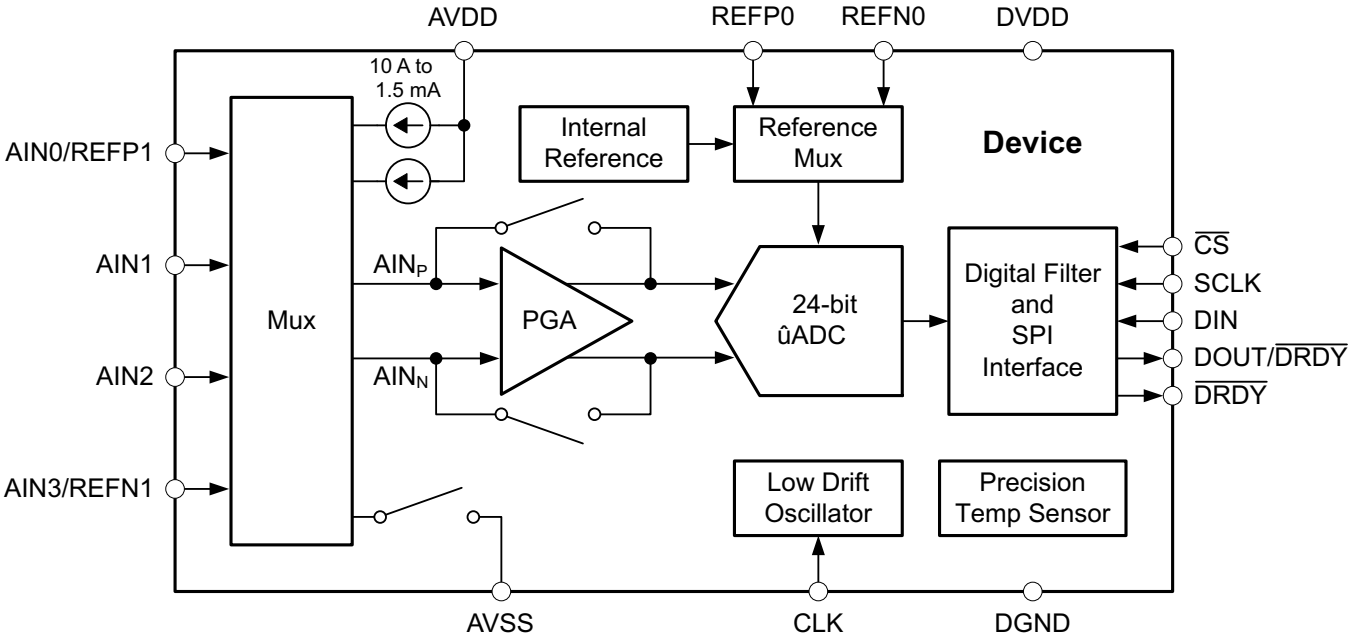


Figure 19. ADS1220 Block Diagram

6.2 Isolated Signal Path Selection: SN74LVC125ARGYR Plus S5394-CLB

- 4 channel buffer (2 per direction) SN74LVC125ARGYR
- Transformer based solution S5394-CLBT
- Small size (3.65mm × 3.65mm)
- Temperature range up to 85°C
- Low power (10µA)
- Output current capability (±50mA)
- Functional isolation up to 1.5kVrms working voltage

SN74LVC125ARGYR is used to send the signal across a transformer to the DAC and to recover the Acknowledge pulse from the DAC on the secondary side back to the micro-controller on the primary side (latch structure).

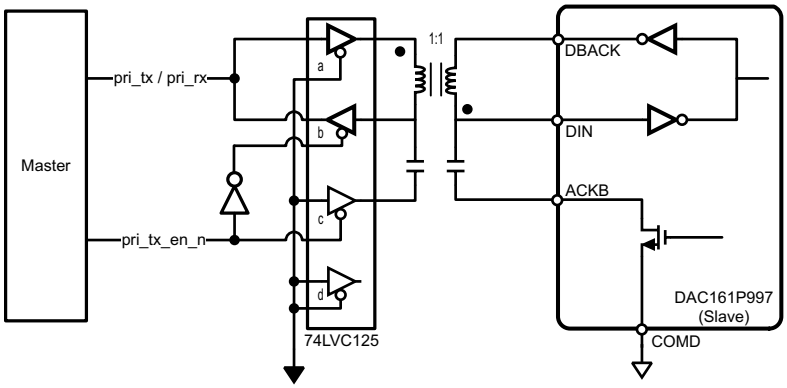


Figure 20. Isolate Signal Path Block Diagram (SWIF plus Transformer)

6.3 Power Component Selection

Please refer to TIDA-00167 for detailed description.

6.3.1 High-Voltage LDO for Providing the Non-Isolated Intermediate Voltage – TPS7A1601

The TPS7A1601 was selected. It outperforms all the other LDOs by its low Iq (5 μA typical), its 3 V to 60V wide input voltage range, its low dropout voltage (60 mV typical @ 20 mA) and by the fact that it is available in a space saving 3 × 3 mm ^{2} SON-8 package. The block diagram in Figure 21 illustrates the comprehensive set of additional features that come with the TPS7A1601.

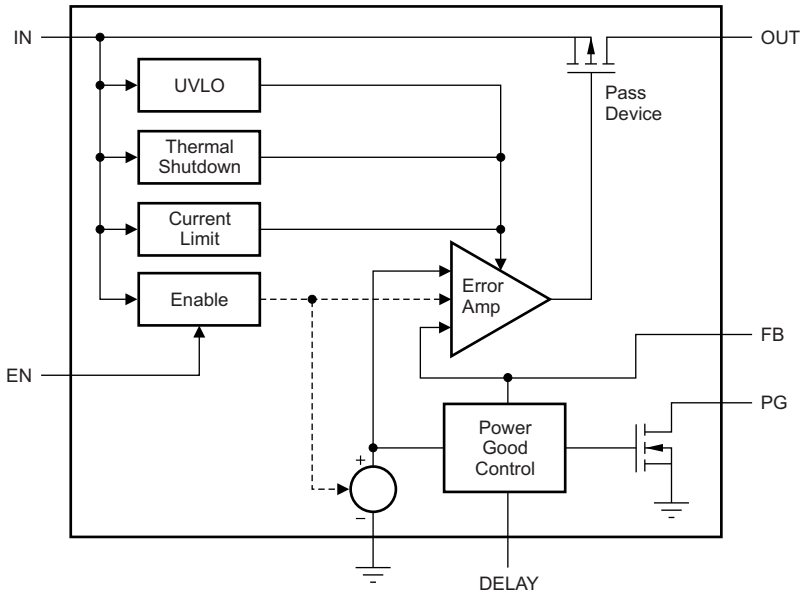


Figure 21. TPS7A1601 Block Diagram

Besides the thermal- and the over current-protection, dedicated ENABLE (EN) and PowerGood (PG) pins are provided. A DELAY pin enables system designers even to program a specific Power Good delay by a single capacitor (C_{DELAY}), usable to implement dedicated system sequencing solutions if needed. The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high.

The 60V maximum input voltage of the TPS7A1601 (absolute maximum rating is 62 V) provides a good cost- / performance- / size-trade-off between the needed input overvoltage protection diode (TVS) and the input voltage capability of the LDO. The use of a FET as internal pass device supports the ultra-low 5 μA of quiescent current and a dropout voltage scaling which is almost linear with the output current of the LDO, see Figure 22.

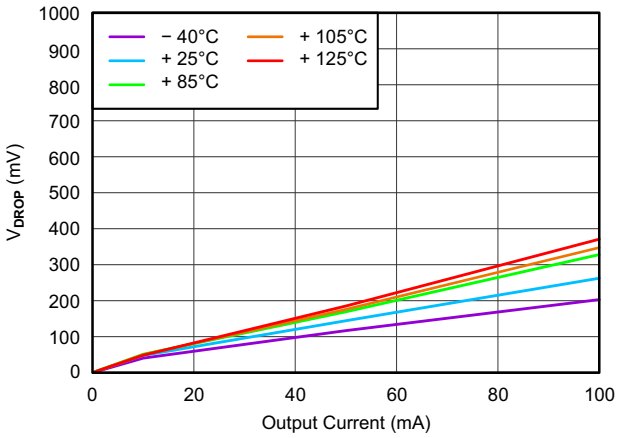


Figure 22. TPS7A1601 - Dropout Voltage vs. Output Current

6.3.2 Low Noise, High PSRR LDOs Used as Post-Regulators to Provide Isolated and Non-Isolated 3.3V Rails- TPS71733

The transmitter circuitry uses 2 LDOs as post regulator to provide stable and noise-free 3.3V to the analog and digital parts on the isolated and non-isolated side of the transmitter

The TPS71733 was selected. Main criteria for this choice have been its 6.5V maximum input voltage capability with an absolute maximum rating of 7V, its availability in a space saving 2 × 2 mm^2 SON-6 package and its outstanding 67 dB PSRR @ 100 kHz. This specification holds even true for very small VIN-VOUT difference voltages of 0.25V, as highlighted in Figure 23, which is valid over the full operating temperature range TJ = –40°C to +125°C.

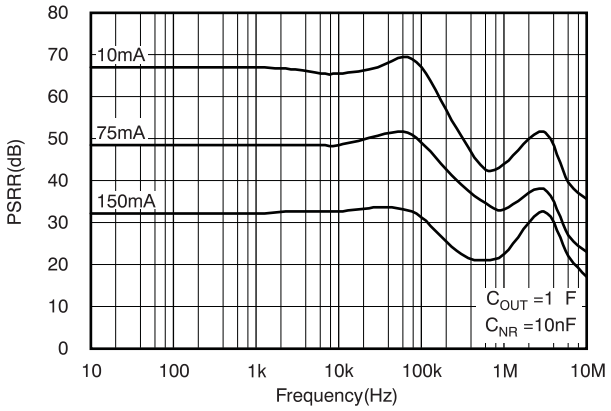


Figure 23. TPS71733 – PSRR vs. Frequency @ VIN – VOUT = 0.25V

The Noise Reduction pin allows the connection of an optional external noise reduction capacitor to bypass noise generated by the internal band-gap reference and to improve PSRR while an internal quick-start circuit fast-charges this capacitor (Figure 24).

The device uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations over the full operating temperature range. The TPS71733DSE, which is the device in the smallest package (1.5mm × 1.5mm WSON), is fully specified for an operating temperature range from TJ = –40°C to +125°C.

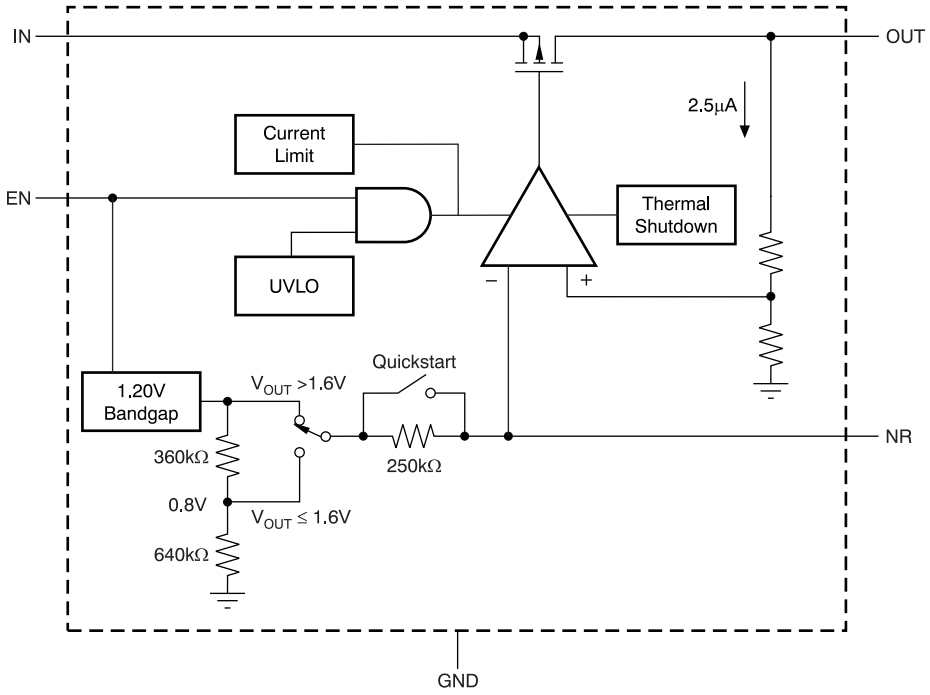


Figure 24. TPS71733 – Functional Block Diagram

6.3.3 TPS60402 to Drive the Power Transformer of the Isolated DC/DC Converter

Special care was needed for the selection of the best suited device for driving the power transformer. Key aspects for finding this device have been:

- High efficiency:
  - Low switching frequency
  - Low quiescent current (Iq)
- High integration level: needed for smallest size solution – the integration of the switches (FETs) is highly desirable.
- Fixed switching frequency: preferable from a noise and system accuracy perspective.

Taking all of the above listed part requirements into account, the **TPS60400 family** (Figure 25) was selected.

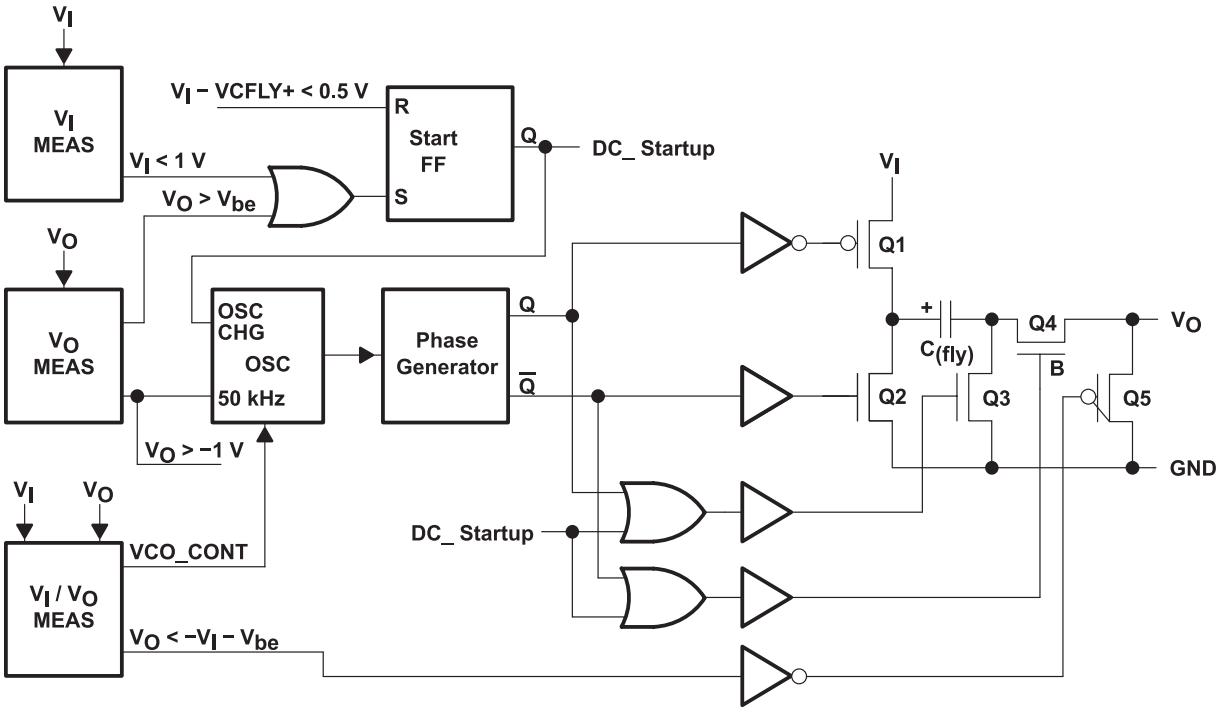


Figure 25. TPS60400 Family - Functional Block Diagram

The main applicable and beneficial features of the device family can be summarized as:

- Input voltage range from 1.6 V to 5.5 V
- Small 5-pin SOT23 package
- Integrated switches (FETs)
- Internal fixed frequency oscillator (for TPS60401 … TPS60403)
- Multiple switching frequency versions
- Devices available with quiescent current down to 65 μA

Out of this family, the TPS60402 was chosen. With its 50 kHz switching frequency and 120 μA quiescent current, it offers a good trade-off between efficiency and solution size.

6.4 MCU Selection: MSP430F5172

The MCU selected for this application is the **MSP430F5172** (Figure 26). The MSP430F51x2 series are microcontroller configurations with two 16-bit high-resolution timers, two universal serial communication interfaces (USCI_A0 and USCI_B0), a 32-bit hardware multiplier, a high-performance 10-bit analog-to-digital converter (ADC), an on-chip comparator, a three-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins.

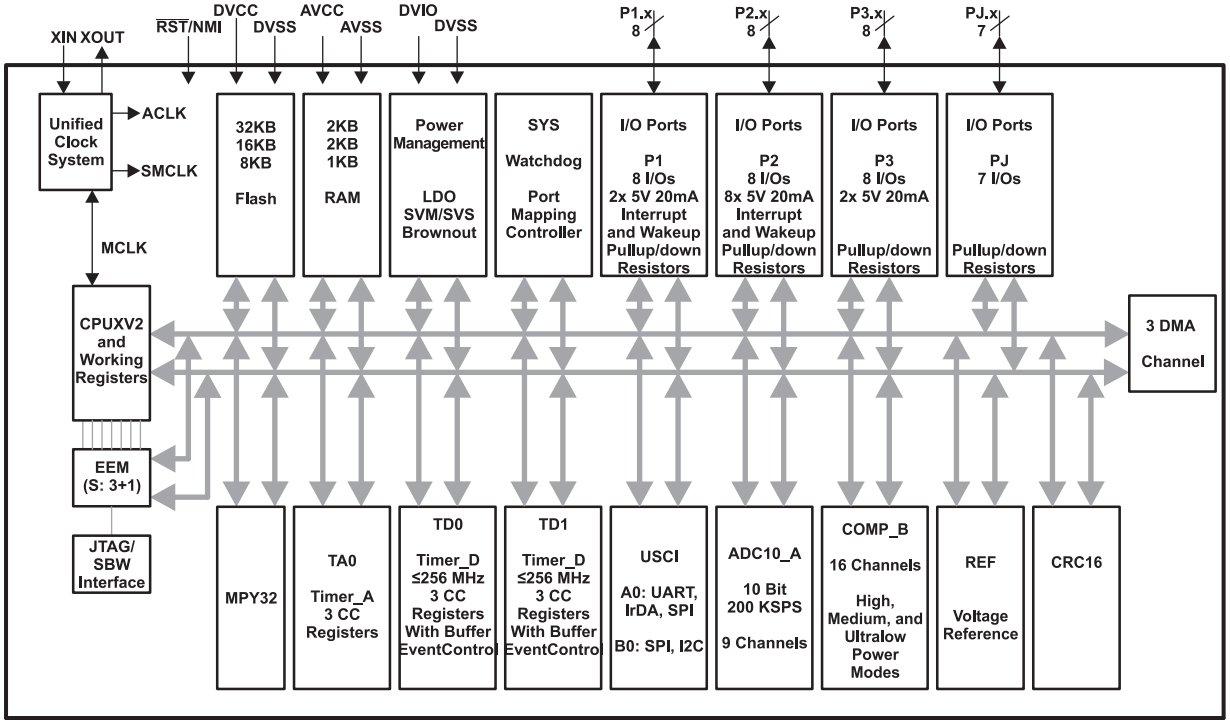


Figure 26. MSP430F5172 Block Diagram

Some of the highlighted features of MSP430F5172 are:

- Low Supply Voltage Range: 3.6 V Down to 1.8 V
- Ultra-Low Power Consumption:
  - Active Mode (AM): 180 µA/MHz
  - Standby Mode (LPM3 WDT Mode, 3 V): 1.1 µA
  - Off Mode (LPM4 RAM Retention, 3 V): 0.9 µA
  - Shutdown Mode (LPM4.5, 3 V): 0.25 µA
- Wake up from Standby Mode in less than 5 µs
- 16-Bit RISC Architecture, Extended Memory, 40-ns Instruction Cycle Time
- Flexible Power-Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals (XT1)
  - High-Frequency Crystals up to 25 MHz (XT1)

- Hardware Multiplier Supports 32-Bit Operations
- Three-Channel DMA
- Up to Twelve 5-V-Tolerant Digital Push/Pull I/Os With Up to 20-mA Drive Strength
- 16-Bit Timer TD0 With Three Capture/Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TD1 With Three Capture/Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TA0 With Three Capture/Compare Registers
- Universal Serial Communication Interfaces
  - USCI_A0 Supports
    - Enhanced UART Supports Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 Supports
    - I^2C
    - Synchronous SPI
- 10-Bit 200-ksps Analog-to-Digital Converter (ADC)
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - Up to Eight External Channels, Two Internal Channels, including Temperature Sensor
- Up to 16-Channel On-Chip Comparator including an Ultra-Low-Power Mode
- Serial Onboard Programming, no external programming voltage needed
- Available in 40-Pin QFN (RSB), 38-Pin TSSOP (DA), and 40-Pin Die-Sized BGA (YFF) Packages

6.5 DAC Selection

The DAC selected for this application is **DAC161P997** (Figure 27). It is a 16-bit DAC and an obvious choice as it was designed specifically for industry standard 4 to 20mA current loops. It is an ideal choice for sensor nodes limited to 3.3mA power consumption. In addition, it offers an easy to use and low-power interface for data isolation (SWIF, see Figure 20).

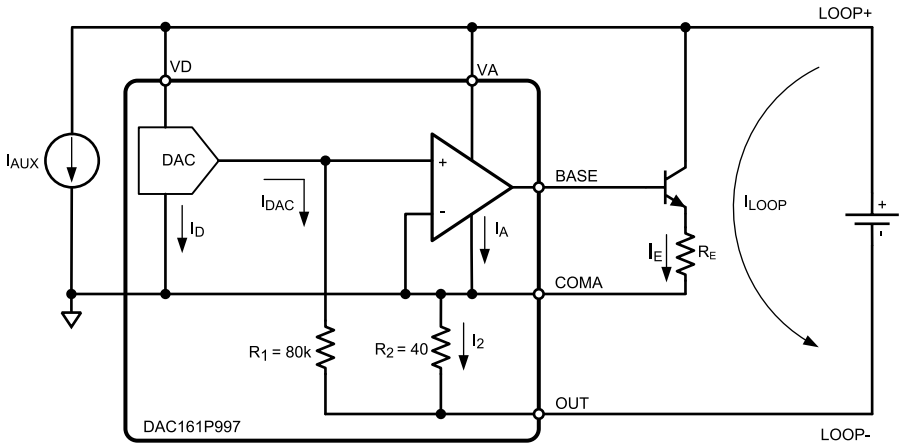


Figure 27. DAC161P997 Block Diagram

Some of the highlighted features of DAC161P997 are:

- 16-bit resolution
- Very low power supply current < 125µA (max)
- Pin programmable power-up condition
- Loop error detection and reporting
- Programmable output current error levels
- Ultra low power internal reference and internal oscillator
- SPI Compatible interface
- **SWIF (single wire interface for low power data path isolation)**
- No external precision components
- Integrating all precision elements on-chip in small 4mm × 4mm 16-pin QFN package

7 Analog Front End Design

The thermocouple is connected to AN0 and AN1 that are the most precise inputs (smaller input currents) of the ADS1220 since they are not connected to the internal current sources (IDAC). The RTD (pt100) is connected to AN2 and AN3 so that a current can be injected in the resistor.

For the RTD (used as Cold Junction Compensation) a 2 wires configuration is used.

7.1 Thermocouple Channel Configuration

This measurement channel uses the internal voltage reference integrated in the ADS1220. Considering that the device provides a 2.048V reference voltage and considering that the maximum thermocouple voltage is 54.886mV (see look up table, Figure 7), the maximum gain can be calculated as follows:

$$Gain_{MAX} = V_{ref}/V_{TC\ max} = 2.048V/54.886mV = 37.3V/V$$

A PGA gain of 32V/V is then the closest selection.

The typical bandwidth of thermocouples is in the range of few Hz. For this reason, an output data rate of 20SPS.

This choice will also insure very low noise at the input.

All considerations on common mode restrictions and accuracy of the channel are covered in Section 9 and Section 10.

7.2 Cold Junction Compensation Channel Configuration

An RTD is used as cold junction compensation. Because of the small distance between the RTD and the ADS1220 on the board (see layout pictures), the leads resistance is very small. In this case, a two-wire configuration is enough.

The voltage measured across the RTD is proportional to temperature (determined by the characteristics of the RTD). The reference to the device is also derived from the IDAC and an external precision resistor. This resistor determines the reference voltage to the ADC as well as the input common mode of the PGA. Because of that, the current source (only one is needed) is set at a value of 250µA and the precise reference resistor has been chosen to be R_{REF} = 6490Ω. As a result, the voltage reference value is around 1.6V.

This ratiometric approach ensures a greater effective number of bits (ENOB) because the noise in the IDAC reflects in the reference as well as in the input, and thus tends to cancel off.

Considering that the target operating range is -40°C to 85°C, from the RTD Pt100 look up table, we can find the according resistance value of 84.27Ω to 130.9Ω. So the resulting minimum and maximum voltage input are:

$$V_{min} = 84.27\Omega \times 250\mu A /1000 = 21.0675\ m\ V$$

$$V_{max} = 130.9\Omega \times 250\mu A/1000 = 32.725\ mV$$

These values, combined with a voltage reference of 1.6V, lead to a **gain of 32** for this channel as well.

8 Error Sources

The total system accuracy can be calculated as the quadratic sum of the errors on the individual blocks of the acquisition chain. The error can be both systematic and random; can be temperature dependent or just related to the manufacturing repeatability of all components. As a result, there are parts of the error that can be calibrated and part of it that will be still present also after calibration.

The main contributors to the total error are:

Input Filters mismatch (precision and drift)

- Analog Front End (accuracy and drift)
  - ADC and PGA Gain Error and drift
  - ADC Reference Error
  - ADC Linearity Error
  - ADC and PGA Offset and drift
- Cold Junction measurement Error (accuracy and drift)
  - ADC and PGA Gain Error and drift
  - Reference resistor accuracy and drift
  - ADC Linearity Error
  - ADC and PGA Offset and drift
- Power supply noise
- Firmware Errors (Look up Tables and Cold Junction compensation)

Here the focus will be on the Filters, AFE and Cold Junction measurement.

9 Input Filters Design

9.1 Design Target

The main target is to keep the filter initial error contribution to the total error comparable or smaller than the initial error of the thermocouple sensor itself. Considering the manufacturing limitations of the Type K thermocouple (mainly related to the purity of materials), the initial error of the Thermocouple sensor (tolerance class 1) is typically **smaller than 1.5°C between -200°C and 375°C and then better than 0.4% up to 1375°C (maximum thermocouple temperature range).** See Section 5.1.

Regarding the error that cannot be calibrated (noise and drift), the target is to design filter that do not degrade the performances of the ADS1220. The system works at 20SPS at a gain of 32, so the **input-referred noise is 0.23µV** (see Table 4). The noise introduced by the filters should be less than that.

Table 4. ADS1220 Input Referred Noise in μV_{rms} (μV_{pp})

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	3.71 (13.67)	1.54 (5.37)	1.15 (4.15)	0.80 (3.36)	0.35 (1.16)	**0.23 (0.73)**	0.10 (0.35)	0.09 (0.41)
45	7.36 (29.54)	2.93 (13.06)	1.71 (9.28)	0.88 (4.06)	0.50 (2.26)	0.29 (1.49)	0.19 (0.82)	0.12 (0.51)
90	10.55 (47.36)	4.50 (20.75)	2.43 (11.35)	1.51 (6.65)	0.65 (3.62)	0.42 (2.14)	0.27 (1.22)	0.18 (0.85)
175	11.90 (63.72)	6.45 (34.06)	3.26 (17.76)	1.82 (11.20)	1.01 (5.13)	0.57 (3.09)	0.34 (2.14)	0.26 (1.60)
330	19.19 (106.93)	9.38 (50.78)	4.25 (26.25)	2.68 (14.13)	1.45 (7.52)	0.79 (4.66)	0.50 (2.69)	0.34 (1.99)
600	24.78 (151.61)	13.35 (72.27)	6.68 (39.43)	3.66 (19.26)	2.10 (12.77)	1.14 (6.87)	0.70 (4.76)	0.55 (3.34)
1000	37.53 (227.29)	18.87 (122.68)	9.53 (58.53)	5.37 (31.52)	2.95 (18.08)	1.65 (10.71)	1.03 (6.52)	0.70 (4.01)
2000	36.23 (265.14)	18.24 (127.32)	9.24 (65.43)	5.49 (37.02)	2.89 (18.89)	1.77 (12.00)	1.13 (7.60)	0.82 (5.81)

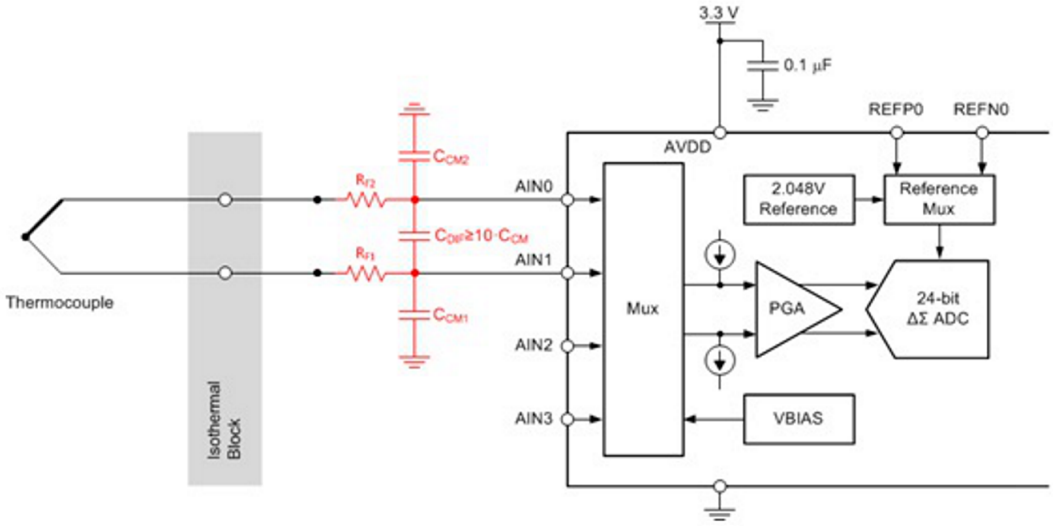
Table 5. Offset and Gain of the ADS1220

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO Offset voltage (input-referred)	PGA disabled, TA = +25°C, differential inputs		±4		µV
	PGA = 1, TA = +25°C, differential inputs	-30	±4	30	µV
	PGA = 2…128, TA = +25°C, differential inputs		±4		µV
Offset drift	PGA = 1…128, TA = –40°C to +85°C		0.08	0.3	µV/°C
	PGA = 1…128, TA = –40°C to +125°C		0.25		µV/°C
Offset match	Match between any two inputs		±20		µV
GE Gain error	PGA = 1…128, TA = +25°C	-0.1%	±0.015%	0.1%	
Gain drift	PGA = 1…128, TA = –40°C to +125°C		1	4	ppm/°C

9.2 Input Filter Function

The importance of signal conditioning is critical in any design. Due to the effects of aliasing, any ADC, regardless of architecture, need some amount of filtering on its inputs to reduce noise in the system. Because of the digital filter in delta sigma ADCs, the requirements of an external analog filter are significantly reduced, but some filtering is still needed. A simple filter, such as the one shown in Figure 28, will offer a great balanced differential filter design.

For the filter design using the ADS1220, a very simple first order filter is being used. This is due to the expected small form factor and cost requirements for this reference design. This filter could easily be cascaded into higher order filters to provide greater higher frequency noise immunity.



NOTE:

- All selected capacitors are ±10% accurate.
- All selected resistors are 1% accurate and present a 100ppm/°C drift.

Figure 28. Signal Conditioning with First Order Low-Pass Filter

9.3 Differential and Common Mode Filter Capacitors Ratio

The differential filter is also great for reducing both common mode and differential noise components. The resistors used to develop the filter also serve to limit current to the inputs of any device that follows the filter. When sized accordingly, this can allow significant robustness to the inputs and protect from ESD and long term overvoltage conditions. The filter shown in Figure 29 is a very commonly used structure for differential signals. However, there are a few important points to keep in mind when selecting components. Because mismatches in the common-mode capacitors cause differential noise, it is recommended that the differential capacitor be at least 10× greater than the common-mode capacitors. To achieve good electromagnetic interference (EMI) immunity, it is important to remember that simply placing large capacitors in the signal path and supply are not effective at attenuating high noise frequency components. Using small (10nF and lower) capacitors with low equivalent series resistance (ESR) and low dielectric absorption (DA) in parallel with another higher capacitance capacitor on sensitive supply and signal paths can offer significant improvements to EMI immunity. The mismatch in common-mode capacitors has been simulated using TINA (TI spice based simulator).

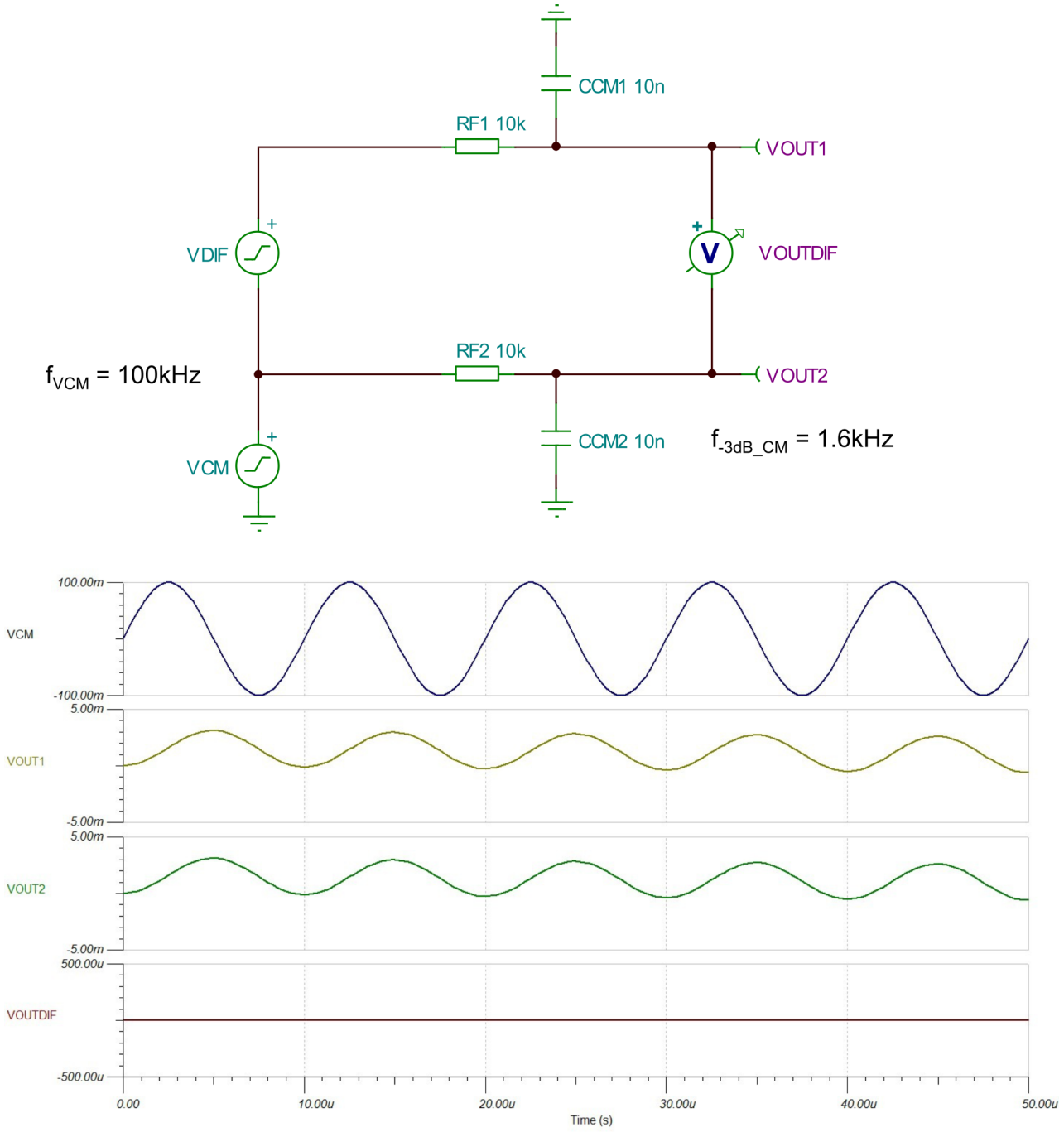


Figure 29. Common-Mode Filter Ideal Matching

When using CM-filter only and the two C_{CM} are matched, there will not be any differential output signal.

When the two C_{CM} are mismatched, the accuracy of the selected capacitors of the filter is 10%. From the circuit shown in Figure 30, there is 1nF difference between the two common-mode capacitors, which will introduce big noise in the differential output.

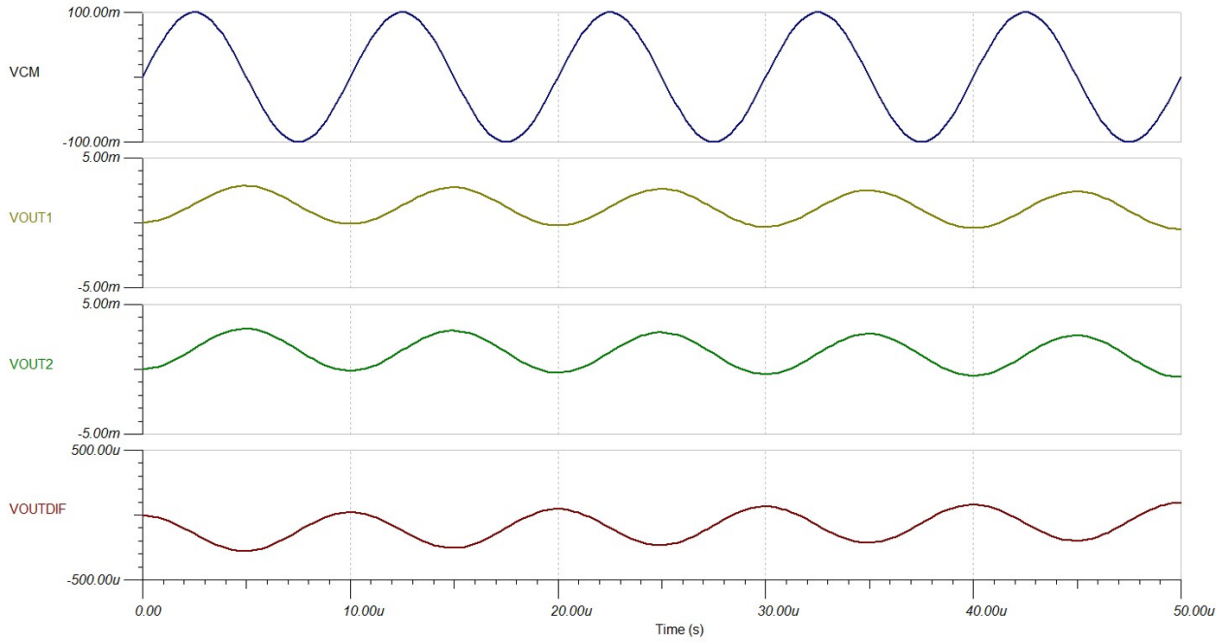


Figure 30. Mismatched Common-Mode Capacitors

In Figure 31, the differential filter has been added. The value of the differential capacitor is the same as the CM-capacitor. The result is that the undesired differential output is reduced but still considerable.

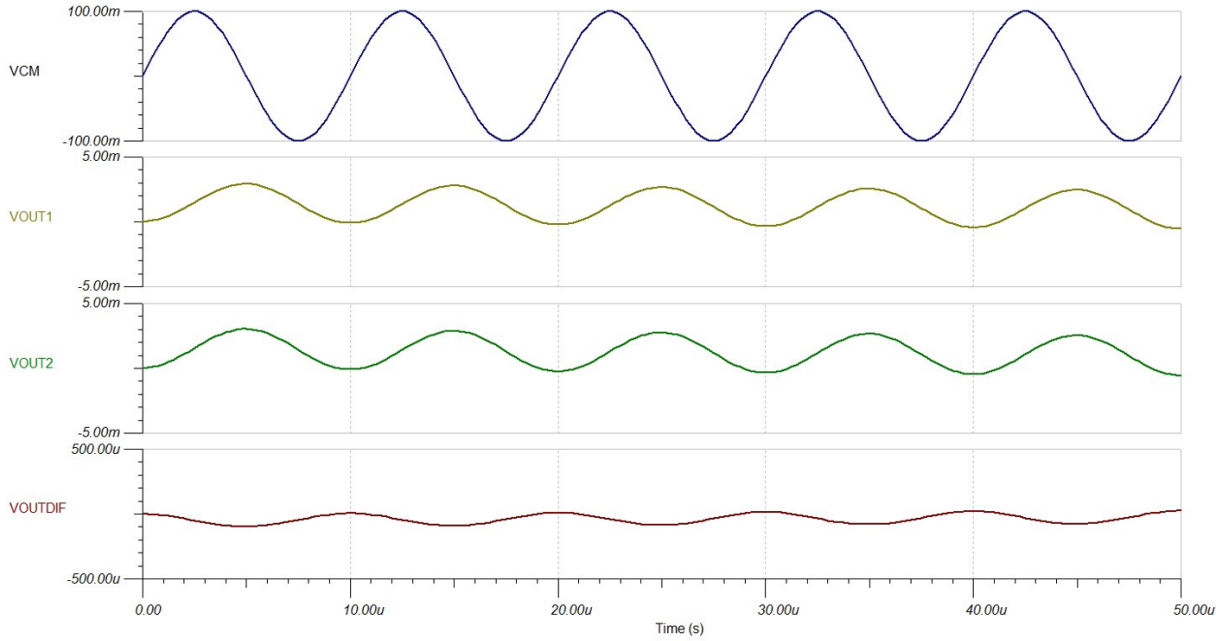


Figure 31. Adding Differential Mode Filter

When the value of the capacitor is increased (in the example in Figure 32, 20× bigger than CM capacitor), the noise caused by common-mode voltage will be greatly reduced.

So in order to get rid of the CM-capacitors mismatched noise, differential filter capacitor should be at least 10× greater than CM-capacitors:

$$C_{DIFF} = 10 \times C_{CM}$$

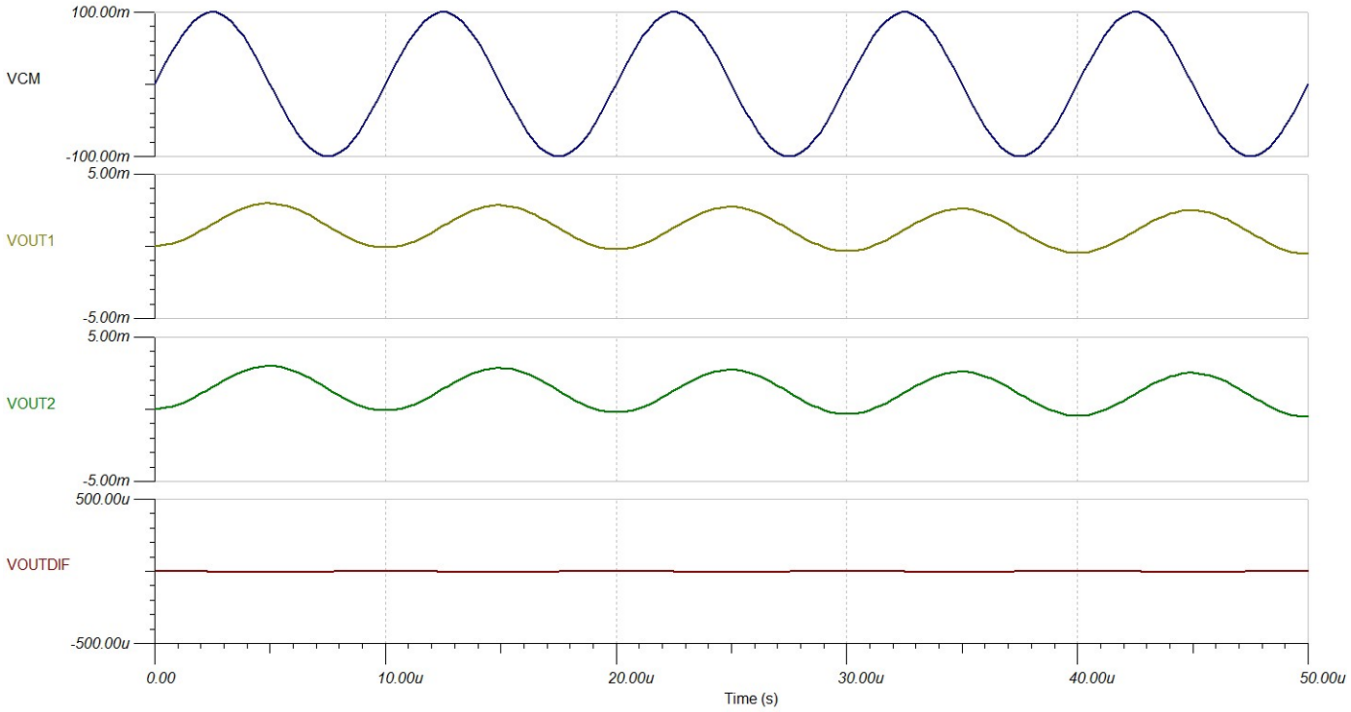


Figure 32. Increase Differential Mode Filter Capacitor

9.4 Input Filter Noise Contribution (Capacitor Value Selection)

The resistors in the input filters add a small amount of noise so for very high precision designs that thermal noise should be accounted for when choosing the size of these components. For this design, they will be sized to keep their noise contribution to less than input-referred noise 0.23μV of the front end (see Figure 30 from the ADS1220 datasheet, SBAS501). A small amount of noise from these components will become useful later to employ some dithering to the system to obtain higher resolution. Resistors are perfect for this because the noise they generate is very statistically Gaussian and very easy to average out. Using the Johnson-Nyquist equation for resistor noise:

$$v_n = \sqrt{4kTR\Delta f}$$

Where:

k = 1.38 × 10^{-23}J/K, T = 298K

In order to find the total output noise, the above spectral density has to be integrated over the noise bandwidth Δf. The RC circuit creates a one pole filter for the noise.

Expressed in Hertz, this noise bandwidth is:

$$\Delta f = \frac{1}{2\pi}\int_0^\infty \frac{d\omega}{1+(\omega C_1 R_{DIFF})^2} = \frac{\pi}{2\pi \times 2C_1 R_{DIFF}} = \frac{1}{4C_1 R_{DIFF}}$$

$$C_1 = (C_{DIFF} + \frac{C_{CM}}{2})$$

$$R_{DIFF} = R_{F1} + R_{F2}$$

$$v_n = \sqrt{4kTR_{DIFF}\frac{1}{4C_1 R_{DIFF}}}$$

$$v_n = \sqrt{\frac{kT}{C_1}}$$

$$v_n^2 = \frac{kT}{C_1}$$

$v_n \le V_{rms}$, so

$$C_1 \ge kT/(0.0529(\mu V)^2 = 0.077\mu F$$

From the calculation, it is clear that the impact of the resistor on the noise is not relate to the resistor itself, but depends on the value of the capacitor. The condition for the design is: $C_1 = (C_{DIFF} + ½C_M) \ge 0.077\mu F$, and $C_{DIFF} = 10 \times C_{CM}$, so CDIFF and CCM are selected as 4.7μF and 0.27μF, respectively, to fully satisfy with the requirements.

$$v_n = \sqrt{\frac{kT}{C_1}}$$

Where, C_1 = 4.7 + 0.135 = 4.835μF, so

$$v_n = 0.029\mu V \ll 0.23\mu V$$

9.5 Input Filter Capacitors Accuracy Impact

In case the values of the capacitor are at the corner case of the specifications, only the cutoff frequency of the input filter will change slightly but with no impact on the overall performances of the system.

Regarding the common mode to differential noise, since 4.7μF and 0.27μF are used, and considering $C_{DIFF} = 4.7(1 - 10\%), C_{CM} = 0.27(1 + 10\%)$, $C_{DIFF}/C_{CM} = 14.2$, it is above $C_{DIFF} = 10 \times C_{CM}$, there is not impact.

In addition, $C_1 = (C_{DIFF} + ½C_M)(1 - 10\%) = 4.3515\mu F$ is still much bigger than 0.077μF, which is the system requirement for the capacitor to keep the noise in the target specifications.

9.6 Cutoff Frequency (Resistor Value Selection)

The filter is important for rejecting any noise that might be subjected to the ADC inputs that are near the modulator sampling speed. The modulator sampling speed is usually hundreds or even thousands of times higher than the actual ADC output data rate. Noises at these frequencies have no way of being rejected digitally by the data-converter and must be rejected through analog input filtering. Delta sigma ADCs will specify the frequency that the modulator samples at to allow external filters to be designed accordingly. The ADS1220, for example, has **a modulator sampling frequency of 256kHz.**

The input filter also performs as an **antialiasing filter**. Errors introduced through input filters can be usually calibrated out in most systems. However, for this un-calibrated example, the ADS1220 has roughly 10MΩ of differential input impedance. This increases gain error as sensor output and filter impedances increase. In selecting the filter for this design there will be a tradeoff between lowering the cutoff and using small value components. Ideally, a lower cutoff frequency and a higher the order filter is preferred for a design with a thermocouple due to the low bandwidth of the sensor (<1Hz). However, designing an extremely aggressive high order passive filter will introduce large resistances in front of the ADC, which will interact with the differential input impedance of the ADS1220.

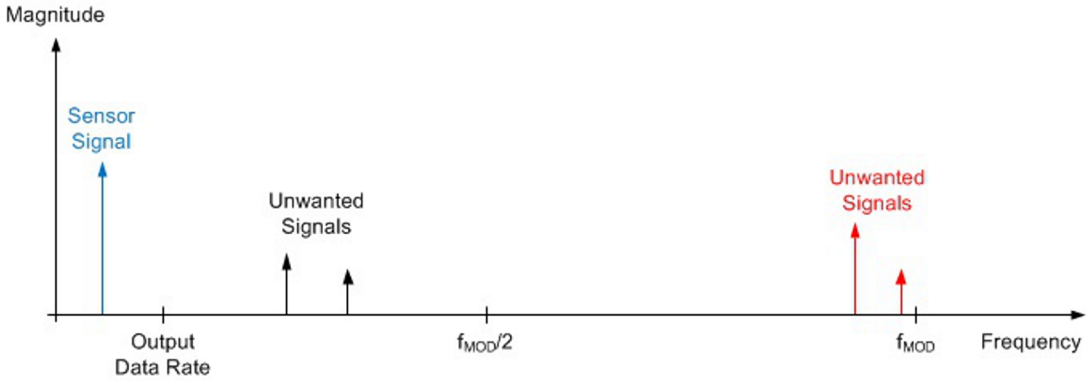


Figure 33. Unwanted Signal in the Frequency Domain

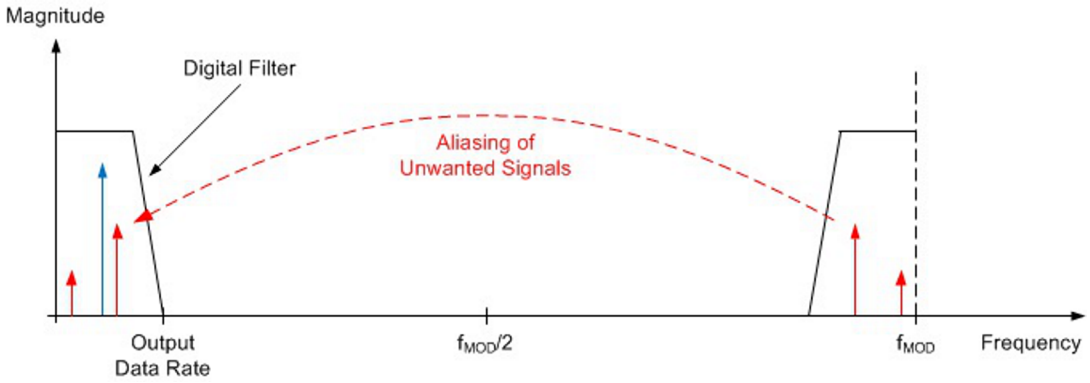


Figure 34. Aliasing After Sampling

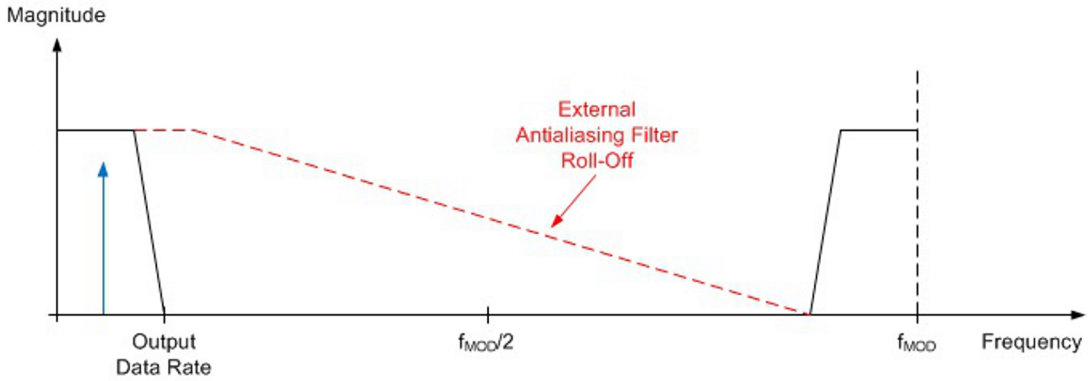


Figure 35. Antialiasing Filter

The inside digital filter cannot get rid of the aliasing signal brought by the modulator. So the input filter can act as an antialiasing filter. For this design the target is to keep the signal rejection at 256kHz at least -80dB. The -80dB is somewhat arbitrary and depends on the expected noise environment the system will be deployed in. In this case, -80dB corresponds if the injected unwanted signal is as big as 5mV, it will attenuate to 0.5 µV.

Given that: -80 db = 20log[10^{-4}]

The filter will need to reduce noise at 256kHz by a factor 10000. Now that the rejection at 256kHz of 80dB is desired, a cutoff frequency to achieve this can easily be calculated. Since the first order filter in this design rejects at 20dB per decade, the corresponding -3dB frequency would be simply be 4 decades down from 256kHz or 25.6Hz. The transfer function of the filter is:

$$\ddot{A} = \frac{\ddot{U}_0}{\ddot{U}_1} = \frac{1}{1 + j\omega R_{DIFF}(C_{DIFF} + 1/2C_{CM})}$$

If the attenuation at 256kHz is -80dB, the magnitude of the transfer function will be:

$$\frac{1}{\sqrt{1 + (\omega R_{DIFF}(C_{DIFF} + \frac{1}{2C_{CM}}))^2}} = \frac{1}{10000}$$

Where $\omega = 2\pi \times 256kHz$, and simplifying the equation:

$$\frac{1}{2\pi * 256kHz R_{DIFF}(C_{DIFF} + \frac{C_{CM}}{2})} = \frac{1}{10000}$$

$$\frac{1}{2\pi * 25.6Hz R_{DIFF}(C_{DIFF} + \frac{C_{CM}}{2})} = 1$$

So the cutoff frequency is 25.6Hz.

With a desired cutoff frequency in mind, actual component values can be selected. Because of the previous considerations and of how common and physically small in ceramic form they are, CDIFF and CCM are selected as 4.7μF and 0.27μF, respectively. With these components selected, the equation above can be re-arranged to solve for RF1:

$$R_{F1} = \frac{1}{4\pi f_{C-DM}(C_{DIFF} + \frac{C_{CM}}{2})}$$

$$= \frac{1}{4\pi \times 25.6Hz \times (4.7\ \mu F + \frac{0.27\ \mu F}{2})}$$

$$= 643.24\ \Omega$$

However, a potential **noise coming from the isolated power** has to be considered. Power supply can inject disturbances because of incompletely filtered switching ripple and irradiated energy. Assuming a 60kHz switching frequency of the DC-DC converter, noise at this frequencies and its harmonics has to be considered. The filter rejection at 60kHz is -67.4dB. Moreover, in this case, there is a digital filter (Figure 36) in the ADS1220, which can attenuate the noise of additional -40dB and the total rejection at 60kHz will be around -100dB. So it means that as long as the R_{DIFF} is bigger than 643Ω, there will be at least -80dB of filter attenuation at 256kHz and -100dB at 60kHz.

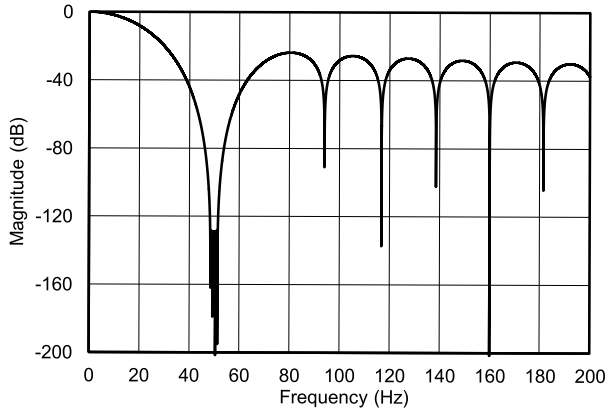


Figure 36. ADS1220 Digital Filter Response

9.7 Absolute Maximum Ratings for ADS1220 Input Pins

In addition to the filter cutoff frequency, this filter needs to be able to protect the ADS1220 in worst-case conditions. To select a suitable resistance for the protection, the Absolute Maximum Ratings section of the ADS1220 datasheet (SBAS501) has to be considered. This is present on all TI data-converter datasheets.

Table 6. ADS1220 Absolute Maximum Ratings

PARAMETER		VALUE		
		MIN	MAX	UNIT
AVDD to AVSS		–0.3	+7	V
DVDD to DGND		–0.3	+7	V
AVSS to DGND		–2.8	+0.3	V
Analog input current	Momentary	–100	+100	mA
	Continuous	–10	+10	mA

The ADS1220 can withstand up to 10mA of continuous current on any of its inputs and no more than 7V. That means that in order to limit the current to less than 10mA, the series resistance would need to be:

RF1 = Overvoltage amount (V)/Maximum rated continuous input current (A) = 7V/10mA = 700Ω

This also satisfies the 50V momentary overvoltage according to the datasheet maximum ratings.

The actual filter cutoff with these values is 24Hz with a 256kHz filter rejection of 80.7dB, and a 60kHz filter rejection of 68.13dB.

9.8 Filter Error Calculation

The anti-aliasing filter is the largest source of **un-calibrated systematic error**. It presents a significant source of **gain error** to the system and has to be calibrated out in most of the systems. Given that 1400Ω of total series input resistance has been added to the signal chain (R_{F1} + R_{F2} = 2 × 700), it will interact with the ~10MΩ differential input impedance of the ADS1220. This will manifest itself as a gain error in the system (**resistive voltage divider**). Based on these values, it can be expected that the filter will cause the following error to the DC signal:

$$R_{DIFF} = R_{F1} + R_{F2}$$

$$Error\% = R_{DIFF}/(R_{DIFF} + InputZ)$$

Considering the initial error target for initial error (see Section 9.1), Error% ≤ 0.4%

$$R_{DIFF}/(R_{DIFF} + InputZ) \leq 0.4\%$$

$$R_{DIFF} = 2 \times R_{F1(2)} \leq 40k\Omega$$

So the range of $R_{F1(2)}$ is: 700 ≤ $R_{F1(2)}$ ≤ 20k

A value of **1kΩ** for $\mathbf{R_{F1(2)}}$ has been selected for this design.

In addition to these errors, the drift of the selected resistor has to be considered. As mentioned already, the selected components have 100ppm/°C drift. The initial or nominal operating temperature of the system is 25°C while the temperature range is from -40°C to 85°C. So the max ΔT = 25 - (-40) = 65°C.

The % drift of resistor is:

$$(100^{ppm}/°C) \times 65°C = 0.65\%$$

As a result, this will cause a gain drift in the acquisition chain:

$$\text{Gain drift} = (\text{Error\%(drift)} - \text{Error\%}) \times 1000000$$

$$= \left(\frac{R_{DIFF}(1 + 0.65\%)}{R_{DIFF}(1 + 0.65\%) + InputZ} - \frac{R_{DIFF}}{R_{DIFF} + InputZ} \right) * 1000000$$

For a 1kΩ resistor, this would be: 2.25ppm

This drift has to be compared to the gain drift of ADS1220 to be sure it does not degrade the front end performances: $(1^{ppm}/°C) \times 65°C = 65ppm$

2.25ppm << 65ppm

9.9 Differential Input Current Error Calculation

The Thermocouple and the filters are connected to AIN0 and AIN1, so the influence of differential input current at these input pins has to be considered. These currents will flow in the resistors and will generate a voltage error; this sets a limit to the upper value of the filter resistors themselves.

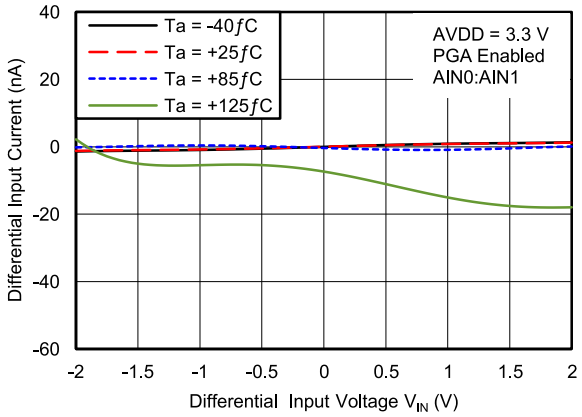


Figure 37. Differential Input Current vs Differential Input Voltage (PGA Enabled)

From Figure 37 and considering the system operates from -40°C to 85°C, it is evident that the current is not 0A. Considering a maximum input current of 1nA and R_{DIFF} = 1kΩ + 1kΩ = 2kΩ:

$$V_{error} = I_{DIFF} \times R_{DIFF} = 2\mu V$$

This error cannot be calibrated out since the current behavior is not well controlled and characterized.

The actual filter cutoff with these values becomes 16Hz with a 256kHz filter rejection of 83.8dB. Filter error% will be 0.02%. This error will scale with input signal, so at 0V differential input, there will be no error. However at the largest thermocouple voltage from the Omega K-type thermocouple of 1375°C a 54.89mV signal will be attenuated to:

$$V_{actual} \times (1 - Error\%) = V_{Measured}$$

$$54.89mV \times (100\% - 0.02\%) = 54.879mV$$

This 11μV of error corresponds to roughly 0.27°C of error at 1375°C and scales linearly with temperature. As a benchmark, this indicates that at 1375°C, every 0.1% of error contributes about 1.39°C of total system error.

9.10 Input Filter Resistors Accuracy Error Calculation

The accuracy of the R_{F1} and $C_{DIFF}C_{CM}$ will influence the attenuation at 256kHz. Substitute the value of $R_{DIFF}C_{DIFF}C_{CM}$, in the following equation, the amplitude of the transfer function is:

$$\left|\ddot{A}\right| = \frac{1}{\sqrt{1+\left(\omega R_{DIFF}\left(C_{DIFF}+\frac{C_{CM}}{2}\right)\right)^2}}$$

$$\left|\ddot{A}\right| = \frac{1}{\sqrt{1+\left(2\pi * 256kHz * 2k\Omega * (1-1\%) * (4.7+0.135)\,\mu F * (1-10\%)\right)^2}}$$

$$\left|\ddot{A}\right| = \frac{1}{13851.72}$$

$$-20\log\left|\ddot{A}\right| = -82.8dB$$

The attenuation at 256kHz can be lower, but is still below -80dB and does not influence the result of our filter.

On the other side, the accuracy of R_{F1} (1%) creates a mismatch in the value of the tow resistors. Mismatched values for R_{F1} and R_{F2} will cause any **common mode input to be transferred as differential mode** at the ADS1220 input. This has a big impact on the Common Mode Rejection Ratio of the complete signal chain.

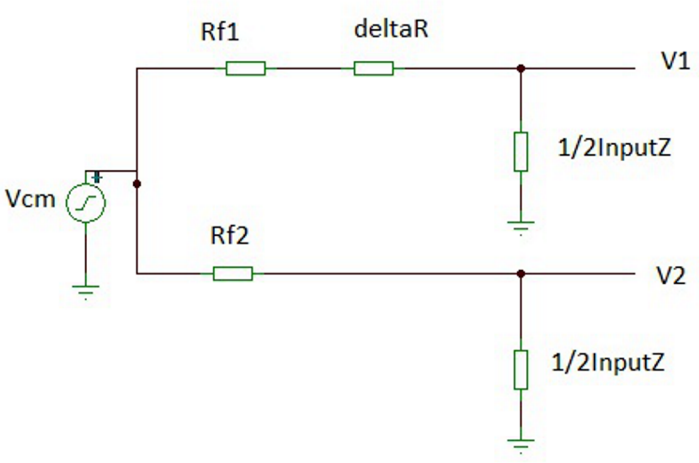


Figure 38. Simplified Circuit of R_{f1} Mismatched

Since the accuracy of R_{F1} is 1%, the biggest ΔR will be:

$$\Delta Rmax = R_{F1}(1 + 1\%) - R_{F2}(1 - 1\%) = 20\Omega$$

$$R^*_{F1} = R_{F1}(1 + 1\%) = 1010\Omega,\ R^*_{F2} = R_{F1}(1 - 1\%) = 990\Omega$$

$$InputZ = \sim 10M\Omega$$

Using the maximum allowed common mode voltage:

$$Vcm = V_{DD} - 0.2V = 3.1V$$

$$V1 = (V_{CM}/(R_{F1} + \Delta R + \tfrac{1}{2}InputZ)) \times \tfrac{1}{2}RZ = 3.099374V$$

$$V2 = (V_{CM}/(R_{F1} + \tfrac{1}{2}RZ)) \times \tfrac{1}{2}InputZ = 3.099386V$$

$$V_{error} = V2 - V1 = 12.79\mu V$$

To limit this error that cannot be neglected, a biasing circuit has been introduced (R_{bias}) to limit the V_{CM} filter error.

9.11 R_{Bias} (Bias Resistor)

The biasing resistors RB1 and RB2 (see Figure 39) are used to set the common-mode voltage of the thermocouple within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD/ 2) to allow the input circuit (shown in Figure 40) of the ADS1220 to work properly.

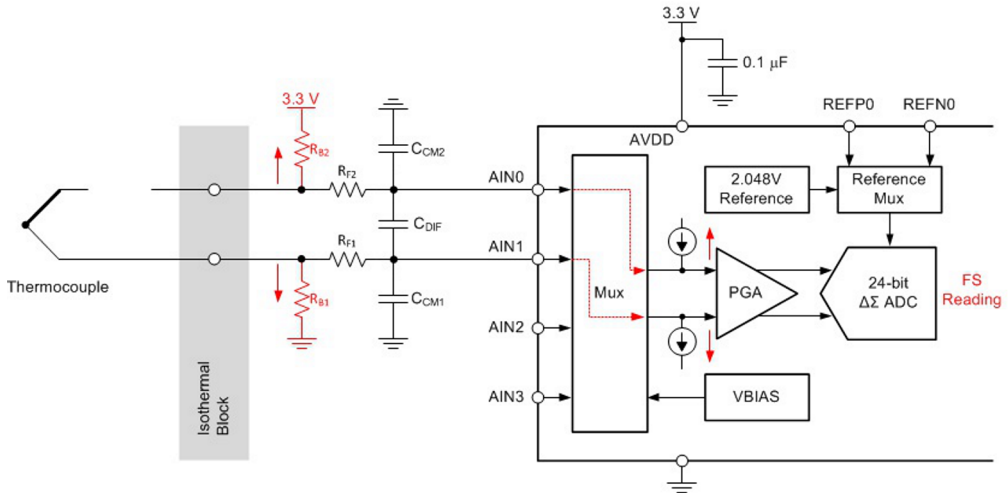


Figure 39. Biasing Resistors RB1 and RB2

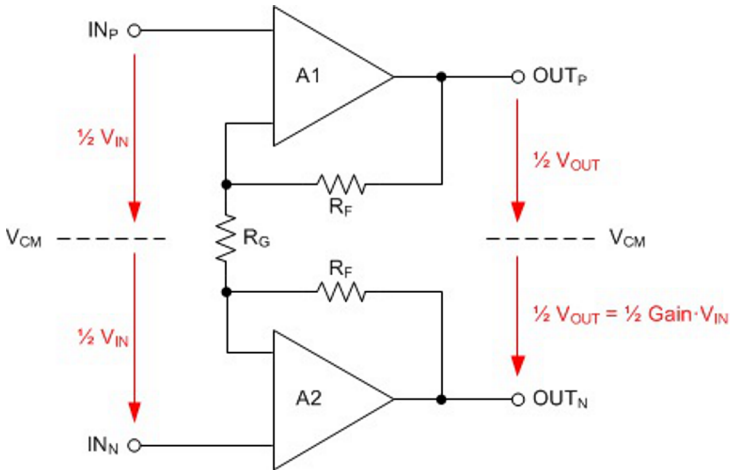


Figure 40. Common-Mode Voltage Limitation in the ADS1220

Referring to the equivalent circuit at the input of the ADS1220 shown in Figure 40, A1 and A2 are no rail-to-rail output amplifiers; They can only drive ~0.2V to the rails. Therefore, OUT_P and OUT_N have to be > (AVSS + 0.2V) or < (AVDD - 0.2V) at all times for the amplifiers to stay in their linear operating regions.

So,

$$V_{OUTN} = V_{CM} - ½Gain \times V_{IN} \geq AVSS + 0.2V$$
$$V_{CM} \geq AVSS + 0.2V + ½Gain \times V_{IN}$$

Accordingly,

$$V_{CM} \leq AVDD - 0.2V - ½Gain \times V_{IN}$$

Assuming there are no biasing resistors RB1 and RB2, the thermocouple signal is purely differential but is not biased to any voltage reference. Potentially the common mode (bias voltage) can be anywhere between 0 and 3.3V. This means the conditions for the common mode voltage can be violated. If the circuit is biased to just above ground or just below 3.3V to be in the specified range the circuit will work but there will be a resulting error due to the non-ideal CMRR (common mode rejection ratio) of the ADS1220. Being CMRR >90dB (see ADS1220 datasheet and Table 7), the resulting input error voltage (ΔV_{os}) can be calculated:

$$CMRR(dB) = 20\log_{10} (\Delta V_{cm}/\Delta V_{os})$$
$$\Delta V_{CM} = \Delta V_{CM} - (V_{DD}/2$$

Assuming a worst case condition, V_{CM} = 3.3V:

$$\Delta V_{CM} = 3.3 - (V_{DD}/2$$
$$\Delta V_{os} = \Delta V_{cm} \times 10^{-CMRR(dB)/20}$$
$$\Delta V_{os} < 52.18\ \mu V$$

Table 7. ADS1220CMRR Common-Mode Rejection Ratio

PARAMETER	TEST CONDITIONS	VALUE		
		MIN	TYP	UNIT
CMRR Common-mode rejection ratio	At dc and PGA = 1	90	105	dB
	f_{CM} = 50 Hz, DR = 2000 SPS	95	115	dB
	f_{CM} = 60 Hz, DR = 2000 SPS	95	115	dB

This error can be considered a pure offset at the input even bigger than the intrinsic m maximum offset voltage of the ADS1220 (30 µV in worst case). This is an additional reason to include RB1 and RB2 in the passive filter. Anyways when choosing the values of the biasing resistors, care must be taken so that the biasing current (flowing though the resistors) does not degrade measurement accuracy. First of all RB1 and RB2 have to be much bigger than the input filter resistor so that they do not influence the filter transfer function. Moreover, **the biasing current flows as well through the thermocouple where it can cause self-heating and additional voltage drops in the thermocouple leads.** RB1 and RB2, in addition to biasing the thermocouple, are also useful to detect an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs AIN0 and AIN1 to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

Based on these considerations, the biasing resistors are chosen in the range of **some Megohms.** This might lead to the wrong conclusion that they introduce high noise in the circuit.

The noise introduced by RB1 and RB2 can be represented with a series voltage source as shown in Figure 41.

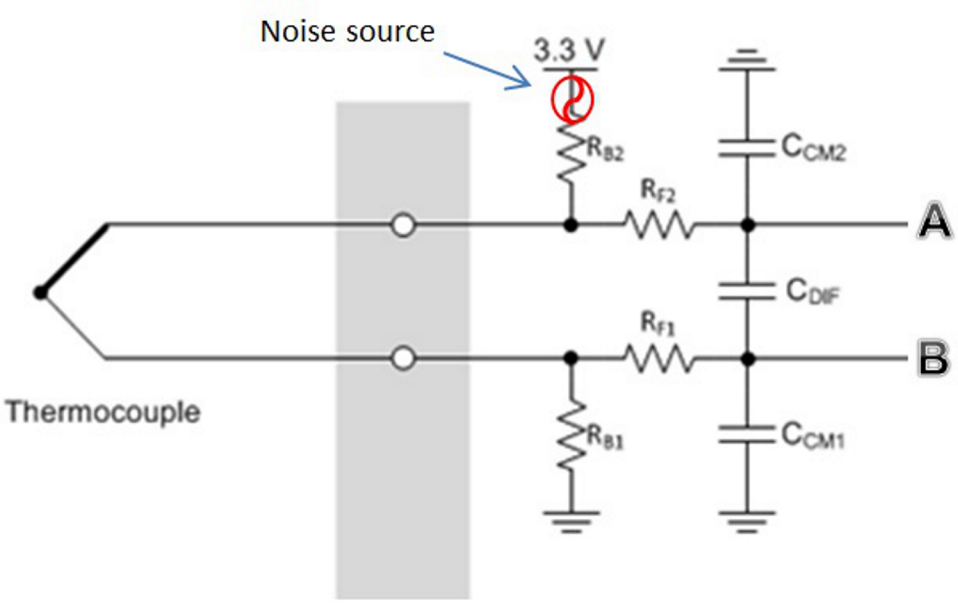


Figure 41. Biasing Resistors Noise Model

The circuit can be simplified after some considerations (see Figure 42).The Thermocouple can be considered as a short as first approximation. 3.3V is a DC so can be considered as ground for AC analysis or noise analysis. This means that R_{B1} and R_{B2} are in parallel for the noise. We can combine the two resistors into one (Rb × 2). And node A and B are in the same voltage level since the circuit is completely symmetrical. It means C_{DIFF} has a voltage drop of 0V and consequentially C_{CM1} is in parallel to C_{CM2} (Ccm × 2).

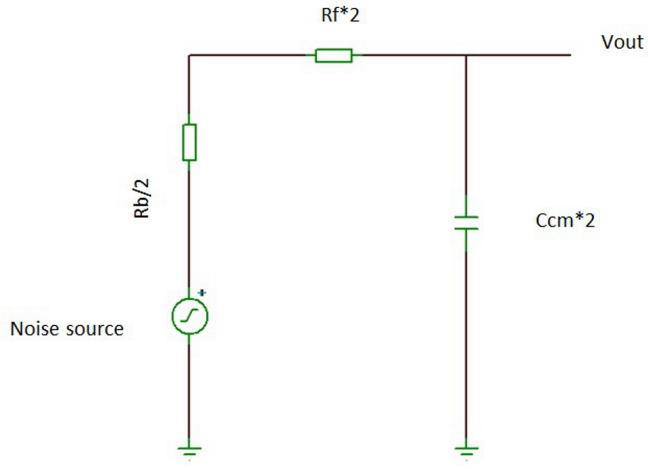


Figure 42. Simplified Circuit for R_{Bias} Noise

Also in this case, we want to keep their noise contribution to less than input-referred noise of the ADS1220 (0.23µV). Using the Johnson-Nyquist equation for resistor noise:

$$v_n = \sqrt{4kTR\Delta f}$$

Where: v_n = 0.23µV, T = 298K

$$\Delta f = \frac{1}{2\pi}\int_0^{\infty}\frac{d\omega}{1+(\omega 2 * C_{CM}R_1)^2} = \frac{\pi}{2\pi \times 4C_{CM}R_1} = \frac{1}{8C_{CM}R_1}$$

$$R_1 = \frac{R_{B1}}{2} + R_{F1} * 2$$

$$v_n = \sqrt{4kTR_1\frac{1}{8C_{CM}R_1}}$$

$$v_n = \sqrt{\frac{kT}{2C_{CM}}}$$

$$v_n^2 = \frac{kT}{2C_{CM}}$$

$v_n \le V_{rms}$, so

$$C_{CM} \ge kT/(0.0529(\mu V)^2 \times 2) = 0.0385\mu F$$

It means that as showed already the noise of R_{B1} is not related to the value itself, but related to the value of C_{CM}. We chose C_{CM} as 0.27µF, which is much bigger than the C_{CM} value we need. **So there is not a limit on the value for R_{B1} based on noise considerations.**

The main constraint on the biasing resistors is then coming from the current they inject into the thermocouple. For this design, a value of **2MΩ** has been selected. In this case, the current that will flow on the Thermocouple can be easily calculated:

$$I_{error} = AVDD/(R_{PU} + R_{PD}) = 3.3V/4M\Omega = 0.825\mu A$$

The input referred error depends on the current and on the total resistance of the Thermocouple (summarized in Table 8).

Table 8. Thermocouple Lead Resistance by Type and Wire Size

AWG No.	Diameter (inches)	ISA Type K Chromel-P/ Alumel	ISA Type J Iron/ Constantan	ISA Type T Copper/ Constantan	ISA Type E Chromel/ Constantan	ISA Type N Nicrosil/ Nisil	ISA Type S PT-PT 10% RH	ISA Type R PT-PT 13% RH
8	.1285	.0365	.2185	.0186	.0437	.0485	.011	.011
12	.0808	.0916	.0533	.0455	.1099	.1225	.028	.029
14	.0641	.1466	.085	.0735	.1752	.1947	.045	.047
16	.0508	.2331	.136	.117	.2775	.3100	.071	.073
18	.0403	.3706	.218	.1874	.4454	.4926	.116	.119
20	.0320	.5894	.349	.2991	.7030	.7812	.185	.190
22	.0253	.9368	.544	.4751	1.1206	1.2498		
24	.0201	1.4901	.878	.7526	1.78	1.980	.464	.478
26	.0159	2.3811	1.405	1.204	2.836	3.164	.740	.760
28	.0126	3.768	2.235	1.9159	4.512	5.039		
30	.0100	5.984	3.551	3.0431	7.169	8.000	1.85	1.91

Assuming a Type K thermocouple having AWG number 26 with 10m (32 feet) length:

$$R = 32 \times 2.3811 = 76\Omega$$

So the resulting voltage error is:

$$0.825\mu A \times 76\Omega = 62.7\mu V$$

This corresponds to roughly 1.58°C and compared to the offset error of ADS1220 (4µV typical, 30µV max), this error cannot be neglected. Obviously, this is just an offset and **can be calibrated out at system level**.

Unfortunately, the resistor drift introduces a non-systematic error.

The offset drift of the ADC is only 0.08µV/°C(max 0.3µV/°C).

Considering as an example the a thermocouple resistance $R_{TC} = 100\Omega$

and a drift of R_{B1}:

$$(100ppm/°C) \times 65°C = 0.65\%$$

$$I_{offset\ drift} = [3.3V/(4M\Omega(1-0.65\%))] - 0.825\mu A = 0.0054\mu A$$

So the resulting error is:

$$100\Omega \times 0.0054\mu A = 0.54\mu V$$

Consider the TC resistance can go as high as some kΩ, the offset drift will deteriorate the ADC1220 performances if only 0.08µV/°C (max 0.3µV/°C). **This implies that this topology has to be improved.**

Placing R_{B1} and R_{B2} on only one end of the Thermocouple (see Figure 43) will allow for better results.

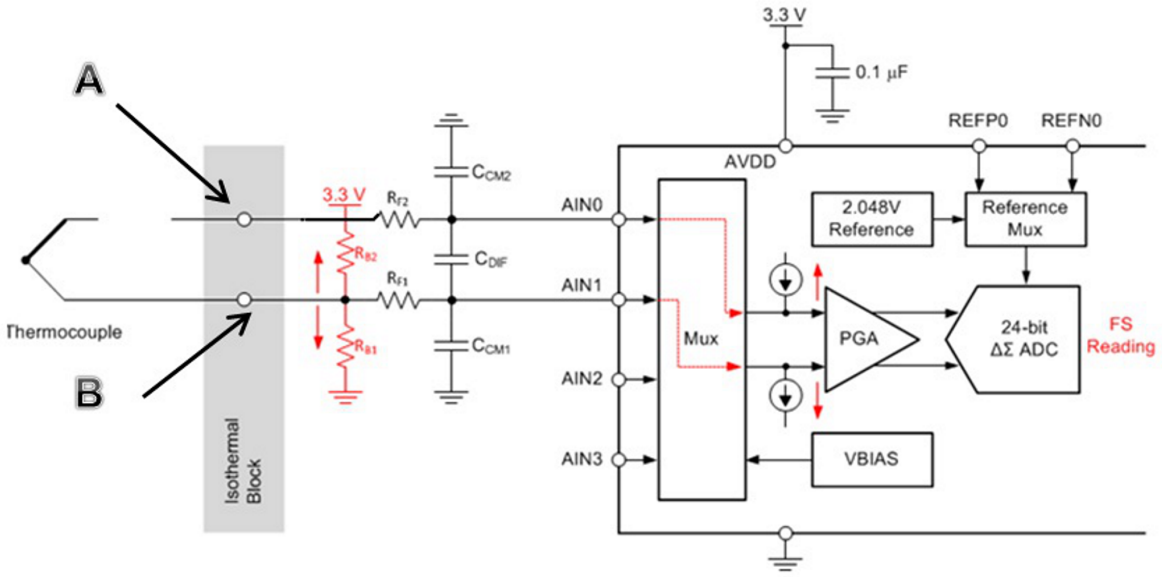


Figure 43. Improved Biasing Circuit

In this circuit configuration, there will be **no current flowing in the thermocouple** itself. The only drawback is a small change in the common mode of the input signal that is now not biased at Vdd/2 anymore.

V_{CM} is,

$$V_A = (V_{DD}/2) + V_{diff}$$
$$V_B = V_{DD}/2$$
$$V_{CM} = (V_A + V_B)/2 = (V_{DD}/2 + V_{diff}/2)$$

$\Delta V_{CM} = (V_{CM} - 1)/2V_{DD} = V_{diff}/2$

The thermocouple can go to 1375°C, so the maximum input voltage (see Section 5.2) is 54.889mV.

$\Delta V_{CM} = V_{diff}/2 = 27.44mV$

$$\Delta V_{os} = \Delta V_{cm} \times 10^{-CMRR(dB)/20}$$
$$\Delta V_{os} = 0.86\mu V$$

This error has to be compared with the offset voltage of ADS1220 4µV (max 30µV), being 0.86 < 4, this error does not degrades too much the front end performances.

Now, having a known common mode value, the error introduced by the mismatched input filter resistors can be calculated according to the considerations done in Section 9.10 (refer to Figure 38):

$$V_{CM} = 43.9445mV$$
$$V1 = [V_{CM}/(R_{F1} + \Delta R + ½RZ)] \times ½RZ = 43.93562mV$$
$$V2 = [V_{CM}/(R_{F1} + ½RZ)] \times ½RZ = 43.93580mV$$
$$V_{error} = V1 - V2 = 0.18\mu V$$

This result is also negligible compared to the ADS1220 offset specifications. The drift of the 2 R_B should be simultaneous, if they are placed close to each other so there is no impact on the measurement.

9.12 Total Filter Error

Summarizing all the above contributions:

1. Noise: R_F 0.029µV, R_B 0.0872µV
2. Inaccuracy of capacitor: 0.001 µV
3. Filter error: 11µV
4. R_F mismatch: 0.18µV
5. Inaccuracy of R_F: 0.11µV
6. Drift of R_F: 0.123µV
7. Offset error: 0.86 µV
8. Inaccuracy of R_B: 0.529 µV

And summing them:

$$Total\ filter\ error = \sqrt{0.029^2 + 0.0872^2 + 0.001^2 + 11^2 + 0.18^2 + 0.11^2 + 0.123^2 + 0.86^2 + 0.529^2} = 11.05$$

Corresponding to a temperature of ~0.279°C

Most of this error is deterministic and can be calibrated out. Only the drift and noise will stay after the calibration.

$$Total\ ideal\ calibrated\ filter\ error = \sqrt{0.029^2 + 0.0872^2 + 0.123^2} = 0.154$$

Corresponding to ~0.004°C

10 Thermocouple Channel Error Calculation

As for the filters, the main design target is to keep initial error contribution to the total error comparable or smaller than the initial error of the thermocouple sensor itself. Considering the manufacturing limitations of the Type K thermocouple (mainly related to the purity of materials), the initial error of the Thermocouple sensor (tolerance class 1) is typically **smaller than 1.5°C between -200°C and 375°C and then better than 0.4% up to 1375°C (maximum thermocouple temperature range).** See Section 5.1.

The error calculation is then split in two parts. Low temperature (-200°C to 375°C) and high temperature (from 375°C to 1375°C) to make a direct comparison with the sensor initial accuracy. Considering the low temperature range, the maximum differential input signal is 15.34mV and the minimum is -3.554mV.

So in this range:

$$\text{sensitivity} = [15.34\text{mV} - (-3.554\text{mV})]/[375°\text{C} - (-100°\text{C})] = 39.77\mu\text{V}$$

Based on that, the ADS1220 specifications can be translated into temperature (typical values).

10.1 Error in Typical Corner

The initial errors at 25°C (those that can be corrected by calibrating the system) are:

1. **Offset error:** 4µV

   Corresponding to 4µV/(39.77µV/°C) = 0.10°C
2. **Gain error:** 150ppm

   Corresponding to (150ppm × 15.34mV)/(39.77µV/°C) = 0.06°C
3. **Reference voltage accuracy** can be calculated as follows:

   $$\text{Inaccuracy} = [(2.048 - 2.045)/((2.048 + 2.045)/2)] \times 100\% = 0.1465\%$$

   Considering that for an ADC:

   $$\text{CODE} = V_{IN} \times (2^{24}/V_{REF})$$

   This will translate into an additional gain error:

   $$\text{error}(\mu\text{V}) = (V_{IN}/(1 - 0.1465\%)) - V_{IN} = 22.5\mu\text{V}$$

   Corresponding to 22.5µV/(39.77µV/°C) = 0.566°C
4. **INL (Integral nonlinearity):** 6ppm

   The error of INL with respect to the input signal is:

   $$\text{error}(\mu\text{V}) = 6\text{ppm} \times \text{full scale} = 6\text{ppm} \times ((2 \times V_{REF})/\text{PGA})) = 0.77\mu\text{V}$$

   Corresponding to 0.77µV/(39.77µV/°C) = 0.02°C

In addition, there are **all drift errors and non-deterministic errors** (for example, noise) that cannot be corrected by calibration. Being the initial or nominal operating temperature of the system is 25°C while the temperature range is from -40°C to 85°C, maximum temperature span is $\Delta\mathbf{T}$ = 25 - (-40) = 65°C.

1. **Offset drift:** 0.08µV/°C

   The offset drift in ADS1220 temperature span is:

   $$V_{\text{offset drift}} = (0.08\mu\text{V/°C}) \times 65°\text{C} = 5.2\mu\text{V}$$

   Corresponding to 5.2µV/(39.77µV/°C) = 0.13°C
2. **Gain drift:** 1ppm/°C

   The gain drift in ADS1220 temperature span is:

   $$V_{\text{gain drift}} = V_{IN}((1\text{ppm/°C}) \times 65°\text{C}) = V_{IN} \times 65\text{ppm} = 0.996\mu\text{V}$$

   Corresponding to 0.996µV/(39.77µV/°C) = 0.025°C

3. **Reference drift:** 5ppm/°C

$$V_{reference\ drift} = V_{REF}((5ppm/°C) \times 65°C) = V_{REF} \times 325ppm = 665.6\mu V$$
$$CODE = V_{IN} \times (2^{24}/(V_{REF} + V_{reference\ drift}))$$
$$CODE = V_{IN} \times (2^{24}/(V_{REF}(1 + drift\%)))$$
$$drift\% = (V_{reference\ drift}/V_{REF}) \times 100\% = 0.0325\%$$

So

$$error(\mu V) = V_{IN} - (V_{IN}/(1 + 0.0325\%)) = 4.98\mu V$$

Corresponding to 4.98µV/(39.77µV/°C) = 0.125°C

4. **ADC-PGA noise:** 0.23µV

Corresponding to 0.23µV/(39.77µV/°C) = 0.006°C

So we can add up the errors, and then get the **total un-calibrated** errors from **-100°C to 375°C (considering maximum ambient temperature span** Δ**T** = 25 - (-40) = 65°C).

$$Typ\ non-calibrated\ error < \sqrt{0.1^2 + 0.06^2 + 0.566^2 + 0.02^2 + 0.13^2 + 0.025^2 + 0.125^2 + 0.006^2} = 0.61°C$$

After system calibration, only offset drift, Gain drift, and Reference drift are left. So:

$$Typ\ IDEAL\ CALIBRATED = \sqrt{0.13^2 + 0.025^2 + 0.125^2 + 0.006^2} = 0.18°C$$

Looking at the high temperature (375°C to 1375°C), the maximum differential input signal is 54.886mV in the look up table for 1375°C.

Sensitivity of the thermocouple: 39.543µV/°C, so:

$$sensitivity = (54.886 - 15.343)/(1375 - 375) = 39.543\mu V/°C$$

1. **Offset error:** 4µV

Corresponding to 4µV/(39.543µV/°C) = 0.10°C

2. **Gain error:** 150ppm

Corresponding to (150ppm × 54.886mV)/(39.543µV/°C) = 0.21°C

3. **Reference voltage accuracy:** 0.1465%

$$error(\mu V) = (V_{IN}/(1 - 0.1465\%)) - V_{IN} = 80.34\mu V$$

Corresponding to 80.34µV/(39.543µV/°C) = 2.03°C

4. **INL (Integral nonlinearity):** 6ppm

The error of INL with respect to the input signal is

$$error(\mu V) = 6ppm \times full\ scale = 6ppm \times ((2 \times V_{REF})/PGA) = 0.77\mu V$$

Corresponding to 0.77µV/(39.543µV/°C) = 0.02°C

As before, all **drift errors and non-deterministic** errors can be calculated as follows (maximum temperature span is Δ**T** = 25 - (-40) = 65°C.

1. **Offset drift:** 0.08µV/°C

$$V_{offset\ drift} = (0.08\mu V/°C) \times 65°C = 5.2\mu V$$

Corresponding to 5.2µV/(39.543µV/°C) = 0.13°C

2. **Gain drift:** 1ppm/°C

$$V_{gain\ drift} = V_{IN}((1ppm/°C) \times 65°C) = V_{IN} \times 65ppm = 3.57\mu V$$

Corresponding to 3.57µV/(39.543µV/°C) = 0.09°C

3. **Reference drift:** 5ppm/°C

$$V_{reference\ drift} = V_{REF}((5ppm/°C) \times 65°C) = V_{REF} \times 325ppm = 665.6\mu V$$

$$CODE = V_{IN} \times (2^{24}/(V_{REF} + V_{reference\ drift}))$$

$$CODE = V_{IN} \times (2^{24}/(V_{REF}(1 + drift\%)))$$

$$drift\% = (V_{reference\ drift}/V_{REF}) \times 100\% = 0.0325\%$$

So

$$error(\mu V) = V_{IN} - (V_{IN}/(1 + 0.0325\%)) = 17.83\mu V$$

Corresponding to 17.83µV/(39.543V/°C) = 0.451°C

4. **ADC-PGA noise:** 0.23µV

Corresponding to 0.23µV/(39.543µV/°C) = 0.006°C

So we can add up the errors, and then get the **total un-calibrated** errors from **375°C to 1375°C (considering maximum ambient temperature span** Δ**T** = 25 - (-40) = 65°C.

$$Typ\ non-calibrated\ error < \sqrt{0.1^2 + 0.21^2 + 2.03^2 + 0.02^2 + 0.13^2 + 0.09^2 + 0.451^2 + 0.006^2} = 2.10°C$$

While

$$Typ\ IDEAL CALIBRATED = \sqrt{0.13^2 + 0.09^2 + 0.451^2 + 0.006^2} = 0.478°C$$

From the above, it is evident that the value of gain error, reference voltage accuracy, gain drift, reference drift is related to the value of V_{IN}, and the value of offset error, INL, offset drift is fixed. It means that the total error is a functional of V_{IN}.

Figure 44 summarize all the results in a graph comparing the Thermocouple sensor accuracy to the one of the front end for calibrated and non-calibrated systems at maximum ΔT and typical and worst case conditions. This shows that the acquisition system is not the dominant contributor to the total accuracy even when no calibration is performed.

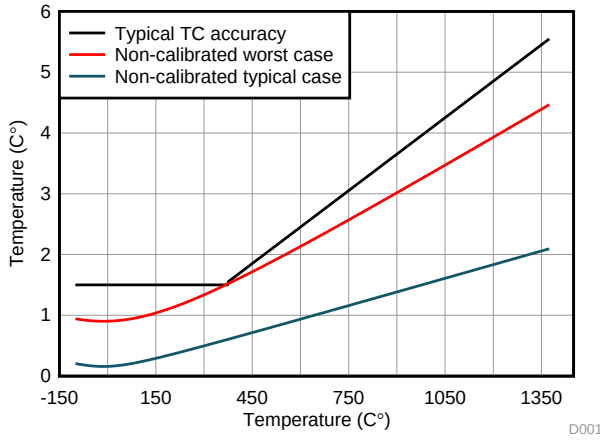


Figure 44. Calculated Error in °C as a Function of the Measured Temperature

10.2 Error in Worst Case Corner

Considering the **worst case corners specifications:**

- Offset error: 30µV
- Gain error: 1000ppm
- INL: 15ppm
- Offset drift: 0.3µV/°C
- Gain drift: 4ppm/°C
- Reference drift: 40ppm/°C (characterization suggest this number is more likely in the range of 25ppm/°C)

Based on the same calculations explained before:

- Temperature range (-100°C to 375°C)
- Offset error: 0.754°C
- Gain error: 0.386°C
- Reference voltage accuracy: 0.556°C
- INL: 0.05°C
- Offset drift: 0.49°C
- Gain drift: 0.10°C
- Reference voltage drift: 1.0°C
- ADC-PGA noise: 0.006°C

All the errors are added up as ideal un-calibrated.

$$Max\ non-calibrated\ error < \sqrt{0.754^2 + 0.386^2 + 0.556^2 + 0.05^2 + 0.49^2 + 0.10^2 + 1.0^2 + 0.006^2} = 1.51°C$$

$$Max\ IDEAL\ CALIBRATED = \sqrt{0.05^2 + 0.49^2 + 0.10^2 + 1.0^2 + 0.006^2} = 1.12°C$$

- Temperature range (375°C to 1375°C)
- Offset error: 0.754°C
- Gain error: 1.39°C
- Reference voltage accuracy: 2.03°C
- INL: 0.05°C
- Offset drift: 0.49°C
- Gain drift: 0.361°C
- Reference voltage drift: 3.60°C
- ADC-PGA noise: 0.006°C

$$Max\ non-calibrated\ error < \sqrt{0.754^2 + 1.39^2 + 2.03^2 + 0.05^2 + 0.49^2 + 0.361^2 + 3.60^2 + 0.006^2} = 4.47°C$$

$$Max\ IDEAL\ CALIBRATED = \sqrt{0.05^2 + 0.49^2 + 0.361^2 + 3.60^2 + 0.006^2} = 3.65°C$$

Typical calibrated thermocouple sensors can be as accurate as 0.25°C up to 150°C and better than 0.2% at higher temperatures (see blue curve in Figure 45). This front end typical error stays below 0.12°C up to 150°C and below 0.03% in the higher temperature range.

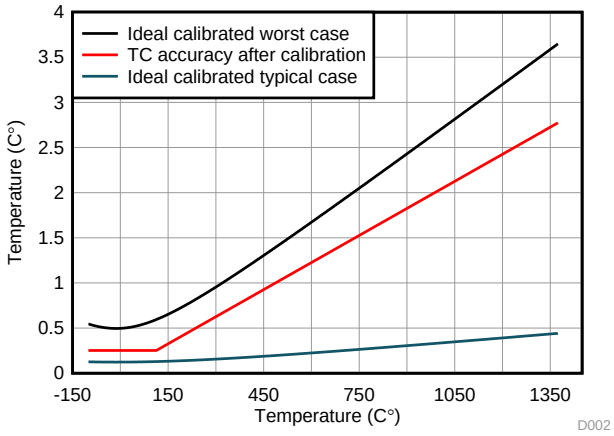


Figure 45. Calculated Error in °C as a Function of the Measured Temperature in a Calibrated System

11 RTD Channel Error Calculation

As mentioned already, an RTD is used as cold junction compensation in the range of -40°C to 85°C. A two-wire connection with one current source of 250µA is implemented. The reading is a ratiometric reading. The ADS1220 uses an external reference that is built injecting the same excitation current used for the RTD in a precise, low drift reference resistor (R_{REF} = 6490Ω). By doing that, the measured value is independent form the precision of the current itself but is only related to the ratio of the 2 resistors (RTD and reference resistor). Please refer to TIDA-00165 for detailed description.

From the RTD (Pt100) look up table (see Section 5.4), the minimum and maximum resistance values in our temperature range can be found. These are, respectively, **84.27Ω** to **130.9Ω** (-40°C to 85°C).

So minimum and maximum voltage input are:

$$V_{min} = 84.27\Omega \times 250\mu A/1000 = 21.0675mV$$
$$V_{max} = 130.9\Omega \times 250\mu A/1000 = 32.725mV$$

So, the ADC input voltage to temperature relation is:

$$V_{change} = (32.725mV - 21.0675mV)/(85°C - (-40°C)) = 0.09326mV/°C$$

1. **Offset error:** 4µV
   Corresponding to 4µV/(93.26µV/°C) = 0.043°C
2. **Gain error:** 150ppm

   $$32.725mV \times 150ppm/1000 = 4.9087\mu V$$

   Corresponding to 4.9087µV/(93.26µV/°C) = 0.052°C
3. **Reference resistor accuracy:** 0.1%

   $$\text{maximum variation of } R_{ref} = 6490\Omega \times 0.1\% = 6.49\Omega$$

   The maximum change in voltage is: 6.49Ω × 250µA = 1.6225mV

   $$CODE = V_{IN} \times (2^{24}/(V_{REF} + V_{reference\ change}))$$
   $$CODE = V_{IN} \times (2^{24}/(V_{REF}(1 + accuracy\%)))$$
   $$accuracy\% = (V_{reference\ change}/V_{REF}) \times 100\% = 0.1\%$$

   So

   $$error(\mu V) = V_{IN} - (V_{IN}/(1 + 0.1\%)) = 32.69\mu V$$

   Corresponding to 32.69µV/(93.26µV/°C) = 0.35°C
4. **INL (Integral nonlinearity):** 6 ppm
   The error of INL with respect to the input signal is

   $$error(\mu V) = 6ppm \times \text{full scale} = 6ppm \times ((2 \times V_{REF})/PGA) = 0.608\mu V$$

   Corresponding to 0.608µV/(93.26µV/°C) = 0.0065°C

All **drift errors and non-deterministic** errors can be calculated as follows (being a ratiometric measurement, maximum Δ**T** is at 85°C and is **equal to** 85°C -25°C = 60°C).

1. **Offset drift:** 0.08µV/°C

   $$V_{offset\ drift} = (0.08\mu V/°C) \times (85°C - 25°C) = 4.8\mu V$$

   Corresponding to 4.8µV/(93.26µV/°C) = 0.0515°C

2. **Gain drift:** 1ppm/°C

$$V_{gain\ drift} = V_{IN}((1ppm/°C) \times 60°C) = V_{IN} \times 60ppm = 1.96\mu V$$

Corresponding to 1.96µV/(93.26µV/°C) = 0.021°C

3. **Reference drift:** 10ppm/°C

$$V_{reference\ drift} = V_{REF}((10ppm/°C) \times 60°C) = V_{REF} \times 600ppm = 973.5\mu V$$

$$CODE = V_{IN} \times (2^{24}/(V_{REF} + V_{reference\ drift}))$$

$$CODE = V_{IN} \times (2^{24}/(V_{REF}(1 + drift\%)))$$

$$drift\% = (V_{reference\ drift}/V_{REF}) \times 100\% = 0.06\%$$

So

$$error(\mu V) = V_{IN} - (V_{IN}/(1 + 0.06\%)) = 19.62\mu V$$

Corresponding to 19.62µV/(93.26V/°C) = 0.21°C

4. **ADC-PGA noise:** 0.23µV

Corresponding to 0.23µV/(93.26µV/°C) = 0.002°C

As a result the total **non-calibrated errors is:**

$$Typ\ non-calibrated\ error < \sqrt{0.043^2 + 0.052^2 + 0.35^2 + 0.0065^2 + 0.0515^2 + 0.021^2 + 0.21^2 + 0.002^2} = 0.419°C$$

The ideal calibrated system error is obtained summing only offset drift, Gain drift, Reference drift, and noise:

$$Typ\ IDEAL\ CALIBRATED = \sqrt{0.021^2 + 0.0515^2 + 0.21^2 + 0.002^2} = 0.217°C$$

Non-calibrated and calibrated error from -40°C to 85°C are shown in Figure 46.

Considering now the **worst case corners specifications:**

$$Max\ non-calibrated\ error < \sqrt{0.322^2 + 0.351^2 + 0.351^2 + 0.016^2 + 0.19^2 + 0.08^2 + 0.21^2 + 0.002^2} = 0.662°C$$

$$Max\ IDEAL\ CALIBRATED = \sqrt{0.016^2 + 0.19^2 + 0.08^2 + 0.21^2 + 0.002^2} = 0.298°C$$

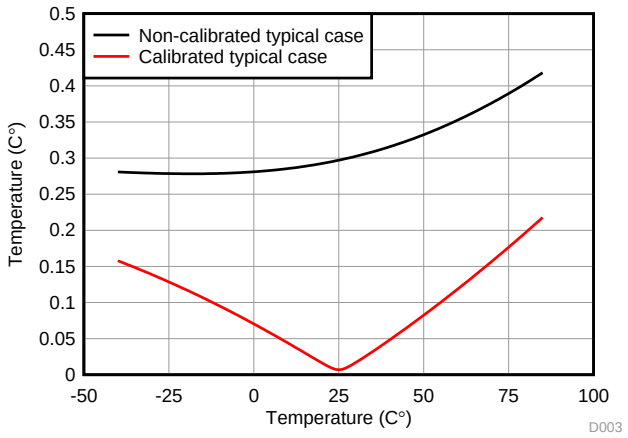


Figure 46. Typical Calibrated and Non-Calibrated Error of RTD

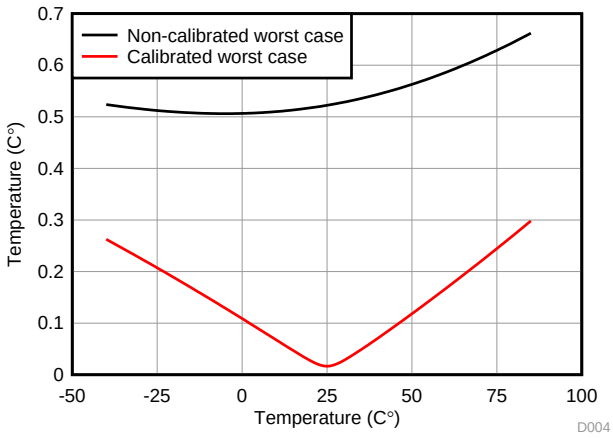


Figure 47. Worst Case Calibrated and Non-Calibrated Error

12 Total Error Calculation (Filters, Thermocouple, and RTD)

The total error will be the result of all the above calculations.

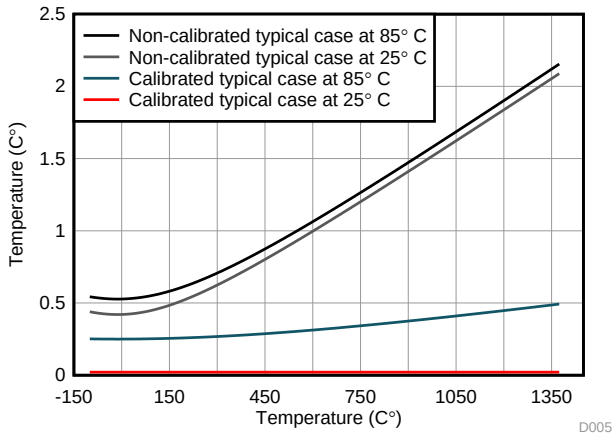


Figure 48. Typical Calibrated and Non-Calibrated Total Front End Error (at 25°C and 85°C)

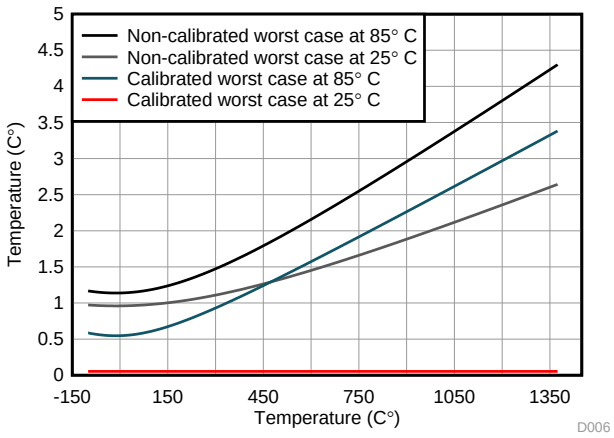


Figure 49. Worst Case Calibrated and Non-Calibrated Total Front End Error (at 25°C and 85°C)

13 Look Up Table Error Contribution

It is often considered that SW is a black box which does not impact the total accuracy of the system and that it may even improve performances thanks to averaging, damping, diagnostics, sensor linearization and temperature compensation capabilities.

However one should carefully consider this assumption. For instance the ITS-90 defines polynomial equations of the 10th degree and exponential component for Thermocouple type K, however most sensor transmitter do not compute those polynomial equations and even less the exponential compensation. The most selected solution is look-up tables with linear interpolation between the data-points as described before.

As an example, the following two pictures show the maximum error over the temperature range in two extreme cases in terms of definition of the look-up tables.

While the details of defining the look-up tables goes beyond the scope of this design guide, one should ensure like this was done for this design that the total contribution of the SW when computing the temperature (thermocouple voltage read, RTD temperature read, thermocouple cold junction compensation) is negligible towards the total error budget.

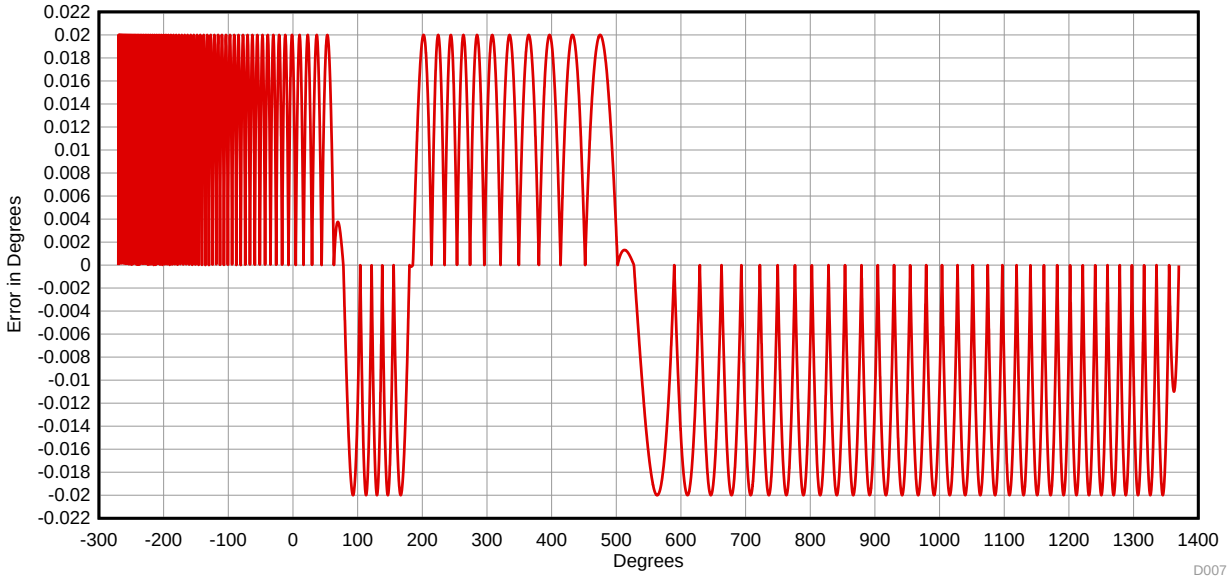


Figure 50. Examples of the Error Intruded by the Software by Using Different Look Up Tables

14 MCU Operation and Software Design

14.1 Software

This code runs on a MSP430F5172 and is designed to implement an isolated Thermocouple Temperature Transmitter application highlighting the ADS1220. The temperature reading is sent out on a 4-20mA signal using the DAC161P997. The data link to the DAC161P997 is a Single Wire Interface (SWIF) which allows sensor data to be transferred in digital format over an isolation boundary using a single isolation component. This code also addresses system-level calibration - both offset and gain that can be implemented to improve ADC and DAC accuracy as well as also includes linear interpolation to address the non-linearity of the TC and RTD element which is used for CJC.

14.2 Software Flow

The calculation procedure to achieve cold junction compensation is simple and can be done in several ways. One typical way is to interleave readings between the thermocouple inputs and the RTD inputs. This needs one RTD result for every thermocouple ADC voltage measured. If the cold junction is in a very stable environment, more periodic cold junction measurements may be sufficient. These operations, in turn, will yield two results for every thermocouple measurement and cold junction measurement cycle: the thermocouple voltage or V_{TC}, and the RTD voltage or V_{RTD}. In order to account for the cold junction, the RTD voltage must first be converted into temperature and the temperature is then converted to a voltage that is proportional to the thermocouple currently being used, to yield V_{CJC}. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding the two voltages then yields the thermocouple-compensated voltage V_{Actual}, where $V_{CJC} + V_{TC} = V_{Actual}$. V_{Actual} is then converted to temperature using the same lookup table from before, and yields T_{Actual}. A block diagram showing this process is given in Figure 51.

The offset drift of the ADS1220 can be minimized by doing two measurements and swapping the two inputs for the second measurements. Taking a measurement in both configurations and averaging the two readings will greatly reduce the effects of the offset drift. This "chopping technique" is used for Thermocouple measurement and RTD measurement.

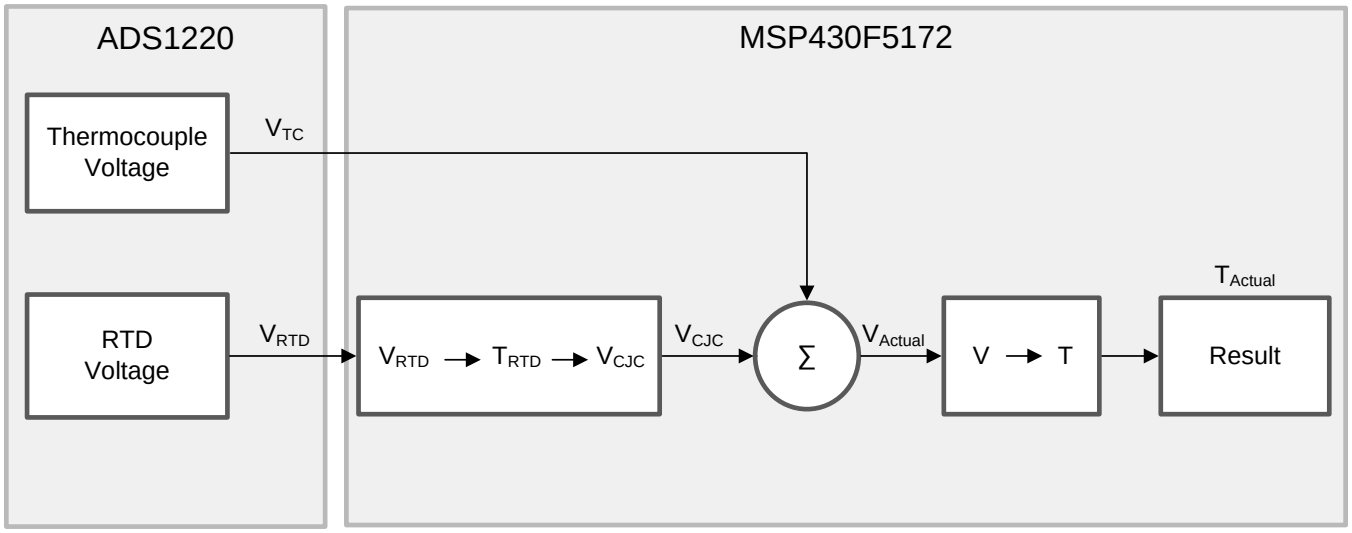


Figure 51. Software Flow Diagram for Thermocouple Linearization

14.3 Software Update

For MSP430 Firmware updates, Code Composer Studio is recommended. Code Composer Studio™ (CCStudio) is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. For Programming and Debugging, the MSP430F5172 implements an Embedded Emulation Module (EEM). It is accessed and controlled through either 4-wire JTAG mode or Spy-Bi-Wire mode. On this Reference Design, the Spy-Bi-Wire mode is supported only. For more details on how the features of the EEM can be used together with Code Composer Studio (CCS), see SLAA393. The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data input/output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For Programming and debugging purposes the SBWTCK, SBWTDIO, VCC and GND from the Debugger needs to be connected on J8 (see Figure 52).

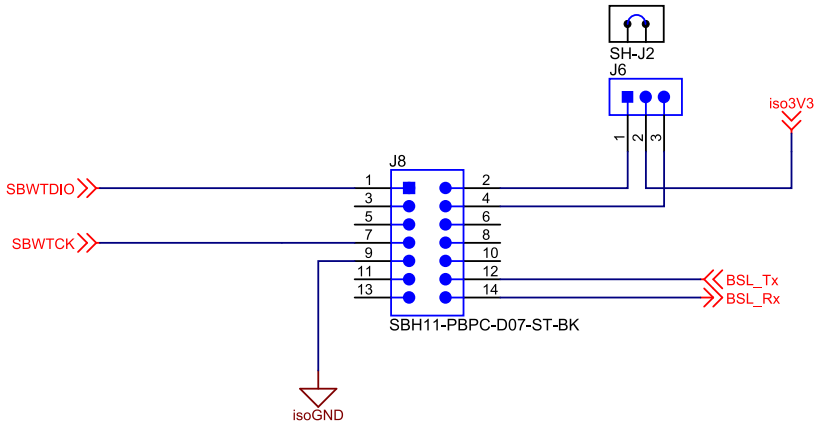


Figure 52. JTAG Connection

With the proper connections, a MSP430 Debugger Interface (such as the MSP-FET) can be used to program and debug code on the Reference Design.

CAUTION

Special care should be taken during debug to avoid damages due to different power domain in conflicts (TPS71733DSE power and debugger tools power), read following section carefully.

14.3.1 Power During Debugging

The TPS71733DSE supplies 3.3V to the MSP430F5172, if a voltage in the range of 9V to 30V is supplied to the 4-20mA loop. Normally the MSP430F5172 is powered from this 3.3V.

If this local 3.3V supply from the TPS71733DSE is used during debug, make sure pin 2 and pin 3 are connected on jumper J6. If there is no local power and power from the Debugger Interface is used, make sure pin 1 and pin 2 are connected on jumper J6 (see Figure 52).

14.4 Software Files

To download the software files for the reference design, see the design files at TIDA-00189.

15 DAC Design (4-20mA Output)

To better understand the design criteria for the 4-20mA loop using DAC161x997 family, refer to TIDA-00165, Chapter 5.5.

The main difference between DAC161S997 (used in TIDA-00165) and DAC161P997 (used in this design) is the **isolated signal path leveraging the SWIF (Single Wire Interface)**. See Figure 53.

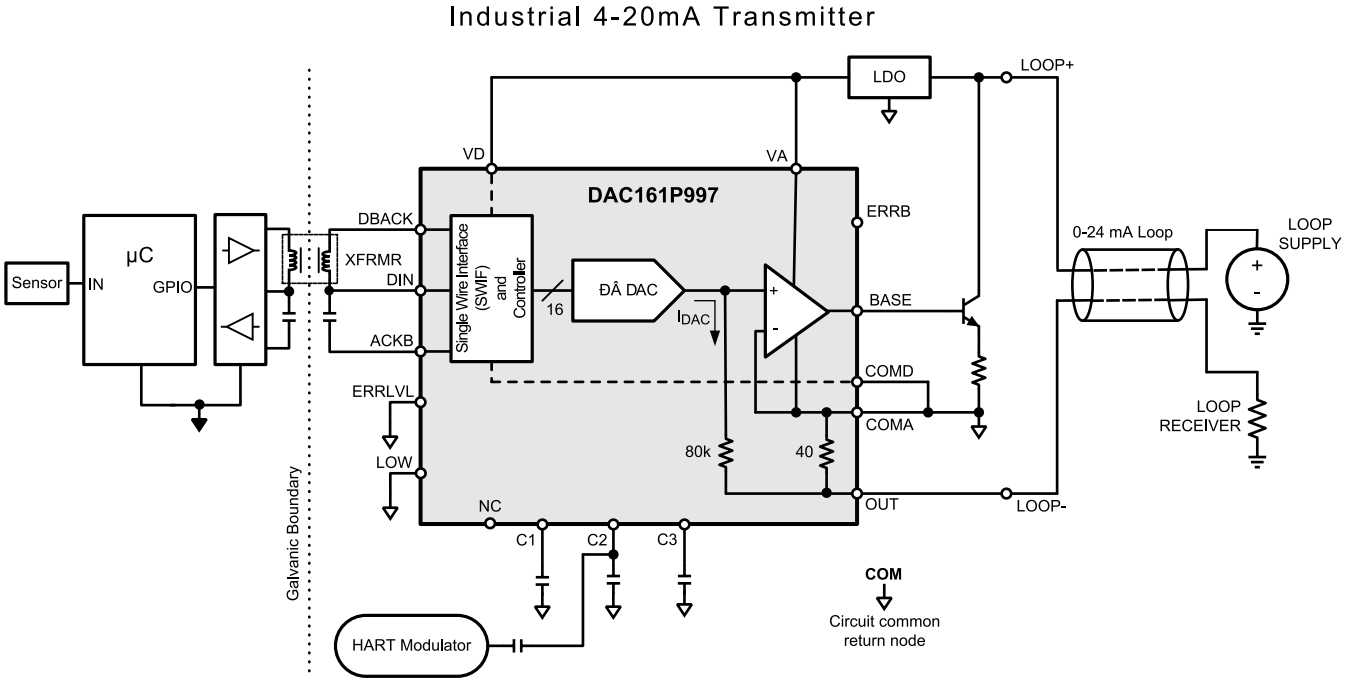


Figure 53. Simplified Diagram for Data Transmission from the MCU to the DAC

15.1 Single-Wire Interface (SWIF)

SWIF is a versatile and robust solution for transmitting digital data over the galvanic isolation boundary using just one isolation element: a pulse transformer. Digital data format achieves the information transmission without the loss of fidelity which usually afflicts transmissions employing PWM (Pulse Width Modulation) schemes. Digital transmission format also makes possible data differentiation: user can specify whether given data word is a DAC input to be converted to loop current, or it is a device configuration word. SWIF was designed to use in conjunction with pulse transformer as an isolation element. The use of the transformers to cross the isolation boundary is typical in the legacy systems due to their robustness, low-power consumption, and low cost. However, system implementation is not limited to the transformer as a link since SWIF easily interfaces with opto-couplers, or it can be directly driven by a CMOS gate. SWIF incorporates a number of features that address robustness aspect of the data link design:

- Bidirectional signal flow: the DAC161P997 can issue an ACKNOWLEDGE pulse back to the master transmitter, via the same physical channel, to confirm the reception of the valid data
- Error Detection: SWIF protocol incorporates frame length detection and parity checks as a method of verifying the integrity of the received data
- Channel Activity Detection: SWIF can monitor the data channel and raise an error flag should the expected activity drop below programmable threshold, due to , for example, damage to the physical channel

In the typical system, the Master is a microcontroller. SWIF has been implemented on a number of popular microcontrollers where it places minimum demands on the hardware or software resources even of the simple 8-bit devices. SWIF gives the system designer flexibility is balancing the trade-offs between the data rate, activity monitoring functionality and the power consumption in the transformer coupled data channel. At lowest data rates, with long inactive inter-frame periods, the power consumed by SWIF is negligible.

More detailed information on the implementation of the interface can be found in the DAC161P997 datasheet.

15.2 Loop Current Compliance and NAMUR

One important point to underline is the compliance of this design with NAMUR. NAUMAR NE43 is an international association of process instrumentation user companies who has worked on improving the diagnostic coverage in 4 to 20mA analog output transmitters to address associated safety issues. It provides the guideline for signaling failure information to the safety interlock systems over 4 to 20mA loop. It recommends using 3.8mA to 20.5mA as an extended measurement information range, whereas loop current below 3.6mA or above 21mA to be interpreted as diagnostic failure information range. Choose $I_{LOOP\ (MAX)}$ = 24mA, depending upon DAC capability and also to comply with NAUMAR NE43 recommendation as shown in Figure 54.

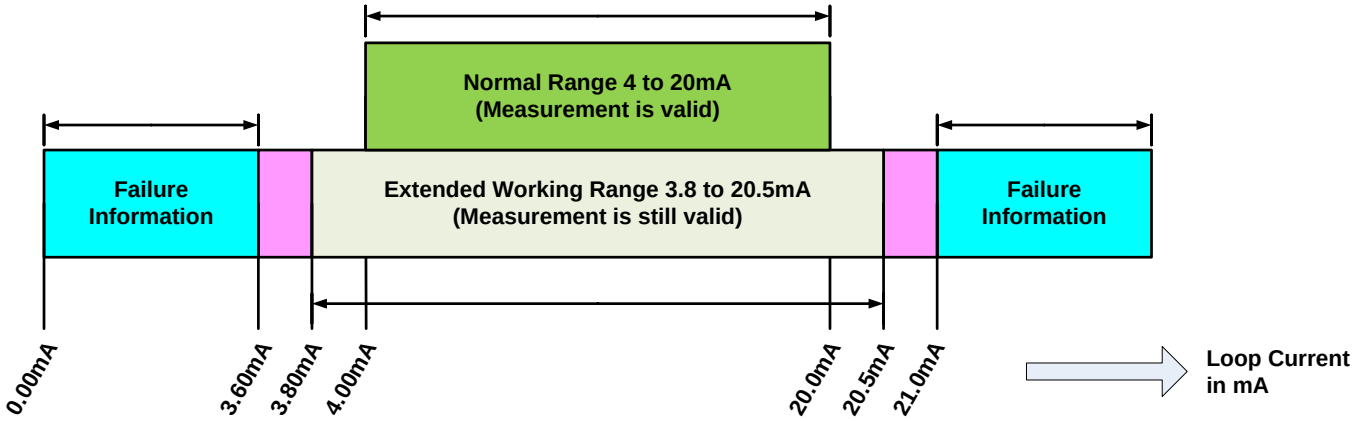


Figure 54. NAMUR NE43 Recommendation

16 Power Supply and Loop Input Protections Design

Please refer to TIDA-00167 to get a deep understanding of the design of this peculiar function of the design. TIDA00167 is a dedicated design for loop powered isolated transmitters.

The power management of the transmitter is a central part of the complete transmitter design. It provides multiple functions needed in the transmitter, finally determining the total performance. As shown in Figure 55, these functions can be split into:

- Loop input protection
- Provision of the non-isolated intermediate voltage (4.7V)
- Isolated DC/DC conversion
- Filtering the ripple caused by the isolated DC/DC converter
- Post regulation to provide stable and noise-free non-isolated 3.3 V (3V3)
- Post regulation to provide stable and noise-free isolated 3.3V (iso3V3)

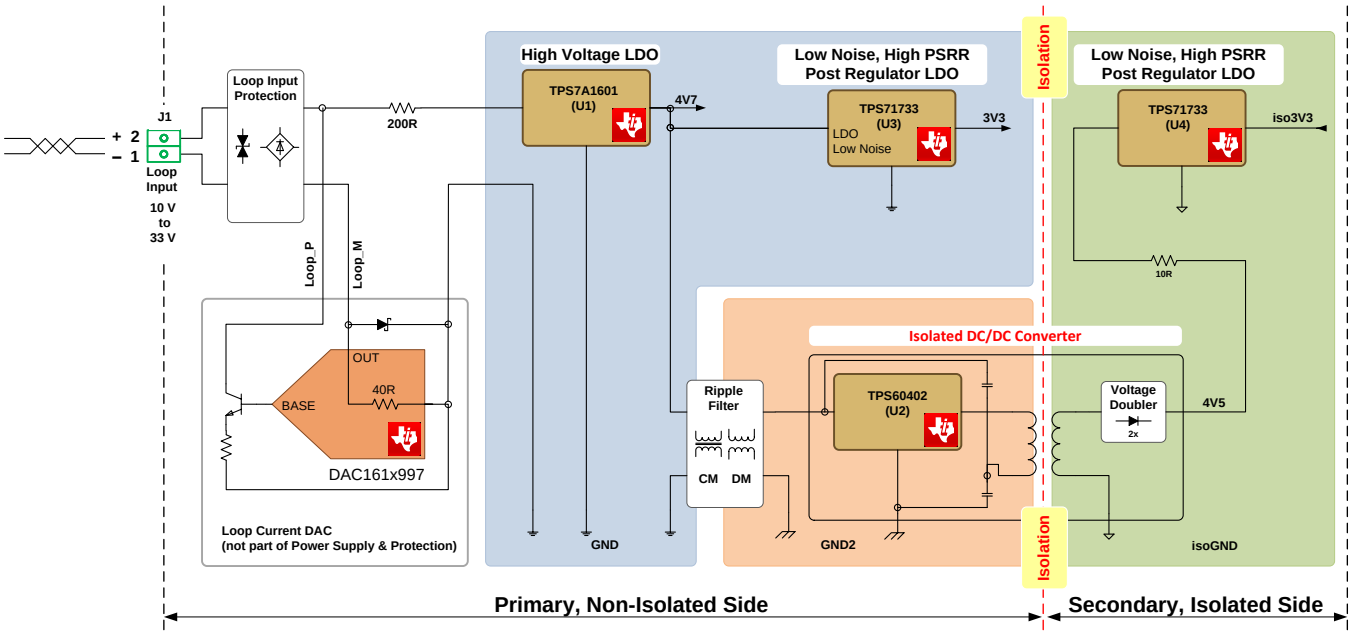


Figure 55. Block Diagram of Power Supply and Loop Input Protection

17 Getting Started with the Hardware

1. Install Code Composer Studio before connecting MSP-FET to PC. During CCS installation, USB drivers are installed automatically. Make sure to use the latest CCS version, otherwise the USB drivers might not be able to recognize the MSP-FET.
2. Connect the MSP-FET to a USB port on the PC with the provided USB cable.
3. The following procedure applies to operation under Windows:
   (a) After connecting to the PC, the MSP-FET should be recognized automatically, as the USB device driver has been already installed together with the IDE.
   (b) If the driver has not been installed yet, the Found New Hardware wizard starts. Follow the instructions and point the wizard to the driver files.
   (c) The default location for CCS is c:\ti\ccsv6\ccs_base\emulation\drivers\msp430\USB_CDC.
4. After connecting to a PC, the MSP-FET performs a self-test. If the self-test passes successfully, the green LED stays on.
5. If the local 3.3V supply from the TPS71733DSE is used during debug, make sure pin 2 and pin 3 are connected on jumper J6. If there is no local power and power from the Debugger Interface is used, make sure pin 1 and pin 2 are connected on jumper J6.
6. Connect the MSP-FET to the Thermocouple Transmitter board with the 14-conductor cable.
7. Import the CCS project (TIDA-00189) into CCS and download the firmware to the MSP430 on the Thermocouple Transmitter board.
8. The UART backchannel function of the MSP-FET can be used for debug purposes (#define UART_ENABLE) to see the conversion results. The MSP430F5172 communicates then to a virtual COM Port using the UART backchannel function of the MSP-FET.

18 Test Set Up

18.1 Basic TI Design Bring-up

For the initial TI Design bring-up, the following equipment is needed:

- TIDA-00189 board (MSP430 pre-programmed)
- Power supply for Loop power (typ. 24Vdc) – here: CL3001
- Ampere meter to measure the loop current – here: CL3001
- Thermocouple or Precise voltage source to provide the temperature equivalent voltage – here: CL3001
- Optional: multimeter and oscilloscope

Connections

1. Configure the TI Design as follows:
   - J2: short
   - J6: 1-2
   - J7: 2-3
2. Connect a power Supply (24Vdc) in series with a precise current meter to J1 and set the current limit of the power supply to 50mA.
3. Connect a precise voltage source (-7mV…+56mV) to the Thermocouple Input J3. Alternatively, a thermocouple Type K can be connected to J3, as well.
4. Verify the following voltages:
   - J1, PIN 2–1 (GND): 24V
   - TP3–TP4 (GND): 4.7V
   - TP9–TP5 (isoGND): 3.3V
   - TP10–TP5 (isoGND): 3.3V

The setup is shown in Figure 56. After providing the loop power of 24Vdc, the measured loop current will be the current set by the DAC161P997 IERRL or IERRH register. Default configuration for IERRL is 3.375mA and for IERRH is 21.75mA. With J7 IERRL (J7: 2-3) or IERRH (J7: 1-2) can be selected. Please refer to Table 9 for further details.

Once the MSP430 firmware is running, the measured loop current will change according to the provided voltage (temperature when a Thermocouple Type K is connected) at J3.

By setting the voltage at J3 to -5.891mV (corresponds to a temperature of -200°C at CJC of 0°C), the measured loop current should be 4mA.

Table 10 gives an overview of temperatures (voltages) and the corresponding ideal loop current. In addition, the measured loop current is provided, as well.

NOTE: The thermocouple temperature was provided with the equivalent voltage according to Type K table that is valid for a cold junction temperature of 0°C. Therefore, the onboard PT100 that measures the CJC was replaced with the PT100 simulator, set to 0°C.

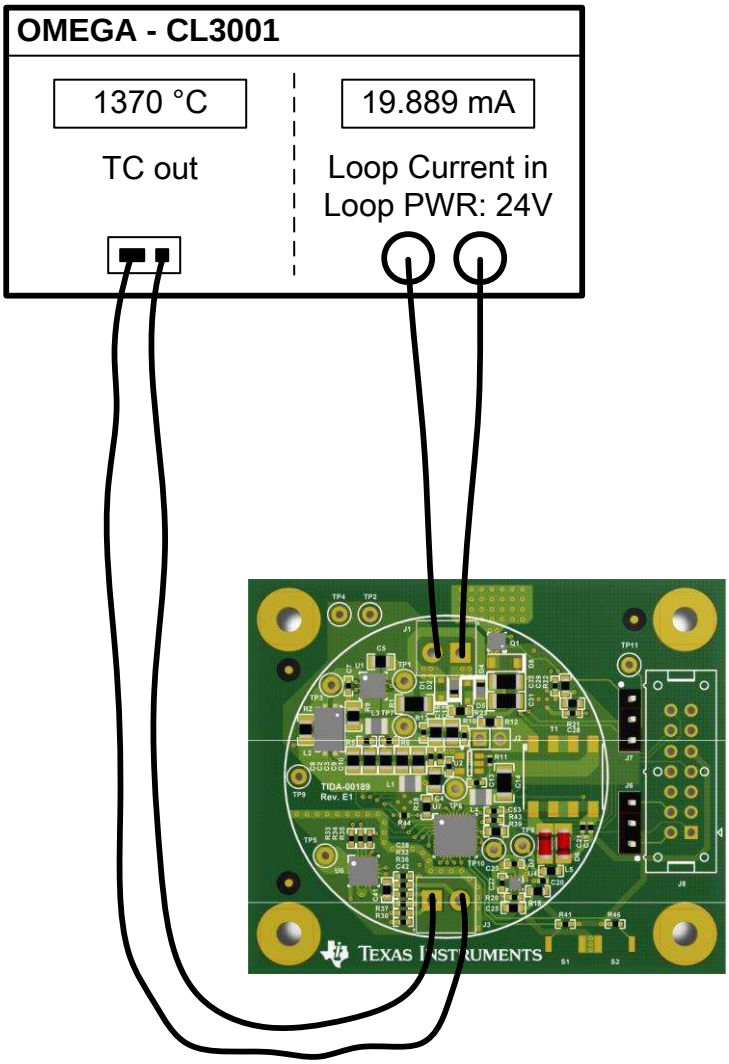


Figure 56. Basic Test Setup

Table 9. Connectors, Testpoints, and Switches

Connectors/TPs/ Switches	Description
J1	4-20mA Loop: 10Vdc – 33Vdc Supply
J2	For Testing purpose: remove R12 and place a short between 1-2 of J2 with a wire. A current probe can be used to measure the current of primary side of the of the isolated DC/DC converter.
J3	Thermocouple Input
J6	Selection between external/internal supply for the MSP430 programmer
J7	Set the DAC161P997 output current level (ERRLVL) at power up. 1-2: IERRH, 2-3: IERRL
J8	MSP430 programming tool (JTAG) and UART
TP1	Input of the High-Voltage LDO U1
TP2	Power Good Signal of the High-Voltage LDO U1
TP3	Output Voltage of High-Voltage LDO U1
TP4	GND
TP5	isoGND
TP6	Switchnode of Halfbridge
TP7	GND2
TP8	Isolated voltage output of the DC/DC converter
TP9	Non-isolated 3.3V output of the low-noise LDO U3
TP10	Isolated 3.3V output of the low-noise LDO U4
S1	Switch to enter/exit the DAC Test mode
S2	Switch to increase the DAC current output in steps of 2mA (only in DAC test mode – activate with S1)

Table 10. Thermocouple Temperature, Equivalent Voltage, and Ideal and Measured Loop Current

Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]	Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]
-200	-5.891E-06	4.0000	4.0026	**590**	2.448E-05	12.0407	12.0407
-190	-5.730E-06	4.1018	4.1051	**600**	2.491E-05	12.1425	12.1423
-180	-5.550E-06	4.2036	4.206	**610**	2.533E-05	12.2443	12.2436
-170	-5.354E-06	4.3053	4.3079	**620**	2.575E-05	12.3461	12.3459
-160	-5.141E-06	4.4071	4.4089	**630**	2.618E-05	12.4478	12.4477
-150	-4.913E-06	4.5089	4.511	**640**	2.660E-05	12.5496	12.5498
-140	-4.669E-06	4.6107	4.6128	**650**	2.702E-05	12.6514	12.6508
-130	-4.411E-06	4.7125	4.7138	**660**	2.745E-05	12.7532	12.7527
-120	-4.138E-06	4.8142	4.8159	**670**	2.787E-05	12.8550	12.8549
-110	-3.852E-06	4.9160	4.9169	**680**	2.829E-05	12.9567	12.957
-100	-3.554E-06	5.0178	5.0187	**690**	2.871E-05	13.0585	13.0588
-90	-3.243E-06	5.1196	5.1208	**700**	2.913E-05	13.1603	13.1598
-80	-2.920E-06	5.2214	5.2226	**710**	2.955E-05	13.2621	13.2615
-70	-2.587E-06	5.3232	5.3237	**720**	2.997E-05	13.3639	13.3637
-60	-2.243E-06	5.4249	5.4258	**730**	3.038E-05	13.4656	13.4659
-50	-1.889E-06	5.5267	5.5276	**740**	3.080E-05	13.5674	13.5667
-40	-1.527E-06	5.6285	5.6297	**750**	3.121E-05	13.6692	13.6687
-30	-1.156E-06	5.7303	5.7315	**760**	3.163E-05	13.7710	13.771
-20	-7.775E-07	5.8321	5.8324	**770**	3.204E-05	13.8728	13.8727

Table 10. Thermocouple Temperature, Equivalent Voltage, and Ideal and Measured Loop Current (continued)

Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]	Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]
-10	-3.919E-07	5.9338	5.9346	**780**	3.245E-05	13.9746	13.975
0	1.974E-15	6.0356	6.0364	**790**	3.286E-05	14.0763	14.076
10	3.969E-07	6.1374	6.1375	**800**	3.328E-05	14.1781	14.1778
20	7.981E-07	6.2392	6.2396	**810**	3.368E-05	14.2799	14.2799
30	1.203E-06	6.3410	6.3414	**820**	3.409E-05	14.3817	14.3817
40	1.612E-06	6.4427	6.4435	**830**	3.450E-05	14.4835	14.4828
50	2.023E-06	6.5445	6.5451	**840**	3.491E-05	14.5852	14.5848
60	2.436E-06	6.6463	6.6463	**850**	3.531E-05	14.6870	14.6867
70	2.851E-06	6.7481	6.7484	**860**	3.572E-05	14.7888	14.7888
80	3.267E-06	6.8499	6.8501	**870**	3.612E-05	14.8906	14.8907
90	3.682E-06	6.9517	6.9513	**880**	3.652E-05	14.9924	14.9928
100	4.096E-06	7.0534	7.0534	**890**	3.693E-05	15.0941	15.0939
110	4.509E-06	7.1552	7.1551	**900**	3.733E-05	15.1959	15.1955
120	4.920E-06	7.2570	7.2572	**910**	3.773E-05	15.2977	15.2977
130	5.328E-06	7.3588	7.359	**920**	3.812E-05	15.3995	15.3996
140	5.735E-06	7.4606	7.46	**930**	3.852E-05	15.5013	15.5006
150	6.138E-06	7.5623	7.5622	**940**	3.892E-05	15.6031	15.6027
160	6.540E-06	7.6641	7.6639	**950**	3.931E-05	15.7048	15.7046
170	6.941E-06	7.7659	7.7661	**960**	3.971E-05	15.8066	15.8067
180	7.340E-06	7.8677	7.8678	**970**	4.010E-05	15.9084	15.9086
190	7.739E-06	7.9695	7.9689	**980**	4.049E-05	16.0102	16.0096
200	8.138E-06	8.0712	8.0709	**990**	4.089E-05	16.1120	16.1117
210	8.539E-06	8.1730	8.1731	**1000**	4.128E-05	16.2137	16.2137
220	8.940E-06	8.2748	8.2752	**1010**	4.166E-05	16.3155	16.3161
230	9.343E-06	8.3766	8.3762	**1020**	4.205E-05	16.4173	16.4171
240	9.747E-06	8.4784	8.478	**1030**	4.244E-05	16.5191	16.5189
250	1.015E-05	8.5802	8.5802	**1040**	4.283E-05	16.6209	16.6211
260	1.056E-05	8.6819	8.6823	**1050**	4.321E-05	16.7226	16.7228
270	1.097E-05	8.7837	8.784	**1060**	4.360E-05	16.8244	16.825
280	1.138E-05	8.8855	8.8862	**1070**	4.398E-05	16.9262	16.9262
290	1.179E-05	8.9873	8.9869	**1080**	4.436E-05	17.0280	17.028
300	1.221E-05	9.0891	9.0891	**1090**	4.474E-05	17.1298	17.1301
310	1.262E-05	9.1908	9.1911	**1100**	4.512E-05	17.2316	17.2323
320	1.304E-05	9.2926	9.2931	**1110**	4.550E-05	17.3333	17.333
330	1.346E-05	9.3944	9.394	**1120**	4.587E-05	17.4351	17.4363
340	1.387E-05	9.4962	9.4962	**1130**	4.625E-05	17.5369	17.5374
350	1.429E-05	9.5980	9.598	**1140**	4.662E-05	17.6387	17.6391
360	1.471E-05	9.6997	9.7001	**1150**	4.700E-05	17.7405	17.7412
370	1.513E-05	9.8015	9.8007	**1160**	4.737E-05	17.8422	17.8431
380	1.555E-05	9.9033	9.9028	**1170**	4.774E-05	17.9440	17.944
390	1.598E-05	10.0051	10.005	**1180**	4.811E-05	18.0458	18.0464
400	1.640E-05	10.1069	10.1068	**1190**	4.847E-05	18.1476	18.148
410	1.682E-05	10.2087	10.208	**1200**	4.884E-05	18.2494	18.2504
420	1.724E-05	10.3104	10.31	**1210**	4.920E-05	18.3511	18.3519
430	1.767E-05	10.4122	10.4118	**1220**	4.957E-05	18.4529	18.4531

Table 10. Thermocouple Temperature, Equivalent Voltage, and Ideal and Measured Loop Current (continued)

Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]	Thermocouple Temp [°C]	Equivalent Voltage @CJC=0°C [V]	Ideal Loop Current [mA]	Measured Loop Current [mA]
440	1.809E-05	10.5140	10.5139	**1230**	4.993E-05	18.5547	18.5553
450	1.852E-05	10.6158	10.6157	**1240**	5.029E-05	18.6565	18.657
460	1.894E-05	10.7176	10.7169	**1250**	5.064E-05	18.7583	18.7592
470	1.937E-05	10.8193	10.8189	**1260**	5.100E-05	18.8601	18.8608
480	1.979E-05	10.9211	10.9208	**1270**	5.136E-05	18.9618	18.962
490	2.022E-05	11.0229	11.0229	**1280**	5.171E-05	19.0636	19.0643
500	2.064E-05	11.1247	11.1247	**1290**	5.206E-05	19.1654	19.166
510	2.107E-05	11.2265	11.2256	**1300**	5.241E-05	19.2672	19.2683
520	2.150E-05	11.3282	11.3278	**1310**	5.276E-05	19.3690	19.37
530	2.192E-05	11.4300	11.4296	**1320**	5.311E-05	19.4707	19.4713
540	2.235E-05	11.5318	11.5317	**1330**	5.345E-05	19.5725	19.5731
550	2.278E-05	11.6336	11.6335	**1340**	5.380E-05	19.6743	19.6751
560	2.320E-05	11.7354	11.7346	**1350**	5.414E-05	19.7761	19.7773
570	2.363E-05	11.8372	11.8367	**1360**	5.448E-05	19.8779	19.8784
580	2.405E-05	11.9389	11.9385	**1370**	5.482E-05	19.9796	19.9803

19 Test Results

The following sections are showing the test results of the different sub-systems of the TI Design. Figure 57 is showing the test setup. The system is powered by the CL3001 from Omega with 24Vdc that is also set to measure the loop current. The CL3001 is providing, in addition, the thermocouple voltage and measured with the 6.5 digital multimeter HP34401 directly at J3. The cold junction temperature is set with the PT100 Simulator.

All data coming from the ADS1220 to the MSP430 and the calculated values can be read via UART on J8. All instruments are connected via GPIB to a PC. The UART interface of the TI Design is connected through the MSP430 programmer as a virtual COM Port to the PC. A Matlab script sets the instruments accordingly, reads the required measured data and in addition also reads the data from the MSP430 via UART. All results are stored in Excel files for further post-processing and generating the graphs. For temperature testing, the TI Design is placed inside a climate chamber.

NOTE: Since a voltage source is used providing the equivalent thermocouple voltage instead of connecting an actual thermocouple sensor, the CJC is in most measurements set with the PT100 Simulator to 0°C.

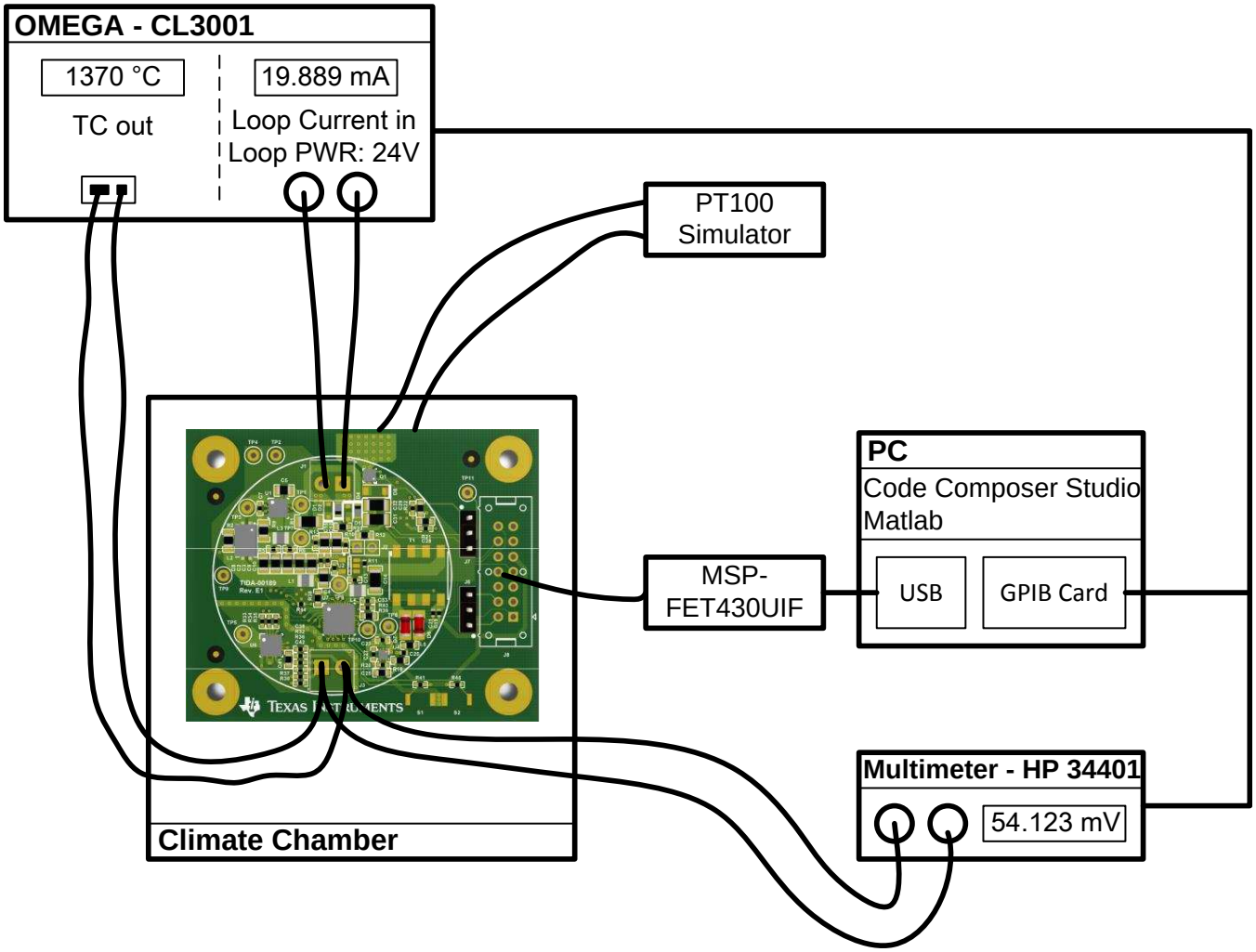


Figure 57. Test Setup

19.1 ADS1220

In this TI Design, ADS1220 is using two input channels. One channel is measuring the thermocouple input and the second channel is measuring the temperature at the cold junction. The next sections are focusing on those two inputs.

19.2 RTD Channel

The RTD channel for the Cold Junction Compensation (CJC) is connected to the ADS1220 inputs AIN2 and AIN3. A PT100 sensor is used to measure the temperature at connector J3. To test this channel without the uncertainty of the PT100 element, a PT100 Simulator is used to provide the equivalent resistor values to emulate different temperatures. With 23 fixed-precision resistors, the PT100 Simulator Type1049 from Time Electronics gives accurate reference values that are better than Class A and Class B PT100 Sensors and similar to Class AA PT100 Sensors. Figure 58 is showing the different temperature errors of PT100 sensors in comparison to the PT100 Simulator.

To minimize the error from the PT100 Simulator, each value was measured to see the actual resistor value and the corresponding temperature. Table 11 is an overview of the Temperatures that can be selected, the equivalent resistor values according to the Calendar-van-Dusen formula, the measured numbers (resistor and temperature), and the resulting error given as a temperature delta. By applying, for example, 100°C to the RTD channel, it will actually represent a temperature of 100.286°C.

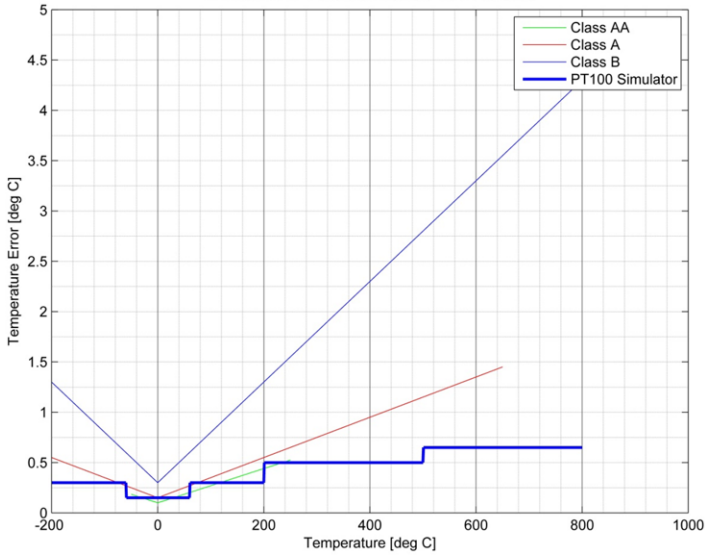


Figure 58. Temperature Error vs Temperature of PT100 Sensors (Class AA, A, B) and PT100 Simulator

Table 11. Resistor Values and Corresponding Temperature of PT100 Simulator

Temp [°C]	Corresponding Resistor Values According to Calendar-van-Dusen Formula [Ohm]	Measured Resistor Values (OMEGA CL3001) [Ohm]	Measured Equivalent Temperatures (OMEGA CL3001) [°C]	Temp Delta
-200	18.52	18.586	-199.842	0.158
-100	60.256	60.312	-99.862	0.138
-50	80.306	80.351	-49.894	0.106
-20	92.16	92.168	-19.983	0.017
-10	96.086	96.103	-9.96	0.04
0	100	100.046	0.117	0.117
10	103.903	103.944	10.104	0.104
20	107.794	107.84	20.12	0.12
30	111.673	111.714	30.108	0.108
40	115.541	115.569	40.07	0.07
50	119.397	119.419	50.053	0.053
60	123.242	123.316	60.187	0.187
80	130.897	130.942	80.11	0.11
100	138.506	138.617	100.286	0.286
150	157.325	157.418	150.244	0.244
200	175.856	175.892	200.098	0.098
250	194.098	194.098	250.003	0.003
300	212.052	212.066	300.043	0.043
400	247.092	247.097	400.012	0.012
500	280.978	280.999	500.058	0.058
600	313.708	313.727	600.055	0.055
700	345.284	345.367	700.271	0.271
800	375.704	375.72	800.045	0.045

19.2.1 Noise Histogram of the RTD Channel

To get the ADC noise Histogram of the RTD channel, the PT100 was replaced with the PT100 Simulator and set to 0°C (100Ω), which is according to Table 11, 0.117°C (100.046Ω). The raw ADC codes (acquired by the MSP430 and sent via UART to the PC) were captured at three different ambient temperatures. Figure 59 shows the histogram at 3 ambient temperatures. The peak-to-peak spread of the codes is in the range of 270 (275 codes @-35°C; 270 codes @25°C; 268 codes @85°C).

$$LSB = (2 \times V_{REF})/(G \times (2^{24} - 1)) = (2 \times 1.6225V)/(32 \times (2^{24} - 1)) = 6.044nV$$

$$Noise_{\mu Vpp} = LSB \times Spread_{ADC\ Code} = 6.044nV \times 270 = 1.632\mu V$$

$$Noise_{^\circ C} = Noise_{\mu Vpp}/(Sensitivity_{PT100} \times I_{RTD}) = 1.632\mu V/(0.385 \times 250\mu A) = 0.017^\circ C$$

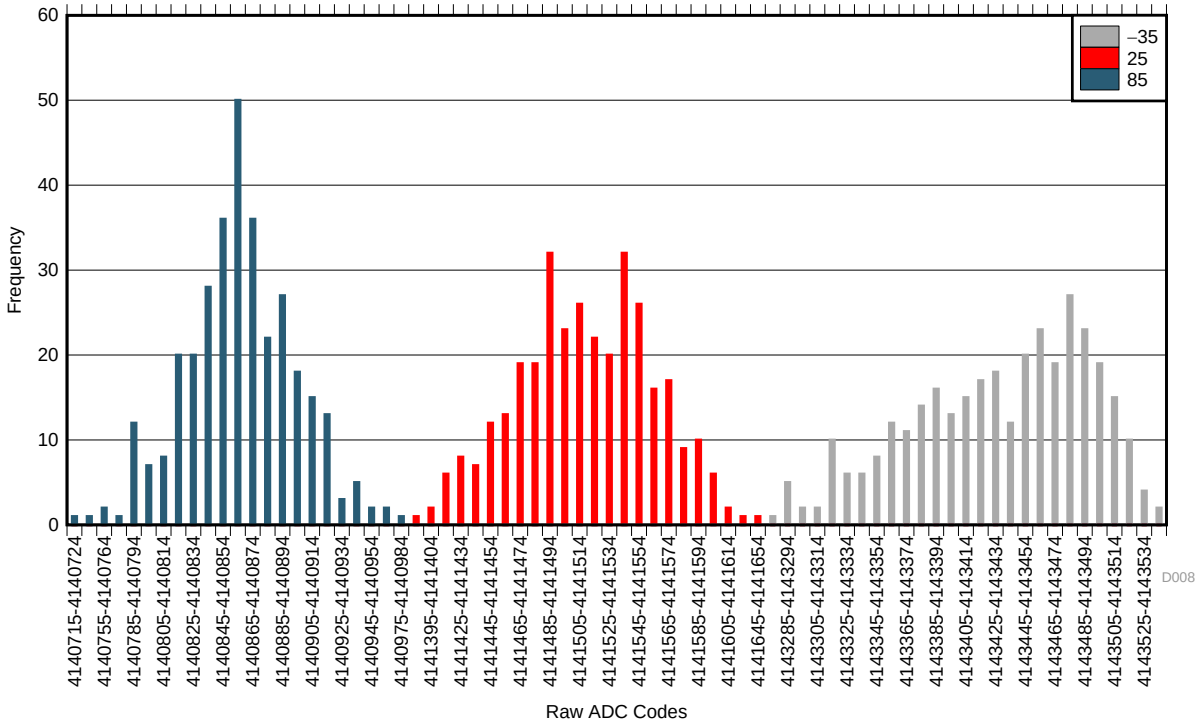


Figure 59. Noise Histogram of RTD Channel

19.2.2 Temperature Error of the RTD Channel

In Figure 60, the RTD channel error over temperature is plotted. Eight different precision-resistor values were provided to the RTD input, emulating temperatures of -100°C, -50°C, -20°C, 0°C, 20°C, 50°C, 80°C, and 100°C. All tests were done at -40°C, 25°C, and 85°C ambient temperature. The RTD channel error has direct impact to the overall system accuracy.

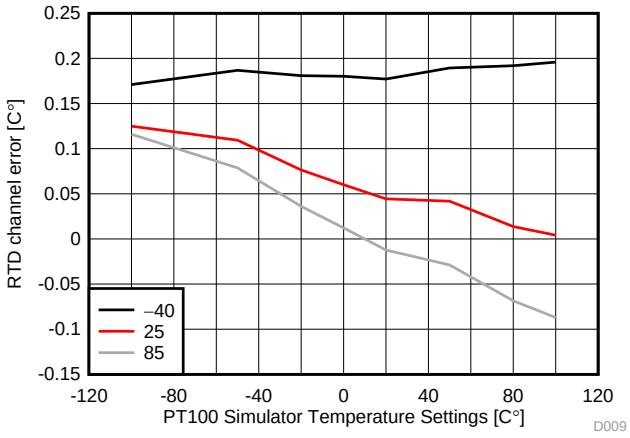


Figure 60. Temperature Error of the RTD Channel

19.3 Thermocouple Channel

To test the thermocouple channel of the ADS1220, the equivalent thermocouple voltages were provided to the input. Those voltages can be either calculated with the formulas for a given type of thermocouple or with a table. Both are only valid when the junction temperature is at 0°C. To eliminate the uncertainty of the junction temperature, the PT100 element on the TI Design was replaced by the PT100 simulator set to 0°C and, in addition, the MSP430 also provides the pure TC temperature (without the calculation of the cold junction). The setup shown in Figure 57 is used for this purpose.

The first set of plots shows the Temperature Error of the Thermocouple channel without the calculation of the Cold Junction Compensation. The equivalent thermocouple voltages were swept from -200°C to +1370C in steps of 10°C. Figure 61 shows the Error at 3 different ambient temperatures without gain calibration. This Temperature Error is only the error of the TC channel and does not count for the RTD channel.

The TC channel can be further improved by performing a gain calibration. The easiest way is a one point gain calibration. This one point calibration was done at room temperature. Additional calibration points at different ambient temperatures will increase the accuracy of the results, however, this has not been done in this report. For the gain calibration several measurements were taken for a thermocouple temperature of 1370°C. The resulting ADC codes were averaged and compared with the ideal expected ADC code. Table 12 lists those values and the resulting gain correction factor for the thermocouple channel.

Table 12. Gain Correction Factor of Thermocouple Channel

Mean of Measured ADC Codes	Ideal ADC Code for 1370°C	TC Gain Correction Factor
1839678629	1839420407	0.999859638

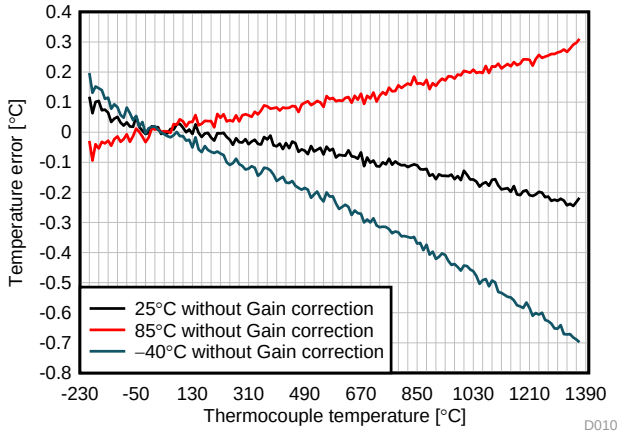


Figure 61. Temperature Error Without Gain Correction Over Temperature

In Figure 62, the temperature error at 25°C with gain correction factor has improved compared to the error without the gain correction factor. The error of the Thermocouple channel at 25°C is now minimized across the entire input range (-200°C to 1370°C).

By taking the entire set of data again over ambient temperature, however, now with gain correction factor the resulting temperature error can be seen in Figure 63. Comparing the results without gain calibration (Figure 61) with the results with gain calibration (Figure 63), it can be seen the graphs are rotated by the calibration factor around the crossing point of the three curves. It is just calibrated for 25°C. The same could now also be done, for example, with 85°C and -40°C.

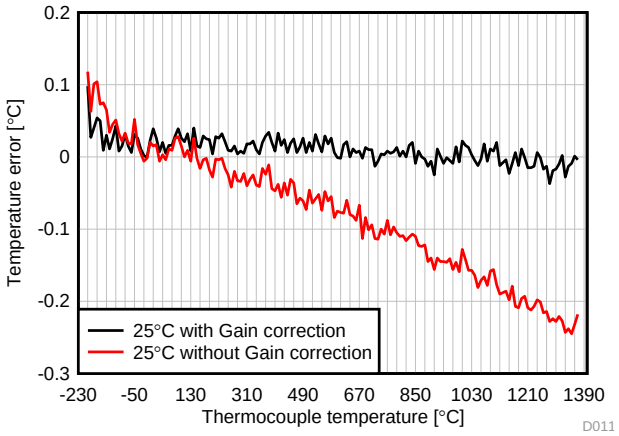


Figure 62. Temperature Error With and Without Gain Correction at 25°C

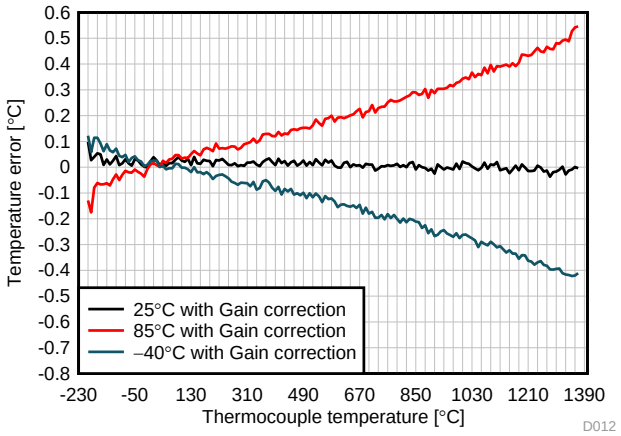


Figure 63. Temperature Error With Gain Correction Over Temperature

19.4 Combined Results – Thermocouple plus Cold Junction Compensation

The RTD channel is still set with the PT100 Simulator to 0°C. From Figure 64, it can be seen the measured RTD value is not exactly 0°C, but roughly 0.117°C. This is actually also the temperature that is provided with the equivalent precision resistor. Please refer to Table 11 for the details. The second curve in Figure 64 shows the Temperature Error of thermocouple measurement combined with the CJC measurement (RTD channel).

NOTE: From the test setup, the provided TC voltages are only valid for a cold junction temperature of 0°C. Since the resistor value at the RTD channel does not exactly provide 100Ω, there is a small setup error. However, in Figure 64, it can be seen that the TC with CJC graph is offset by the RTD value. The assumption is to have the RTD value at 0°C, however, it actually is 0.117°C.

Figure 65 and Figure 66 show the same as Figure 64, just at different ambient temperatures. Figure 67 shows the combination.

Here it can be seen that the three different graphs for the Thermocouple with CJC are shifted by the corresponding measured RTD value. Thus, the overall accuracy is dependent also on the RTD accuracy.

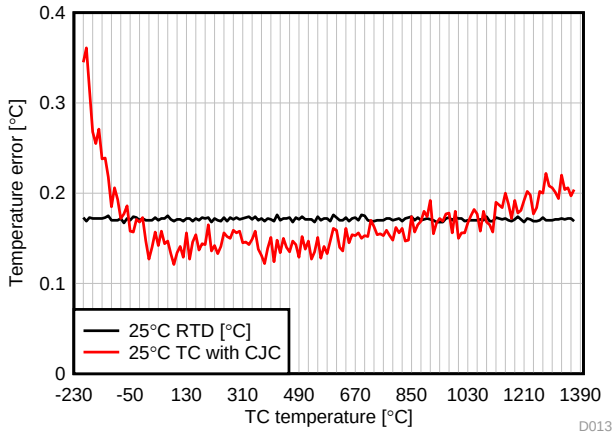


Figure 64. Temperature Error with Cold Junction Compensation, Measured Cold Junction (Set to 0°C) at 25°C Ambient Temperature

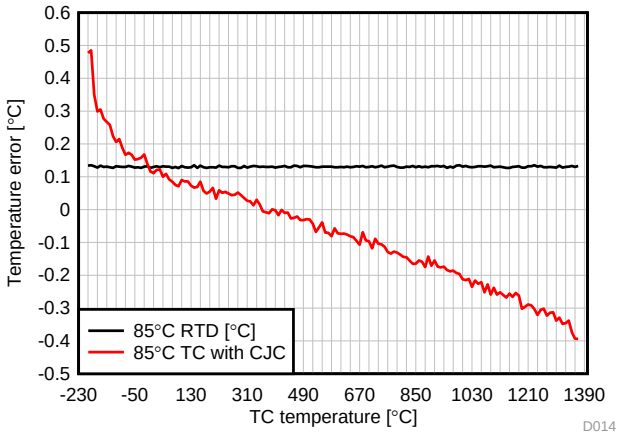


Figure 65. Temperature Error with Cold Junction Compensation, Measured Cold Junction (Set to 0°C) at 85°C Ambient Temperature

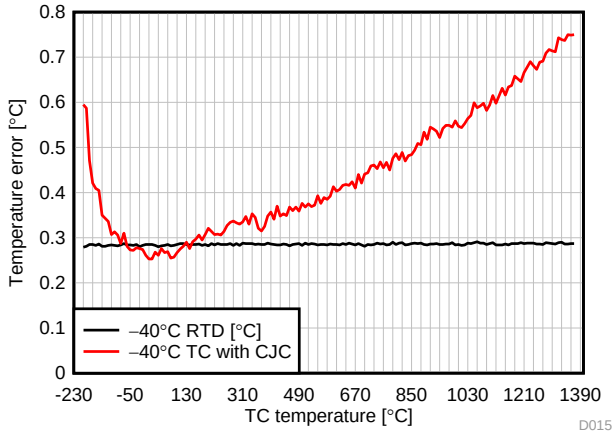


Figure 66. Temperature Error with Cold Junction Compensation, Measured Cold Junction (Set to 0°C) at -40°C Ambient Temperature

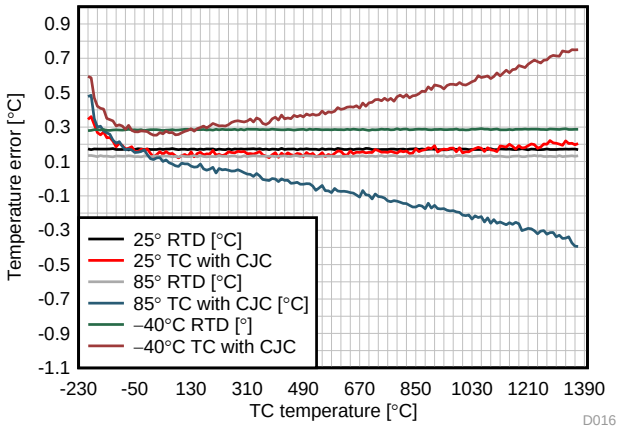


Figure 67. Temperature Error with Cold Junction Compensation, Measured Cold Junction (Set to 0°C) Across Ambient Temperature

19.5 DAC161P997

For testing the DAC161P997 in the TI Design, a test mode is incorporated in the MSP430 firmware. By pushing the button S1, the system enters this test mode. In this test mode, the DAC outputs a fix current, starting at 2mA. This value can be incremented in steps of 2mA by pushing S2. With pressing S1 again, it exists the test mode. This is useful for calculating the DAC offset and gain error.

The following graphs (Figure 68, Figure 69, and Figure 70) show the Loop Current error. For this test, the DAC sets the loop current from 2mA to 24mA in steps of 50uA. The Loop Current error is the difference between the set value and the measured value. The test was done at 25°C (Figure 68), 85°C (Figure 69) and -40°C (Figure 70). At every ambient temperature, the test was done 3 times. Figure 71 shows the combination of all those DAC measurements.

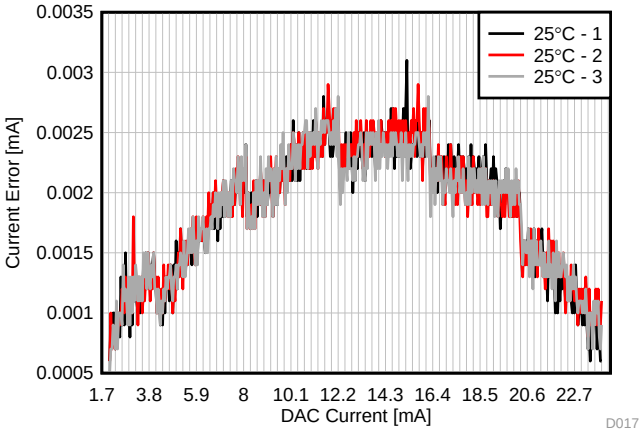


Figure 68. Loop Current Error at 25°C (3 Sets of Measurements)

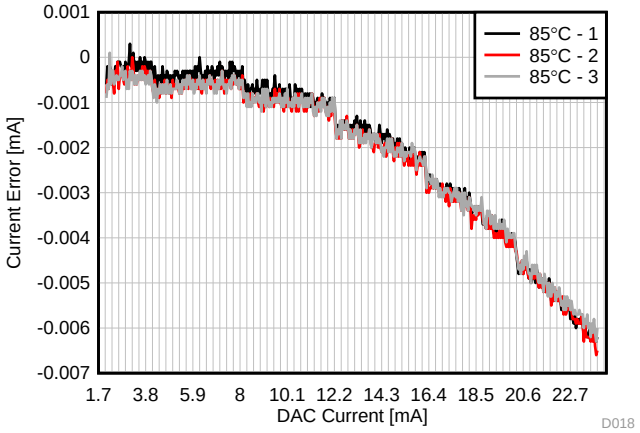


Figure 69. Loop Current Error at 85°C (3 Sets of Measurements)

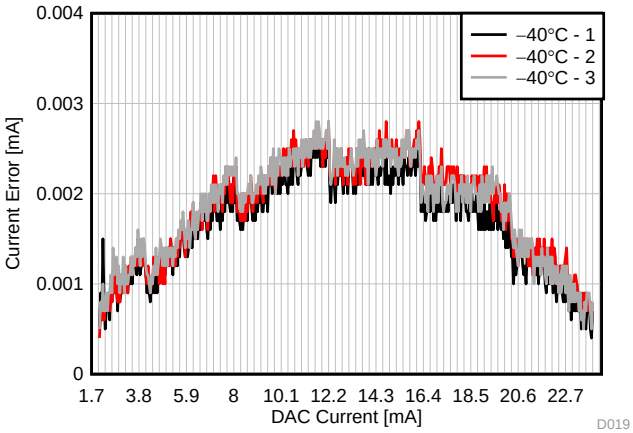


Figure 70. Loop Current Error at -40°C (3 Sets of Measurements)

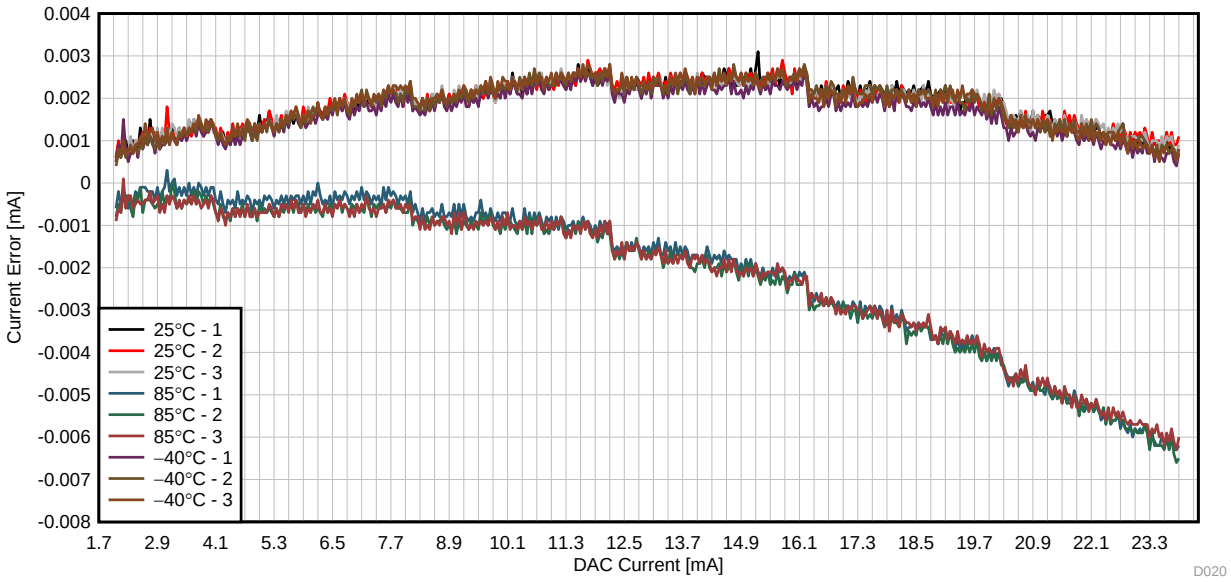


Figure 71. Loop Current Error Over Ambient Temperature

19.6 System Performance

The MSP430 software maps the temperature range from -200°C to +1372°C in the 4-20mA loop current (16mA range). Thus, 1°C is equivalent to 16mA/1582°C = 10.178uA. In Figure 72, the loop current error is shown versus the input temperature across ambient temperature. The overall error across ambient temperature is in the range of 7.5uA, which corresponds to a temperature error of approximately 0.74°C. Figure 73 shows the same plot, however, with Overall Temperature error reading. Figure 74 is focusing just on the results at room temperature.

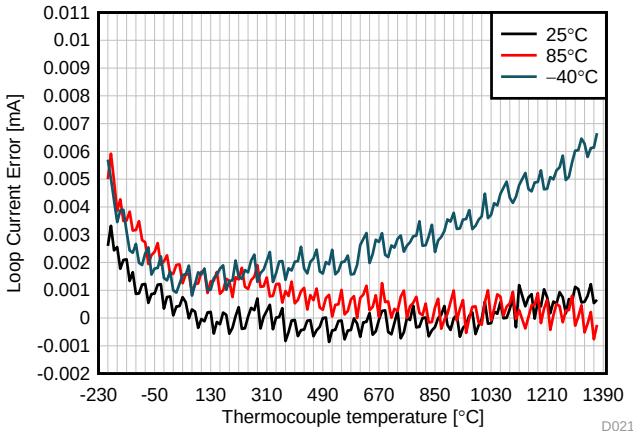


Figure 72. System Loop Current Error Over Ambient Temperature

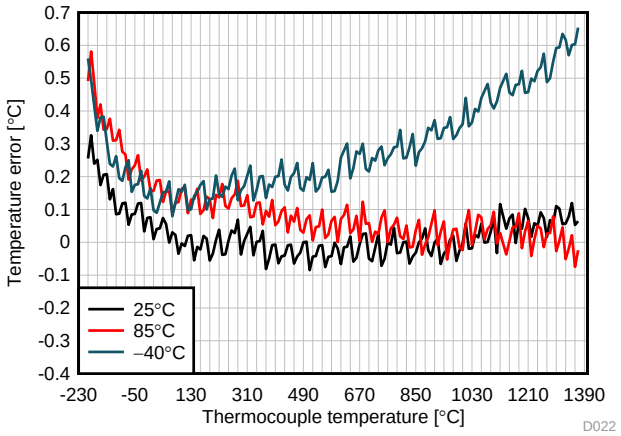


Figure 73. System Temperature Error Over Ambient Temperature

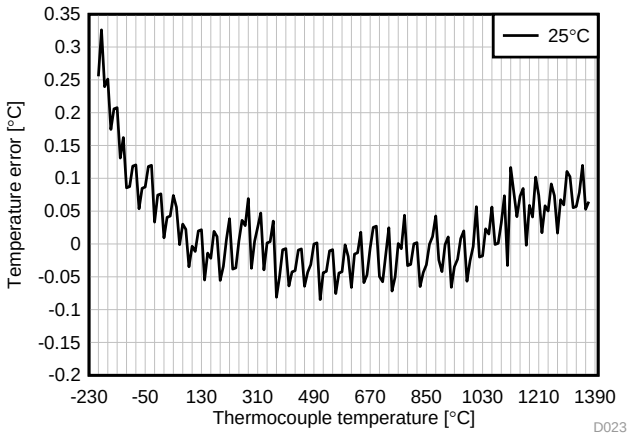


Figure 74. System Temperature Error at 25°C

19.7 Conclusion

The several building blocks of the TI Design were tested, as well as the entire system. The overall temperature error tested across an ambient temperature range from -40°C to +85°C and the thermocouple range from -200° to +1370°C is approximately 0.74°C. The three main contributors to this error are:

1. ADS1220 (temperature dependency)
2. Calculation inside the software
3. Test Setup

19.8 Error Contributor and System Improvements

ADS1220 and DAC161P997 error contribution is mainly due to the ambient temperature. One possibility to have less impact on the ambient temperature is to also calibrate the system at several ambient temperatures rather than calibrating only at, for example, room temperature.

Another approach is given in Section 19.8.1.

19.8.1 ADS1220 References

The temperature drift of the reference directly influences the quality of the measurements.

For the Thermocouple measurements, the ADS1220 is using its internal reference. By using an external reference with less drift across temperature the error can be further minimized.

Since the RTD channel is a ratiometric measurement, the internal reference does not influence the accuracy, however, the external reference resistor R31. The used reference resistor R31 has a value of 6.49k with 0.1% tolerance and 25ppm/°C. The usage of a resistor with, for example, 10ppm/°C will improve the accuracy of this channel.

19.8.2 Software Calculations

The entire system also has several calculation steps. Each of them adds rounding errors and errors because of linear interpolation.

The measured RTD voltage is first translated into the resistor value. With the help of a look up table, the equivalent temperature is being calculated. The table has a resolution of 1°C, which means anything in between will be based on a 2 point linear interpolation. Since the behavior of a PT100 element is not 100% linear, an error will be introduced. From this point, another look up table translates the temperature into the equivalent thermocouple voltage where it will be add to the actual measured thermocouple voltage for cold junction compensation. From this point, the actual temperature is then converted into the corresponding loop current. Loop current to DAC code translation will add another rounding error.

Alternatives can be to use the polynomial equations for voltage to temperature calculation (and conversely) instead of using the look up tables or using higher resolution tables.

19.8.3 Test Setup

As mentioned earlier, the cold junction compensation adds an error, because the provided thermocouple voltages are only valid at a cold junction of 0°C. The resistor value that is used instead of a PT100 element represents a temperature of 0.117°C (at room temperature). The equivalent thermocouple voltage coming from the power source is introducing, as well, a slight error of up to 5µV.

Additional tests with a thermocouple placed in a block calibrator would provide more accurate test results.

20 Schematic

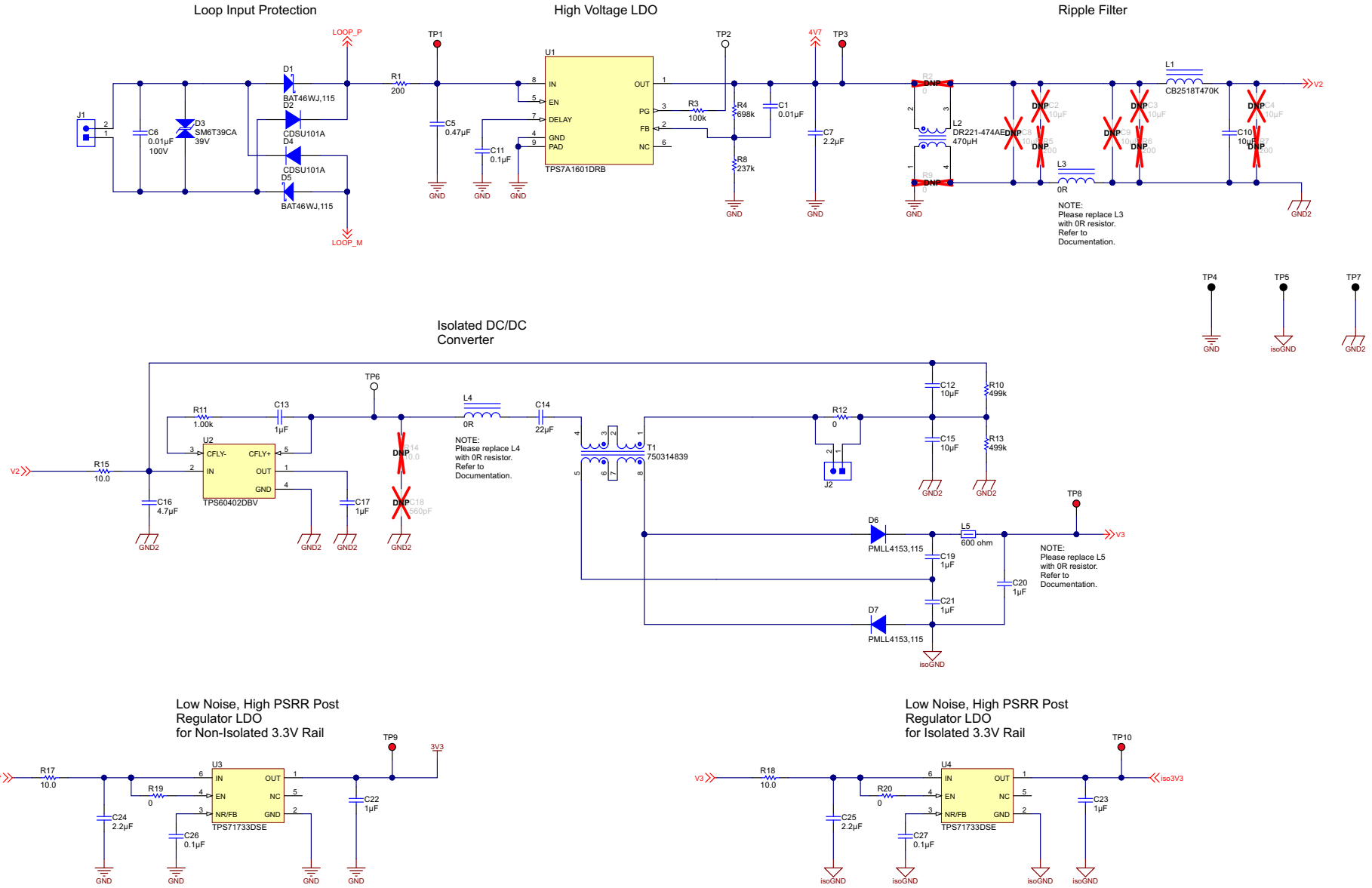


Figure 75. Schematic - Power Supply and Protection

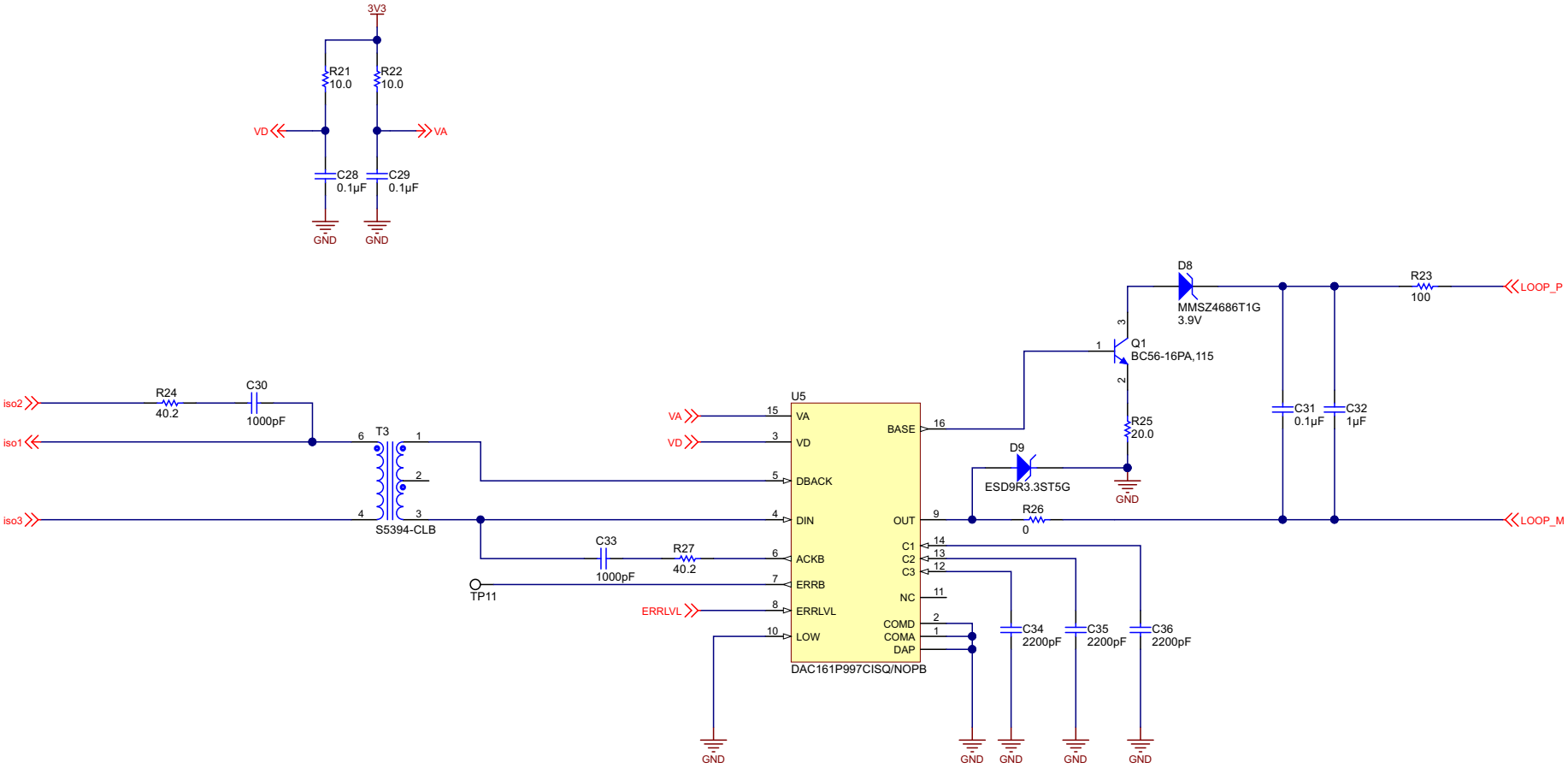


Figure 76. Schematic - Loop Current - DAC

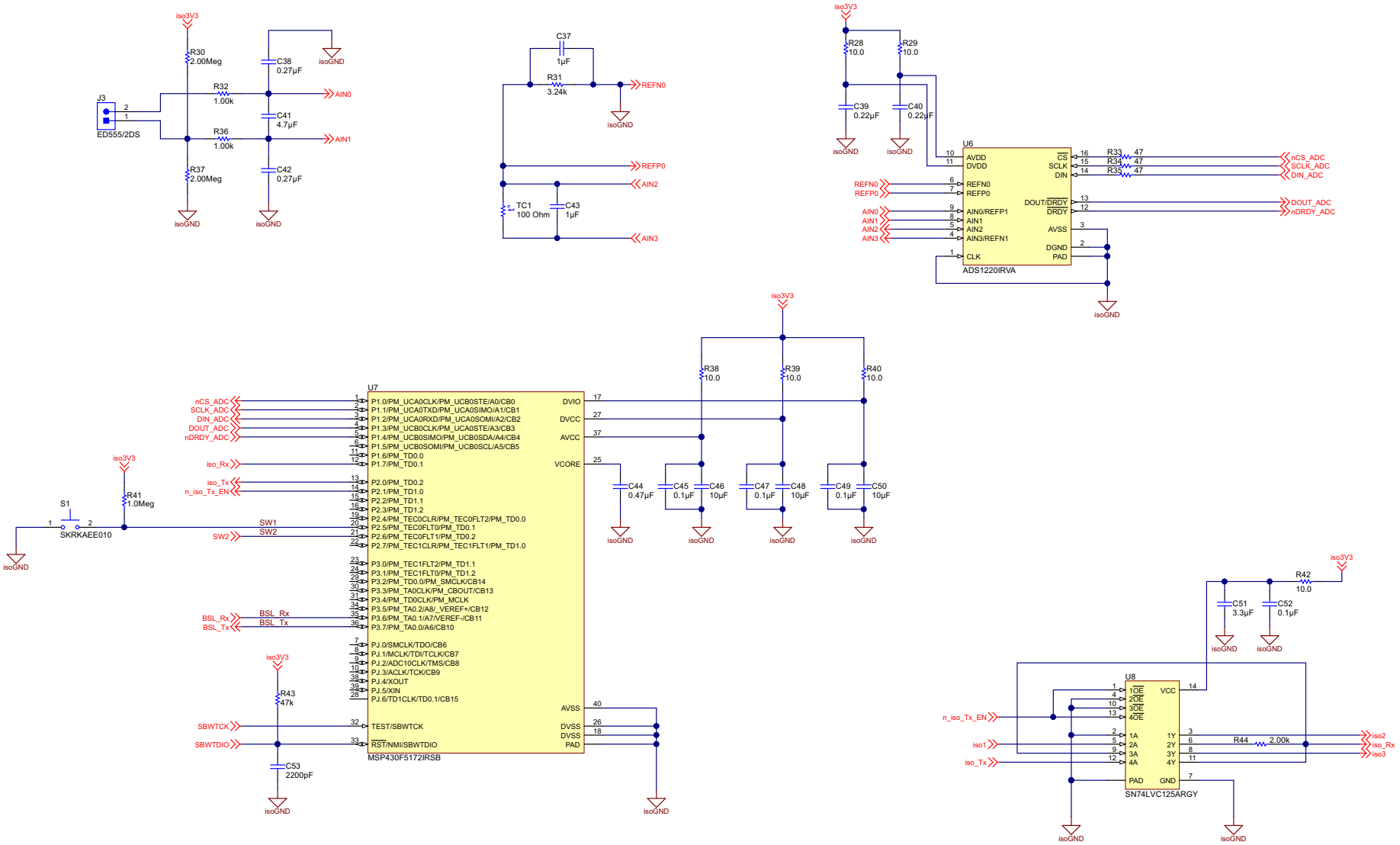


Figure 77. Schematic - Analog Front-End, MCU, and Isolated Data

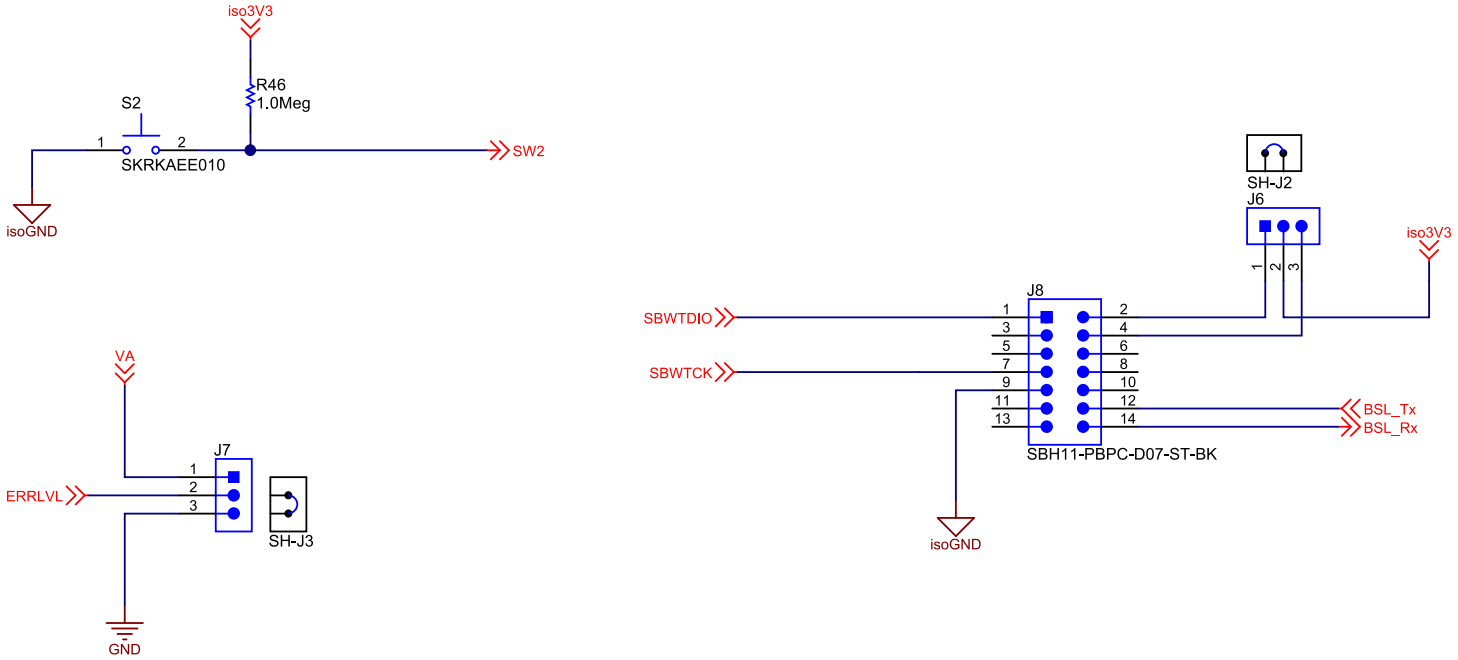


Figure 78. Schematic

21 Bill of Materials

Table 13. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		TIDA-00189	Any		
C1	1	0.01µF	CAP, CERM, 0.01µF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A103KA01D	MuRata		
C5	1	0.47µF	CAP, CERM, 0.47µF, 100V, +/-10%, X7R, 0805	0805	GRM21BR72A474KA73L	MuRata		
C6	1	0.01µF	CAP, CERM, 0.01µF, 100V, +/-10%, X7R, 0603	0603	GRM188R72A103KA01D	MuRata		

Table 13. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C7	1	2.2µF	CAP, CERM, 2.2µF, 16V, +/-10%, X5R, 0402	0402	C1005X5R1C225K050BC	TDK		
C10, C12, C15	3	10µF	CAP, CERM, 10µF, 10V, +/-10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata		
C11, C52	2	0.1µF	CAP, CERM, 0.1µF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A104KA01D	MuRata		
C13, C17, C19, C20, C21, C22, C23, C37, C43	9	1µF	CAP, CERM, 1µF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A105KE15D	MuRata		
C14	1	22µF	CAP, CERM, 22µF, 10V, +/-10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata		
C16	1	4.7µF	CAP, CERM, 4.7µF, 10V, +/-20%, X5R, 0402	0402	GRM155R61A475M	MuRata		
C24, C25	2	2.2µF	CAP, CERM, 2.2µF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata		
C26, C27, C45, C47, C49	5	0.1µF	CAP, CERM, 0.1µF, 6.3V, +/-10%, X7R, 0402	0402	GRM155R70J104KA01D	MuRata		
C28, C29	2	0.1µF	CAP, CERM, 0.1µF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata		
C30, C33	2	1000pF	CAP, CERM, 1000pF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C102KA01D	MuRata		
C31	1	0.1µF	CAP, CERM, 0.1µF, 100V, +/-5%, X7R, 1206	1206	12061C104JAT2A	AVX		
C32	1	1µF	CAP, CERM, 1µF, 100V, +/-10%, X7R, 1206	1206	GRM31CR72A105KA01L	MuRata		
C34, C35, C36, C53	4	2200pF	CAP, CERM, 2200pF, 6.3V, +/-10%, X7R, 0402	0402	GRM155R70J222KA01D	MuRata		
C38, C42	2	0.27µF	CAP, CERM, 0.27µF, 6.3V, +/-10%, X5R, 0402	0402	GRM155R60J274KE01D	MuRata		

Table 13. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C39, C40	2	0.22µF	CAP, CERM, 0.22µF, 6.3V, +/-10%, X5R, 0402	0402	GRM155R60J224KE01D	MuRata		
C41	1	4.7µF	CAP, CERM, 4.7µF, 6.3V, +/-10%, X5R, 0603	0603	GRM188R60J475KE19D	MuRata		
C44	1	0.47µF	CAP, CERM, 0.47µF, 6.3V, +/-10%, X7R, 0603	0603	GRM188R70J474KA01D	MuRata		
C46, C48, C50	3	10µF	CAP, CERM, 10µF, 6.3V, +/-20%, X5R, 0402	0402	CL05A106MQ5NUNC	Samsung		
C51	1	3.3µF	CAP, CERM, 3.3µF, 10V, +/-10%, X5R, 0603	0603	GRM188R61A335KE15D	MuRata		
D1, D5	2	100V	Diode, Schottky, 100V, 0.25A, SOD-323F	SOD-323F	BAT46WJ,115	NXP Semiconductor		
D2, D4	2	90V	Diode, Switching, 90V, 0.1A, SOD-523F	SOD-523F	CDSU101A	Comchip Technology		
D3	1	39V	Diode, TVS, Bi, 39V, 600W, SMB	SMB	SM6T39CA	ST Microelectronics		
D6, D7	2	75V	Diode, Fast Rectifier, 75V, 0.2A, 3.7x1.6x1.6mm	3.7x1.6x1.6mm	PMLL4153,115	NXP Semiconductor		
D8	1	3.9V	Diode, Zener, 3.9V, 500mW, SOD-123	SOD-123	MMSZ4686T1G	ON Semiconductor		
D9	1		TVS DIODE 3.3VWM 7.8VC SOD923	SOD-923	ESD9R3.3ST5G	ON Semiconductor		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J3	2		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology		
J2	1		Header, 100mil, 2x1, Tin plated, TH	Header 2x1	90120-0122	Molex		
J6, J7	2		Header, 100mil, 3x1, Tin plated, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		

Table 13. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J8	1		Header (shrouded), 100 mil, 7x2, Gold plated, TH	7x2 Shrouded Header	SBH11-PBPC-D07-ST-BK	Sullins Connector Solutions		
L1, L3	2	47µH	Inductor, Wirewound, Ferrite, 47µH, 0.11A, 1.235 ohm, SMD	2.5x1.8x1.8mm	CB2518T470K	Taiyo Yuden		
L2	1	470µH	Coupled inductor, 470µH, 0.1A, 0.35 ohm, +/-30%, SMD	5.0x3.3x3.3mm	DR221-474AE	Bourns		
L4	1	33µH	Inductor, Wirewound, Ferrite, 33µH, 0.13A, 0.7 ohm, SMD	2.5x1.8x1.8mm	CB2518T330K	Taiyo Yuden		
L5	1	600	Ferrite Bead, 600 ohm @ 100MHz, 0.2A, 0603	0603	BLM18HG601SN1D	MuRata		
Q1	1	V	Transistor, NPN, 80V, 1A, SOT1061	SOT1061	BC56-16PA,115	NXP Semiconductor		
R1	1	200	RES, 200 ohm, 1%, 0.25W, 1206	1206	CRCW1206200RFKEA	Vishay-Dale		
R3	1	100k	RES, 100k ohm, 1%, 0.063W, 0402	0402	CRCW0402100KFKED	Vishay-Dale		
R4	1	698k	RES, 698k ohm, 1%, 0.063W, 0402	0402	CRCW0402698KFKED	Vishay-Dale		
R8	1	237k	RES, 237k ohm, 1%, 0.063W, 0402	0402	CRCW0402237KFKED	Vishay-Dale		
R10, R13	2	499k	RES, 499k ohm, 1%, 0.063W, 0402	0402	CRCW0402499KFKED	Vishay-Dale		
R11, R32, R36	3	1.00k	RES, 1.00k ohm, 1%, 0.063W, 0402	0402	CRCW04021K00FKED	Vishay-Dale		
R12	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale		
R15, R17, R18, R21, R22, R28, R29, R38, R39, R40, R42	11	10.0	RES, 10.0 ohm, 1%, 0.1W, 0603	0603	CRCW060310R0FKEA	Vishay-Dale		
R19, R20	2	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R23	1	100	RES, 100 ohm, 0.1%, 0.1W, 0603	0603	RT0603BRD07100RL	Yageo America		
R24, R27	2	40.2	RES, 40.2 ohm, 1%, 0.063W, 0402	0402	CRCW040240R2FKED	Vishay-Dale		

Table 13. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R25	1	20.0	RES, 20.0 ohm, 1%, 0.1W, 0603	0603	CRCW060320R0FKEA	Vishay-Dale		
R26	1	0	RES, 0 ohm, 5%, 0.25W, 1206	1206	CRCW12060000Z0EA	Vishay-Dale		
R30, R37	2	2.00M	RES, 2.00 Megohm, 1%, 0.063W, 0402	0402	CRCW04022M00FKED	Vishay-Dale		
R31	1	3.24k	RES, 3.24k ohm, 0.1%, 0.333W, 1206	1206	PFC-W1206R-12-3241-B	TT Electronics/IRC		
R33, R34, R35	3	47	RES, 47 ohm, 5%, 0.063W, 0402	0402	CRCW040247R0JNED	Vishay-Dale		
R41, R46	2	1.0M	RES, 1.0 Megohm, 5%, 0.063W, 0402	0402	CRCW04021M00JNED	Vishay-Dale		
R43	1	47k	RES, 47k ohm, 5%, 0.063W, 0402	0402	CRCW040247K0JNED	Vishay-Dale		
R44	1	2.00k	RES, 2.00k ohm, 1%, 0.063W, 0402	0402	CRCW04022K00FKED	Vishay-Dale		
S1, S2	2		Switch, Push Button, SMD	2.9x2x3.9mm SMD	SKRKAEE010	Alps		
SH-J2, SH-J3	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
T1	1	3mH	Transformer, 3mH, SMT	9.78x10.54x9.14mm	750314839	Wurth Elektronik eiSos		
T3	1	400µH	Transformer_400µH, SMT	8.89x5.46x6.99mm	S5394-CLB	Coilcraft		
TC1	1	100	Temperature Sensor, 100 ohm, 1%, 1206	1206	PTS120601B100RP100	Vishay/Beyschlag		
TP1, TP3, TP8, TP9, TP10	5	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP2, TP6, TP11	3	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		
TP4, TP5, TP7	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1	1		60-V, 5-µA IQ, 100-mA, Low-Dropout Voltage Regulator with Enable and Power-Good, DRB0008A	DRB0008A	TPS7A1601DRB	Texas Instruments		None

Table 13. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U2	1		UNREGULATED 60-mA CHARGE PUMP VOLTAGE INVERTER, DBV0005A	DBV0005A	TPS60402DBV	Texas Instruments		None
U3, U4	2		Low Noise, High-Bandwidth PSRR Low-Dropout 150mA Linear Regulator, DSE0006A	DSE0006A	TPS71733DSE	Texas Instruments		None
U5	1		Single-Wire 16-bit DAC for 4-20mA loops, RGH0016A	RGH0016A	DAC161P997CISQ/NOPB	Texas Instruments		None
U6	1		Low-Power, Low-Noise, 24-Bit Analog-to-Digital Converter for Small Signal Sensors, RVA0016A	RVA0016A	ADS1220IRVA	Texas Instruments		None
U7	1		Mixed Signal Microcontroller, RSB0040B	RSB0040B	MSP430F5172IRSB	Texas Instruments		None
U8	1		QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS, RGY0014A	RGY0014A	SN74LVC125ARGY	Texas Instruments		None
C2, C3, C4, C8, C9	0	10µF	CAP, CERM, 10µF, 10V, +/-10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata		
C18	0	560pF	CAP, CERM, 560pF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H561KA01D	MuRata		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		
R2, R9	0	0	RES, 0 ohm, 5%, 0.125W, 0805	0805	CRCW08050000Z0EA	Vishay-Dale		
R5, R6, R7	0	200	RES, 200 ohm, 1%, 0.063W, 0402	0402	CRCW0402200RFKED	Vishay-Dale		
R14	0	10.0	RES, 10.0 ohm, 1%, 0.063W, 0402	0402	CRCW040210R0FKED	Vishay-Dale		

22 PCB Layer Plots

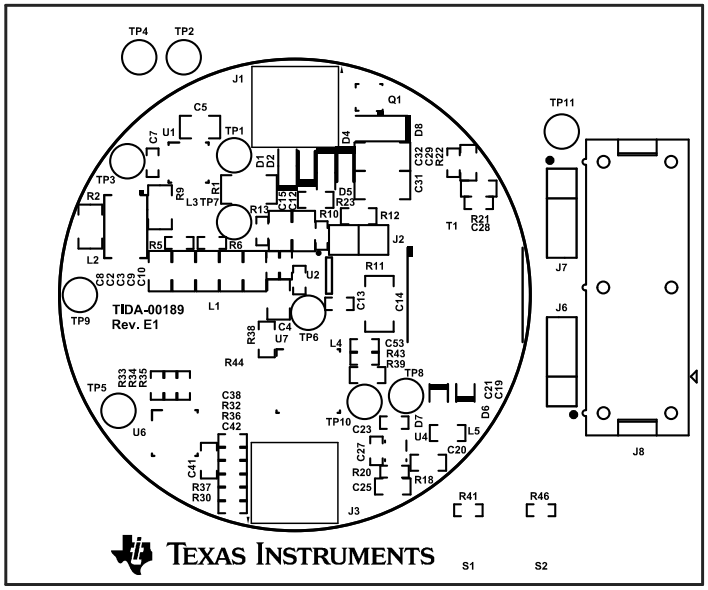


Figure 79. Top Overlay

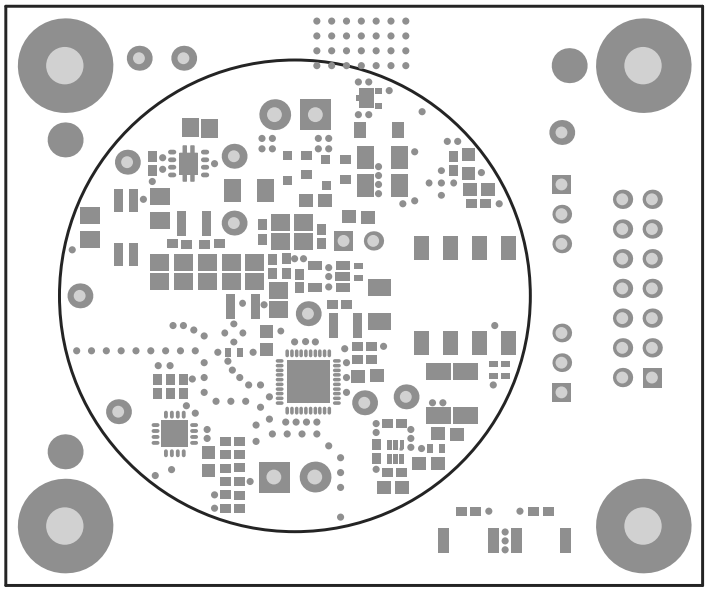


Figure 80. Top Solder

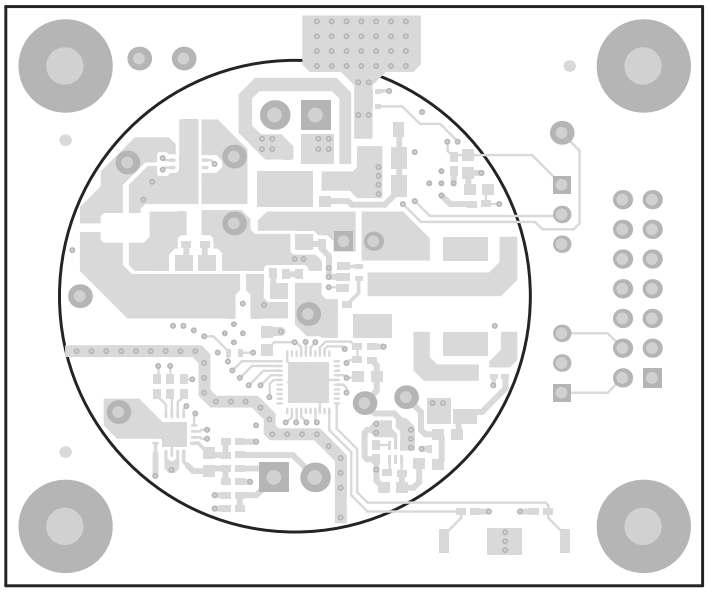


Figure 81. Top Layer

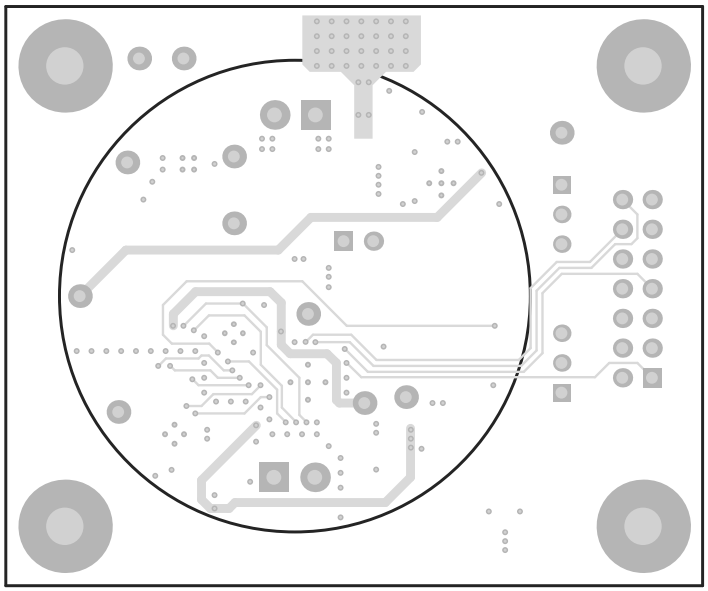


Figure 82. Inner Layer

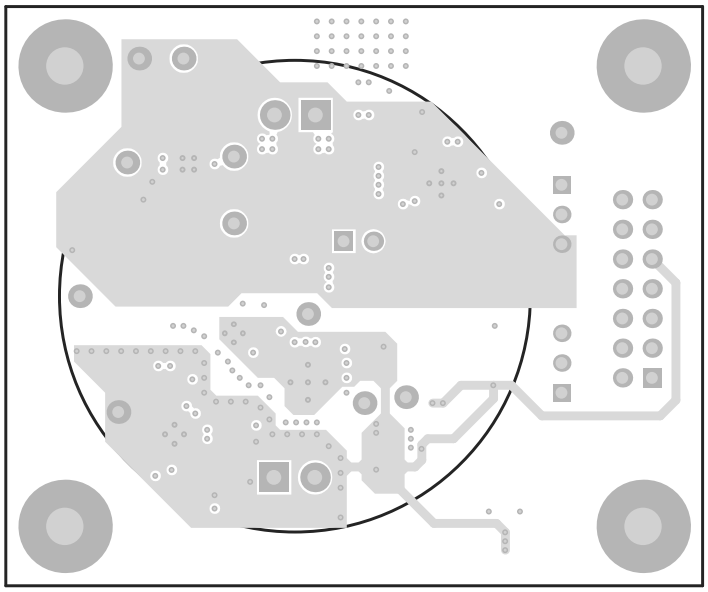


Figure 83. Ground Layer

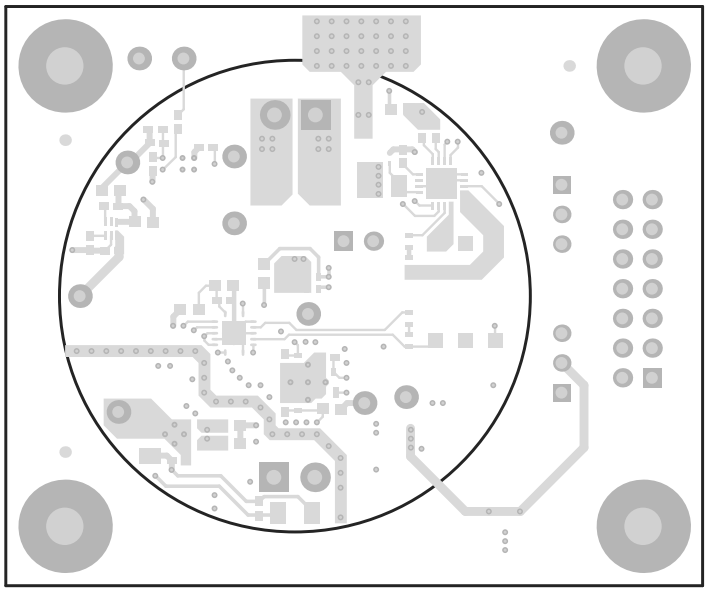


Figure 84. Bottom Layer

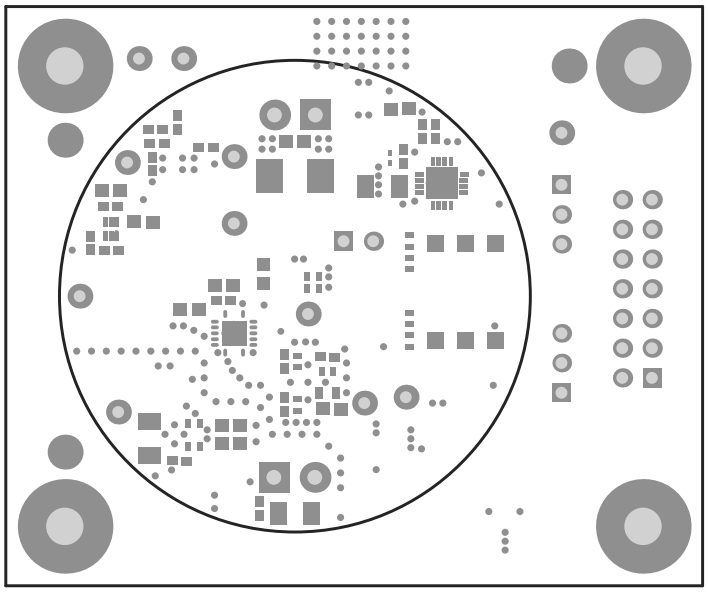


Figure 85. Bottom Solder

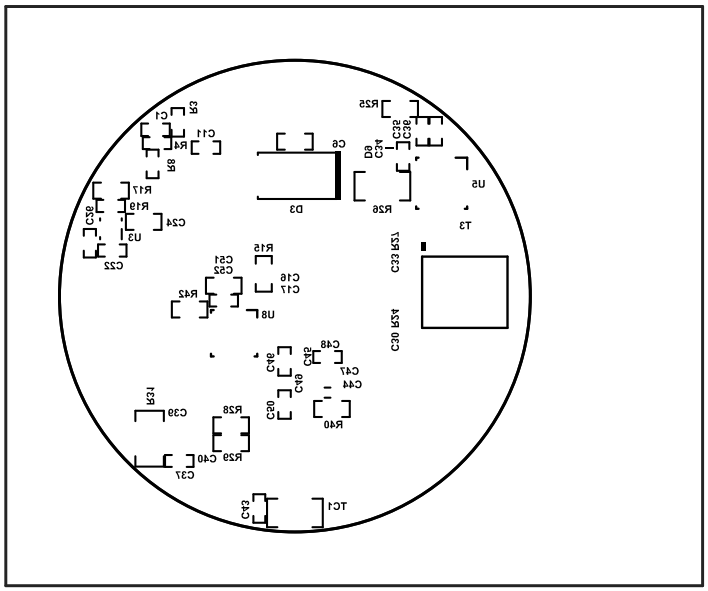


Figure 86. Bottom Overlay

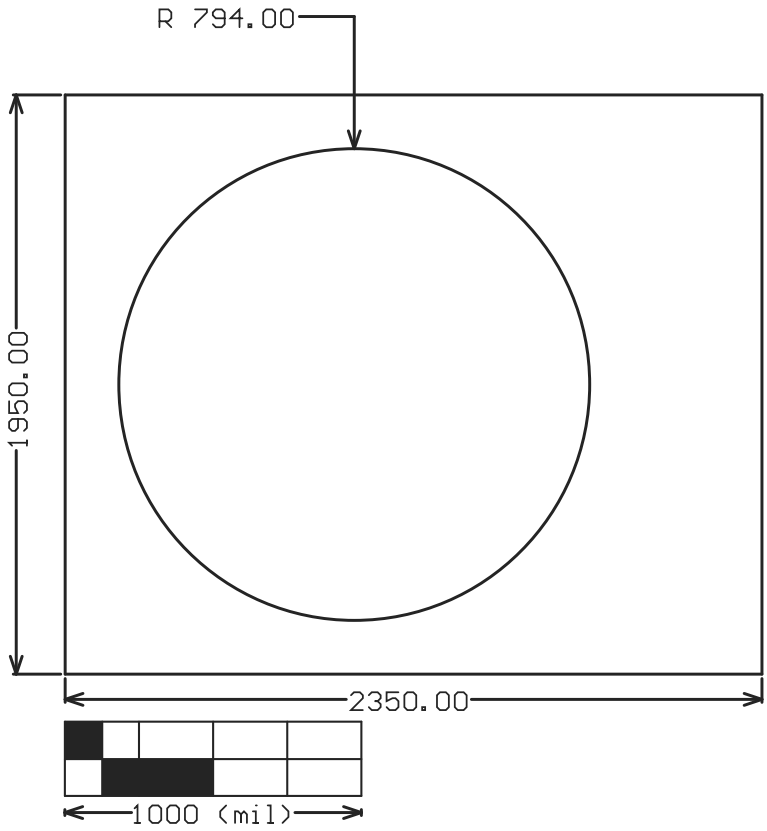
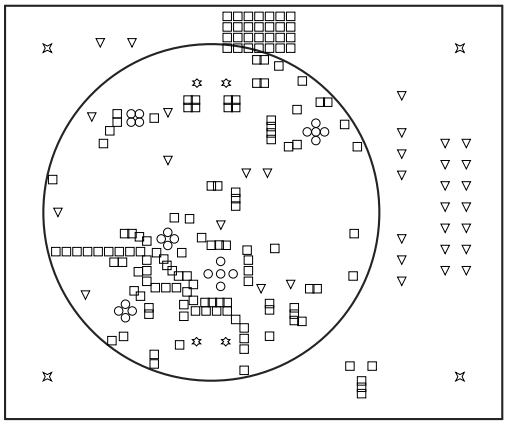


Figure 87. Board Dimensions



Symbol	Hit Count	Tool Size	Plated	Hole Type
○	22	7.874mil (0.2mm)	PTH	Round
□	147	10mil (0.254mm)	PTH	Round
▽	33	40mil (1.016mm)	PTH	Round
☼	4	50mil (1.27mm)	PTH	Round
⌑	4	125.984mil (3.2mm)	PTH	Round
	210 Total			

Drill Table

Figure 88. Drill Drawing

23 Altium Project Files

To download the Altium project files for each board, see the design files at TIDA-00189.

24 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00189.

25 Software Files

To download the software files for the reference design, see the design files at TIDA-00189.

26 About the Author

This document and the design concept and definition have been done by Giancarlo Candela. The full system design implementation and testing has been done by Alexander Weiler. Thomas Schneider has written the firmware. Juergen Schneider has conceived the innovative solution for the isolated power.

GIANCARLO CANDELA works in the Industrial Systems team at Texas Instruments Germany, where he is responsible for defining reference design and solutions for Industrial Sensor Transmitters. Giancarlo brings to this role his experience in system and product definition for high-precision analog and innovative sensing technologies.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (October 2014) to B Revision	Page
• Changed Figure 30	31
• Changed Figure 31	31
• Changed Figure 32	32

Revision A History

Changes from Original (October 2014) to A Revision	Page
• Changed gain from 3 to 32	28
• Changed the order of the design files, moved Schematics ahead of BOM	76

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