TI Designs

Thunderbolt™ Single Port Design Outline

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1 Introduction

This design guide will help a developer get started with a Thunderbolt™ single port design. For more information on Thunderbolt please refer to www.ti.com/thunderbolt

Single port Thunderbolt devices can come in two different forms. Self powered devices have an external supply to provide power to the device or bus powered device which use the available 10W provided. This design can be configured for both self or bus powered applications. Thunderbolt certification and testing has been completed for this design.

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2 High Level Design Information

2.1 Design Block Diagram

A Thunderbolt single port design consists of two main blocks, Thunderbolt data and power blocks. The Thunderbolt data block consists of a Thunderbolt controller and support system with various control signals. The Thunderbolt power block consists of all the needed supplies for a Thunderbolt system. There are three main power supplies in present in the system; main Thunderbolt power which powers the Thunderbolt controller and support system, Thunderbolt cable power which is needed to power the active Thunderbolt cable, and PCIe supply for PCIe bridge devices. Please check the block diagram below.

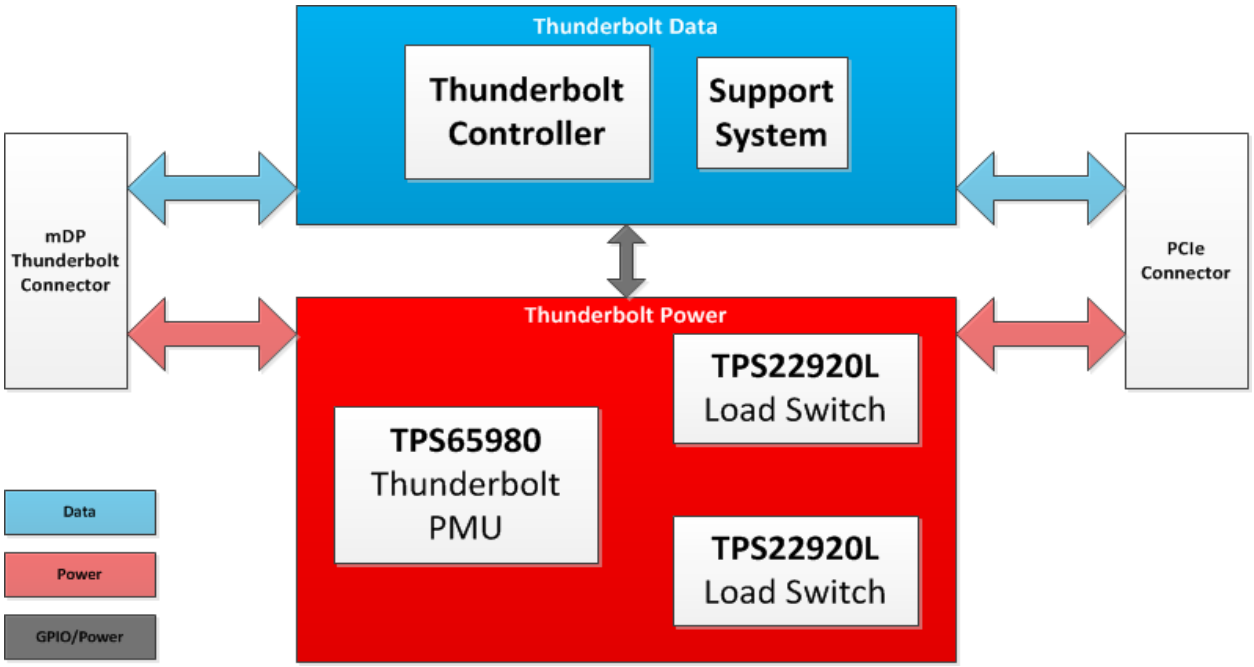

Figure 1. Design Block Diagram

2.2 TPS65980 Thunderbolt Bus Power Management Unit

The TPS65980 is the first fully integrated Thunderbolt Bus PMU which provides the needed power supplies (Thunderbolt main supply, Thunderbolt Cable supply, and PCIe supply) while meeting all of the power sequencing requirements of Thunderbolt. The TPS65980 also provides the needed control signals that interface between the Thunderbolt power and data blocks. The TPS65980 integrates many discrete subsystems which saves significantly on BOM cost, solution size, and reduces the design complexity. Find more information at http://www.ti.com/product/tps65980.

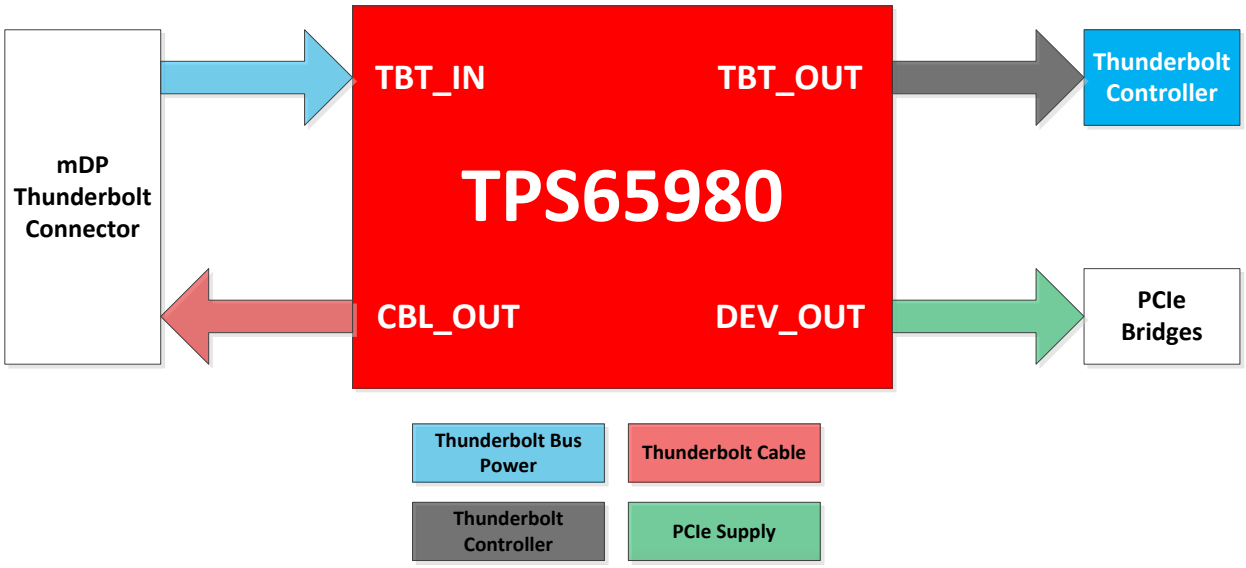

Figure 2. TPS65980 Power Diagram

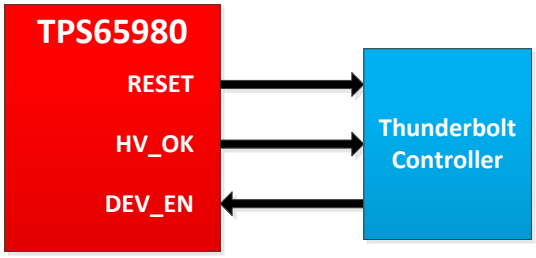

Figure 3. TPS65980 Control Signal Diagram

3 Design Details & Schematic

3.1 Schematic Net Description

Net	Description
Power Rails	
Main_Thunderbolt_Rail	Main 3.3V power rail that powers the Thunderbolt Controller and must remain constant during all operations of the systems
Cable_Power	3.3V current limited power rail that is sent back down the Thunderbolt cable to provide power to the active cable circuitry
PCIe_Aux_Supply	3.3V rail controlled by Thunderbolt controller to power PCIe bridge functions
Thunderbolt_Power_In	Thunderbolt bus power input from Thunderbolt connector
External_12V	External supply for self powered systems
TBT_IN	External_12V & Thunderbolt_Power_In diode-or for TPS65980 power input
Thunderbolt_High_Speed _Rail	Thunderbolt controller generated low voltage
Thunderbolt_High_Speed_Core_Rail	Thunderbolt controller input core voltage (TPS22920L)
Thunderbolt_Active_Rail	3.3V power rail for Thunderbolt active link (TPS22920L)
PCIe_12V	12V PCIe connector supply for self powered systems
Signal Nets	
Thunderbolt_Wake_EN	Thunderbolt controller generated signal to power up Thunderbolt_Active_Rail, and signal Thunderbolt link
External_Supply_Present	TPS3700 generated signal to indicated that external 12V supply is present in the system
PCIe_Aux_Supply_EN	Thunderbolt controller generated signal to control PCIe_Aux_Supply from TPS65980 (DEV_OUT)
RESET_N	TPS65980 generated signal to indicate to the Thunderbolt controller that Main_Thunderbolt_Rail is active
PCIe_Connector_Reset	Buffered PCIe reset signal from Thunderbolt controller
Thunderbolt_Controller_PCIe_Reset	Thunderbolt controller generated signal for PCIe reset
Thunderbolt_Data_R_0_P Thunderbolt_Data_R_0_N Thunderbolt_Data_R_1_P Thunderbolt_Data_R_1_N Thunderbolt_Data_D_1_P Thunderbolt_Data_D_1_N Thunderbolt_Data_D_0_P Thunderbolt_Data_D_0_N	Thunderbolt high speed data lines
LSTX LSRX Buffer_LSRX	Low speed RX and TX data lines
Config_1 Config_2	Thunderbolt configuration pins

3.2 Schematic: TPS65980 Block

Check the figure below for the TPS65980 schematic. The schematic for The TPS65980 uses 20uF (C44, C56, C49) for TBT_IN and may be increased to 52uF, the maximum allowed bus power capacitance. The TBT_OUT capacitance for the TPS65980 is limited to 68uF. C43, 64, C50 are the output capacitance for the TPS65980 and C65, C66, C67, C68 are the input capacitance to the Thunderbolt controller which is supplied through TBT_OUT. Careful consideration of inductor current rating and capacitor de-rating is recommended, as it is in every system. For a quick start the TPS65980EVM schematic can be used as a reference.

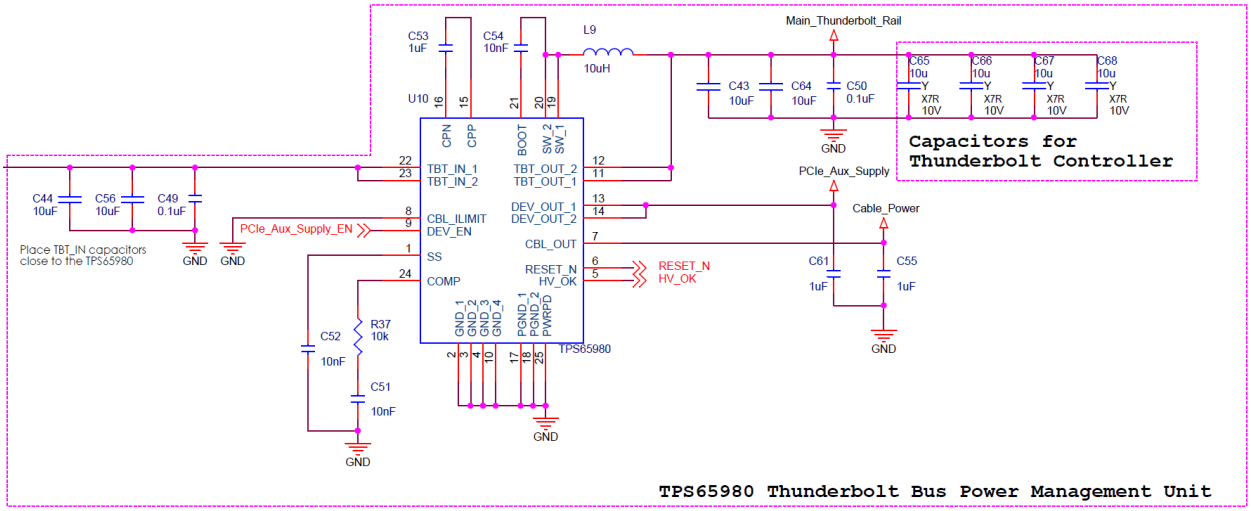

Figure 4. TPS65980 Schematic

When doing layout for the TPS65980 it is best to follow the Figure 5. below. Most of the components are placed on the top side of the board with the exception of the DEV_OUT cap which is placed on the bottom side. DEV_OUT is best routed to the bottom layer of the board to allow for closer placement of the inductor. When sufficient top side ground and vias from the PowerPad to ground plane are used the best thermal performance is achieved. Placing the TBT_IN capacitors close to the device and allowing the PGND and GND from TBT_IN capacitors to share the top plane will limit the amount of noise generated by the TPS65980 power stage. The TBT_OUT capacitor(s) should be placed closed to the TPS65980 and right after the inductor.

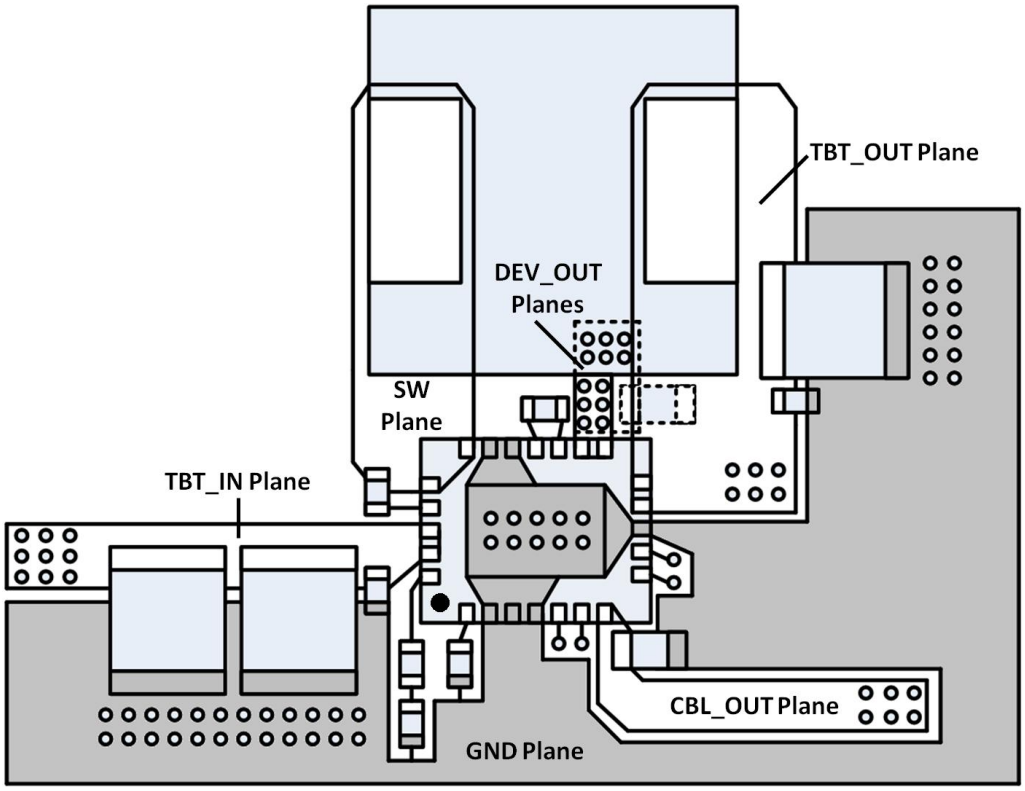

Figure 5. TPS65980 Layout Example

3.3 Schematic: TPS22920L for Thunderbolt_Active_Rail

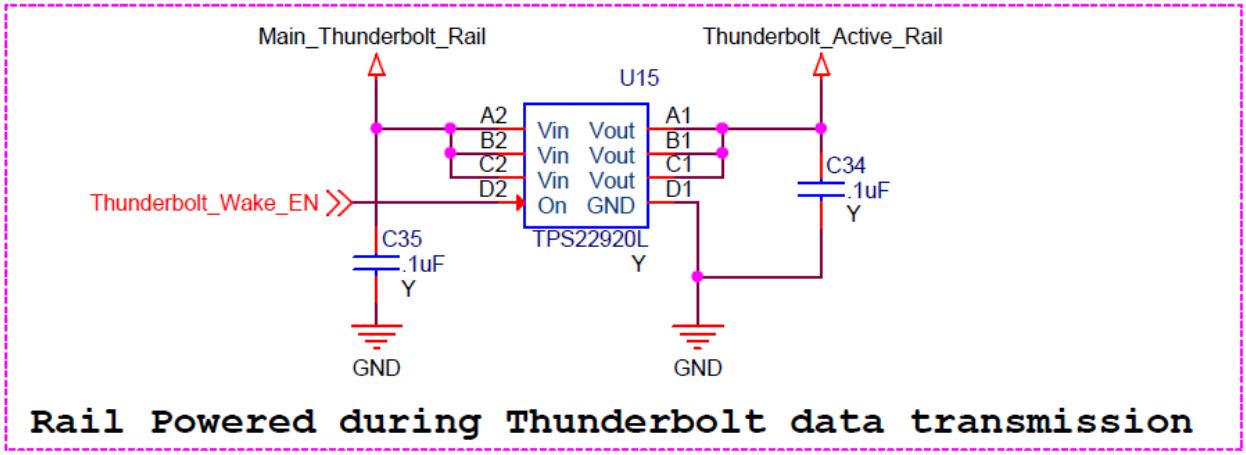

Figure 6. TPS22920L Schematic for Thunderbolt_Active_Rail

3.4 Schematic: TPS22920L for Thunderbolt_High_Speed_Core_Rail

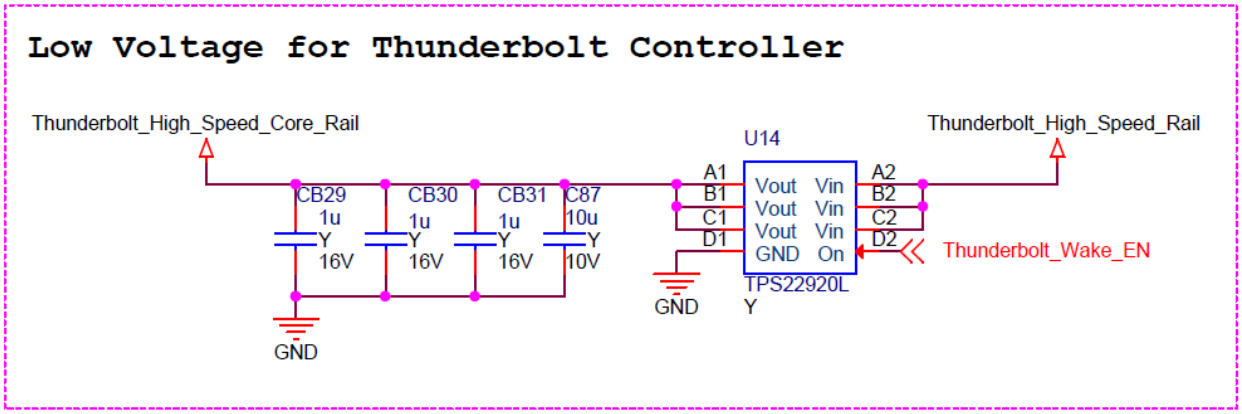

Figure 7. TPS22920L Schematic for Thunderbolt_High_Speed_Core_Rail

3.5 Schematic: Bus Power or Self Power Configuration

The design covered can be configured as a bus or self powered system. For bus powered systems the self powered components maybe removed from the design and the vice-a-versa for a self powered system. When used in a bus power configuration, J2 power jack, DB2 & DB3 “diode or”, U13 TPS3700, and Q2 & Q3 with passives should be removed. Self powered applications should include all of the components in the design.

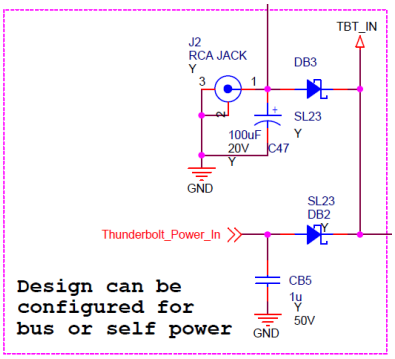

Figure 8. Bus or Self Power Input

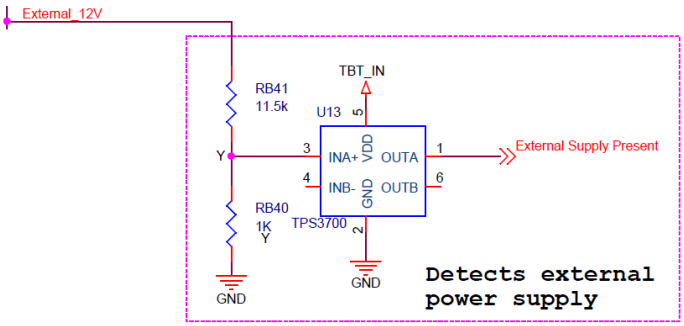

Figure 9. External Supply Present Schematic

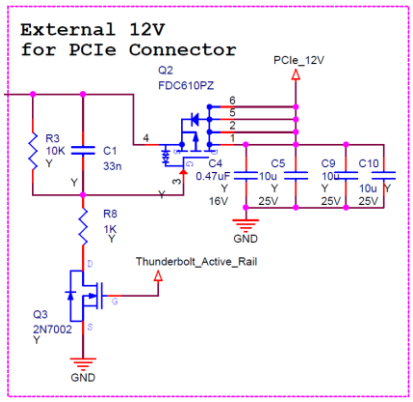

Figure 10. PCIe_12V Control from External Power

3.6 Schematic: Thunderbolt Connector & Control Signals

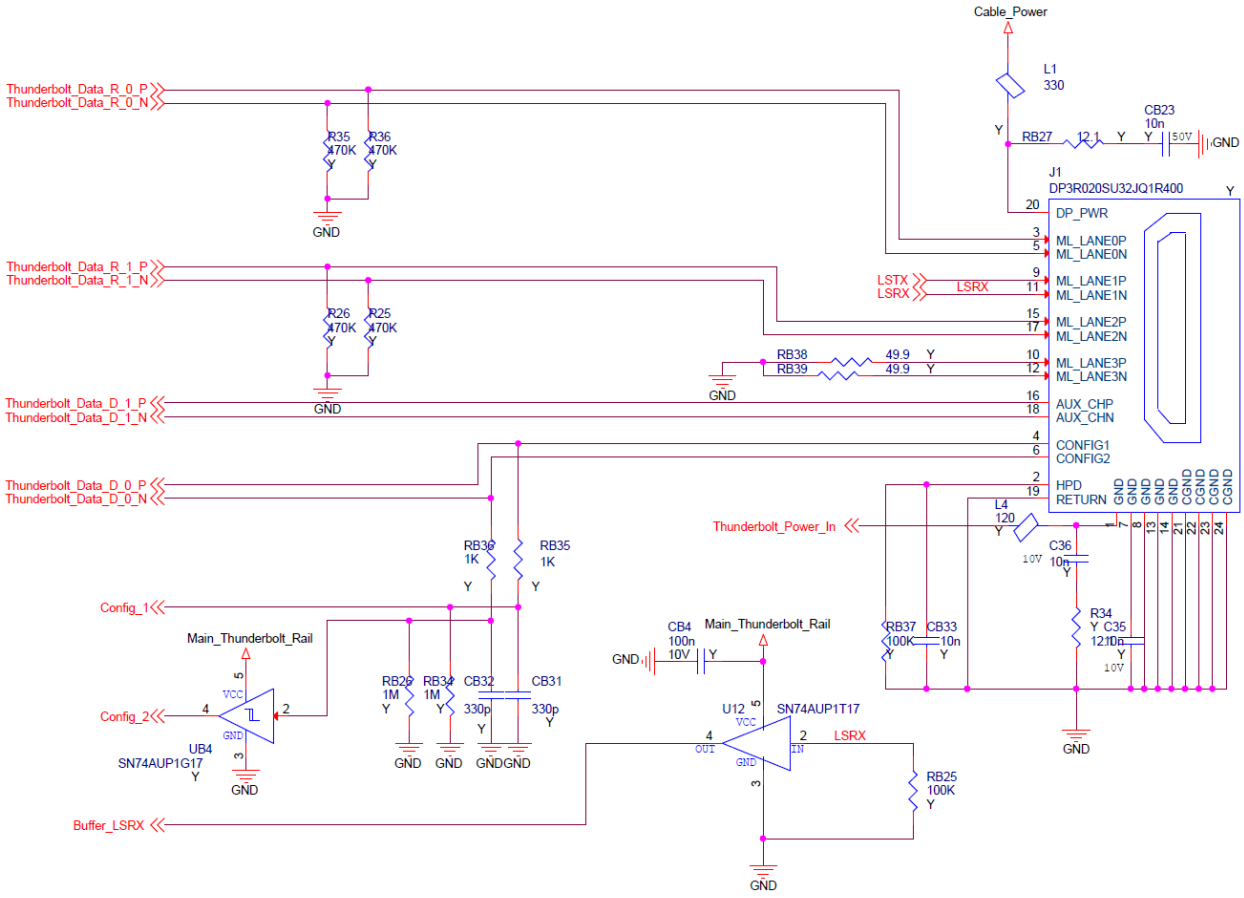

Figure 11. Thunderbolt Connector

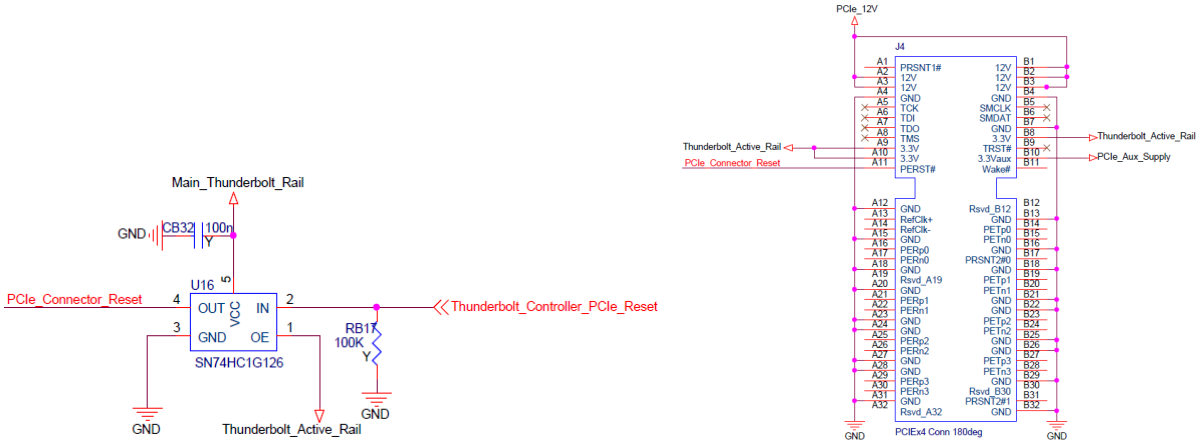

Figure 12. PCIe Connector and PCIe Reset Schematic

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