Peter Semig, Timothy Claycomb

TI Designs – Precision: Verified Design

Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design

TI Designs – Precision

TI Designs – Precision are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Circuit Description

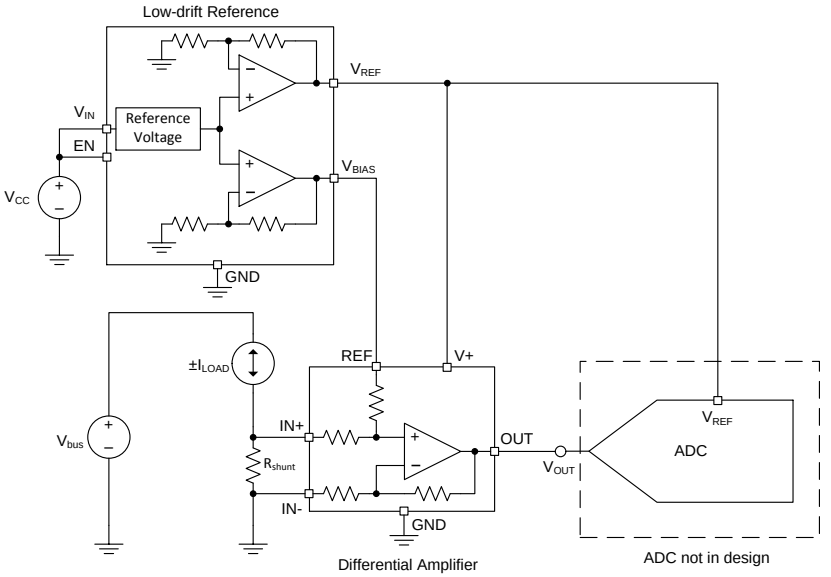
This low-drift, bidirectional, single-supply, low-side current sensing reference design can accurately detect load currents from -2.5 A to +2.5 A. The linear range of the output is from 250 mV to 2.75 V. Positive current is represented by output voltages from 1.5 V to 2.75 V whereas negative current is represented by output voltages from 250 mV to 1.5V. The difference amplifier is the INA213B current shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
REF2030	Product Folder
INA213	Product Folder

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Designs – Precision Library



1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5.0 V
- Load current: ±2.5 A
- Output: 250 mV – 2.75 V
- Maximum Shunt Voltage: ±25 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Calculated, and Measured Performance

				Measured	
	Goal	**Calculated**	**Simulated**	**Un-calibrated**	**Calibrated**
Full Scale Range Error (25ºC)	±0.1%	±0.117%	±0.032%	±0.036%	±0.004%
Full Scale Range Error (-40ºC to 125ºC)	±0.15%	±0.2%	N/A	±0.052%	±0.061%

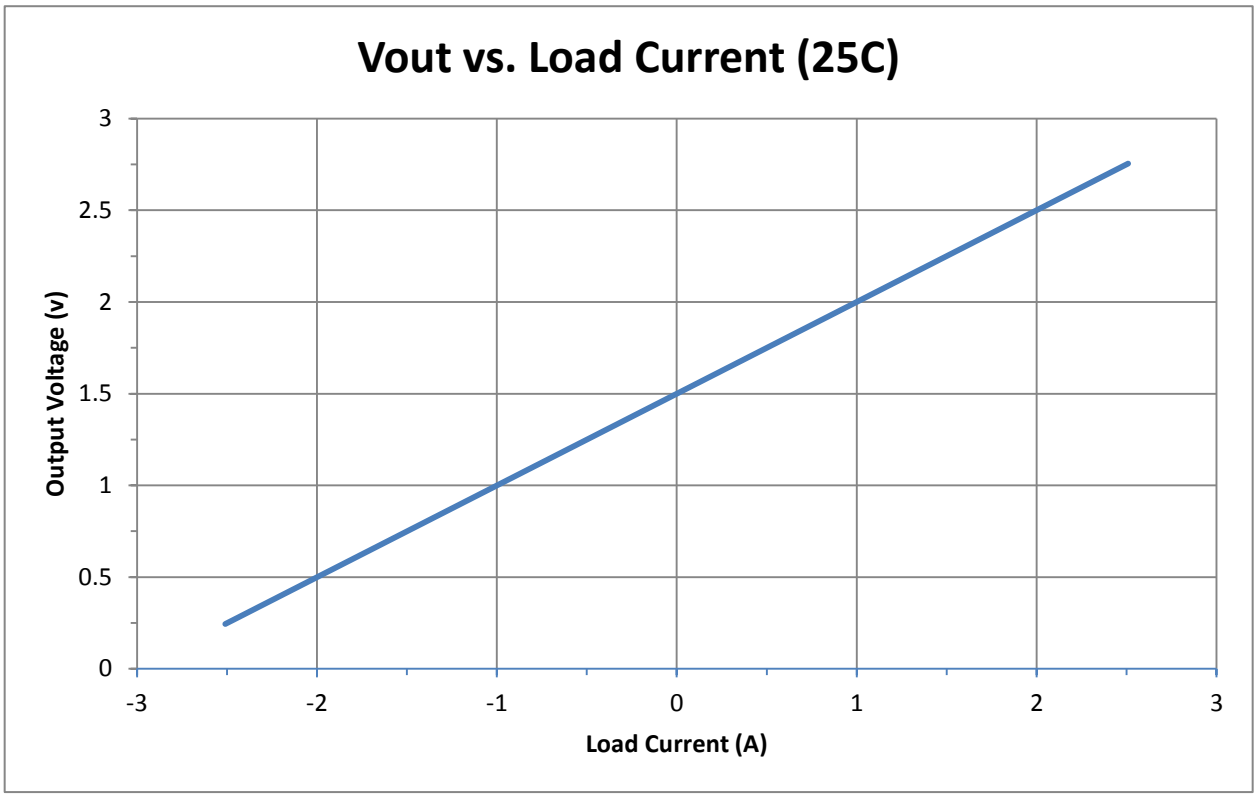


Figure 1: Measured Transfer Function

2 Theory of Operation

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of the bus voltage, V_{bus}. When sensing bidirectional currents, use a differential amplifier with a reference pin. This allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (V+) and the reference voltage (REF, or V_{BIAS}) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 2 depicts the general circuit topology for a low-drift, low-side, bidirectional current sensing solution.

This topology is particularly useful when interfacing with an analog-to-digital converter, as shown on the cover page. Not only will V_{REF} and V_{BIAS} track over temperature, their matching is much better than alternate topologies. A common alternate topology is discussed in Section 7.1.

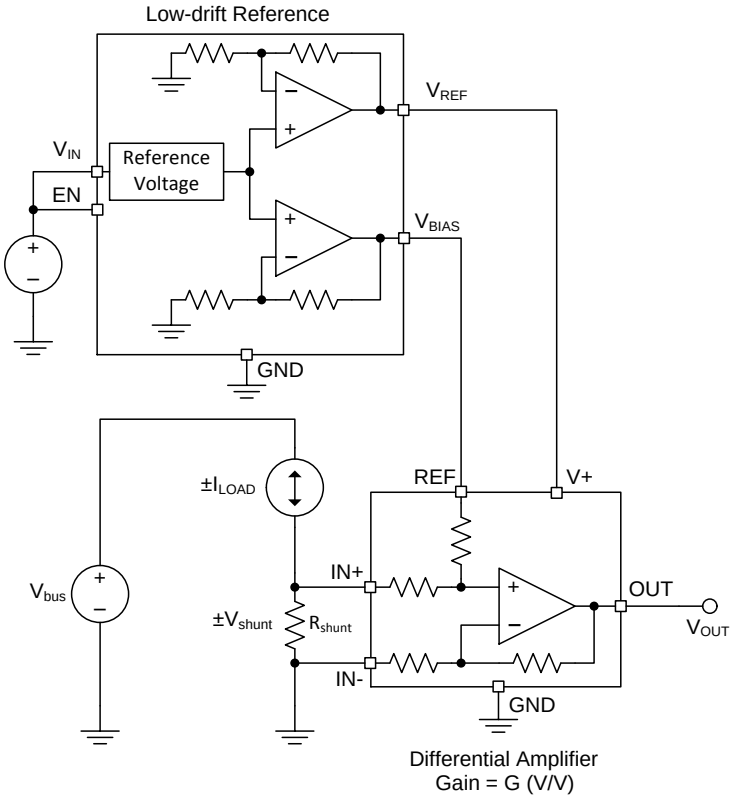


Figure 2: Low-drift, low-side, bidirectional circuit topology

2.1 Transfer Function

The transfer function for the circuit given in Figure 2 is shown in Equation (**1**).

$$V_{OUT} = G \times (\pm V_{shunt}) + V_{BIAS} = G \times (\pm I_{LOAD} \times R_{shunt}) + V_{BIAS} \quad (1)$$

3 Component Selection

3.1 Shunt Resistor (R_{shunt})

As shown in Figure 2, the value of V_{shunt} is the ground potential for the system load. If the value of V_{shunt} is too large, it may cause issues when interfacing with systems whose ground potential is truly 0 V. If the value of V_{shunt} is too negative, it may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore it is important to limit the voltage across the shunt resistor. Equation (2) can be used to calculate the maximum value of R_{shunt}.

$$R_{sh(max)} = \frac{V_{sh(max)}}{I_{load(max)}} \quad (2)$$

Given that the maximum shunt voltage is ±25 mV and load current range is ±2.5 A, the maximum shunt resistance is calculated as shown in Equation (**3**).

$$R_{sh(max)} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{25mV}{2.5A} = 10m\Omega \quad (3)$$

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor was selected because it has the following specifications:

- R_{nom}: 10 mΩ
- Tolerance: 0.1% (max)
- Drift: 15 ppm/ºC (max)
- 4-terminal (Kelvin-connected)

3.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

- Single-supply (3V)
- Reference voltage input
- Low initial input offset voltage (V_{os})
- Low-drift
- Fixed gain
- Low-side sensing (input common-mode range below ground)

For this design, a current shunt monitor (INA213B) was selected. The INA21x family topology is shown in Figure 3.

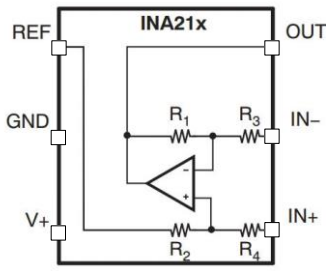


Figure 3: INA21x Current Shunt Monitor Topology

The INA213B has the following specifications:

- Supply Voltage Range: +2.7 V to +26 V
- Common-mode Input: -100 mV < V_{cm} < +26 V
- Output swing (V+ = 3 V): 50 mV < V_{out} < 2.8 V
- Reference voltage input
- V_{os} = ±5 µV (typ)
- $V_{os\text{-}drift}$ = 0.1 µV/ºC (typ)
- Fixed Gain = 50 V/V

Therefore, the INA213B is an excellent choice for this application. Other differential amplifiers were considered but ultimately eliminated for a variety of reasons. In general, instrumentation amplifiers that are powered with a single supply have limited output swing when the input common-mode voltage is near ground. In addition, they require external resistors to set their gain. This is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce the accuracy of the solution at small load currents. In addition, difference amplifiers typically have a gain of 1 V/V. When adjustable, however, they use external resistors which are not conducive to low-drift applications.

3.3 Reference

The reference for this application should have the following features:

- Dual output
  - 3.0V
  - 1.5V
- Low-drift

For this design, the REF2030 was selected. The REF20xx family topology is shown in Figure 4.

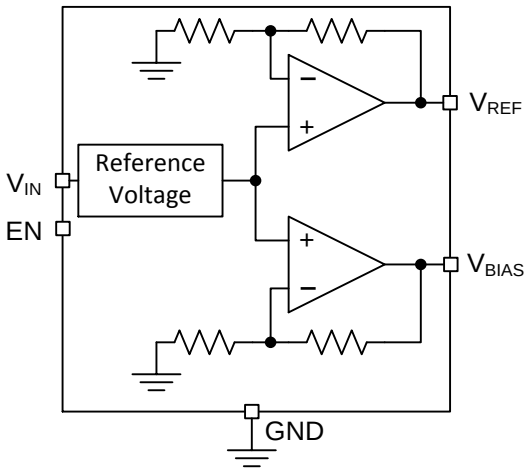


Figure 4: REF20xx Topology

The REF2030 has the following specifications:

- Input Voltage: 3.02V to 5.5 V
- V_{BIAS} output: 1.5 V
- V_{REF} output: 3.0 V
- Output Drift: 3 ppm/ºC (typ), 8 ppm/ºC (max)
- Output voltage accuracy = ±0.05% (max)

4 Simulation & Error Calculation

4.1 Simulation

Figure 5 depicts the TINA-TI® simulation schematic.

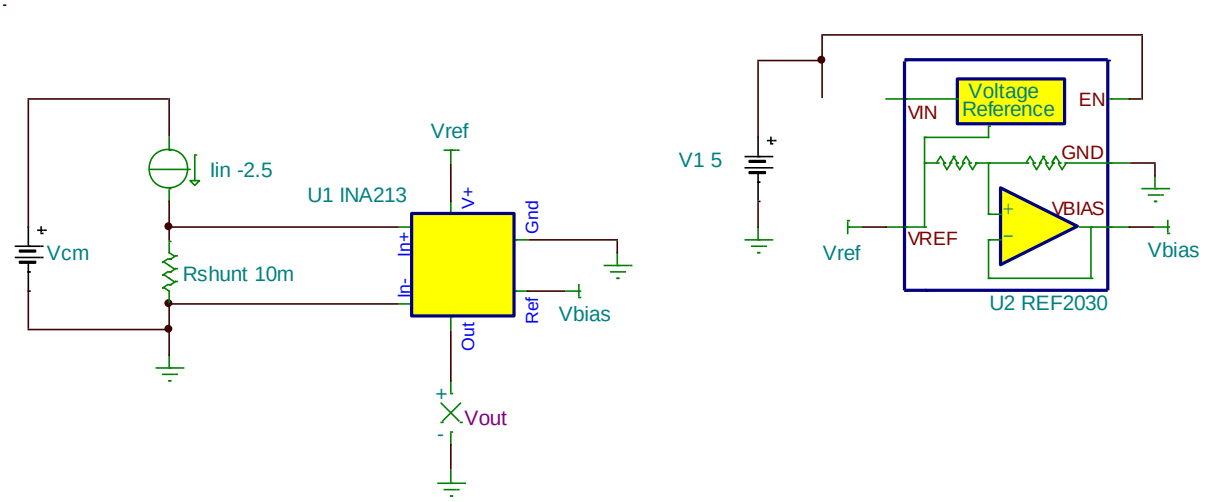


Figure 5: TINA-TI® Schematic

Figure 6 depicts the output for load currents (I_{in}) from -2.5 A to +2.5A. Notice the output is 1.5 V when the input current is 0 A. For positive current (0 A to 2.5 A) the output range is from 1.5 V to 2.75 V. Similarly, for negative currents (0 A to -2.5 A) the output range is from 1.5 V to 250 mV. This is consistent with the original design of the circuit.

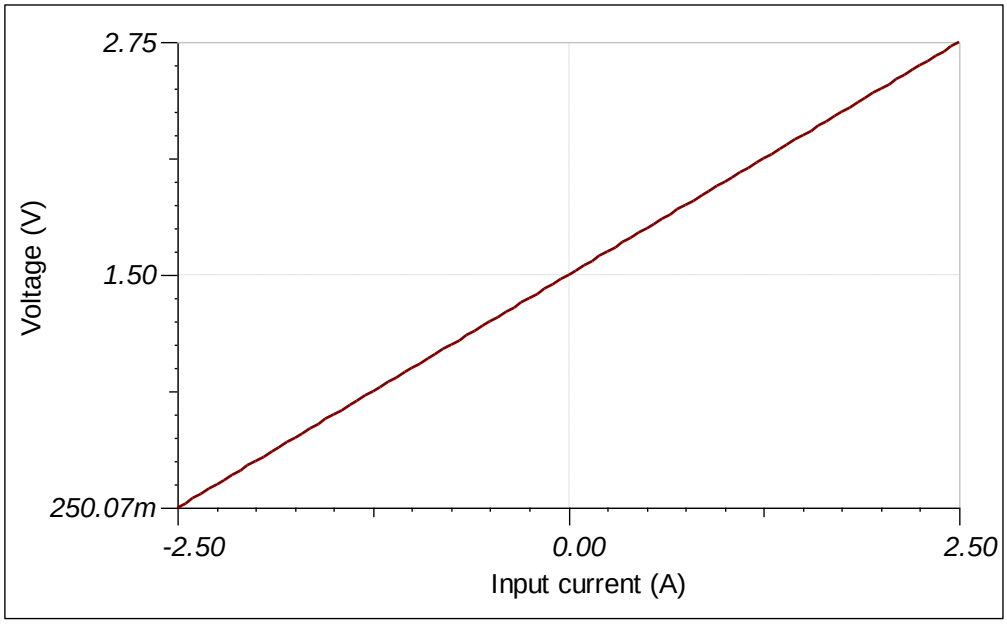


Figure 6: Functionality Simulation

A 1000-point Monte-Carlo analysis of the circuit in Figure 5 was performed after setting the tolerance of R_{shunt} is to 0.1%. Figure 7 depicts a histogram of the output voltage at maximum load current.

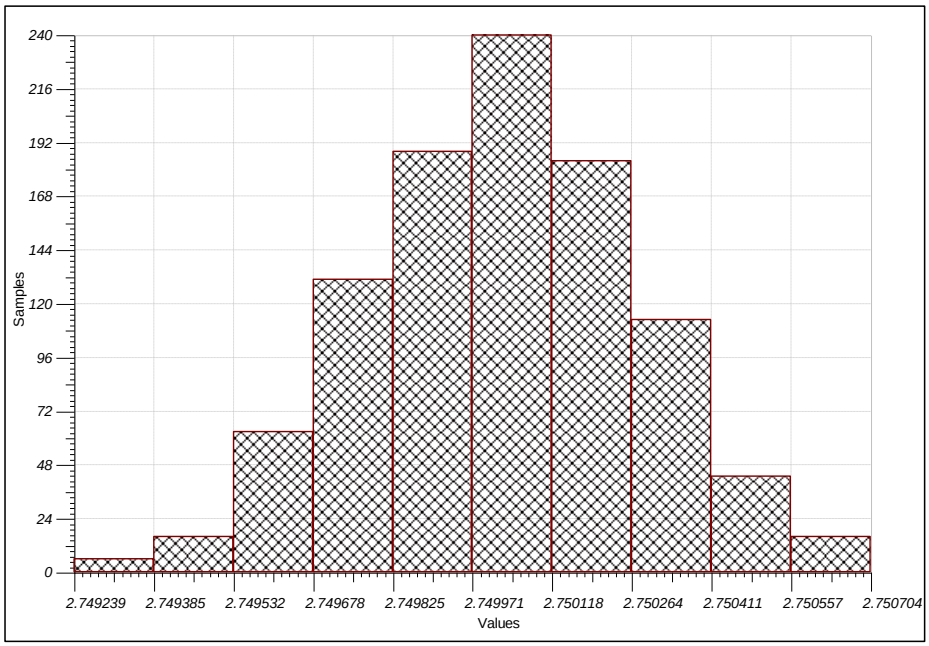


Figure 7: Output Voltage Histogram for Maximum Load (2.5 A)

Please note that this does not include errors associated with temperature drift. In addition, only typical performance of the INA213B and REF2030 are modeled.

The distribution statistics for maximum and minimum load current are summarized in Table 2.

Table 2. DC Transfer Results – Distribution Statistics

	Average (μ)	Std. Dev. (σ)	Nominal
Vout @ -2.5 A	250.06895mV	247.498735uV	250.065852mV
Vout @ 2.5 A	2.750028V	247.499021μV	2.750031V

Using the average (or mean) and the standard deviation from the simulation, a six-sigma (±3**σ**) calculation of the full-scale error for maximum load (2.5 A) is calculated using Equation **(4)**. This represents the error with 99.7% confidence.

$$E_{\%FSR} = 100 \times \frac{(\mu \pm 3\sigma) - V_{out-ideal}}{FSR} = \pm 0.031\% \quad (4)$$

Similarly, the error for minimum load current can be calculated using the same equation.

4.2 Simulated Results Summary

Table 3 is a summary of the simulated error results.

Table 3. Simulated Results Summary

	Goal	Simulated
Full Scale Error @ -2.5 A, 25ºC	±0.1%	±0.032%
Full Scale Error @ +2.5 A, 25ºC	±0.1%	±0.031%

4.3 Error Calculation

Two types of errors will be discussed: initial accuracy and drift. Accuracy errors include:

- Shunt resistor tolerance: α_{shunt_tol} = 0.1% (max)
- INA initial input offset voltage: V_{os_INA} = 5 µV (typ)
- INA PSRR: $V_{os\_INA\_PSRR}$ = 0.1 µV/V (typ)
- INA CMRR: $V_{os\_INA\_CMRR}$ = 120 dB (typ)
- INA gain error: α_{INA_GE} = 0.02% (typ)
- Reference output accuracy: α_{REF_output} = 0.05% (max)

It should be noted that these error sources can be greatly reduced at 25ºC by performing a two point system calibration. Drift errors, on the other hand, can only be reduced by performing the calibration over temperature. The drift errors include:

- Shunt resistor drift: δ_{shunt_drift} = 15 ppm/ºC (max)
- INA offset voltage drift: $\delta_{INA\_drift\_Vos}$ = 0.1 µV/ºC (typ)
- INA gain error drift: $\delta_{INA\_drift\_GE}$ = 3 ppm/ºC (typ)
- Reference output drift: $\delta_{REF\_drift\_output}$ = 3 ppm/ºC (typ)

Equation **(5)** can be used to convert specifications given in parts per million (ppm) to a percentage (%), and vice versa.

$$\% = \frac{ppm}{10{,}000} \quad (5)$$

Equation **(6)** can be used to convert specifications given in decibels (dB) to a linear representation.

$$\frac{V}{V} = \frac{1}{10^{\frac{dB}{20}}} \quad (6)$$

For some error calculations a full-scale range (FSR) is required. The FSR for this design is determined by the voltage across the shunt resistor, which is ±25 mV (or 50 mV).

For drift errors, the largest change in temperature (ΔT) is 100ºC, which is the difference between the maximum specified temperature (125ºC) and room temperature (25ºC). This temperature change is used when calculating drift errors for the shunt resistor and INA213B. Since the REF2030 uses the box method to determine drift, the temperature range used for calculations is the entire operating range, or 165ºC.

Finally, errors due to CMRR and PSRR specifications require an adjustment depending on the difference between the system's requirements and how the devices were characterized. For example, the INA213B was characterized using a common-mode voltage of 12 V. The common-mode voltage in this design is ~0V. This discrepancy causes an input-referred offset voltage.

All calculations for this system can be found in Appendix B.

4.3.1 Initial Accuracy

Table 4 summarizes the initial accuracy calculations from Appendix B.

Table 4. Initial Accuracy Error Summary

	Device			
Error Source	**R_{shunt} (ppm)**	**INA213B (ppm)**	**REF2030 (ppm)**	**Total (ppm, RSS)**
Offset		100 FSR	500 FSR	510 FSR
CMRR		240 FSR		240 FSR
PSRR		4 FSR		4 FSR
Gain Error	1000	200		1020
Total (ppm, RSS)	1000	328 FSR	500 FSR	1165 FSR (0.117%)

4.3.2 Temperature Drift

Table 5 summarizes the total temperature drift calculations from Appendix B.

Table 5. Temperature Drift Error Summary

	Device			
Error Source	**R_{shunt} (ppm)**	**INA213B (ppm)**	**REF2030 (ppm)**	**Total (ppm, RSS)**
Offset Drift		200 FSR	495	534 FSR
Gain Error Drift	1500	300		1530
Total (ppm, RSS)	1500	361 FSR	495	1621 FSR (0.24%)

4.3.3 Total System Error

Equation (**7**) calculate the total system error over temperature.

$$E_{system} = \sqrt{1165 ppm^2 + 1621 ppm^2} = 1996 ppm = 0.2\% \quad (7)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB layout is depicted in Figure 8. Please follow common PCB layout practices such as placing power supply bypass capacitors close to the devices' supply pins. In addition, be sure to Kelvin-connect the shunt resistor. In this case, the shunt resistor has 4 terminals and is already Kelvin-connected. Finally, be sure to minimize any impedance between the shunt and ground plane. This was accomplished by pouring the ground plane without thermal relief spokes and placing the GND connection as close to R_{shunt} as possible.

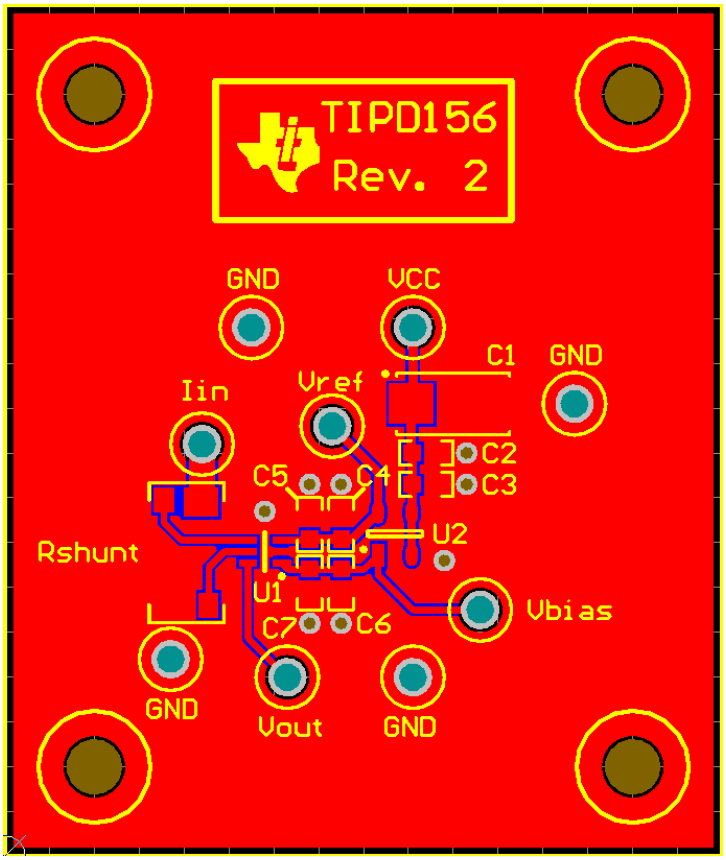


Figure 8: PCB Layout

6 Verification & Measured Performance

6.1 Transfer Function

Data was collected by sweeping the load current from -2.5A to +2.5A and measuring the output of the INA213B. In addition, the load current, reference voltage, and bias voltage were measured. Finally, data was taken at the following temperatures: -40ºC, -25ºC, 0ºC, 25ºC, 50ºC, 85ºC, and 125ºC.

Figure 9 depicts the measured transfer function of the design at 25ºC.

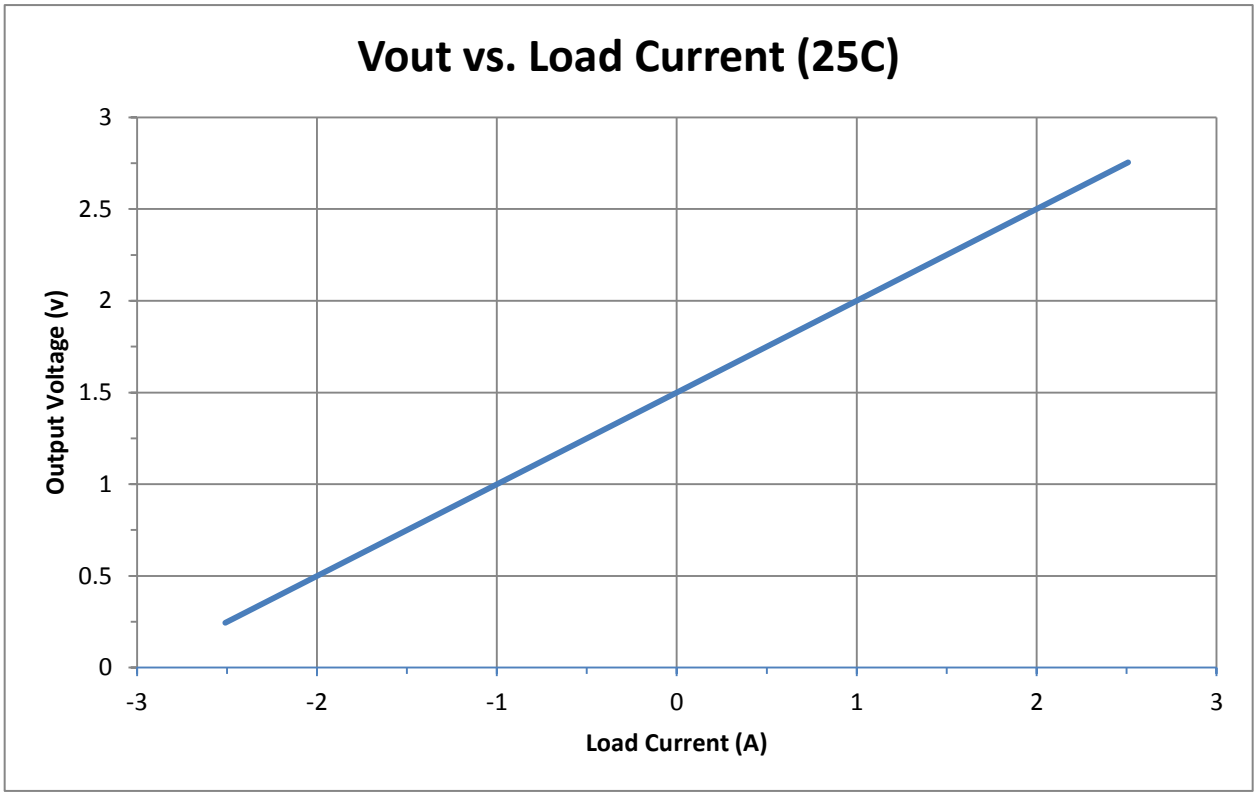


Figure 9: Measured Transfer Function

6.2 Un-calibrated Error

Equation **(8)** was used to calculate the error for each measurement sweep. Un-calibrated error includes both initial accuracy errors (e.g. offset voltage, CMRR, etc.) and errors associated with temperature drift.

Note that the load current was measured and used in the calculations as the ideal load current. This removes any errors associated with the generation of the load current.

$$E_{\%FSR} = 100 \times \frac{V_{out-meas} - V_{out-ideal}}{FSR} \quad (8)$$

Where

$$V_{out-ideal} = V_{bias-ideal} + \left(I_{load-meas} \times R_{shunt-ideal} \times G_{ideal}\right) = 1.5V + \left(I_{load-meas} \times 10m\Omega \times 50\frac{V}{V}\right) \quad (9)$$

$$FSR = V_{out-max-ideal} - V_{out-min-ideal} = 2.75V - 250mV = 2.5V \quad (10)$$

Figure 10 depicts the measured error versus load current for all temperatures.

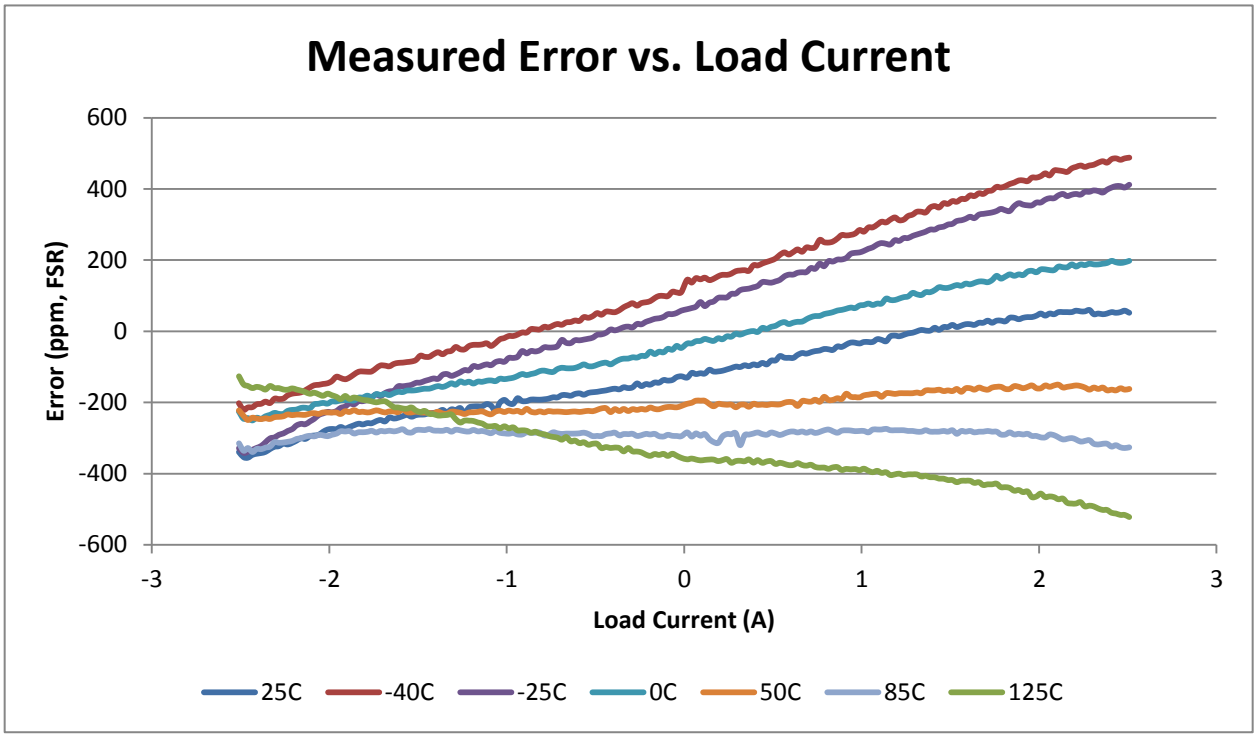


Figure 10: Total Unadjusted Error

The largest error (-522 ppm) occurs at maximum load current and an ambient temperature of 125ºC. The typical calculated error for this design is ±1996 ppm.

Figure 11 shows the measured error of this system with respect to the calculated error limits.

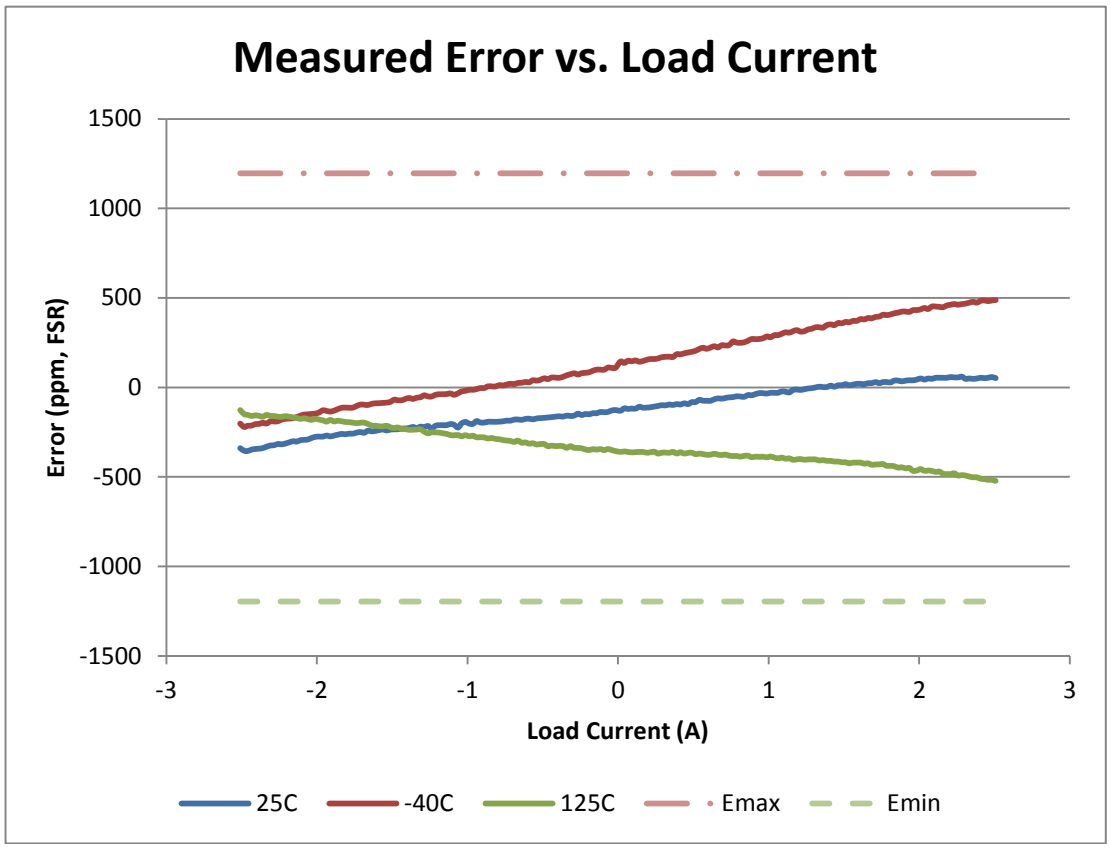


Figure 11: Total Unadjusted Error with Min/Max Error Limits

6.3 Calibration

Performing a 2-point calibration at 25ºC removes the errors associated with offset voltage, gain error, etc. The two data points selected for this calibration occur at ~25% and ~75% of the full load current range, or -1.88623 A and +1.88613 A, respectively. Table 6 depicts the data required for the calibration.

Table 6. Data for Calibration

	Iload(25%) = -1.88623A		**Iload(75%) = +1.88613**	
	Measured (M)	Ideal (I)	Measured (M)	Ideal (I)
Vout (V)	0.556213	0.556885	2.44315	2.443065

The gain correction factor (α) and offset correction factor (β) are calculated as shown in Equations **(11)** and **(12)**, respectively. It is important to note that these values are not gain or offset error terms.

$$\alpha = \frac{V_{out-ideal@75\%} - V_{out-ideal@25\%}}{V_{out-meas@75\%} - V_{out-meas@25\%}} = \frac{2.443065 - 0.556885}{2.44315 - 0.556213} = 0.99959882 \quad (11)$$

$$\beta = \left(\alpha \times V_{out-meas@25\%}\right) - V_{out-ideal@25\%} = (0.99959882 \times 0.556213) - 0.556885 = -895.14153134\ \mu \quad (12)$$

Equation **(13)** can be applied to the un-calibrated output voltage to obtain the calibrated output voltage.

$$V_{out-cal} = (V_{out-uncal} - \beta) \times \alpha \quad (13)$$

Figure 12 compares the un-calibrated and calibrated performance at 25ºC.

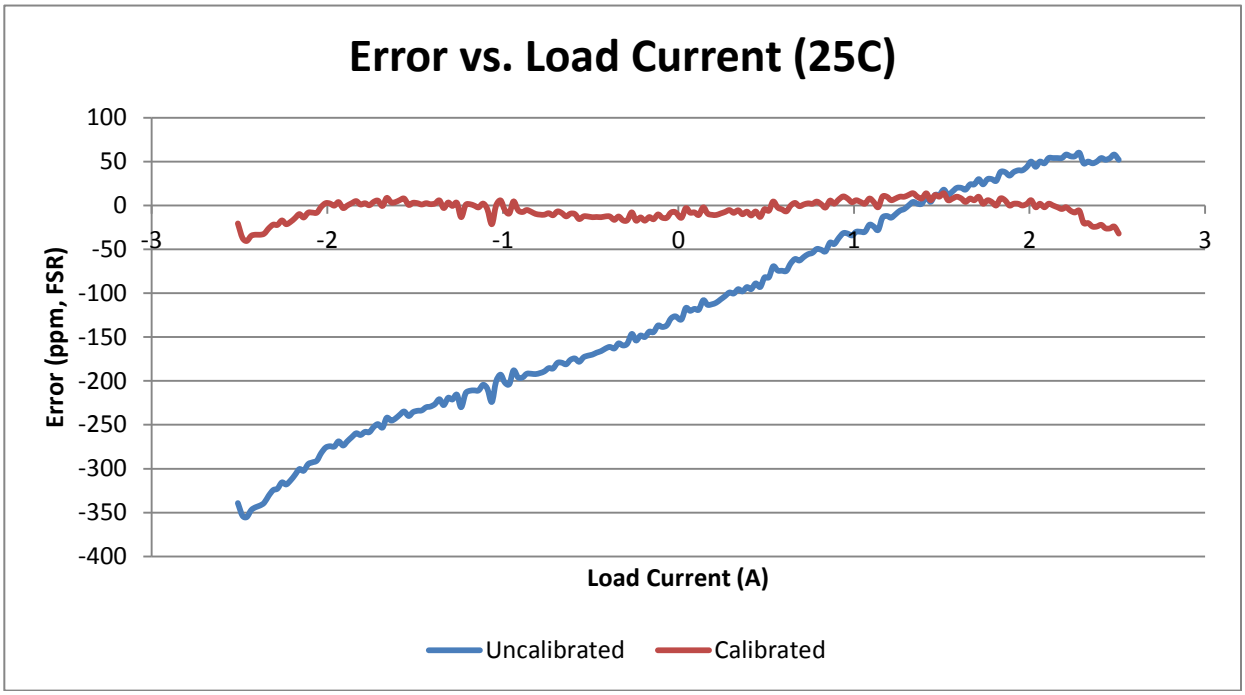


Figure 12: Effect of Calibration at 25ºC

The error decreased from -355 ppm to -40.5 ppm. Applying the correction factors from the 25ºC data to error curves with a similar, positive slope will decrease the error. However, applying the correction factors to an error curve with a negative slope can actually increase the error.

Figure 13 shows that the error at 125ºC increased from -522 ppm to -606 ppm after applying the 25ºC correction factors.

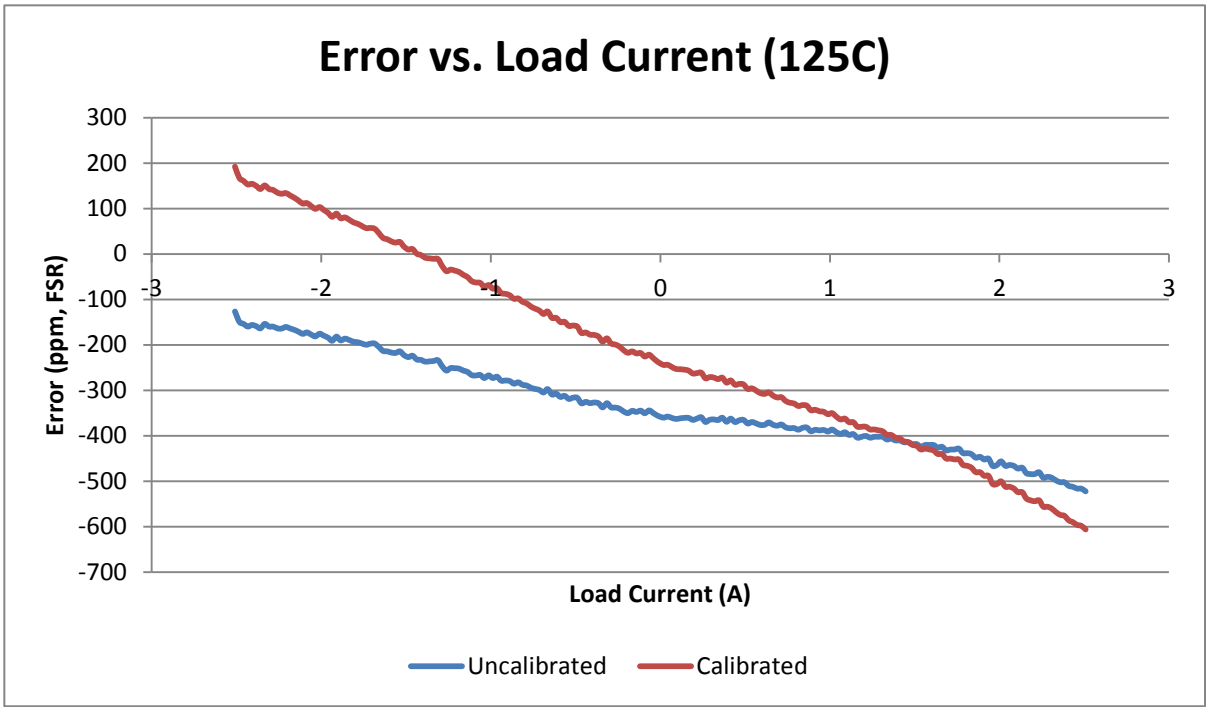


Figure 13: Effect of 25ºC Calibration Factors at 125ºC

Figure 14 shows the calibrated error for all temperatures. The largest error (-606 ppm) occurs at maximum load current and an ambient temperature of 125ºC. This error is larger than the un-calibrated solution. Therefore, if the un-calibrated error is unacceptable, a multi-temperature calibration is required.

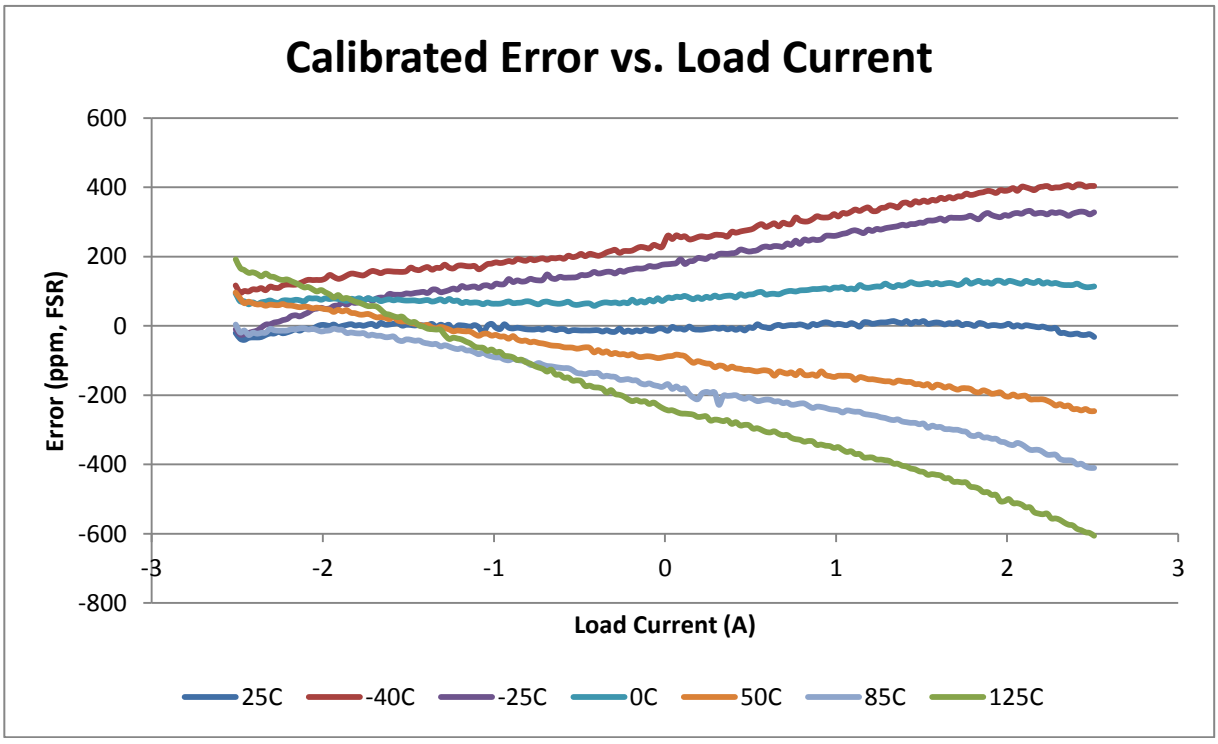


Figure 14: Effects of 25ºC Calibration Factors on All Temps

Table 7 summarizes the measured results.

Table 7. Measured Results Summary

		Measured	
	Goal	**Un-calibrated**	**Calibrated**
Full Scale Range Error (25ºC)	±0.1%	±0.0355%	±0.004%
Full Scale Range Error (-40ºC to 125ºC)	±0.15%	±0.0522%	±0.0606%

7 Modifications

The shunt resistor may be increased/decreased depending on the load current range. In order to maintain the output voltage range, however, the current shunt monitor gain should be increased or decreased accordingly. Please note that current shunt monitors typically have fixed gains. If the load current increases, be sure to keep in mind the power that needs to be dissipated by the shunt resistor.

Besides the shunt resistor and current shunt monitor, the REF2030 may be replaced with a discrete solution. The following section will show the complete analysis for such a modification.

7.1 Discrete Topology

A common method for generating the supply voltage (V_{REF}) and reference voltage (V_{BIAS}) is shown in Figure 15. This method uses 4 discrete components: reference, voltage divider (R_1 and R_2), and a buffer amplifier. The output of the reference device is divided down according to Equation (**14**).

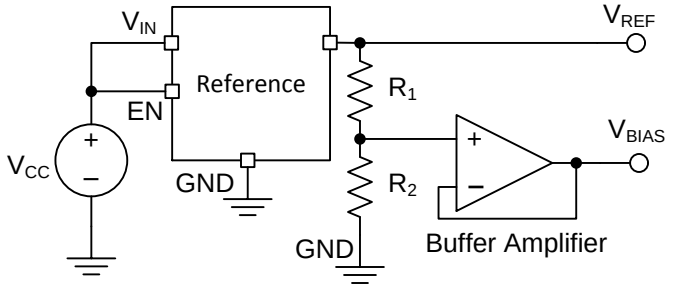


Figure 15: Discrete Topology

$$V_{BIAS} = V_{REF} \times \frac{R_2}{R_1 + R_2} \quad (14)$$

The drift performance of V_{REF} (δ_{VREF}) is determined by the reference drift. Table 8 compares low-drift reference devices with the REF2030.

Table 8. Low-drift Reference Comparison

Device	Output (s) (V)	Drift (ppm/ºC, typ)	Drift Tracking (ppm/ºC, typ)	Accuracy (max)	Cost (1ku)
REF2030	3.0 1.5	3	2	0.05%	$1.40
REF5030	3.0 N/A	2.5	N/A	0.05%	$2.95
REF5030A	3.0 N/A	3	N/A	0.1%	$1.35
REF3230	3.0 N/A	4	N/A	0.2%	$1.70

The REF5030A was selected because of cost and accuracy.

The drift performance of the V_{BIAS} output will depend on the drifts of the reference (δ_{REF}), resistor divider network (δ_{RDIV}), and buffer amplifier (δ_{BUF}). Equation (**15**) depicts the total drift for the V_{BIAS} output (δ_{Vbias}).

$$\delta_{Vbias} = \sqrt{\delta_{REF}{}^2 + \delta_{RDIV}{}^2 + \delta_{BUF}{}^2} \quad (15)$$

A shown by Equation **(16)**, the drift tracking between V_{ref} and V_{bias} is determined by δ_{RDIV} and δ_{BUF} since δ_{REF} is common to both outputs.

$$\delta_{tracking} = \sqrt{\delta_{RDIV}{}^2 + \delta_{BUF}{}^2} \quad (16)$$

The drift and accuracy of the resistor divider network is determined by the drift and tolerance of one of the resistors. For a comparable low-drift solution, each resistor should have no more than 5 ppm/ºC drift and a tolerance of 0.1% or less. As of the publication of this document, the following resistor was selected as the most appropriate choice:

- PCF0603-13-4K99BT1
- Resistance: 4.99kΩ
- Tolerance: 0.1%
- Drift: 5 ppm/ºC
- Total Cost (1ku): $0.48 ($0.24 each)

The drift of the buffer amplifier's error contributions are not as significant as the reference or resistor divider because the full-scale range (FSR) is 1.5V. Targeting 0.1% error due to input offset voltage and 1 ppm/ºC drift error, the amplifier should have less than 1.5 mV offset voltage and 1.5 µV/ºC drift.

Table 9 lists op amps that should be considered for the discrete solution.

Table 9. Op Amps for Discrete Topology

Device	Vos (mV, max)	Vos Drift (µV/ºC, max)	Bandwidth (MHz)	Iq (mA, max)	Cost (1ku)
OPA377	1.0	2	5.5	1.05	$0.40
OPA336NA	0.5	1.5 (typ)	0.1	.032	$0.65
LMV831	1.0	1.5	3.3	0.27	$0.40

The LMV831 is the amplifier of choice due to performance, power, and cost. Note that if the LMV831 is supplied by V_{REF}, there will be no additional error due to CMRR.

Table 10 compares the discrete topology (LMV831, REF5030A, and PCF0603-13-4K99RBT1) with the REF2030 over temperature. The error calculations for the discrete solution can be found in Appendix C.

Table 10. Comparison of REF2030 and Discrete Topologies

Device(s)	Output	Accuracy (ppm)	Drift (ppm)	Total (ppm, RSS)	Tracking (ppm/°C, max)	Matching (ppm, 25°C)	Cost (1ku)
REF2030	3.0V, 1.5V	500	495	704	7	100	$1.40
LMV831 REF5030A R_{shunt}	V_{ref} (3.0V)	1000	495	1116	5	1014 (FSR, RSS)	$2.23
	V_{bias} (1.5V)	1424 (FSR,RSS)	704 (FSR,RSS)	1941 (FSR)			

While the performance of V_{ref} in the discrete topology is close to the REF2030, the V_{bias} output has considerably more error. Note that the total error for V_{bias} includes the error from V_{ref}. While the tracking of the two outputs is slightly better for the discrete topology, the matching of the outputs is dominated by the resistor divider accuracy and offset voltage of the buffer amplifier.

For approximately triple the cost the accuracy of the discrete topology could be increased by selecting 0.01% resistors. This would reduce the V_{bias} accuracy error to 1019 ppm, the V_{bias} total error to 1667 ppm, and the matching error to 194 ppm.

Despite the additional cost and error, the discrete solution has great value when $V_{bias} \neq V_{ref}/2$. The resistor divider can be adjusted accordingly. However, this will introduce an error due to the CMRR of the device. The analysis will be similar to that of the PSRR error calculation.

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments' difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University's Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

Timothy Claycomb joined the Precision Linear Applications team in February 2014. Before joining the team, he was an intern in the summer of 2013. Timothy received his BSEE from Michigan State University.

9 Acknowledgements & References

The authors would like to thank Collin Wells and Art Kay for their technical contributions to this design.

Appendix A.

A.1 Electrical Schematic

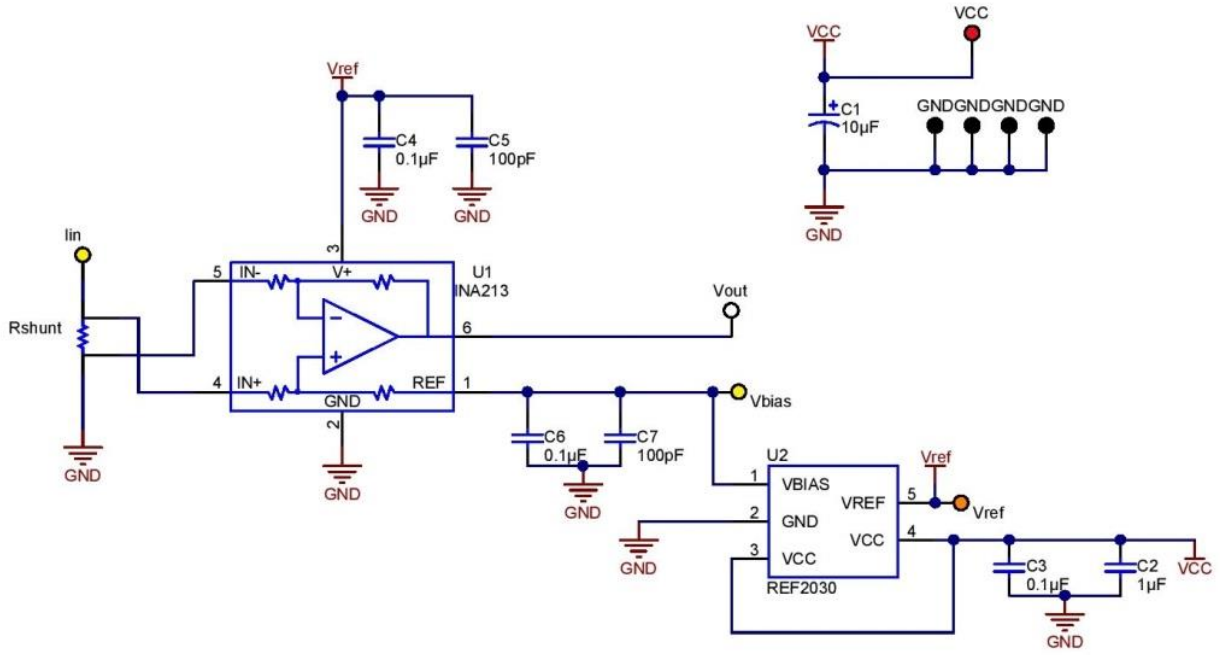


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item #	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Number	Supplier Part Number
1	1	C1	10uF	CAP, TA, 10uF, 25V, +/-10%, 0.5 ohm, SMD	AVX	TPSC106K025R0500	478-1762-1-ND
2	1	C2	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	TDK	C1608X7R1C105K080AC	445-1604-1-ND
3	3	C3, C4, C6	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	AVX	06033C104KAT2A	478-3714-1-ND
4	2	C5, C7	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A	478-1175-1-ND
5	1	Rshunt	10mohm	RES, 0.010 ohm, 0.1%, 1W, CSM2512	Vishay Foil Resistors	Y14870R01000B9W	Y1487-.01-ND
6	1	Vout	White	Test Point, Compact, White, TH	Keystone	5007	5007K-ND
7	1	VCC	Red	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
8	4	GND	Black	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
9	1	Vbias	Yellow	Test Point, Compact, Yellow, TH	Keystone	5009	5009K-ND
10	1	Vref	Orange	Test Point, Compact, Orange, TH	Keystone	5008	5008K-ND
11	1	lin	Yellow	Test Point, Compact, Yellow, TH	Keystone	5009	5009K-ND
12	1	U1		IC OPAMP CURR SENSE 14KHZ SC70-6	Texas Instruments	INA213BDCK	INA213BIDCKR-ND
13	1	U2		Dual output, low-drift reference	Texas Instruments	REF2030AIDDC	
14	4	N/A		STANDOFF HEX 4-40THR ALUM 1L"	Keystone	2205	2205K-ND
15	4	N/A		MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND
16	1	N/A		PCB FOR TI REF DESIGN TIPD156	American PCB Company	TIPD156	

Figure A-2: Bill of Materials

Appendix B.

B.1 MATHCAD Calculations

System Specifications

$R_{shunt} := 10 \cdot 10^{-3}\Omega$

$I_{load\_max} := 2.5A \qquad I_{load\_min} := -2.5A$

$V_{shunt\_max} := R_{shunt} I_{load\_max} = 25 \times 10^{-3} V$

$V_{shunt\_min} := R_{shunt} I_{load\_min} = -25 \times 10^{-3} V$

$FSR := V_{shunt\_max} - V_{shunt\_min} = 50 \times 10^{-3} V$

$T_{ambient} := 25C$

$T_{max} := 125C$

$\Delta T := T_{max} - T_{ambient} = 100 \times 10^{0} C$

Conversions

$dB(x) := \frac{1}{10^{\frac{x}{20}}} \frac{V}{V}$

$ppm := \frac{1}{1000000}$

Shunt Resistor Errors

Accuracy

$E_{shunt\_tol} := \alpha_{shunt\_tol} = 1 \times 10^{3} \cdot ppm$

Drift

$E_{shunt\_drift} := \Delta T \cdot \delta_{shunt\_drift} = 1.5 \times 10^{3} \cdot ppm$

Shunt Specifications

$\alpha_{shunt\_tol} := 0.1\%$

$\delta_{shunt\_drift} := 15 \frac{ppm}{C}$

INA213 Errors

INA Accuracy Specifications

$V_{os\_INA} := 5 \cdot \mu V$ $V_{s\_INA\_spec} := 5V$ $V_{s\_INA\_sys} := 3V$

$V_{os\_INA\_PSRR} := 0.1 \cdot \frac{\mu V}{V}$ $\alpha_{INA\_GE} := 0.02\%$

$V_{cm\_INA\_spec} := 12V$ $V_{cm\_sys} := 0V$ $V_{os\_INA\_CMRR} := dB(120) = 1 \times 10^{0} \cdot \frac{\mu V}{V}$

Accuracy

$$E_{INA\_Vos} := \frac{V_{os\_INA}}{FSR} = 100 \times 10^{0} \cdot ppm$$

$$E_{INA\_PSRR} := \frac{\left(V_{s\_INA\_spec} - V_{s\_INA\_sys}\right) \cdot V_{os\_INA\_PSRR}}{FSR} = 4 \times 10^{0} \cdot ppm$$

$$E_{INA\_GE} := \alpha_{INA\_GE} = 200 \times 10^{0} \cdot ppm$$

$$E_{INA\_CMRR} := \frac{\left(V_{cm\_INA\_spec} - V_{cm\_sys}\right) \cdot V_{os\_INA\_CMRR}}{FSR} = 240 \times 10^{0} \cdot ppm$$

Drift

$$E_{INA\_drift\_GE} := \Delta T \cdot \delta_{INA\_drift\_GE} = 300 \times 10^{0} \cdot ppm$$

$$E_{INA\_drift\_Vos} := \frac{V_{os\_INA\_drift}}{FSR} \cdot \Delta T = 200 \times 10^{0} \cdot ppm$$

INA Drift Specifications

$\delta_{INA\_drift\_GE} := 3 \frac{ppm}{C}$

$V_{os\_INA\_drift} := 0.1 \cdot \frac{\mu V}{C}$

REF2030 Errors

Accuracy

$E_{REF\_output} := \alpha_{REF\_output} = 500 \times 10^{0} \cdot ppm$

REF Accuracy Specifications

$\alpha_{REF\_output} := 0.05\%$

Drift

$E_{REF\_drift} := (165C) \cdot \delta_{REF\_drift\_output} = 495 \times 10^{0} \cdot ppm$

REF Drift Specifications

$\delta_{REF\_drift\_output} := 3 \frac{ppm}{C}$

System Error

Accuracy

$$E_{accuracy\_RSS} := \sqrt{\begin{pmatrix} E_{REF\_output}^{2} + E_{INA\_CMRR}^{2} \cdots \\ + E_{INA\_GE}^{2} + E_{INA\_PSRR}^{2} \cdots \\ + E_{INA\_Vos}^{2} + E_{shunt\_tol}^{2} \end{pmatrix}} = 1.165 \times 10^{3} \cdot ppm$$

$$E_{accuracy\_total} := E_{REF\_output} + E_{INA\_CMRR} + E_{INA\_GE} \cdots = 2.044 \times 10^{3} \cdot ppm$$
$$+ E_{INA\_PSRR} + E_{INA\_Vos} + E_{shunt\_tol}$$

Drift

$$E_{drift\_RSS} := \sqrt{\begin{matrix} E_{REF\_drift}^{2} + E_{INA\_drift\_Vos}^{2} \cdots \\ + E_{INA\_drift\_GE}^{2} + E_{shunt\_drift}^{2} \end{matrix}} = 1.62 \times 10^{3} \cdot ppm$$

$E_{drift\_total} := E_{REF\_drift} + E_{INA\_drift\_Vos} + E_{INA\_drift\_GE} + E_{shunt\_drift} = 2.495 \times 10^{3} \cdot ppm$

Total

$E_{total\_RSS} := \sqrt{E_{accuracy\_RSS}^{2} + E_{drift\_RSS}^{2}} = 1.996 \times 10^{3} \cdot ppm$

$E_{total} := E_{accuracy\_total} + E_{drift\_total} = 4.539 \times 10^{3} \cdot ppm$

Appendix C.

C.1 MATHCAD Calculations for Discrete Solution

System Specifications

$FSR := 1.5V$

$T_{ambient} := 25C \quad T_{max} := 125C$

$\Delta T := T_{max} - T_{ambient} = 100 \times 10^{0} C$

$V_{s\_buf} := 3.0V$

$V_{s\_spec} := 3.3V$

Conversions

$$dB(x) := \frac{1}{10^{\frac{x}{20}}} \frac{V}{V} \quad ppm := \frac{1}{1000000}$$

Resistor Divider Errors

Resistor Specifications

$\alpha_{res\_tol} := 0.1\%$

$\delta_{res\_drift} := 5 \frac{ppm}{C}$

Accuracy

$E_{res\_tol} := \alpha_{res\_tol} = 1 \times 10^{3} \cdot ppm$

Drift

$E_{res\_drift} := \Delta T \cdot \delta_{res\_drift} = 500 \times 10^{0} \cdot ppm$

Buffer Amplifier Errors

Buffer Specifications

$V_{os\_typ} := 0.25mV$

$V_{os\_PSRR} := dB(93) = 22.387 \times 10^{0} \cdot \frac{\mu V}{V}$

$V_{os\_drift} := 0.5 \cdot \frac{\mu V}{C}$

Accuracy

$$E_{buf\_Vos} := \frac{V_{os\_typ}}{FSR} = 166.667 \times 10^{0} \cdot ppm$$

$$E_{buf\_PSRR} := \frac{\left(V_{s\_spec} - V_{s\_buf}\right) \cdot V_{os\_PSRR}}{FSR} = 4.477 \times 10^{0} \cdot ppm$$

Drift

$$E_{buf\_drift\_Vos} := \frac{V_{os\_drift}}{FSR} \cdot \Delta T = 33.333 \times 10^{0} \cdot ppm$$

Reference Errors

Reference Specification

$\alpha_{REF\_output} := 0.1\%$

$\delta_{REF\_drift\_output} := 3\frac{ppm}{C}$

Accuracy

$E_{REF\_output} := \alpha_{REF\_output} = 1 \times 10^{3} \cdot ppm$

Drift

$E_{REF\_drift} := 165C \cdot \delta_{REF\_drift\_output} = 495 \times 10^{0} \cdot ppm$

Alternate System Error

Vref Accuracy

$E_{accuracy\_vref} := E_{REF\_output} = 1 \times 10^{3} \cdot ppm$

Vref Drift

$E_{drift\_vref} := E_{REF\_drift} = 495 \times 10^{0} \cdot ppm$

Vref Total

$E_{total\_vref\_RSS} := \sqrt{E_{accuracy\_vref}^{2} + E_{drift\_vref}^{2}} = 1.116 \times 10^{3} \cdot ppm$

$E_{total\_vref} := E_{accuracy\_vref} + E_{drift\_vref} = 1.495 \times 10^{3} \cdot ppm$

Vbias Accuracy

$$E_{accuracy\_vbias\_RSS} := \sqrt{E_{res\_tol}^2 + E_{buf\_Vos}^2 + E_{buf\_PSRR}^2 + E_{REF\_output}^2} = 1.424 \times 10^3 \cdot ppm$$

$$E_{accuracy\_vbias\_total} := E_{res\_tol} + E_{buf\_Vos} + E_{buf\_PSRR} + E_{REF\_output} = 2.171 \times 10^3 \cdot ppm$$

Vbias Drift

$$E_{drift\_vbias\_RSS} := \sqrt{E_{res\_drift}^2 + E_{buf\_drift\_Vos}^2 + E_{REF\_drift}^2} = 704.369 \times 10^0 \cdot ppm$$

$$E_{drift\_vbias\_total} := E_{res\_drift} + E_{buf\_drift\_Vos} + E_{REF\_drift} = 1.028 \times 10^3 \cdot ppm$$

Vbias Total

$$E_{total\_vbias\_RSS} := \sqrt{E_{total\_vref\_RSS}^2 \cdots + E_{accuracy\_vbias\_RSS}^2 + E_{drift\_vbias\_RSS}^2} = 1.941 \times 10^3 \cdot ppm$$

$$E_{total\_vbias} := E_{accuracy\_vbias\_total} + E_{drift\_vbias\_total} = 3.199 \times 10^3 \cdot ppm$$

Matching

$$\alpha_{matching} := \sqrt{\alpha_{res\_tol}^2 + \left(\frac{V_{os\_max}}{FSR}\right)^2} = 1.014 \times 10^{-3}$$

$$\alpha_{matching} = 1.014 \times 10^3 \cdot ppm$$

Tracking

$$\delta_{tracking\_total} := \delta_{res\_drift} + \frac{V_{os\_drift}}{FSR} = 5.333 \times 10^0 \frac{1}{C} \cdot ppm$$

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265