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TI Designs – Precision: Verified Design

Low-Power Reference and Bipolar Voltage Conditioning Circuit Reference Design for Low-Power ADCs

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Circuit Description

This low-power reference and conditioning circuit attenuates and level-shifts a bipolar input voltage within the proper input range of a single-supply low-power 16-Bit ΔΣ ADC such as the one inside the MSP430 or other similar single-supply ADCs. Precision reference circuits are used to level-shift the input signal, provide the ADC reference voltage and to create a well-regulated supply voltage for the low-power analog circuitry. A low-power zero-drift op amp circuit is used to attenuate and level-shift the input signal.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
REF3330	Product Folder
REF3312	Product Folder
OPA317	Product Folder

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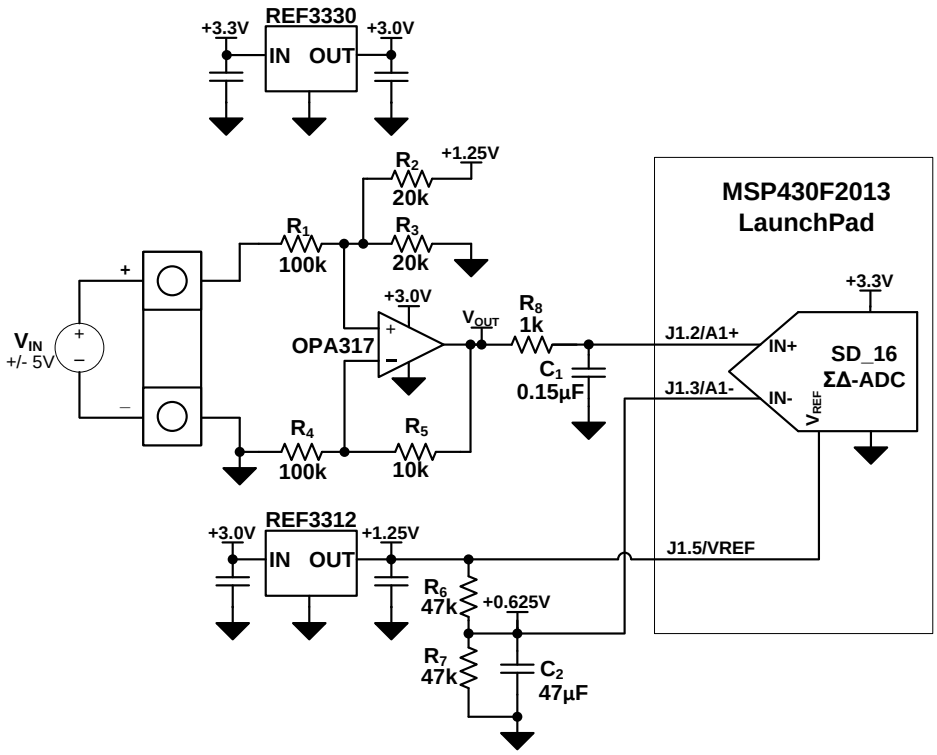

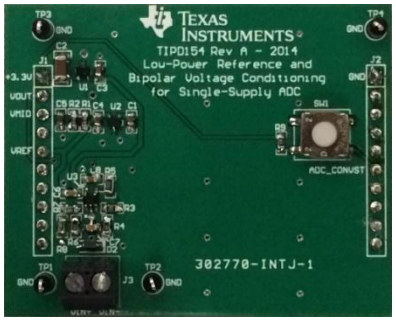

1 Design Summary

The design requirements are as follows:

- Supply Voltage: +3.3 V
- Maximum Input Voltage: +/- 6 V
- Specified Input Voltage: +/- 5 V
- ADC Reference Voltage: 1.25 V

The goal for this design is to accurately condition a ±5 V bipolar input voltage into a voltage suitable for conversion by a low-voltage ADC with a 1.25 V reference voltage, V_{REF}, and an input voltage range of $V_{REF}/2$. The circuit should function with reduced performance over a wider input range of at least ±6V to allow for easier protection of over-voltage conditions. The specific design goals and performance metrics are summarized in Table 1. Figure 1 depicts the measured transfer function and accuracy results.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance for ±5V Input

	Goal	Simulated	Measured
Calibrated Error (%FSR)	0.001	N/A	0.0005
Unadjusted Error (%FSR)	0.15	0.0439	0.0138
Operational Current Consumption (µA)	100	93.07	89.54
60 Hz Rejection (dB)	> 60	60	62

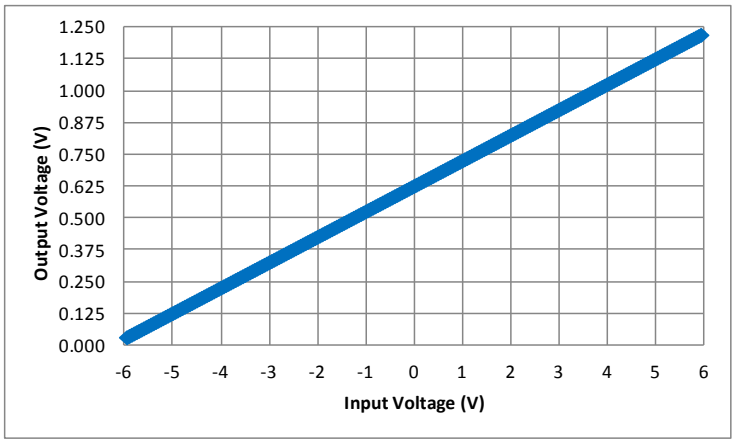

Figure 1: Measured Transfer Function Over the Full ±6V Input Range

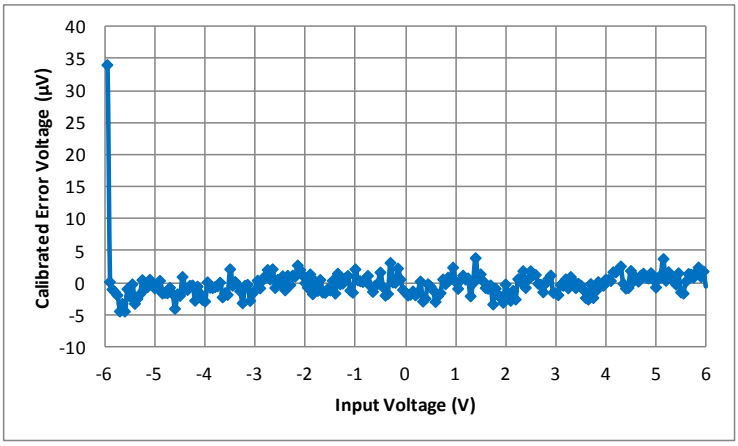

Figure 2: Calibrated Error Voltage

2 Theory of Operation

Figure 3 depicts a simplified schematic for this design showing the MSP430 ADC inputs and full input conditioning circuitry. The ADC is configured for a bipolar measurement where final conversion result will be the differential voltage, V_{DIFF}, between the voltage at the positive and negative ADC inputs, V_{A1+} and V_{A1-}. The bipolar, GND referenced input signal must be level-shifted and attenuated by the op amp such that the output is biased to $V_{REF}/2$ and has a differential voltage that is within the $\pm V_{REF}/2$ input range of the ADC. The transfer function for the op-amp circuit simplifies to Equation 1 if the conditions in Equations 2 and 3 are met. The full transfer function for the input circuitry is shown in Appendix B.1 for reference. The V_{A1-} voltage is based on the resistor divider formed by R_6 and R_7 and will be set to $V_{REF}/2$ by setting R_6 equal to R_7 as shown in Equation 4.

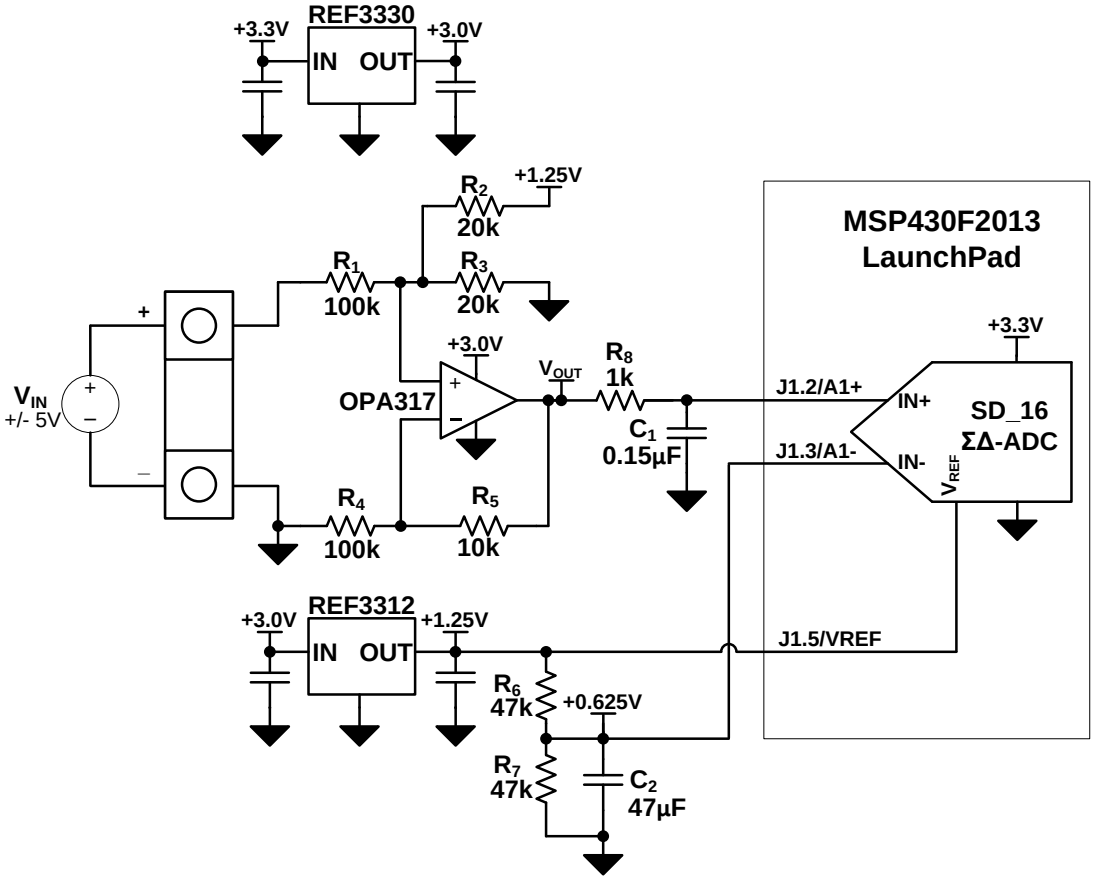

Figure 3: Simplified Circuit schematic

$$V_{A1+} = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} \quad (1)$$

Given

$$R_4 = R_1 \quad (2)$$

and

$$R_5 = R_2 \parallel R_3 \quad (3)$$

$$V_{A1-} = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{V_{REF}}{2} \quad (4)$$

2.1 Op Amp Level-Shift Design

The ratio of R_2, R_3, and the V_{REF} voltage will determine the voltage on the output of the op amp when the differential input is 0 V. The components will be selected such that V_{OUT} is equal to $V_{REF}/2$ voltage when V_{IN} is equal to 0 V as shown in Equations 5 – 7.

$$V_{A1+} = \frac{V_{REF}}{2} = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} \tag{5}$$

Given

$$Vin = 0\,V \tag{6}$$

and

$$R_2 = R_3 \tag{7}$$

The value of R_5 can be solved for by setting R_3 equal to R_2 in Equation 3 as shown in Equation 8.

$$R_5 = \left(\frac{R_2 * R_2}{R_2 + R_2}\right) = \frac{R_2^2}{2 * R_2} = \frac{R_2}{2} \tag{8}$$

2.2 Differential Input Attenuator Design

V_{DIFF} is the difference between the two inputs as shown in Equation 9.

$$V_{DIFF} = (V_{A1+}) - (V_{A1-}) = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} - \frac{V_{REF}}{2} \tag{9}$$

When the ratio of R3 and R2 equals the ratio of R7 and R6, Equation 9 simplifies to Equation 11.

If

$$\left(\frac{R_3}{R_2 + R_3}\right)V_{REF} = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{1}{2}V_{REF} \tag{10}$$

then

$$V_{DIFF} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} \tag{11}$$

The ratio of R_1, R_2, and R_3 can be determined by setting V_{A1+} equal to the maximum V_{DIFF} voltage for a full-scale positive and/or negative input voltage V_{IN_MAX} as shown in Equation 12.

$$V_{A1+} = V_{DIFF\_MAX} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN\_MAX} \tag{12}$$

Since R_2 equals R_3, Equation 12 simplifies to $R_2/2$ resulting in Equation 13.

$$V_{DIFF\_MAX} = \left(\frac{R_2}{2 * R_1}\right)V_{IN\_MAX} \tag{13}$$

2.3 Input Filtering

Both inputs feature first-order low-pass anti-aliasing filters that limit the bandwidth and noise of the input signals applied to the ADC. The A1+ filter is formed by R_8 and C_1 and the equation for the -3dB cutoff frequency is shown in Equation 14.

$$f_{-3dB\_A1+} = \frac{1}{2 * \pi * R_8 * C_1} \tag{14}$$

The A1- input filter is formed by C_2 and the parallel combination of the R_6 and R_7 resistors as shown in Equation 15.

$$f_{-3dB\_A1-} = \frac{1}{2 * \pi * \left(\frac{R_6}{2}\right) * C_2} \quad (15)$$

3 Component Selection

3.1 Voltage References

The REF33xx series of precision low-power voltage references was selected for this design to pair well with the low power consumption of the MSP430 while achieving the target accuracy goals. The 16-bit converter in the MSP430F2013 accepts an external reference voltage from 1 V to 1.5 V with a typical reference input of 1.25 V as shown in Figure 4.

SD16_A, External Reference Input (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

Figure 4: MSP430F2013 SD16_A External Voltage Reference Specifications

The REF3312 was selected to provide the desired 1.25 V reference voltage for the MSP430 ADC. The accuracy of the REF3312 output, shown in Figure 5, will directly affect the accuracy of the entire system and needs to be less than the desired unadjusted error goals. The REF3312 maximum ±0.15% initial accuracy specification is equal to the unadjusted error design goal of 0.15% indicating that most of the error budget in this design needs to be devoted to the reference accuracy.

PARAMETER		CONDITIONS	REF33xx MIN	REF33xx TYP	REF33xx MAX	UNITS
REF3312 (1.25V)						
OUTPUT VOLTAGE						
Initial Accuracy	V_{OUT}	V_{IN} = 5V		1.25		V
			–0.15		+0.15	%
NOISE						
Output Voltage Noise		f = 0.1Hz to 10Hz		35		μV_{PP}

Figure 5: REF3312 Output Accuracy Specifications

The +3.3 V system supply voltage that powers the MSP430 may also supply other devices and therefore may have regulation and noise issues. The REF3330 was selected to create an accurate and stable +3.0 V output that was used by the op amp, REF3312, and other low-power analog circuitry. The REF33xx series has a drop-output voltage of V_{OUT}+200 mV so as long as the input supply remains above +3.2 V the REF3330 will produce a regulated +3.0 V output. The output current for the REF33xx series is specified at +/-5 mA as shown in Figure 6 which is sufficient for REF3312 and a low-power op amp.

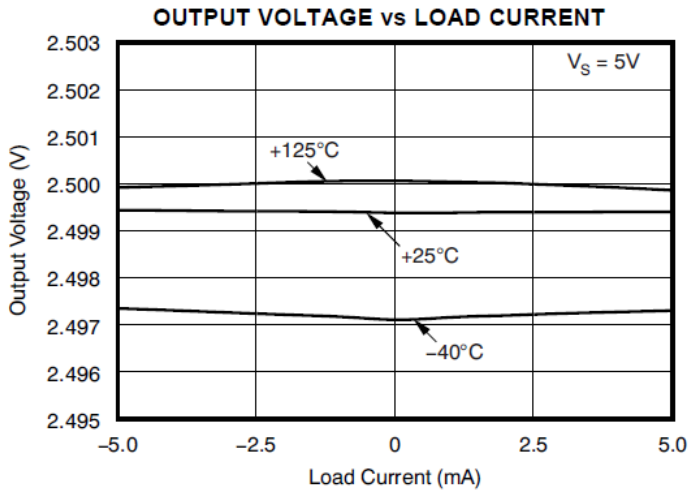

Figure 6: REF33xx Output Voltage vs. Load Current

3.2 Op Amp

The OPA317 was selected because of the low offset voltage, low offset voltage drift, CMRR, and low power consumption. The important dc specifications for the OPA317 can be seen in Figure 7. The maximum offset of 100 µV will account for only 0.001% of the full-scale signal and the low-drift will reduce temperature drift effects. Therefore, as previously mentioned, most of the error in this design will be from the reference accuracy and passive component tolerances.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V

At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA317, OPA2317, OPA4317 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = +5 V		20	±90	µV
		T_A = –40°C to +125°C, V_S = +5 V			±100	µV
dV_{OS}/dT	vs temperature	T_A = –40°C to +125°C		0.05		µV/°C
PSRR	vs power supply	T_A = –40°C to +125°C, V_S = +1.8 V to +5.5 V		1	10	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	95	108		dB
		OPA4317, T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	95	108		dB
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	T_A = –40°C to +125°C, I_O = 0		21	35	µA
	Turn-on time	V_S = +5 V		100		µs

Figure 7: OPA317 dc Specifications

3.3 Input Attenuation and Level Shifting

For this design, the bipolar ±5 V input must be attenuated and level shifted so the differential voltage is within the input range of ±V_{REF}/2, or ±0.625 V. The accuracy of the op amp output and ADC input may degrade near the supply rails and V_{REF} voltage so the output will be designed to produce a 0.125 V to 1.125 V output, or ±0.5 V for a ±5 V input. Scaling the output this way also increases the allowable input range to ±6 V and allows for some under/over-scale voltage measurement and protection.

Equation 13 can be solved to scale the ±5 V input to a ±0.5 V a differential voltage as shown in Equations 16 - 18. R_1 and R_4 will dominate the input impedance for this design and were therefore selected to be 100 kΩ. Higher values can be selected to increase the input impedance at the expense of input noise.

$$R_1 = R_4 = 100 \quad k\Omega \tag{16}$$

$$0.5 \ V = \left(\frac{R_2}{2 * 100 \quad k\Omega} \right) * 5 \ V \tag{17}$$

$$R_2 = R_3 = 20 \quad k\Omega \tag{18}$$

With the value for R_2 and R_3 selected, the value for R_5 can be calculated as shown in Equation 19.

$$R_5 = \frac{R_2}{2} = 10 \quad k\Omega \tag{19}$$

In order for V_{A1-} to equal to $V_{REF}/2$, R_6 needs to equal R_7. The two resistors will be selected to be 47 kΩ to conserve power without creating an impedance too weak to drive the ADC input.

$$R_6 = R_7 = 47 \quad k\Omega \tag{20}$$

3.4 Input Filtering

The MSP430 ADC was configured to run from the 1.1 MHz SMCLK with an over-sampling rate (OSR) of 256 yielding a sample rate of roughly 4.3 kHz. The input filter cutoff frequency was set to 1 kHz to limit the input signal bandwidth as shown in Equation 21 and 22. R_8 was selected to be 1 kΩ to provide isolation from the capacitive load of the low-pass filter thereby reducing stability concerns.

$$f_{-3dB\_A1+} = 1kHz = \frac{1}{2 * \pi * R_8 * C_1} \tag{21}$$

$$C_1 = \frac{1}{2 * \pi * 1k\Omega * 1kHz} = 159 \quad nF \tag{22}$$

C_1 was reduced to 150nF so it could be a standard value.

The A1- input of the ΔΣ converter is not buffered and therefore requires a large capacitor to supply the charge for the internal sampling capacitor. A 47 µF capacitor was selected resulting in the cutoff frequency shown in Equation 23. Applications that can't tolerate such a low frequency cutoff, and therefore long start-up time, should buffer the A1- input with another OPA317 to properly drive the ADC input with a lower input capacitor.

$$f_{-3dB\_A1-} = \frac{1}{2 * \pi * \left(\frac{R_6}{2} \right) * C_2} = 0.144 \quad Hz \tag{23}$$

3.5 Passive Component Tolerances and Materials

Resistors R_1, R_2, R_3, R_4, R_5, R_6, and R_7 directly affect the accuracy of the circuit. To meet the unadjusted accuracy goals of 0.2%, the resistors were chosen to be 0.1%. As described in Reference 1, selecting 0.1% resistors for the construction of the difference amplifier circuit should provide a common-mode rejection (CMRR) of at least 60 dB.

Signal path capacitors should be C0G/NP0 dielectric material to minimize the signal distortion as well as prevent piezo-electric effects that are present with other ceramic capacitor dielectrics.

4 Simulation

The TINA-TI™ simulation circuit for this design can be seen in Figure 8. The dc transfer function results with the component values selected in Section 3 are shown in Figure 9.

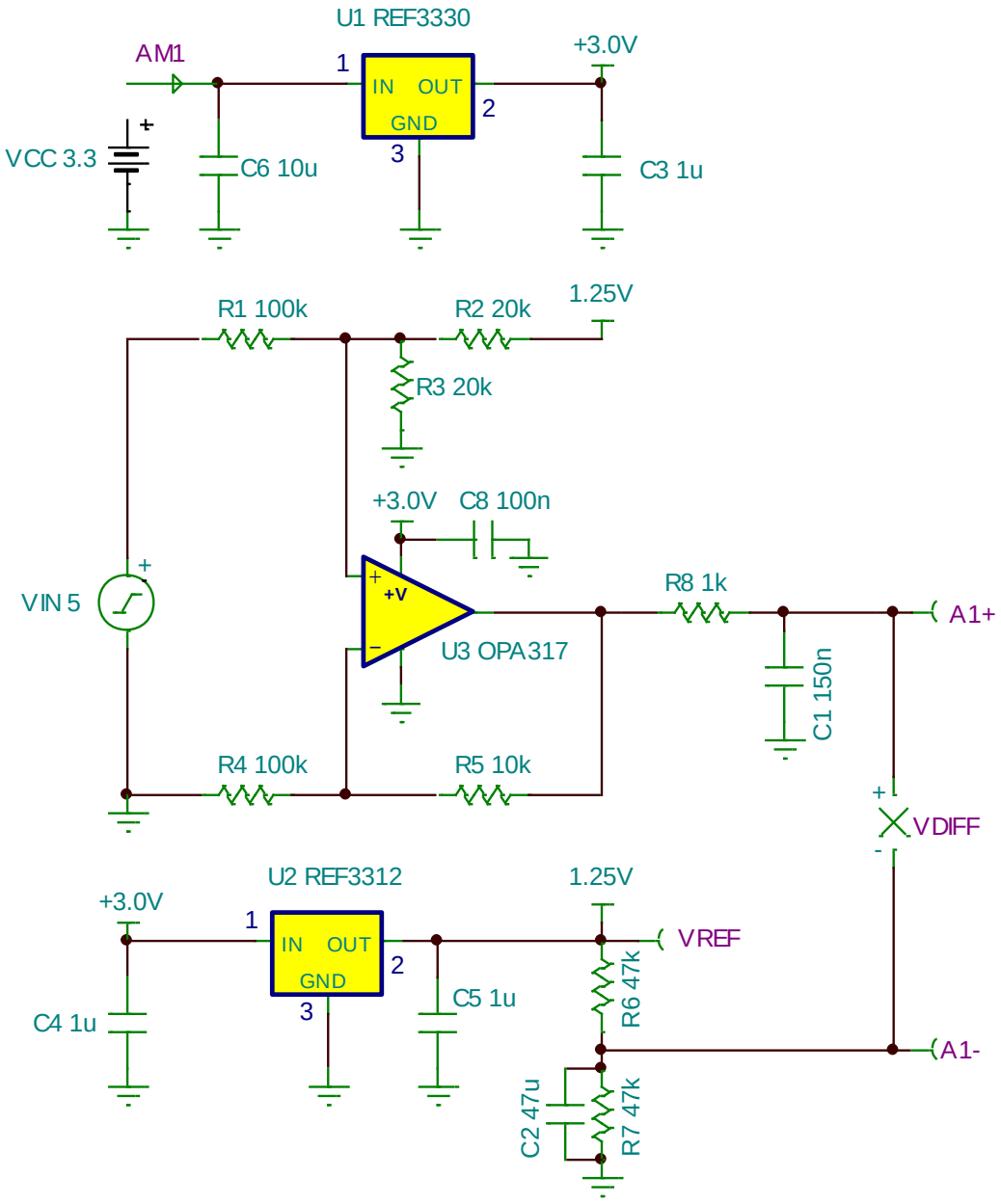

Figure 8: TINA-TI™ – Circuit Schematic

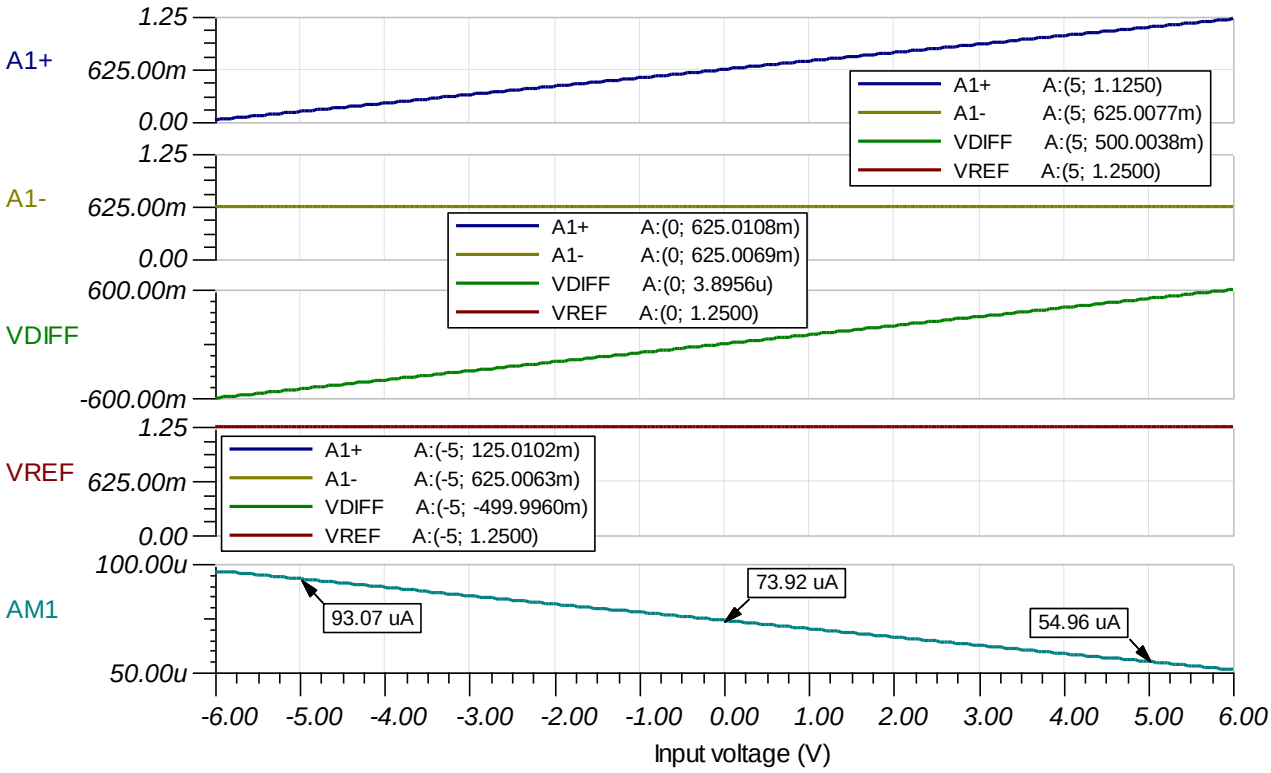

Figure 9: DC Transfer Function Results

A more accurate representation of the circuit results can be obtained by performing a Monte-Carlo analysis on the circuit with the correct component tolerances. Figure 10 displays the histogram for the results with a +5V input and the other results can be found in Appendix B. Table 2 contains the results obtained by creating a histogram of the Monte-Carlo output voltage results obtained from a -5 V, 0 V, and +5 V input.

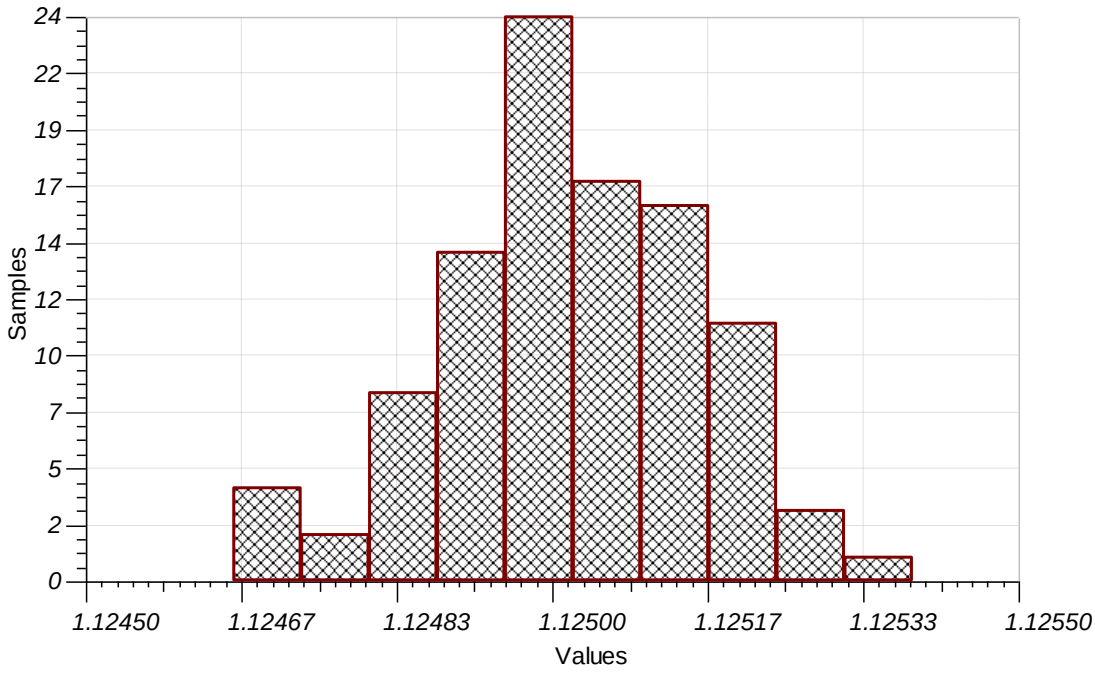

Figure 10: Circuit Output Variation with a Full-Scale +5 V dc Input

Table 2. Histogram Results of the Monte-Carlo Data

		Input Voltage (V)		
Statistic	**Units**	**-5**	**0**	**+5**
Mean Value	**mV**	125.0224	625.0206	1125.0190
Standard Deviation	**µV**	134.6068	82.5096	140.0637
Nominal Value	**mV**	125.0104	625.0111	1125.0124

Using the mean (µ) and standard deviation (σ) from the Monte-Carlo simulation to represent the final production circuit results, a six sigma (-3σ to 3σ) or 99.7% prediction of full-scale error (%FSR) is calculated using Equation 24.

$$\text{Percent Error (\%FSR)} = \frac{(\mu \pm 3\sigma) - V_{OUT\_EXPECTED}}{V_{OUT\_FULL-SCALE}} \times 100 \quad (24)$$

The maximum simulated error at the positive full-scale input of +5 V is ±0.0439% as shown in Equation 25. The maximum simulated error at the negative full-scale input of -5V is ±0.0426%.

$$\text{Percent Error (\%FSR)} = \frac{(1125.0190 \pm (3 * 0.1400637)) - 1125}{1000} \times 100 = 0.0439\ \% \quad (25)$$

Performing a Monte-Carlo ac transfer simulation with the input terminals shorted together provides an accurate representation of the CMRR performance of the circuit. As shown in Figure 11, the low frequency results are dominated by the matching of the 0.1% passive components. The curves in Figure 11 have been adjusted for the gain of the circuit and show at least 60dB of CMRR for signal frequencies up to 5 kHz.

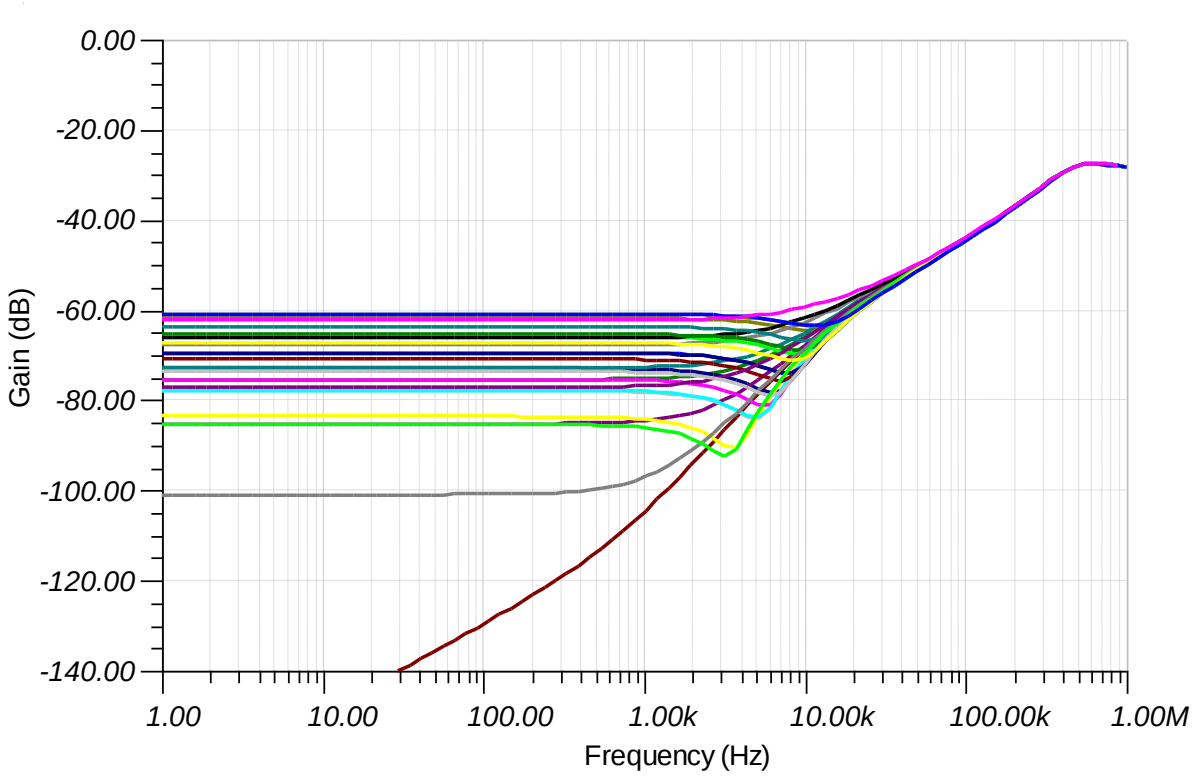

Figure 11: Circuit CMRR Variation over Frequency from Resistor Tolerance

4.1 Simulated Results Summary

The simulated performance is compared to the performance goals set in Section 0 in Table 3.

Table 3: Simulated Performance Result Summary

	Goal	Simulated
Calibrated Error (%FSR)	0.001	N/A
Unadjusted Error (%FSR)	0.15	0.0439
Operational Current Consumption (µA)	100	93.07
60 Hz Rejection (dB)	> 60	60

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. The size of the PCB and connectors were selected to connect directly to the MSP430 LaunchPad.

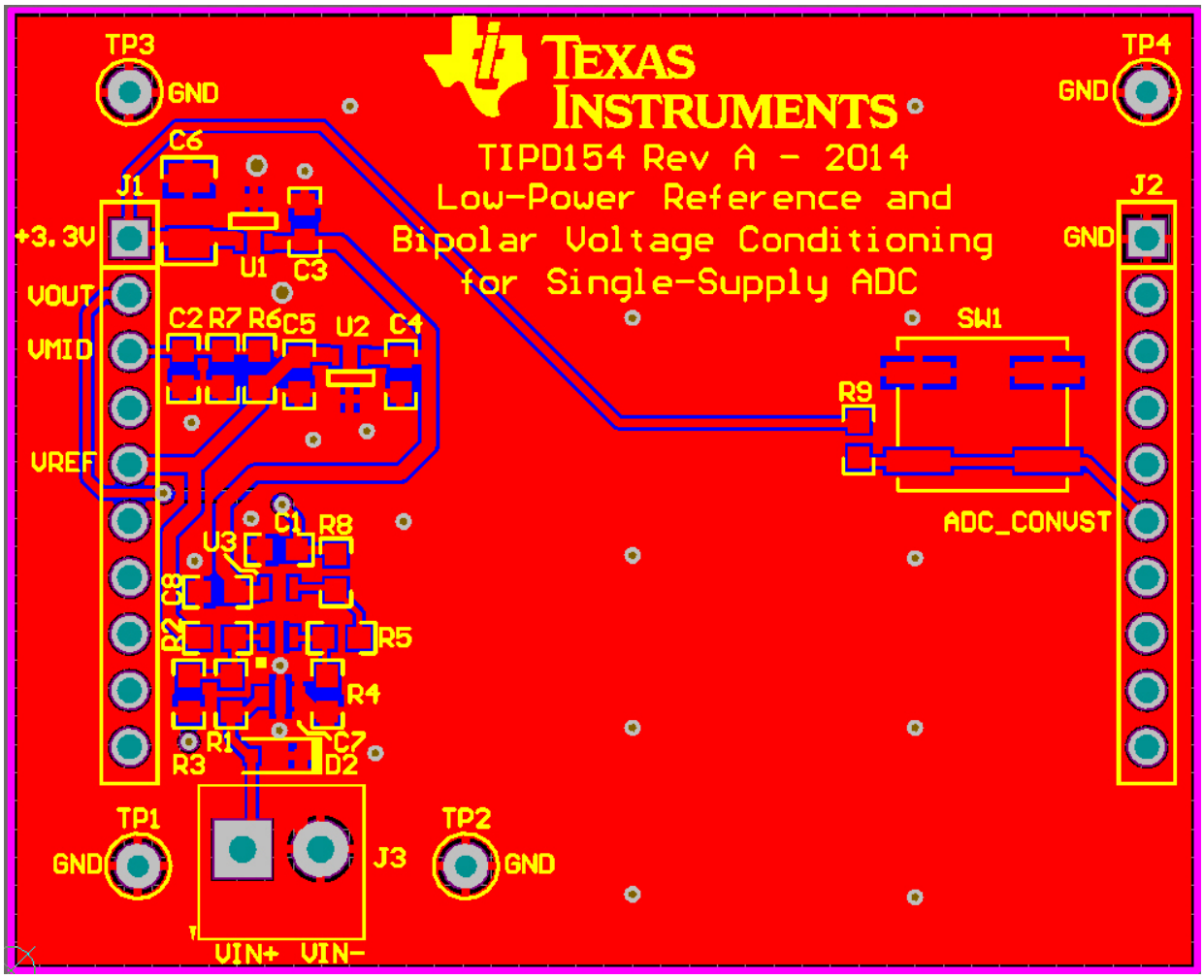

Figure 12: Altium PCB Layout

6 Verification & Measured Performance

This section focuses only on the performance of the reference and input circuitry. It does not take the MSP430 ADC performance into consideration. Complete data with the MPS430F2013 ADC can be found in Appendix B.3.

6.1 DC Performance

The measured dc performance and calculated error of the circuit can be seen in Figure 13 and Figure 14 respectively. By applying a 2-point gain and offset calibration over the specified ±5V input range the calibrated error can be seen in Figure 15. The uncalibrated results show errors of 138 µV or 0.0138 %FSR. The calibrated results with a simple 2-point calibration show errors under 5µV or 0.0005 %FSR in the specified input range of ±5 V. Methods for 2-point calibration are explained in Reference 2.

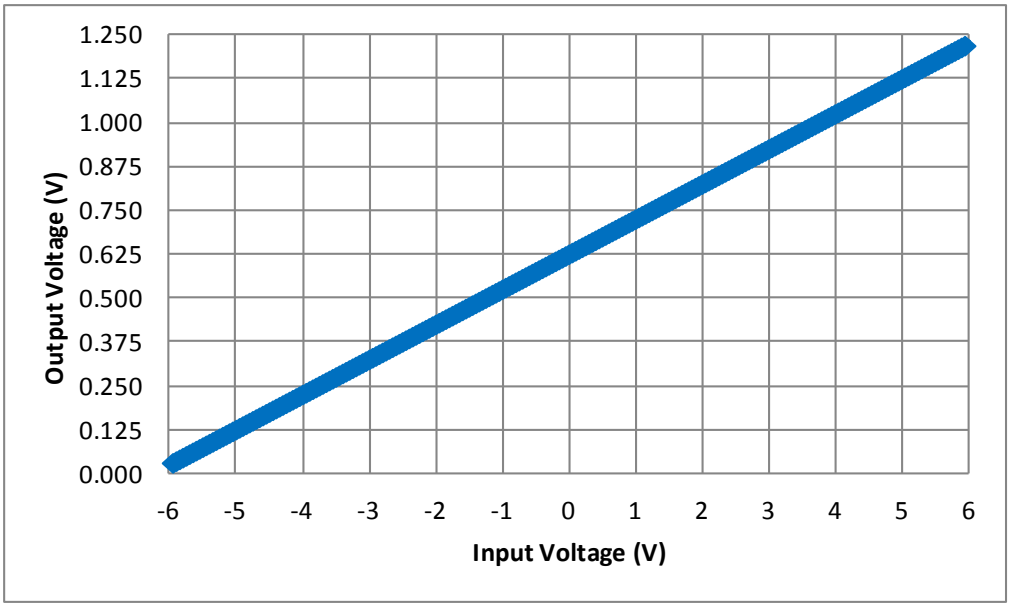

Figure 13. Measured DC Transfer Function with ±6V Input

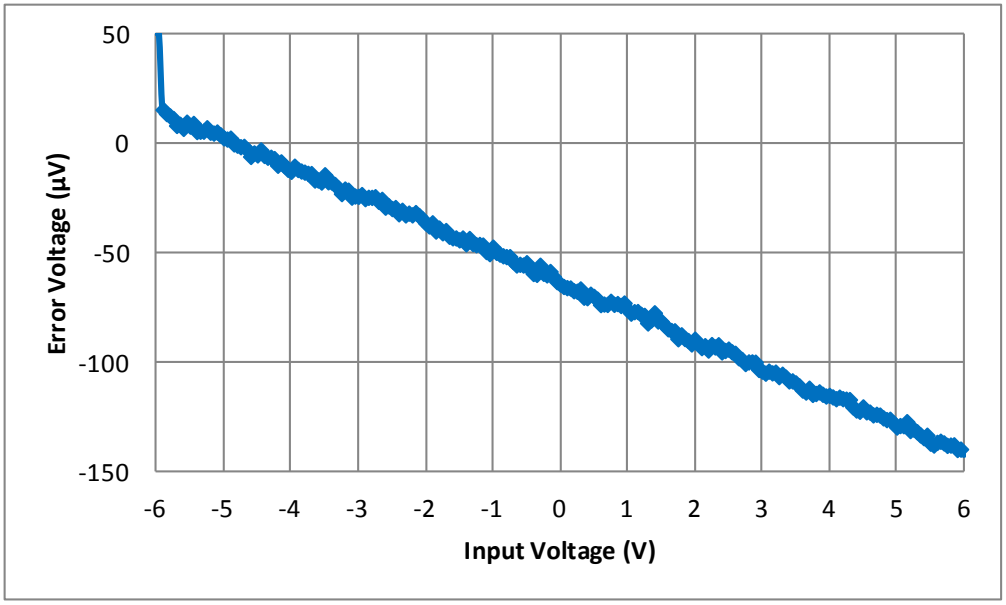

Figure 14. Measured Output Error with ±6V Input

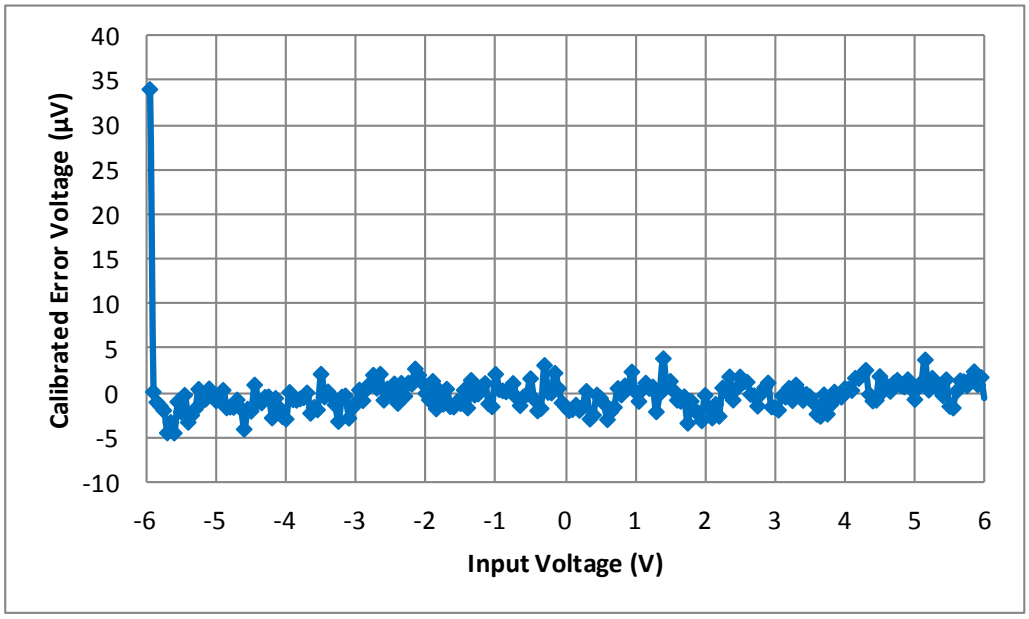

Figure 15. Calibrated Output Error with ±6V Input

6.2 AC Performance

The AC transfer function for the attenuation and level-shifting circuit can be seen in Figure 16.

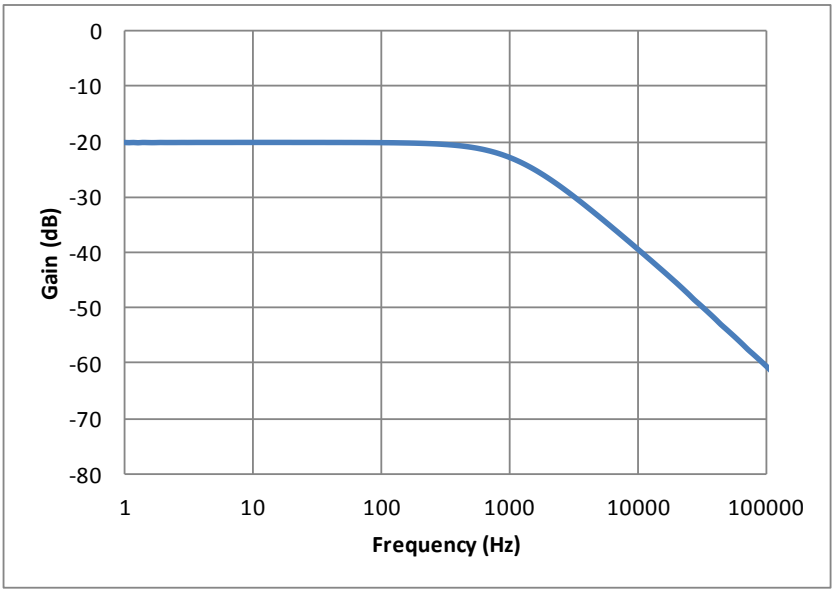

Figure 16. Measured ac Transfer Function

The low-frequency ac CMRR performance was measured to be 62 dB as shown in Figure 17.

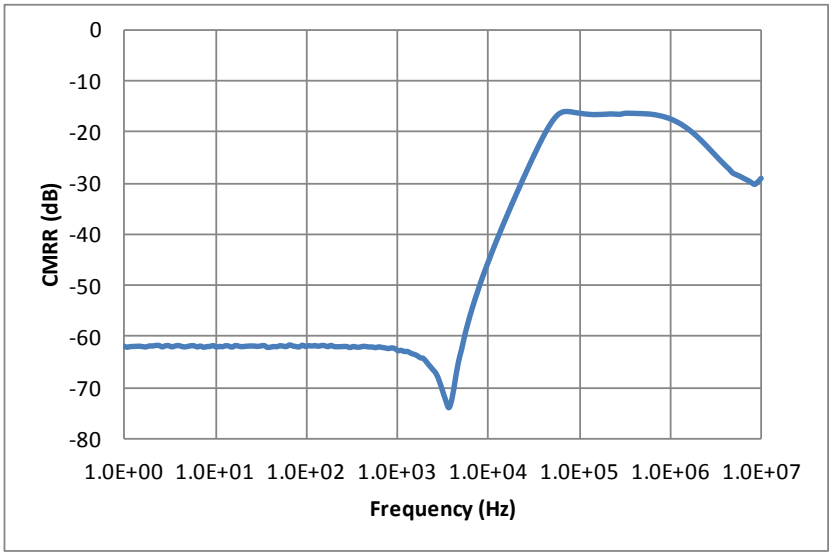

Figure 17. Measured ac CMRR Results

6.3 Measured Results Summary

Table 4. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Calibrated Error (%FSR)	0.001	N/A	0.0005
Unadjusted Error (%FSR)	0.15	0.0439	0.0138
Operational Current Consumption (µA)	100	93.07	89.54
60 Hz Rejection (dB)	> 60	60	62

7 Modifications

The gain and reference levels of this circuit can be adjusted using the equations in Section 2. Table 5 lists other low-power amplifiers with different performance specifications that may have advantages in other circuits. Other similar ΔΣ ADCs may require a buffer for the V_{A1-} for proper conversion results. Higher sampling rate ΔΣ ADCs and SAR ADC topologies will likely require higher bandwidth amplifiers to properly drive the inputs.

Table 5. Alternate Low-Power Op Amps

Op Amp	Supply Voltage (V)	Quiescent Current Typ/Max (µA)	Vos Typ/Max (µV)	Vos Drift (µV/°C)	CMRR Typ/Max (dB)	Gain-Bandwidth (kHz)
OPA317	1.8 – 5.5	21 / 35	20 / 100	0.05	95 / 108	300
OPA330	1.8 – 5.5	21 / 35	8 / 50	0.02	100 / 115	350
OPA333	1.8 – 5.5	17 / 25	2 / 10	0.02	106 / 130	350
OPA369	1.8 – 5.5	0.8 / 1.2	250 / 750	0.4	90 / 100	12
OPA379	1.8 – 5.5	2.9 / 5.5	400 / 1500	0.4	62 / 100	90
LPV511	2.7 - 12	0.88 / 1.2	200 / 3000	0.3	77 / 100	27

8 About the Author

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

Janet Sun is an analog field application engineer in Beijing, China supporting industrial and other performance analog customers. She completed work on this system as well as several others during a 6-month rotation working with the precision amplifier team in Dallas.

9 Acknowledgements & References

1. *Pete Semig, Common-Mode Rejection, Presentation 2012.*
2. *Mock, Mike, 0-1A, Single-Supply, Low-Side, Current Sensing Solution, TIDU040*

Appendix A.

A.1 Electrical Schematic

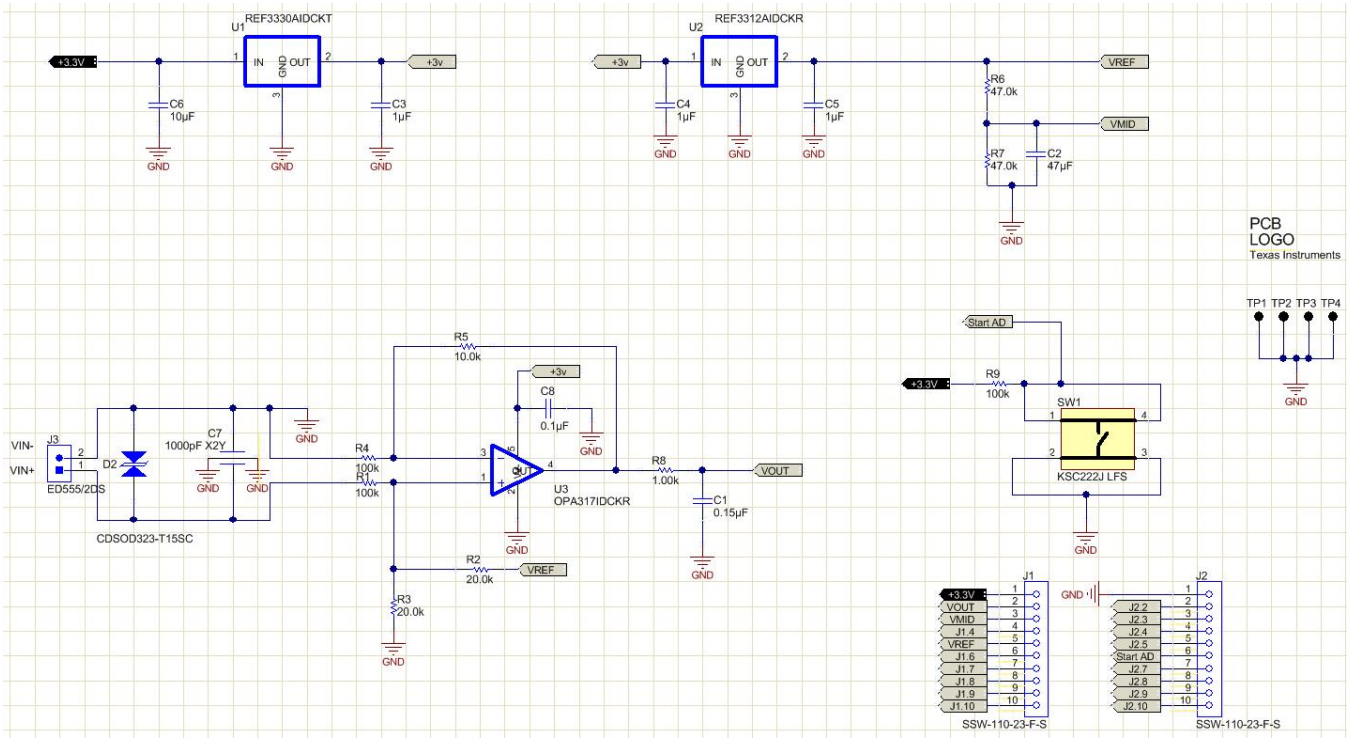

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI Designs Precision - TIPD154 - Low-Power Reference and Bi-Polar Voltage Conditioning for 16-Bit ADC

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	1	C1	0.15uF	CAP, CERM, 0.15uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C154KA01D
2	1	C2	47uF	CAP, CERM, 47uF, 6.3V, +/-20%, X5R, 0603	MuRata	GRM188R60J476M
3	3	C3, C4, C5	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	TDK	C1608X7R1C105K
4	1	C6	10uF	CAP, CERM, 10uF, 16V, +/-20%, X7R, 1206	TDK	C3216X7R1C106M
5	1	C7	1000pF	CAP CER 1000PF 50V 20% X7R 0603	Johanson Dielectrics Inc	500X14W102MV4T
6	1	C8	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H104KA93D
7	1	D1		DIODE TVS ARRAY 15V SOD323	Bourns	CDSOD323-T15SC
8	2	J1, J2		CONN HEADER 10POS SOCKET 2.54MM	Wurth Electronics	61301011821
9	1	J3		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
10	5	R1,R4, R9	100k	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
11	2	R2, R3	20.0k	RES, 20.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-203-B-T5
12	1	R5	10.0k	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-103-B-T5
13	1	R6, R7	47.0k	RES, 47.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-473-B-T5
14	1	R8	1.00k	RES, 1.00k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD071KL
15	1	SW1		SWITCH TACTILE SPST-NO 0.05A 32V	C&K Components	KSC222J LFS
16	4	TP1, TP2, TP3, TP4		Test Point, Miniature, Black, TH	Keystone	5001
17	1	U1		IC, 30 ppm/°C, 3.9 µA 3.0V-Voltage Reference	Texas Instruments	REF3330AIDCKT
18	1	U2		IC, 30 ppm/°C, 3.9 µA 1.25V-Voltage Reference	Texas Instruments	REF3312AIDCKR
19	1	U3		IC OPAMP GP 300KHZ RRO SC70-5	Texas Instruments	OPA317IDCKR

Figure A-2: Bill of Materials

Appendix B.

B.1 Complete Transfer Function

The complete transfer function for the circuit topology featured in this design is shown in the equation below:

$$V_{OUT} = \left(\frac{R_2 * R_5 * R_3 + R_1 * R_5 * R_3}{R_3 * R_4 * R_1 + R_5 * R_4 * R_1 + R_5 * R_3 * R_1} \right) V_{REF} + \left(\frac{R_2 * R_5 * R_4 + R_1 * R_5 * R_4}{R_3 * R_4 * R_1 + R_5 * R_4 * R_1 + R_5 * R_3 * R_1} \right) V_{IN}$$

B.2 Simulated Monte-Carlo Results

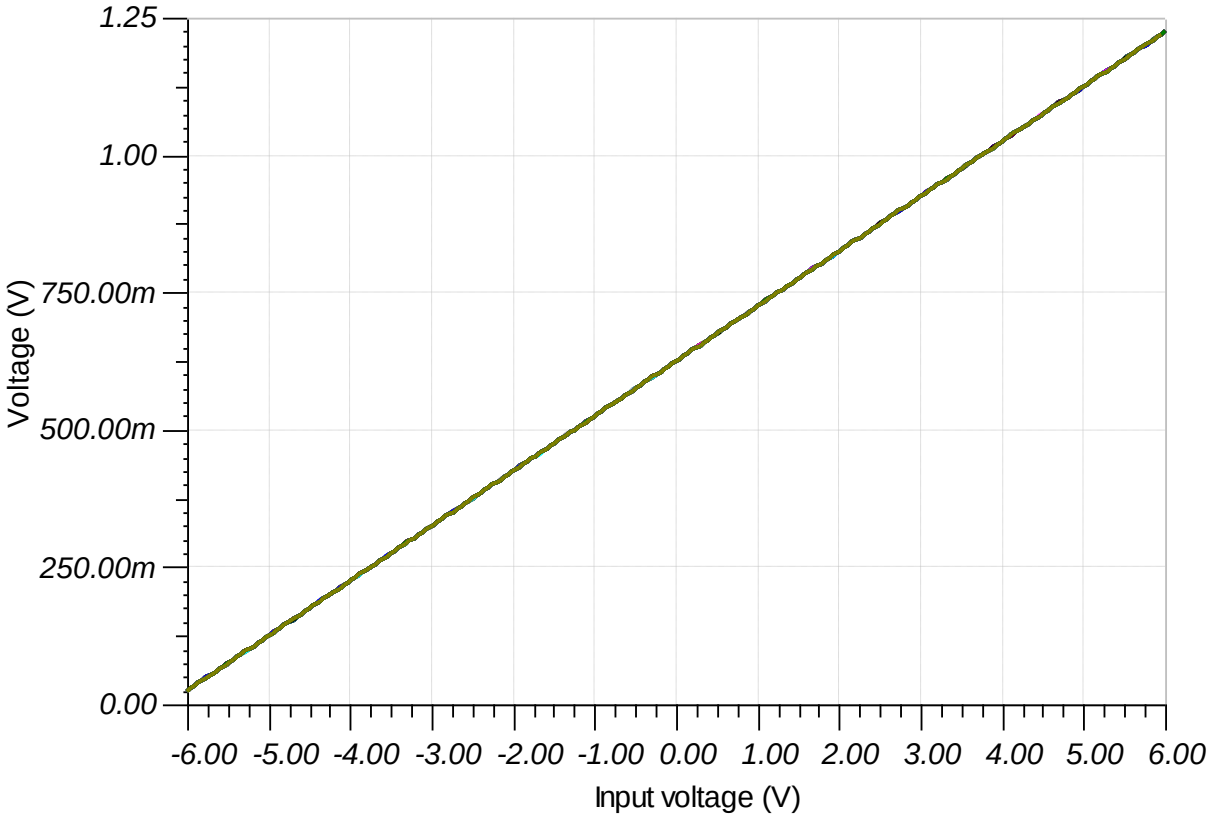

Figure 18: Histogram Transfer Function Results

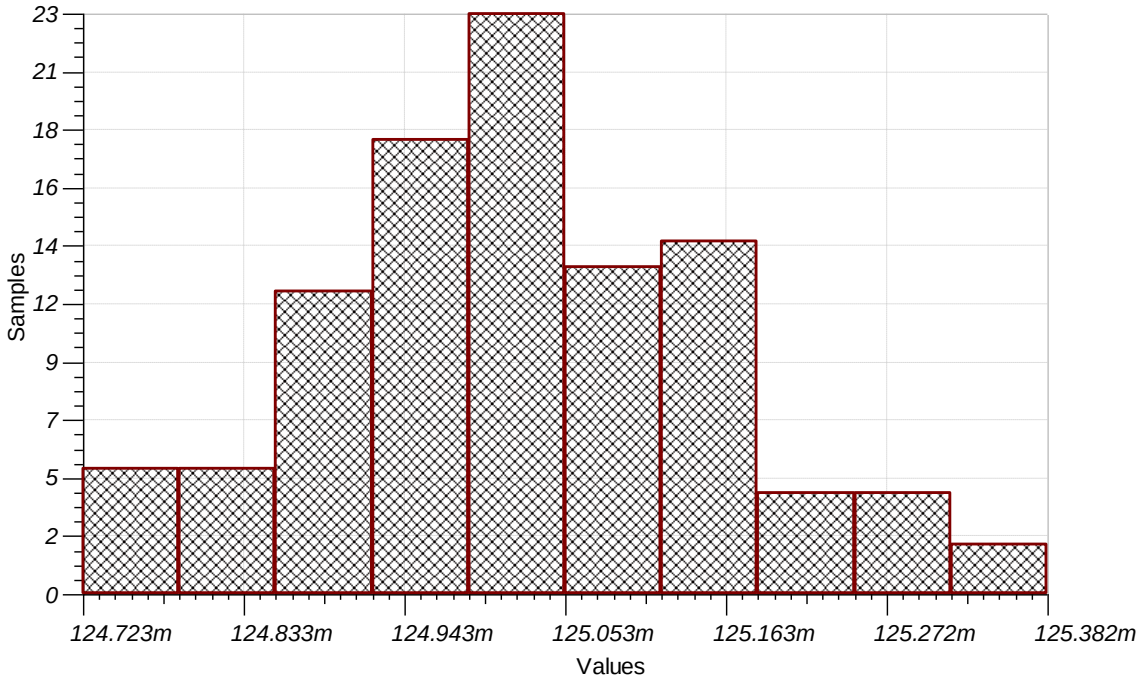

Figure 19: Circuit Output Variation with a Negative Full-Scale +5 V dc Input

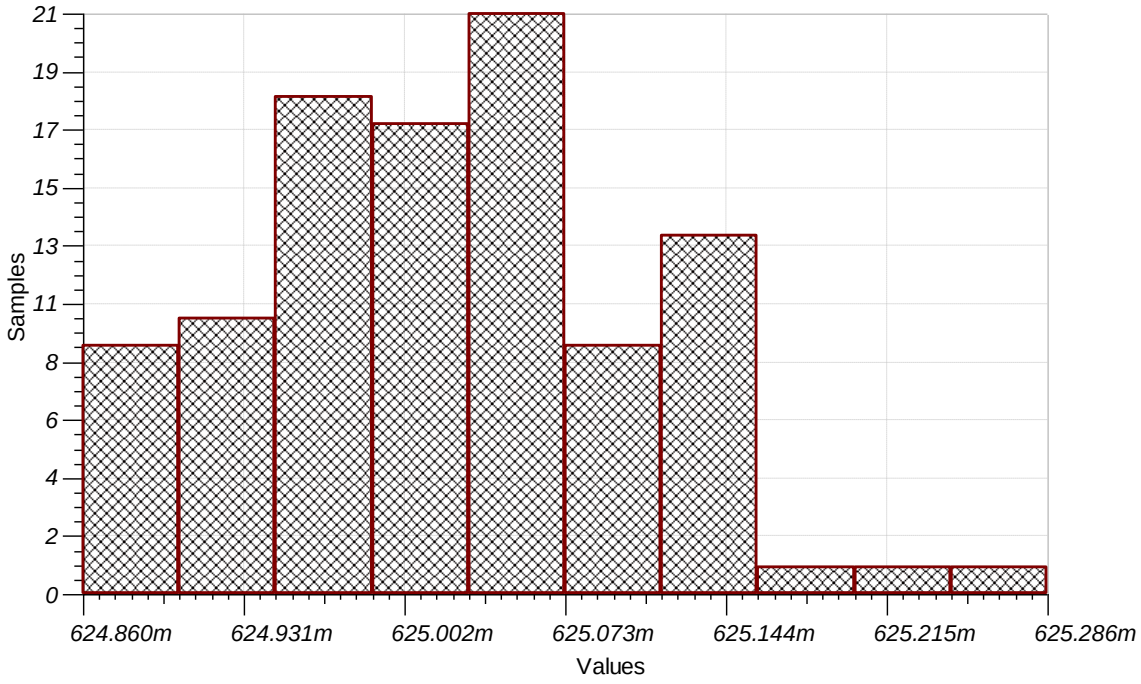

Figure 20: Circuit Output Variation with a 0 V dc Input

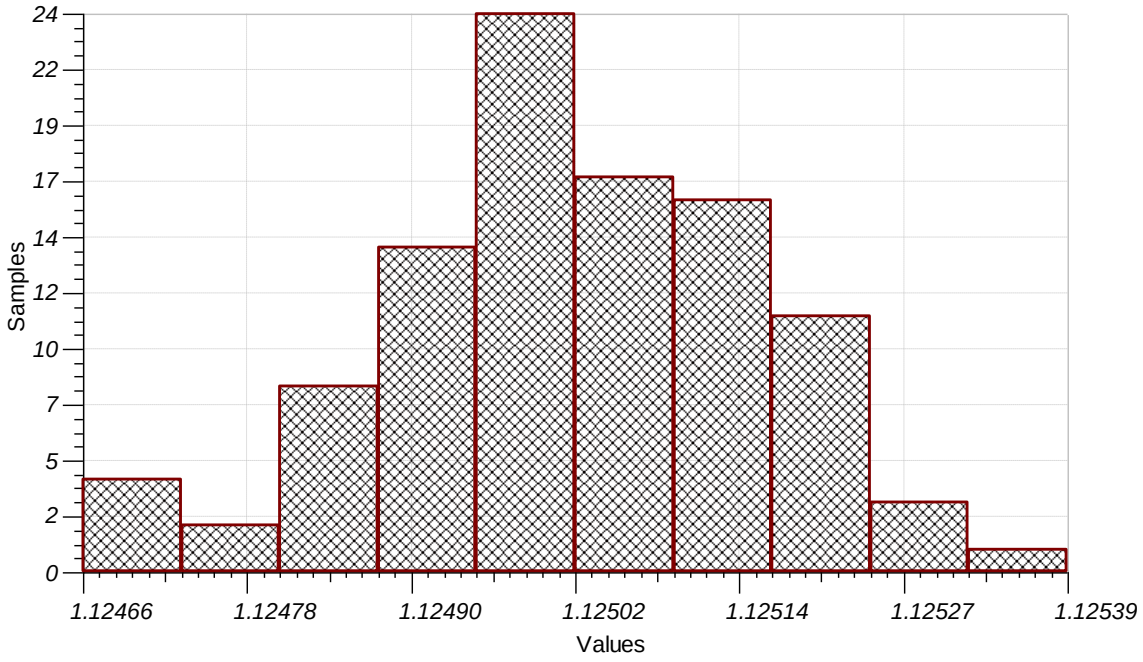

Figure 21: Circuit Output Variation with a Positive Full-Scale +5 V dc Input

B.3 MSP430F2013 SD_16 Measured Results

The measured output code results using the MSP430F2013 SD_16 ΔΣ ADC are shown in Figure 22. The error codes and calibrated error codes are shown in Figure 23 and Figure 24, respectively. The un-calibrated error codes results in approximately 2.86 mV of error or 0.286 %FSR, while the calibrated results reduce the error to approximately 172 µV or 0.017 %FSR.

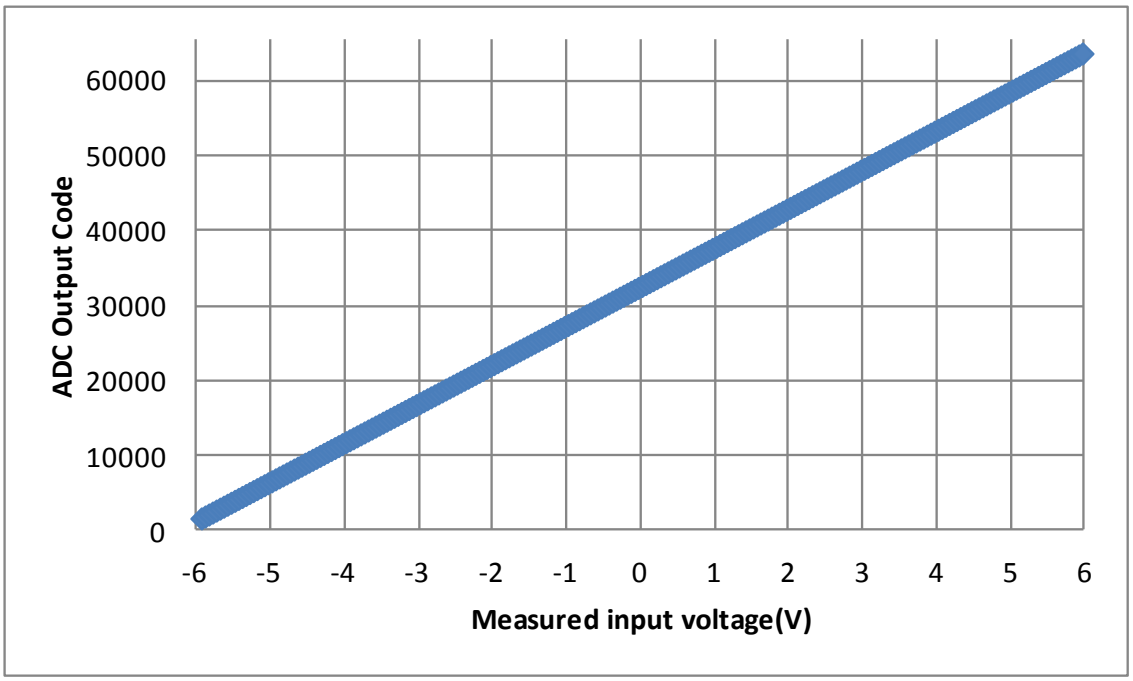

Figure 22: MSP430F2013 Output Code vs. Input Voltage

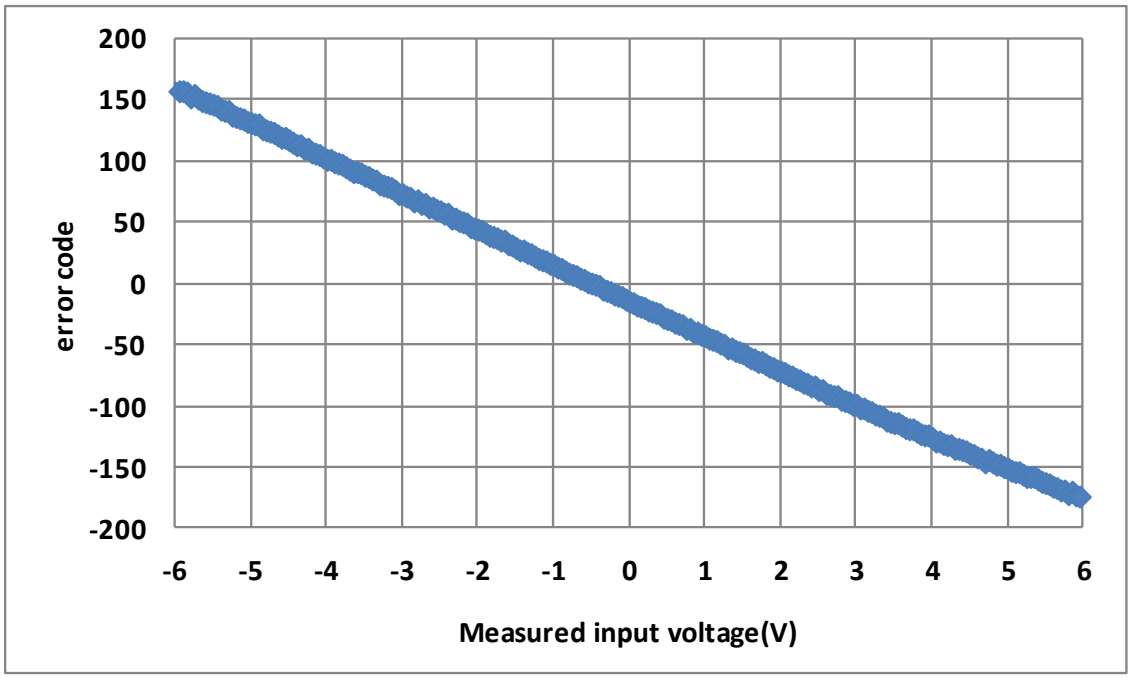

Figure 23: Un-calibrated Error Codes vs. Input Voltage

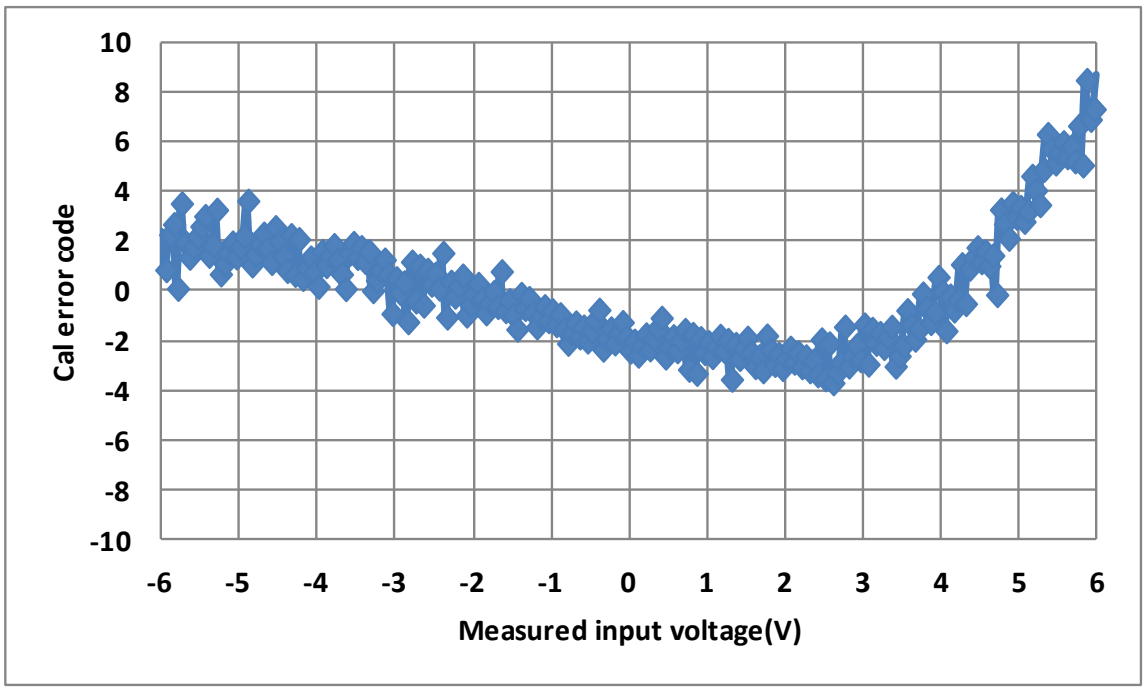

Figure 24: Calibrated Error Codes vs. Input Voltage

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