

# TI Designs

## Zero Drift Analog Front End PGA and Peripherals for MCCB



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### Design Resources

<a href="#">TIDA-00130</a>	Design Folder
<a href="#">PGA116, PGA117</a>	Product Folder
<a href="#">LM5017</a>	Product Folder
<a href="#">LM62BIM3</a>	Product Folder
<a href="#">CSD18537NKCS</a>	Product Folder
<a href="#">LM4041B</a>	Product Folder
<a href="#">TPS7A6533Q</a>	Product Folder
<a href="#">TPS55010</a>	Product Folder
<a href="#">ISO1176</a>	Product Folder
<a href="#">LM293</a>	Product Folder



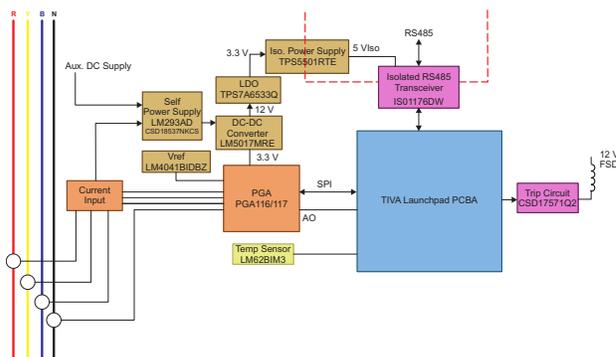
[ASK Our Analog Experts](#)  
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### Design Features

- Architecture enables customers to easily create multiple circuit breaker models with different current ranges
- Using programmable gain control architecture, Fault current sensing range can be increased to > 10 times  $I_r$  and < 0.2  $I_r$
- Lower total manufacturing cost with reduced component count and less calibration time
- Robust design with ambient insensitivity from  $-10^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  and better trip time repeatability
- Wide input DC-DC converter with undervoltage and overcurrent protection
- Self-power (CT powered) supply with reduced CT loading and lower power loss
- Device operating temperature is  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  as required for MCCB/ACB

### Featured Applications

- MCCB – Electronic trip unit (Electronic Release)
- ACB – Electronic trip unit (Electronic Release)
- Self-powered overcurrent, Earth fault, and numerical relays



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## 1 System Description

**MCCB - Electronic Trip Units (MCCB-ETU)** react to the magnitude of the current flowing through the circuit breaker. These trip units are current-sensor powered and require a minimum current to be operational. The electronic trip unit uses digital sampling to determine the RMS value of sinusoidal and nonsinusoidal currents.

Some of the advantages of ETUs are:

- Accurate sensing – pickup and trip timing
- Ambient insensitive from –10 to 70 °C
- Adjustable  $I_r$  (Adjustable overload setting current) for continuous current settings
- Pick-up (A) accuracy  $\pm 10\%$  and time-delay(s) accuracy 0 to –20%

To sense the current input, an amplifier with programmable gain is used for signal conditioning.

Some of the limitations are:

1. Higher DC output offset and low Rail-to-Rail output, therefore limiting the ADC range
2. Pickup and trip timing characteristics vary over –10 to +70°C
3. Suffer from phase reversal problems during short circuit protection resulting in pickup and trip timing repeatability issues
4. Higher input bias current causes loading on the input CT, resulting in measurement nonlinearity
5. TI places the trip units inside the breaker units, subjecting the trip units to higher electromagnetic interference, and requiring external filters
6. Needs more testing during manufacturing

This reference design provides an analog front end amplifier solution that provides the following advantages:

1. Lower DC offset and improved Rail-to-Rail output voltage improves accuracy
2. Accurate and repeatable over –10 to +70°C (less variation in pickup and trip time)
3. Reduced loading on the current transformers due to lower input bias current
4. Does not have phase reversal effects during saturation conditions, resulting in improved repeatability
5. Better Electromagnetic Immunity
6. The improvements listed from 1 to 5 also result in reduced manufacturing time, testing time, and improved yield

The MCCB analog front end amplifier reference design is intended as an evaluation platform for easy evaluation of the MCCB - electronic trip characteristics. The following functionalities have been provided on the reference design:

- Current input measurement with programmable gains, based on PGA116 and PGA117
- TI MOSFET-based self-powered power supply
- DC-DC converter for FSD/Relay supply generation
- Isolated RS-485 communication
- Screw terminals for easy connection
- MCU interface for quick and easy evaluation

The complete design or parts of the design can be used in other self-powered or dual powered (self-powered or 24-V auxiliary input powered) applications like overcurrent, Earth fault and other protection relays.

The design files include PDF schematics, bill of materials (BOM), PDF layer plots, Altium files, and Gerber files.

## 2 Design Specification

### 2.1 PGA with Low Supply Voltage (3.3 VDC)

Inputs:

Programmable gain for R, Y, B, and N inputs.

Gain options:

Binary Gains (PGA116): 1, 2, 4, 8, 16, 32, 64, and 128.

Scope Gains (PGA117): 1, 2, 5, 10, 20, 50, 100, and 200.

Rail-to-Rail operation up to 3.3 V – 50 mV

Low output DC offset voltage < 200  $\mu$ V with highest gain.

#### NOTE:

The design engineer can configure the required gains for evaluation.

The design provides two resistors as burden resistors for CT inputs.

### 2.2 Power Supply

Power supplies generated: > 12 VDC  
~16 VDC  
3.3 VDC

Self-power supply regulation: 39 VDC  $\pm$ 5%

Input supply range for auxiliary input: 20 VDC to 35 VDC

### 2.3 Measurement Reference (1.65 VDC with $\pm$ 0.25%)

The design engineer can select the reference for input current between 0 V and VCC/2, using jumpers. VCC/2 is generated using precision reference. The reference selected is 1.65 V with 0.1% tolerance. Expect a maximum output error less than  $\pm$ 0.25%.

### 2.4 Temp Sensor

The temperature sensor has a 0°C to +90°C temperature range with an accuracy of  $\pm$ 3.0°C at 25°C.

### 2.5 MOSFET Switch

The MOSFET switch contains control for FSD/Relay outputs.

### 2.6 Communication

The interface provided is an isolated RS-485 communication interface to implement Modbus protocol. The design provides an option to mount failsafe and termination resistors.

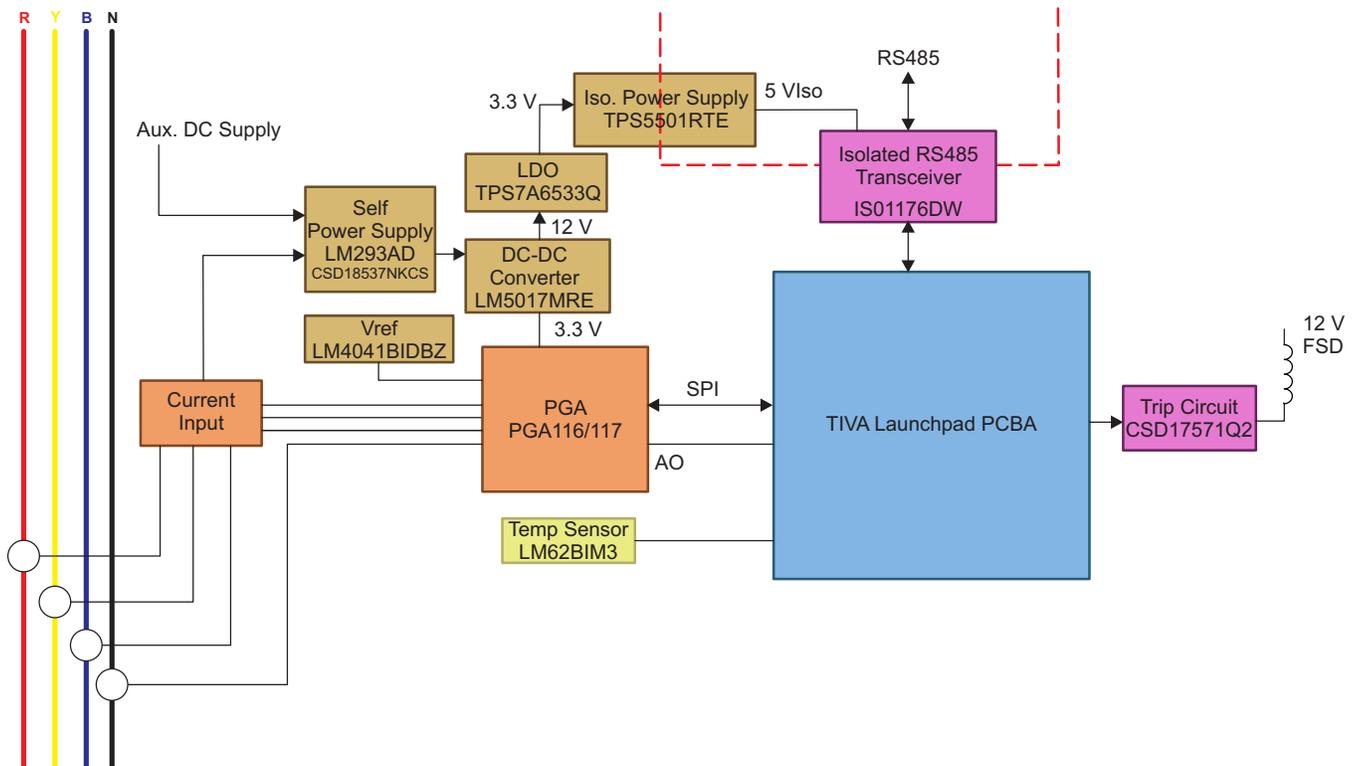
### 2.7 MCU Interface

The current inputs and the temperature inputs interface to Tiva C Series 32-bit MCU. The MCU has an internal 12-bit SAR ADC with multiplexed inputs.

### 3 Block Diagram

The MCCB-ETU analog front end reference design has the following blocks:

1. Programmable gain amplifier, reference, temperature sensor and current input
2. Self-power supply
3. Isolated RS-485 interface
4. MOSFET switch to control Relay/FSD
5. Tiva C series 32-Bit MCU LaunchPad interface



**Figure 1. Block Level Diagram**

#### 3.1 Programmable Gain Amplifier, Reference, and Current Input

Programmable Gain amplifiers are used to amplify the wide range of current inputs. Four input channels of the PGA are utilized for three phase and Neutral current inputs. A stable reference with high accuracy has been provided for accurate measurement over wide temperature. Screw type terminals are provided to connect CT input. A high accuracy temperature sensor is provided.

- 3.2** The self-power supply generates output voltage from the input currents. Three phase input currents generate the required power for the functioning of the electronics. Optionally, the ETU can be powered by auxiliary 24-V DC input. The self-power output is converted to 12 V and 3.3 V for FSD/relay operation and MCU functioning using a DC-DC convertor and LDO.

#### 3.3 Isolated RS-485 Interface

This MCCB-ETU analog front end amplifier design can also communicate the measured data to the supervisory system through the RS-485.

### 3.4 Relay/FSD Control

A MOSFET-based switch provides for Relay/ FSD control, a 12-V supply controls the relay. The design engineer can adjust the output of the DC-DC converter to 15 V or 18 V with programmable resistors.

### 3.5 Tiva C Series LaunchPad Interface

This reference design uses the Tiva C Series 32-bit CPU LaunchPad to measure and transfer the data to a PC-based GUI through a USB interface. The PGA output is connected to the 12-bit ADC of Tiva LaunchPad. The gain and the channel selection for the PGA are done using an SPI interface.

## 4 Circuit Design and Component Selection

Table 1 contains a comparison of different op amps with critical characteristics.

**Table 1. Comparison of Different Op Amps and PGAs with Critical Characteristics**

Characteristics	Application Need	PGA116, PGA117	LMV824-N
Iq Total (Max) (µA)	Low	1.6 mA	1.2 mA
Number of Channels	≥ 4	10 (Muxed)	4
Rail-to-Rail	Rail-to-Rail	In/Out	Out
Operating Temperature Range (C) (Package dependent exception exist)	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C
Vos (Offset Voltage at 25°C) (Max) (mV)	Min offset	0.1	3.5
Offset Drift (Typ) (µV/C)	Min offset drift	1.2	1
Vn at 1 kHz (Typ) (nV/rtHz)	Min noise	12	28
CMRR (Min) (dB)/PSRR	Max	100	90/85
Total Supply Voltage (Max) (+5 V = 5, ±5 V = 10)	3.3 V	5.5 V	5.5 V
Slew Rate (Typ) (V/us)	1	12	1.4
GBW (Typ) (MHz)	1	1.8	5
Pin/Package	14/20 pin SOIC	20pin SOIC	14SOIC,14TSSOP
Settling Time (0.1%) (Typ) (ns)	5 µs to 10 µs	10 µs for 0.01%	NA
ESD-Human model-kV	High	3	2
Gain Error	0.25%	0.10%	External resistors dependent
Gain Drift	>100 PPM	2 PPM/ °C	External resistors dependent
Vo (Swing)	Rail-to-Rail	Vcc-60 mV	Vcc-100 mV

#### 4.1 PGA , Voltage Reference , Temperature Sensor and Current Inputs

The PGA116 and PGA117 (binary/scope gains) offer 10 analog inputs and a four pin SPI Interface with daisy-chain capability in a TSSOP-20 package.

The PGA116 is programmable for binary gains: 1, 2, 4, 8, 16, 32, 64, and 128.

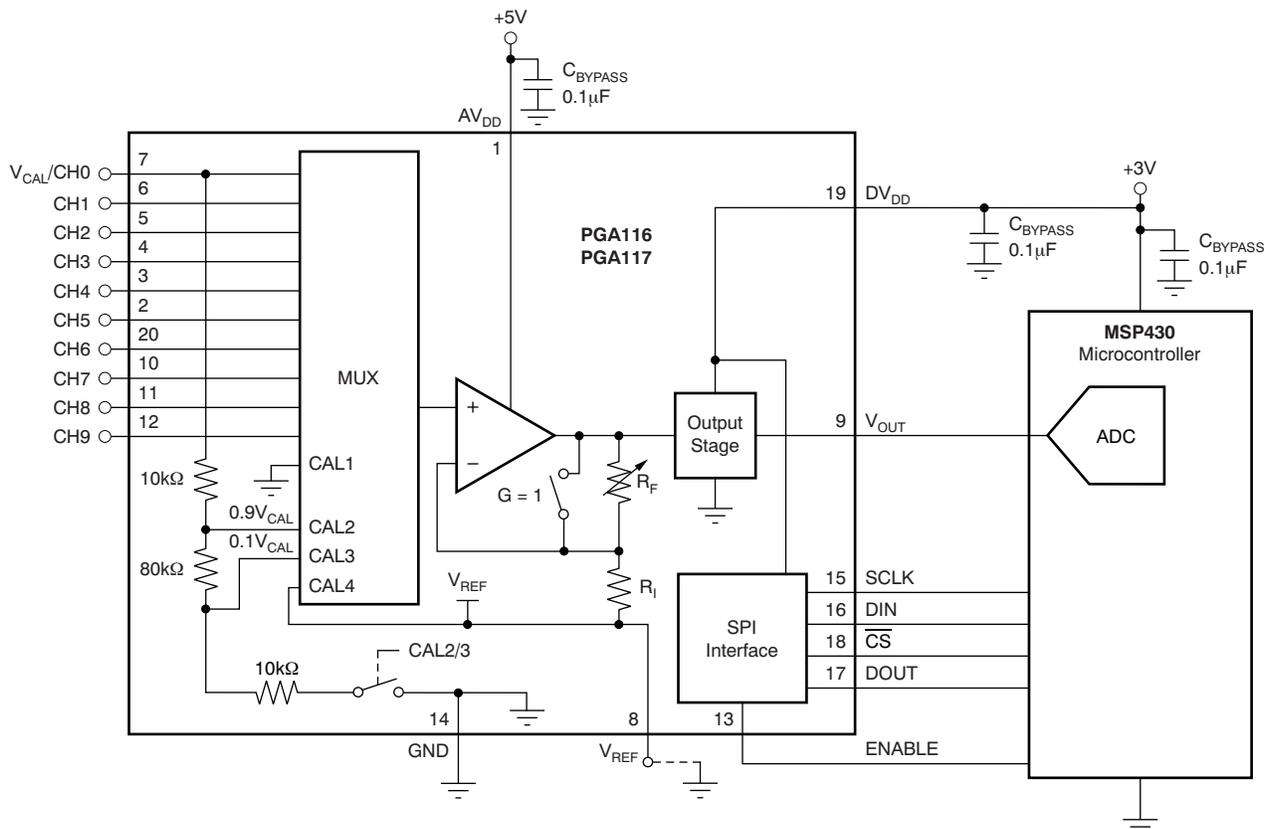
The PGA117 is programmable for scope gains: 1, 2, 5, 10, 20, 50, 100, and 200.

##### Channels configured for measurement

In the current design Channel 0–Channel 3 (designated CH0, CH1, CH2, and CH3) are configured. Based on the current input, the gains of the PGA can be programmed.

Programming of the PGA is done through an SPI interface .

**The programmable gain provides the option to extend the adjustable current range to > 10 In. (nominal current)**

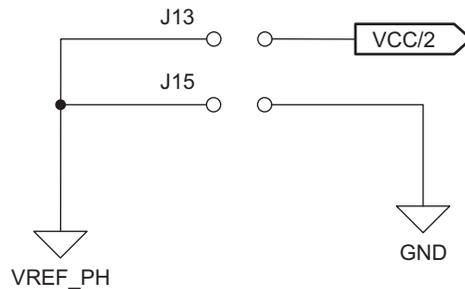


**Figure 2. PGA116/PGA117 Offered in a TSSOP-20 Package**

Some of the critical features are:

- Low noise: 12 nV/ $\sqrt{\text{Hz}}$
- Low offset voltage: 25  $\mu\text{V}$  (Typ), 100  $\mu\text{V}$  (Max)
- Offset drift of 1.2  $\mu\text{V}/^\circ\text{C}$
- Amplifier gain drift of 6 PPM
- Low input offset current:  $\pm 5$  nA max (+25°C)
- SPI Interface (10 MHz) with daisy-chain capability
- Gain switching time: 200 ns
- Extended temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

An SPI interface programs the PGA's gain. The PGA accepts AC input or rectified half wave input. The input is configured with the jumper settings illustrated in [Figure 3](#) and listed in [Table 2](#).



**Figure 3. PGA116 and PGA117 Input Jumper Configuration**

**Table 2. Input Jumper Configuration for PGA116 and PGA117**

Test Condition 1	Jumper J13 is mounted	PGA accepts AC input (J14 must be removed)
Test Condition 2	Jumper J15 is mounted	PGA accepts rectified input (J14 is removed)

1. In case the neutral CT output is not rectified, the output J14 must be mounted to level shift the neutral CT output in condition 2.
2. Do not mount jumpers J13 and J15 together.

The reference design also has an LM4041-N/LM4041-N-Q1 Precision Micro-Power Shunt Voltage Reference for providing the level shifting when the PGA is configured for AC input.

Key Specifications (LM4041-N/LM4041-N-Q1 1.2) include:

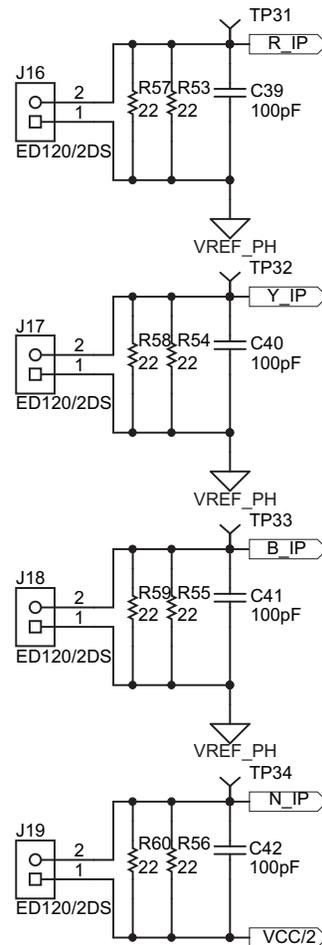
- 0.1% output voltage tolerance
- 20- $\mu$ V RMS Output noise
- Low Temperature coefficient of < 100 PPM/ $^{\circ}$ C

Using the above reference along with the PGA guarantees the trip accuracy over a wide temperature range.

The reference design includes a temperature sensor for thermal overload trip and gain compensation functions as required. The temperature sensor is rated for a 0 $^{\circ}$ C to +90 $^{\circ}$ C range.

### 4.1.1 Current Inputs

Figure 4 shows the current input schematics.



**Figure 4. Current Inputs Schematics**

The board provides the ability to connect up to 4 current inputs. The current input can be AC or half-wave rectified input. The design includes the ability to mount two 22R burdens. The reference design includes a screw type terminal to connect the current input. Based on the secondary current and transformer performance, the design engineer can change the burden resistor. The reference design includes an option to switch burdens using MOSFETs. The option to switch burdens is for a future enhancement and is currently not used in this design. This provision can be used to increase input current range. A Rogowski coil cannot be connected directly and the output from the integrator has to be applied at the current inputs. When the integrator output is applied, burden resistors must be made as do not populate.

#### CAUTION

Do not leave the Current terminal open and apply current during testing. Ensure the current inputs are connected and the terminal screws are tightened before applying current for testing.

## 4.2 Self-Power Supply

Figure 5 illustrates the self-power supply schematic.

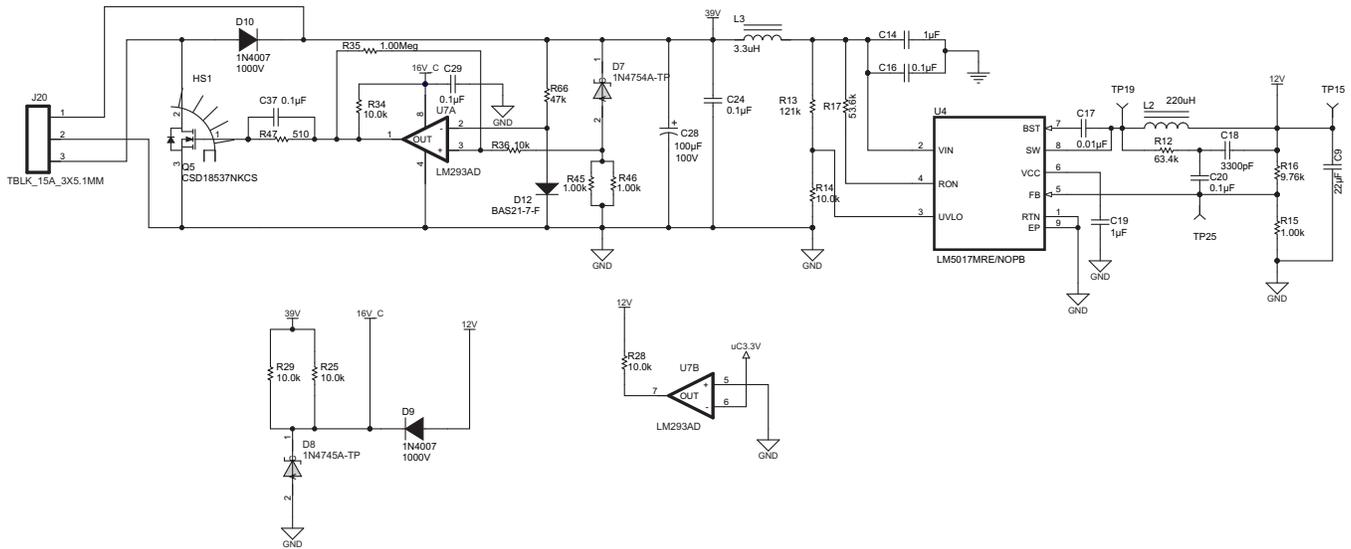


Figure 5. Self-Power Supply

The self-power section has two input provisions:

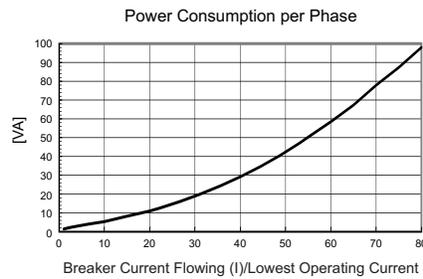
1. Half-wave rectified current inputs
2. Auxiliary DC inputs

The self-power supply generates output voltage from the input currents. The input to the self-power generation circuit is half-wave rectified output from current transformers. The design engineer must connect the rectifier diodes externally. Optionally, power the ETU by auxiliary 24-V input. The Zener diode reference regulates the self-power to 39 V. If the output voltage exceeds 39 V, the comparator switches the MOSFET on and the MOSFET shunts the input current. When the output voltage reduces, the comparator switches the MOSFET off and the input current charges the output capacitor. The 39-V self-power output is converted to 12 V and 3.3 V for FSD/relay operation and electronic circuit functioning using DC-DC converters and LDO. The advantage of the self-power circuit is to reduce CT loading. The critical component in the self-power circuit is the shunt regulation MOSFET. A wide range of MOSFETs are available and are listed in [TI MOSFETs with Current Shunting](#).

### TI MOSFETs with Current Shunting

Product Description	Product Link
60-V, N-Channel NexFET™ Power MOSFET	<a href="#">CSD18537NKCS</a>
60-V, N-Channel NexFET Power MOSFET	<a href="#">CSD18534KCS</a>
80-V, N-Channel NexFET Power MOSFET	<a href="#">CSD19506KCS</a>
80-V, 7.6-mΩ, N-Channel TO-220 NexFET Power MOSFET	<a href="#">CSD19503KCS</a>
100-V, N-Channel NexFET Power MOSFET	<a href="#">CSD19535KCS</a>
100-V, 6.4-mΩ, TO-220 NexFET Power MOSFET	<a href="#">CSD19531KCS</a>

The graph in [Figure 5](#) indicates the power loss in a typical self-power supply.



**Figure 6. Typical Power Consumption for Current/Lowest Operating Current**

**CAUTION**

Do not leave the current terminal open and apply current for testing. Ensure the current inputs are connected and the terminal screws are tightened before applying current for testing.

By using LM5017, the clamping voltage can be increased as the device input is rated up to 100 V. The MCCB-ETU analog front end reference design details shunt clamping, with LM5017 configured in non-isolated output configuration.

### 4.3 Isolated RS-485 Communication Interface

The reference design provides an EMC-compliant isolated 1-Mbps, 3.3 V to 5 V RS-485 interface using an ISO1176 transceiver and the TPS55010. This board provides signal and power isolation with reduced board space and power consumption. The TPS55010 has a higher efficiency and better regulation accuracy since its Fly-Buck™ topology uses primary side feedback that provides excellent regulation over line and load. The TPS55010 provides 3.3 V to 5 V and isolation levels using off-the-shelf Fly-Buck transformers. The transformer chosen here for the design has a 475-μH primary inductance and a dielectric strength of 2500 VAC. The ISO1176 transceiver is an ideal device for long transmission lines since the ground loop is broken to provide for operation with a much larger common mode voltage range. The symmetrical isolation barrier provides 2500 VRMS of isolation between the line transceiver and the logic level interface. The RS-485 bus is available on screw type terminals and connectors.

The RS-485 bus provides an external failsafe biasing that uses external resistor biasing to ensure failsafe operation during an idle bus. If none of the drivers connected to the bus are active, the differential voltage (VAB) approaches zero or in between ±250 mV, allowing the receivers to assume random output states. To force the receiver outputs into a defined state, the design introduces failsafe biasing resistors with terminating resistors of 120 Ω. The RS-485 bus is also protected against EFT, ESD, and surges with the help of transient voltage suppressor diodes (SMCJ15CA, 1500-W series).

### 4.4 FSD/Relay Control

TI has a wide range of MOSFETs that can be used for driving Relay, FSD, Alarms, or LEDs. TI provides a wide range of MOSFETs with a tiny SON2x2 package. [CSD17571Q2](#) is installed in the reference design.

**Table 3. TI MOSFETs for Driving Relay, FSD, ZS0, or LEDs**

Product Description	Product Link
30-V, N-Channel NexFET Power MOSFETs	<a href="#">CSD17571Q2</a>
N-Channel Power MOSFET, CSD13202Q2, 12-V VDS, 9.3 mΩ, R <sub>DS(on)</sub> 4.5 (max)	<a href="#">CSD13202Q2</a>
20-V, N-Channel NexFET Power MOSFET	<a href="#">CSD15571Q2</a>
Automotive 30-V, N-Channel NexFET Power MOSFET	<a href="#">CSD17313Q2Q1</a>
30-V, N-Channel NexFET Power MOSFET	<a href="#">CSD17313Q2</a>
N-Channel, NexFET Power MOSFET	<a href="#">CSD16301Q2</a>

### 4.5 Tiva C Series LaunchPad Interface

The Tiva™ C Series LaunchPad ([EK-TM4C123GXL](#)) is a low-cost evaluation platform for ARM® Cortex™ M4F-based microcontrollers. The Tiva C Series LaunchPad design highlights the [TM4C123GH6PMI](#) microcontroller USB 2.0 device interface, hibernation module, and motion control pulse-width modulator (MC PWM) module. The Tiva C Series LaunchPad also features programmable user buttons and an RGB LED for custom applications. The stackable headers of the Tiva C Series LaunchPad BoosterPack XL interface demonstrate how easy it is to expand the functionality of the Tiva C Series LaunchPad when interfacing to other peripherals on many existing BoosterPack add-on boards as well as future products. [Figure 7](#) shows a photo of the Tiva C Series LaunchPad.

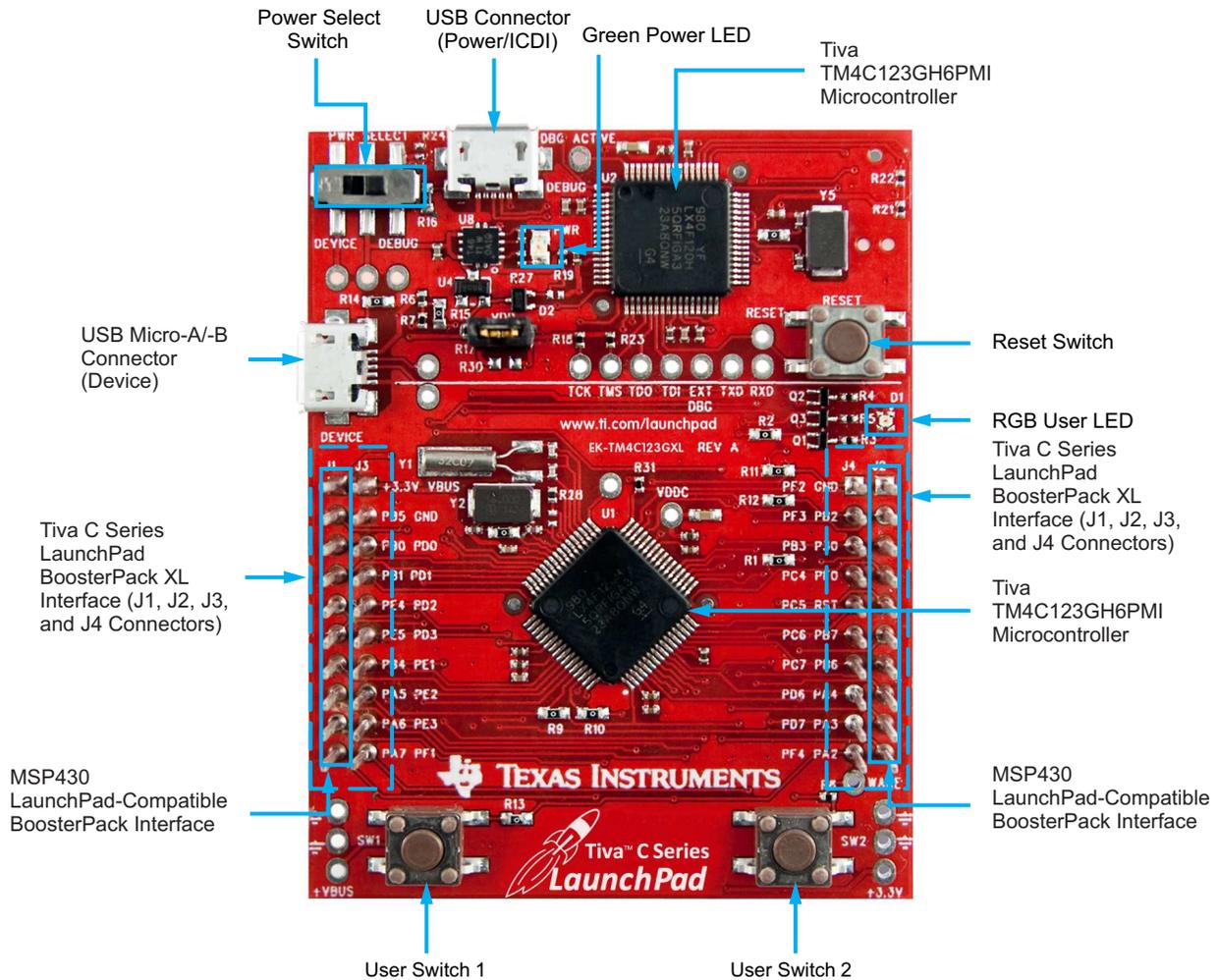


Figure 7. Tiva C Series LaunchPad

For details, refer to [EK-TM4C123GXL](#).

Care must be taken while aligning the Tiva C Series LaunchPad with the reference design board.

Table 4. Mapping Tiva C Series LaunchPad and Reference Design Connectors

Tiva C Series LaunchPad Connector	Reference Design Connector
J1,J3	J1
J4,J2	J11

## 5 Test Results

This section contains descriptions of self-power supply rail, accuracy testing results, and a summary of the test results.

### 5.1 Self-Power Supply Rail

Table 5 includes the self-power supply rail measured results.

**Table 5. Self-Power Supply Rail Measured Results**

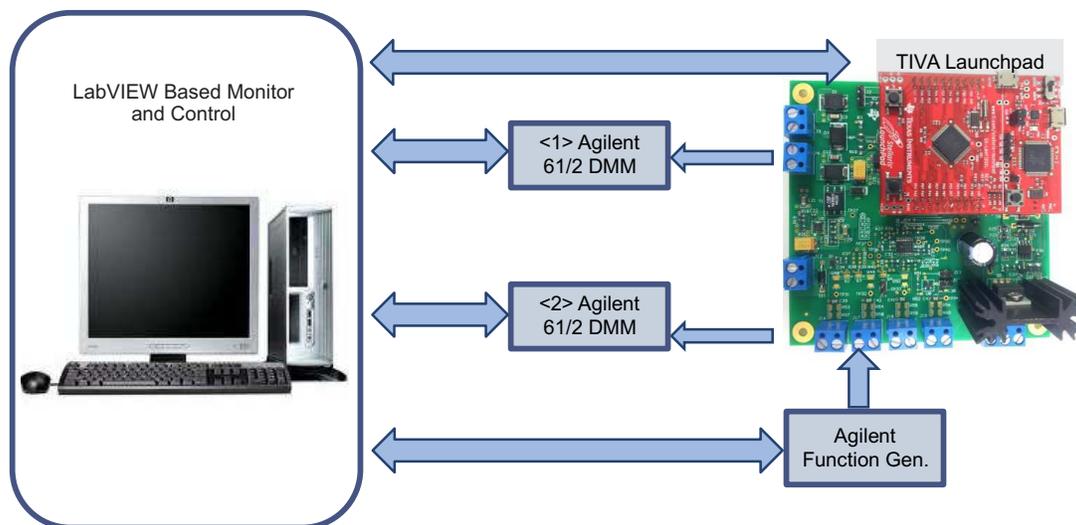
Rails	Measured
39 V	39.80 V
16 V	16.12 V
12 V	12.20 V
3.3 V	3.30 V
Vref (VCC/2)	1.655 V

### 5.2 Accuracy Testing

This section contains test results including the test setup, DC offset, 12-bit ADC measurement results, offset variation over temperature, gain drift over temperature, gain error before saturation, and a summary of the test results.

#### 5.2.1 Test Setup

Figure 8 illustrates the MCCB-ETU test setup.



**Figure 8. TIDA-00128 Test Setup**

#### Setup Description

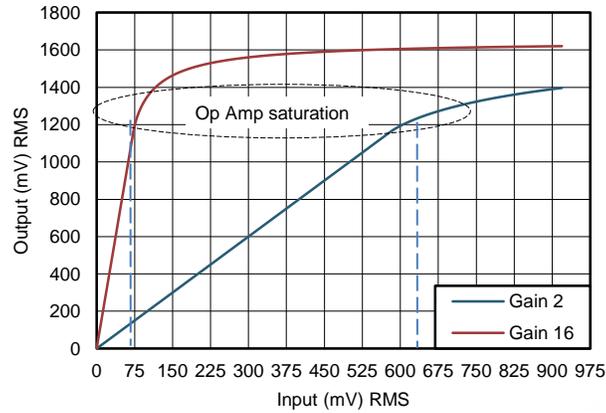
The measurement and characterization setup is made to be controlled by LabVIEW. Utilize the following steps:

1. Variable AC input is provided to the amplifier through J16 to J19.
2. The gain and channel selection for each measurement is configured by SPI Interface using Tiva LaunchPad.
3. The input voltage to amplifier and amplifier output voltages are measured using a multimeter.
4. The measurement is repeated for multiple steps .

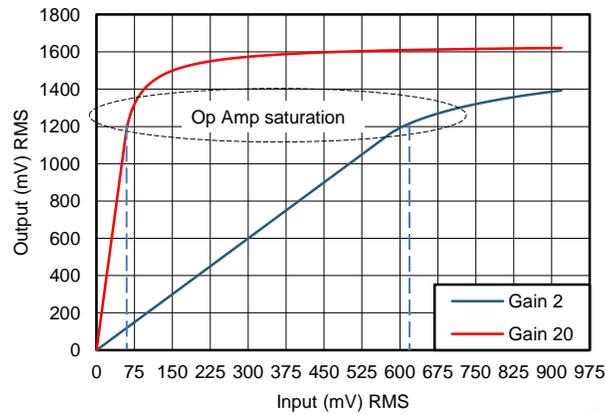
The tests were performed for different PGA gains.

Input Voltage Frequency: 60Hz.

**NOTE:** All the voltages mentioned in [Figure 9](#) through [Figure 18](#) are Root Mean Square Values (RMS).



**Figure 9. PGA116, Saturation**



**Figure 10. PGA117, Saturation**

Table 6 lists the register configuration and timing for PGA.

**Table 6. Register Configuration and Timing for PGA**

Amplifier	Gain	Gain and Channel Register Setting	Input Channel	Delay Before Measuring	SPI Speed	Total Conversion Time per Sample for each Channel <sup>(1)</sup>
PGA116	2	0x2A10	0	> 10 $\mu$ s	1Mbps	35 $\mu$ s
		0x2A11	1			
		0x2A12	2			
		0x2A13	3			
	8	0x2A30	0			
		0x2A31	1			
		0x2A32	2			
		0x2A33	3			
	128	0x2A70	0			
		0x2A71	1			
		0x2A72	2			
		0x2A73	3			
PGA117	2	0x2A10	0			
		0x2A11	1			
		0x2A12	2			
		0x2A13	3			
	10	0x2A30	0			
		0x2A31	1			
		0x2A32	2			
		0x2A33	3			
	200	0x2A70	0			
		0x2A71	1			
		0x2A72	2			
		0x2A73	3			

<sup>(1)</sup> Conversion time per sample = Channel and Gain Setting time – SPI (16.2  $\mu$ s) + PGA Settling time(10  $\mu$ s) + ADC Conversion time – 125 KSPS (8  $\mu$ s) + Software overhead (0.8  $\mu$ s)

### 5.2.2 DC Offset

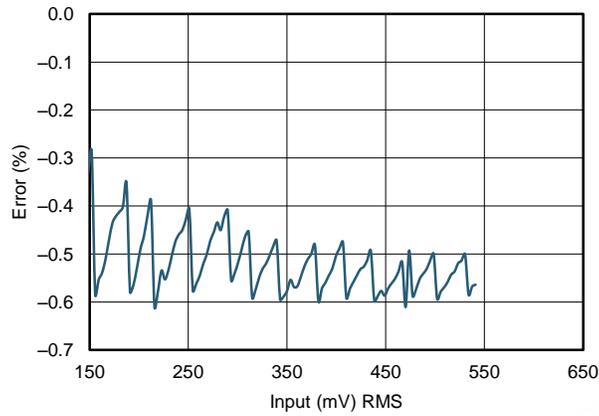
Table 7 output DC offset voltage results measured with Gain 1.

**Table 7. DC Offset**

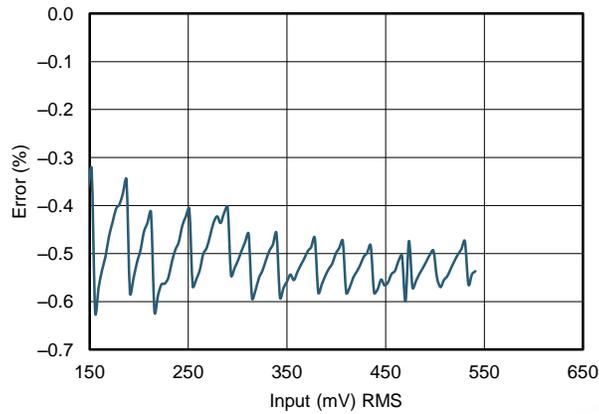
PGA Type	Channel Numbers	Offset ( $\mu$ V)
PGA116	Ch0	< 20
	Ch1	< 20
	Ch2	< 20
PGA117	Ch0	< 20
	Ch1	< 20
	Ch2	< 20

### 5.2.3 Measurement Results with 12-Bit ADC

The graphs in [Figure 11](#) and [Figure 12](#) indicate the uncalibrated error in percentage for PGA116 and PGA117 with Gain 2, when measured using a 12-bit internal ADC of the Tiva 32-bit MCU.



**Figure 11. PGA116 Gain 2, Error in %**



**Figure 12. PGA117 Gain 2, Error in %**

### 5.2.4 Offset Variation over Temperature

The output offset voltage drift is very low for PGA116 and PGA117 with temperature. The offset voltage was measured by keeping the PCB in a chamber set to different temperatures. [Table 8](#) shows the results.

**Table 8. DC offset Drift with Reference to 25°C**

Amplifier	Gain	Input Channel	Offset Drift at -10°C (mV)	Offset Drift at +60°C (mV)	Expected Drift in mV
PGA116	128	1	-4.16	3.834	9.0
		2	-5.83	5.32	
		3	-5.12	4.05	
PGA117	200	1	-5.65	4.654	14.0
		2	-5.542	4.61	
		3	-4.164	3.884	

### 5.2.5 Gain Drift over Temperature

The gain variation of the PGA116 and PGA117 is very low with change in temperature. The gain drift was measured by keeping the PCB in a chamber set to different temperatures. [Table 9](#) shows the results.

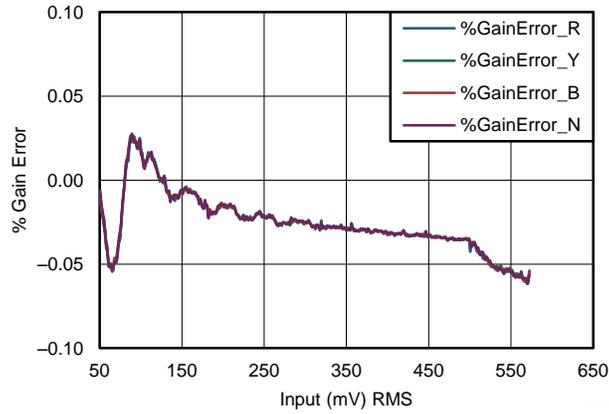
**Table 9. Gain Variation over Temperature**

Amplifier	Input Channels	Gain	Measurement Count at each Temperature	Allowed Drift in PPM	Average Gain Drift in PPM/°C Including Reference Offset and Reference Drift (25°C to 60°C)	Average Gain Drift in PPM/°C Including Reference Drift (25°C to -10°C)
PGA116, PGA117	1	2	5	> 102	30	-28
		8/10	5	> 102	-45	41
		16/20	5	> 102	-38	44
PGA116, PGA117	2	2	5	> 102	30	-45
		8/10	5	> 102	-42	41
		16/20	5	> 102	-55	58
PGA116, PGA117	3	2	5	> 102	28	-37
		8/10	5	> 102	-43	40
		16/20	5	> 102	-60	58

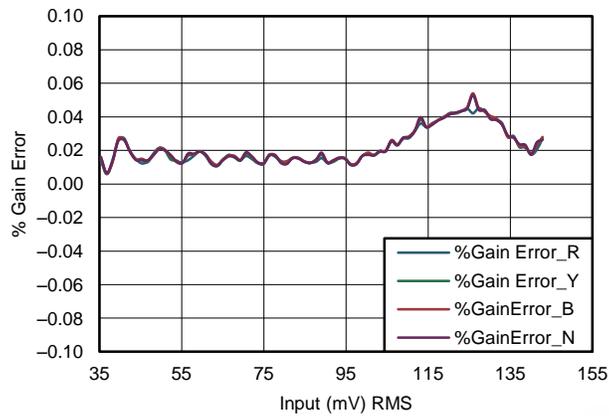
### 5.3 Gain Error

#### 5.3.1 PGA116

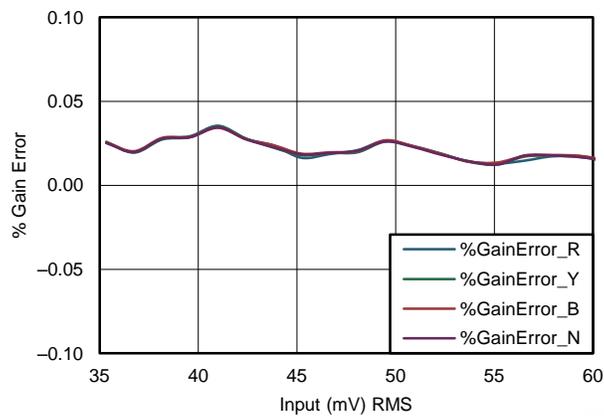
The PGA116 was tested at 25 °C with the input varied. The graphs in [Figure 13](#) through [Figure 15](#) show the gain error plots with respect to input.



**Figure 13. PGA116 Gain 2**



**Figure 14. PGA116 Gain 8**



**Figure 15. PGA116 Gain 16**

### 5.3.2 PGA117

The PGA117 was tested at 25°C with the input varied. The graphs in Figure 16 through Figure 18 show the gain error plots with respect to input.

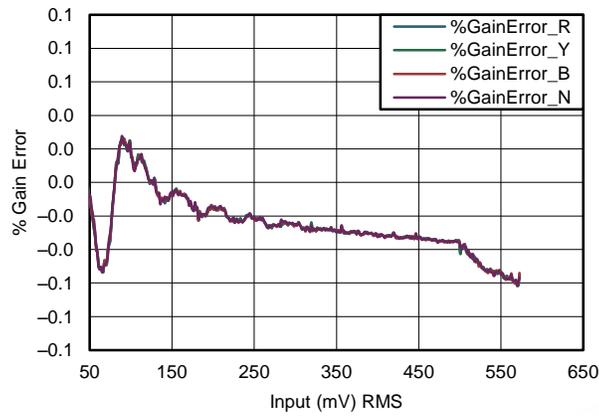


Figure 16. PGA117 Gain 2

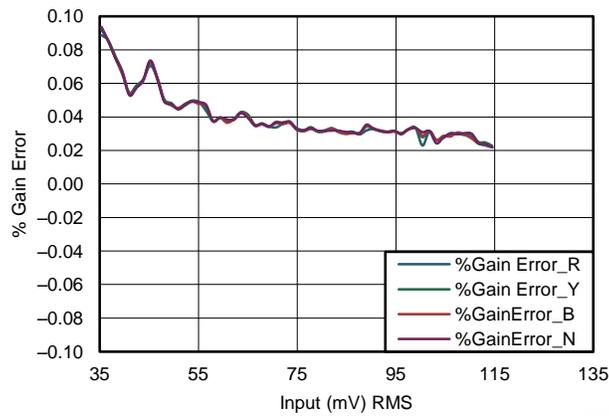


Figure 17. PGA117 Gain 10

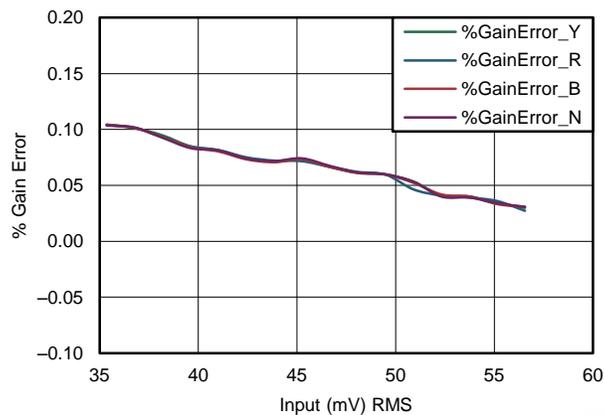


Figure 18. PGA117 Gain 20

## 5.4 Results Summary

The test results are summarized in [Table 10](#).

**Table 10. Test Results Summary<sup>(1)(2)(3)</sup>**

Parameters	Specification	PGA116	PGA117
DC offset	100 $\mu$ V	< 20 $\mu$ V	< 20 $\mu$ V
Gain error	0.1% for up to 32 Gain	< 0.1	< 0.1
Gain Drift	> 102 PPM/ $^{\circ}$ C	Around 50 PPM/ $^{\circ}$ C	Around 50 PPM/ $^{\circ}$ C

<sup>(1)</sup> This is average value for Ch0, Ch1 and Ch2.

<sup>(2)</sup> No calibration or error adjustments have been done during measurement

<sup>(3)</sup> The accuracy can be improved by calibration.

## 6 Schematics

Figure 19 through Figure 25 show the schematics for the zero drift analog front end PGA and peripherals for MCCB.

Page 2	<a href="#">BLOCK DIAGRAM</a>
Page 3	<a href="#">SELF POWER + REGULATOR +FSD +LDO</a>
Page 4	<a href="#">ANALOG FRONT END PGA +REF+TEMP SENSOR</a>
Page 5	<a href="#">ISOLATED RS485 INTERFACE</a>
Page 6	<a href="#">LAUNCH PAD INTERFACE</a>
Page 7	<a href="#">HARDWARE - MISCELLANEOUS</a>

Revision History	
Revision	Notes

**Figure 19. Schematics (1 of 7)**

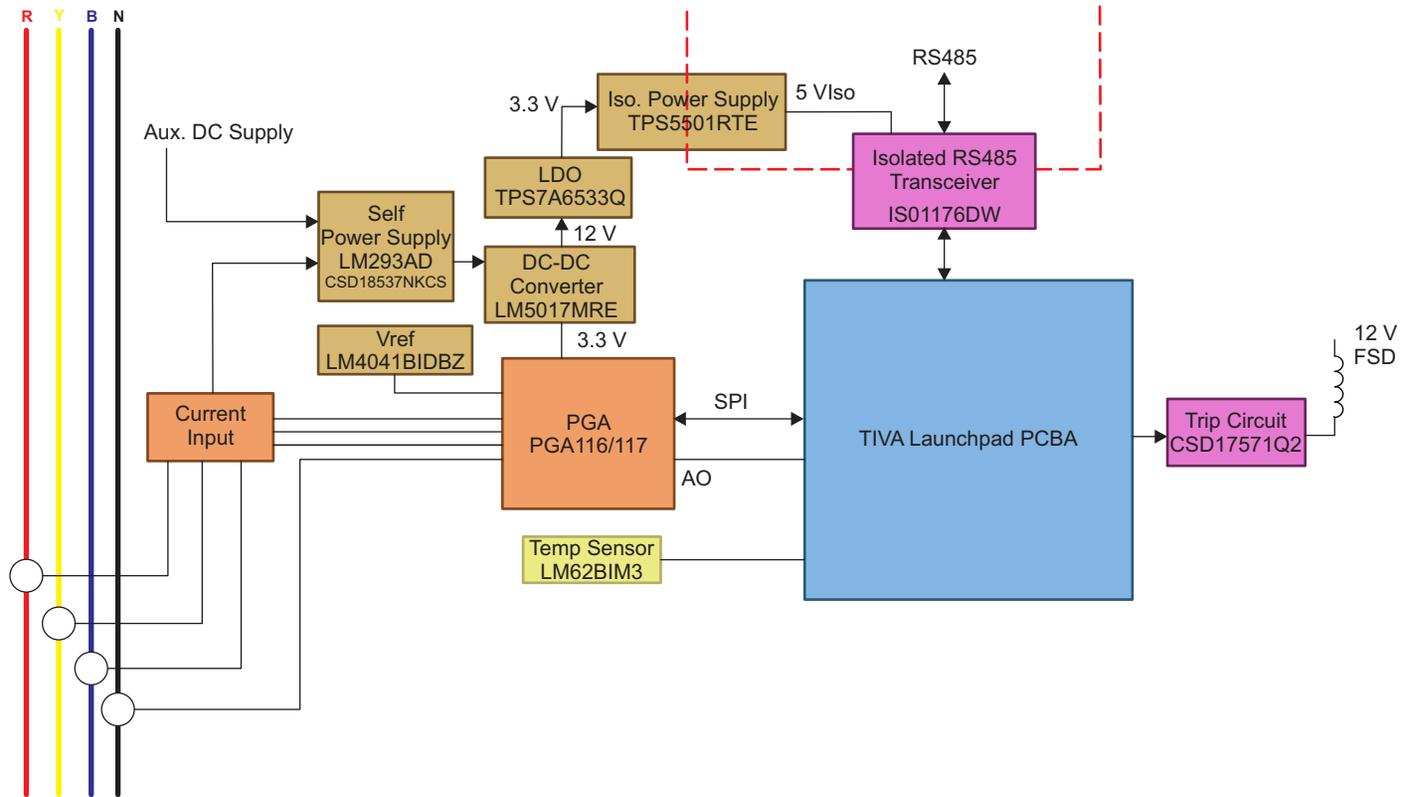


Figure 20. Schematics (2 of 7)



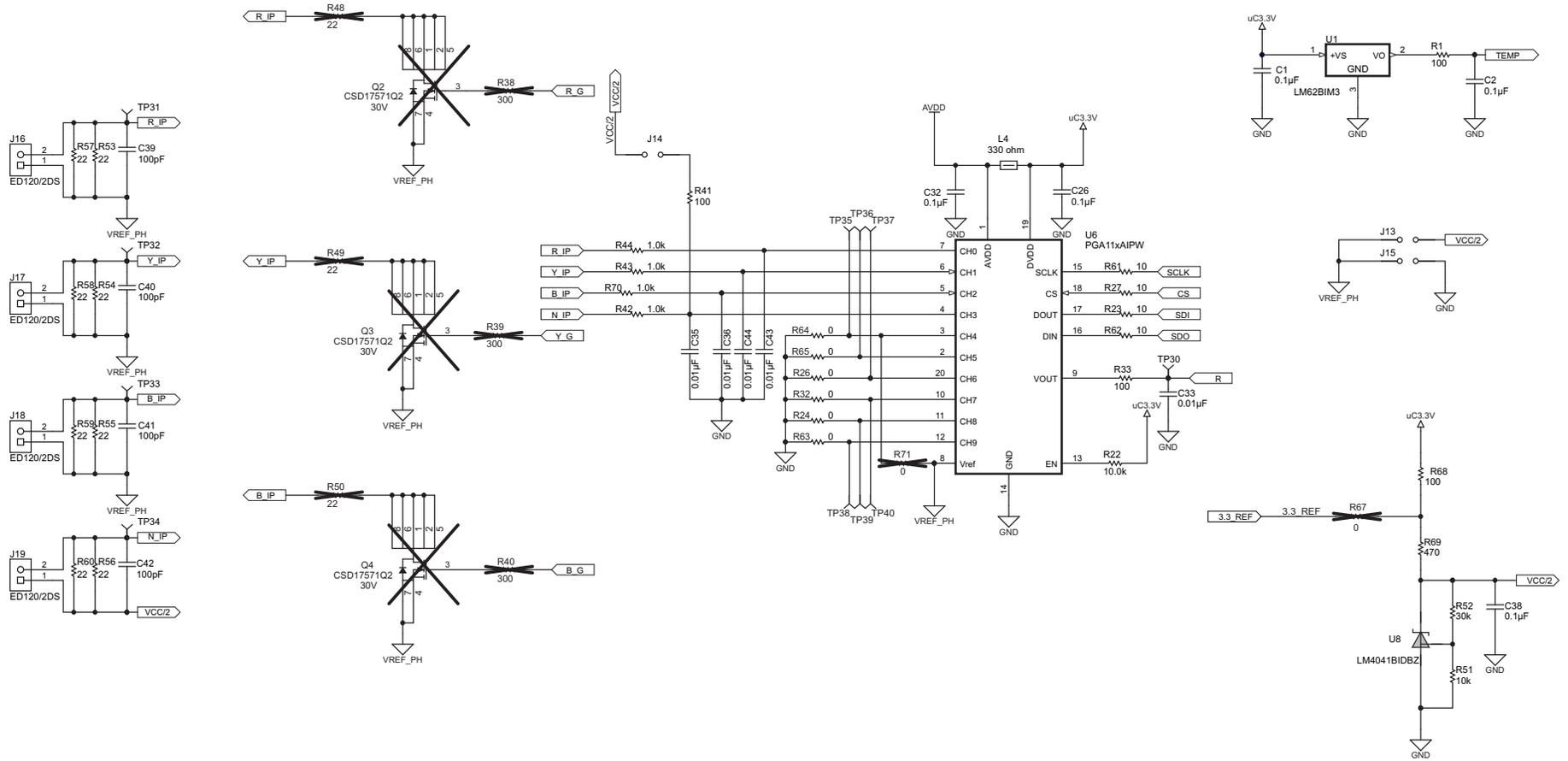


Figure 22. Schematics (4 of 7)

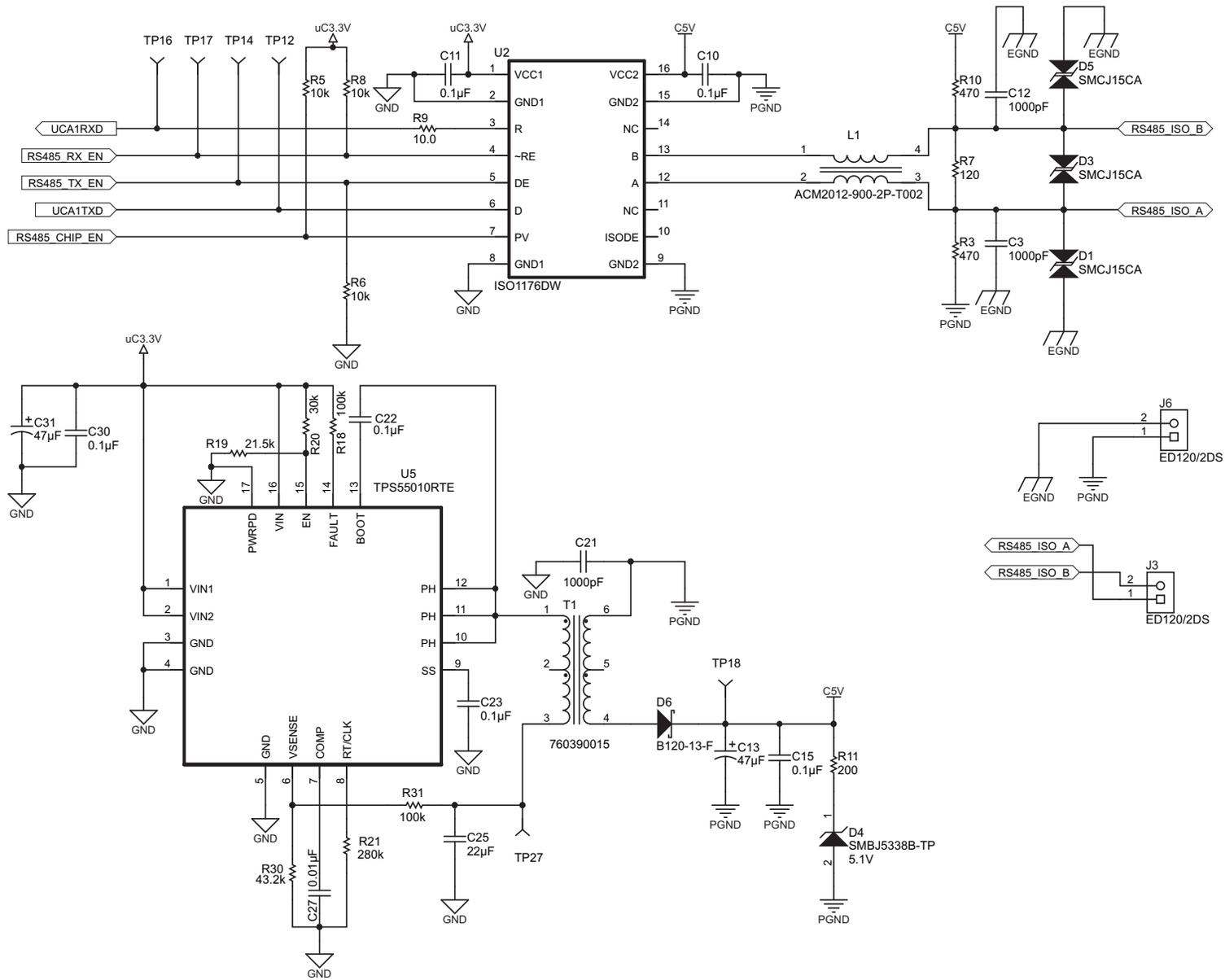


Figure 23. Schematics (5 of 7)

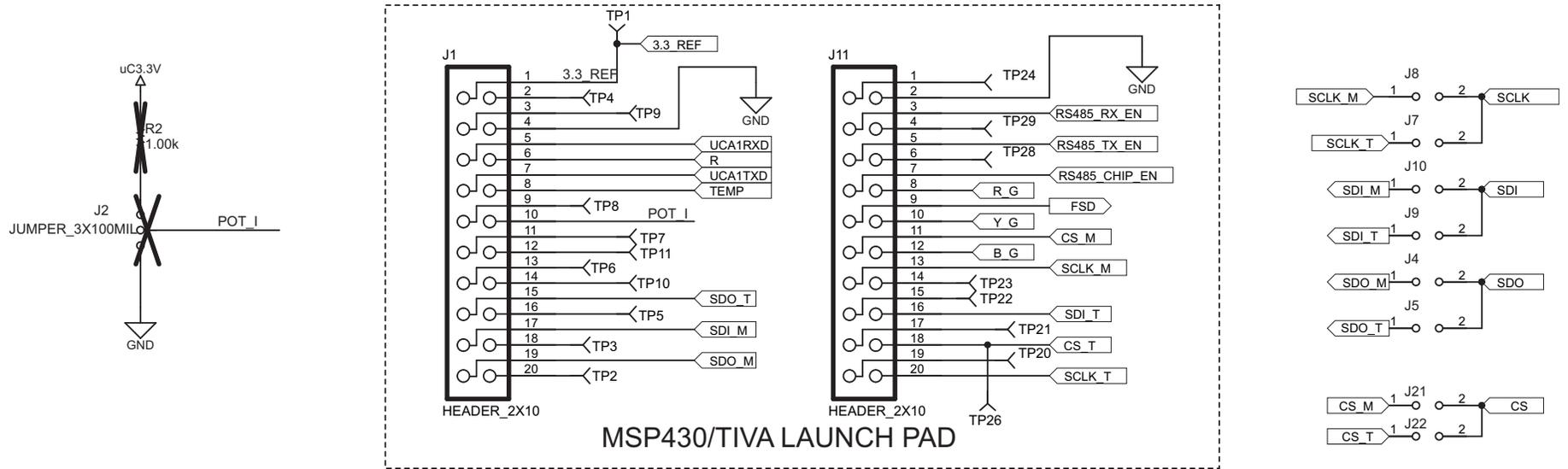
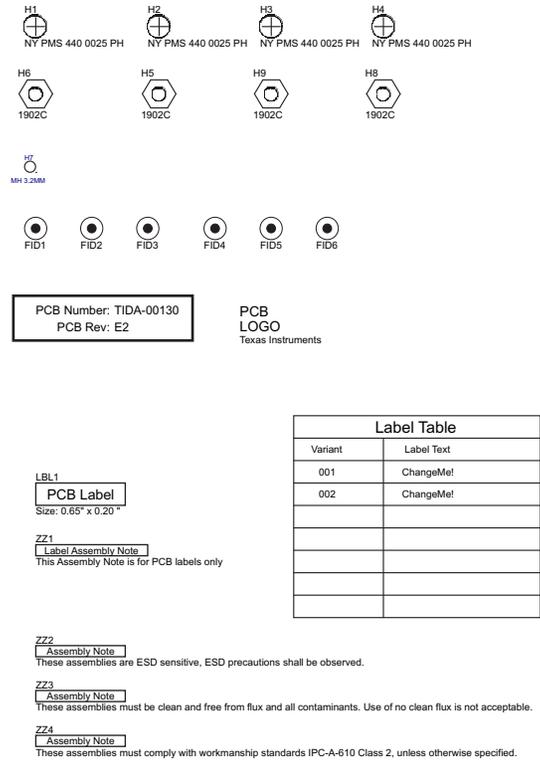


Figure 24. Schematics (6 of 7)



**Figure 25. Schematics (7 of 7)**

## 7 Bill of Materials

Table 11 contains the BOM for the zero drift analog front end PGA and peripherals for MCCB.

**Table 11. Bill of Materials**

Fitted	Description	Designator	Manufacturer	Part Number	Quantity	RoHS	Package Reference
Fitted	Printed Circuit Board	!PCB1	Any	TIDA-00130	1	O	
Fitted	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	C1, C2, C10, C11, C15, C16, C20, C22, C23, C26, C30, C32, C34, C37, C38	AVX	06033C104JAT2A	15	Y	0603
Fitted	CAP, CERM, 1000pF, 1000V, +/-10%, X7R, 1206	C3, C12, C21	Yageo America	CC1206KKX7RCBB102	3	Y	1206
Fitted	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	C4, C7	TDK	C1608X7R1C105K	2	Y	0603
Fitted	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	C5, C8, C29	Kemet	C0603C104K5RACTU	3	Y	0603
Fitted	CAP, TA, 4.7uF, 35V, +/-10%, 1.9 ohm, SMD	C6	Vishay-Sprague	293D475X9035C2TE3	1	Y	6032-28
Fitted	CAP, CERM, 22uF, 16V, +/-10%, X5R, 1206	C9	MuRata	GRM31CR61C226KE15L	1	Y	1206
Fitted	CAP, TA, 47uF, 35V, +/-10%, 0.3 ohm, SMD	C13, C31	Kemet	T495X476K035ATE300	2	Y	7343-43
Fitted	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	C14	MuRata	GRM31CR72A105KA01L	1	Y	1206
Fitted	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603	C17, C27, C33, C35, C36, C43, C44	TDK	C1608C0G1E103J	7	Y	0603
Fitted	CAP, CERM, 3300pF, 50V, +/-10%, X7R, 0603	C18	Kemet	C0603C332K5RACTU	1	Y	0603
Fitted	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0603	C19	TDK	C1608X5R1E105K080AC	1	Y	0603
Fitted	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0805	C24	Kemet	C0805C104K1RACTU	1	Y	0805
Fitted	CAP, CERM, 22uF, 16V, +/-20%, X5R, 1206	C25	AVX	1206YD226MAT2A	1	Y	1206
Fitted	CAP, AL, 100uF, 100V, +/-20%, 0.12 ohm, TH	C28	Rubycon	100YXJ100M10X20	1	Y	10x20mm
Fitted	CAP, CERM, 100pF, 25V, +/-10%, X7R, 0603	C39, C40, C41, C42	AVX	06033C101KAT2A	4	Y	0603
Fitted	Diode, TVS 15V 1500W BIDIR 5% SMC	D1, D3, D5	Littelfuse Inc	SMCJ15CA	3	Y	SMC
Fitted	LED SmartLED Green 570NM	D2	OSRAM	LG L29K-G2J1-24-Z	1		0603
Fitted	Diode, Zener, 5.1V, 5W, SMB	D4	Micro Commercial Components	SMBJ5338B-TP	1	Y	SMB
Fitted	Diode, Schottky, 20V, 1A, SMA	D6	Diodes Inc.	B120-13-F	1	Y	SMA
Fitted	Diode, Zener, 39V, 1W, DO41	D7	Micro Commercial Co	1N4754A-TP	1		DO-41
Fitted	Diode, Zener, 16V, 1W, DO41	D8	Micro Commercial Co	1N4745A-TP	1		DO-41
Fitted	Diode, P-N, 1000V, 1A, TH	D9, D10, D11	Fairchild Semiconductor	1N4007	3	Y	DO-41
Fitted	Diode, Switching, 200V, 0.2A, SOT-23	D12	Diodes Inc.	BAS21-7-F	1	Y	SOT-23
Fitted	FERRITE CHIP 1000 OHM 300MA 0603	FB1	TDK Corporation	MMZ1608B102C	1	Y	0603
Fitted	Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3, FID4, FID5, FID6	N/A	N/A	6		Fiducial
Fitted	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	H1, H2, H3, H4	B&F Fastener Supply	NY PMS 440 0025 PH	4	Y	Screw
Fitted	Standoff, Hex, 0.5"L #4-40 Nylon	H5, H6, H8, H9	Keystone	1902C	4	Y	Standoff
Fitted	Mountin hole, NPTH Drill 3.2mm	H7			1		
Fitted	HEATSINK TO-220 W/PINS 1.5"TALL	HS1	Aavid Thermalloy	513102B02500G	1		1.500x1.375in.
Fitted	Header, Male 2x10-pin, 100mil spacing	J1, J11	Sullins	PEC10DAAN	2		0.100 inch x 10 x 2
Fitted	TERMINAL BLOCK 5.08MM VERT 2POS, TH	J3, J6, J12, J16, J17, J18, J19	On-Shore Technology	ED120/2DS	7	Y	TERM_BLK, 2pos, 5.08mm
Fitted	Header, Male 2-pin, 100mil spacing,	J4, J5, J7, J8, J9, J10, J13, J14, J15, J21, J22	Sullins	PEC02SAAN	11		0.100 inch x 2
Fitted	Terminal Block, 3-pin, 15-A, 5.1mm	J20	OST	ED120/3DS	1		0.60 x 0.35 inch
Fitted	Inductor, Common Mode Filter SMD	L1	TDK	ACM2012-900-2P-T002	1		2.00mm x 1.20mm

**Table 11. Bill of Materials (continued)**

Fitted	Description	Designator	Manufacturer	Part Number	Quantity	RoHS	Package Reference
Fitted	Inductor, 220uH .30A SMD	L2	Bourns	SRR7032-221M	1	Y	7x7mm
Fitted	Inductor, Chip, 3.3uH 770MA 1210 10%	L3	EPCOS Inc	B82422H1332K	1		1210
Fitted	1.5A Ferrite Bead, 330 ohm @ 100MHz, SMD	L4	MuRata	BLM18SG331TN1D	1	Y	0603
Fitted	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	Brady	THT-14-423-10	1	Y	PCB Label 0.650"H x 0.200"W
Fitted	MOSFET, N-CH, 30V, 22A, SON 2X2 MM	Q1	TEXAS INSTRUMENTS	CSD17571Q2	1	Y	DQK
Fitted	MOSFET, N-CH, 60V, 50A, TO-220AB	Q5	Texas Instruments	CSD18537NKCS	1	Y	TO-220AB
Fitted	RES, 100 ohm, 1%, 0.1W, 0603	R1, R33, R41, R68	Vishay-Dale	CRCW0603100RFKEA	4	Y	0603
Fitted	RES, 470 ohm, 1%, 0.125W, 0805	R3, R10	Vishay-Dale	CRCW0805470RFKEA	2	Y	0805
Fitted	RES, 300 ohm, 5%, 0.1W, 0603	R4, R37	Vishay-Dale	CRCW0603300RJNEA	2	Y	0603
Fitted	RES, 10k ohm, 5%, 0.1W, 0603	R5, R6, R8	Vishay-Dale	CRCW060310K0JNEA	3	Y	0603
Fitted	RES, 120 ohm, 5%, 0.125W, 0805	R7	Vishay-Dale	CRCW0805120RJNEA	1	Y	0805
Fitted	RES, 10.0 ohm, 1%, 0.1W, 0603	R9	Vishay-Dale	CRCW060310R0FKEA	1	Y	0603
Fitted	RES, 200 ohm, 1%, 0.1W, 0603	R11	Vishay-Dale	CRCW0603200RFKEA	1	Y	0603
Fitted	RES, 63.4k ohm, 1%, 0.1W, 0603	R12	Vishay-Dale	CRCW060363K4FKEA	1	Y	0603
Fitted	RES, 121k ohm, 0.1%, 0.125W, 0805	R13	Yageo America	RT0805BRD07121KL	1	Y	0805
Fitted	RES, 10.0k ohm, 1%, 0.1W, 0603	R14, R22, R28	Vishay-Dale	CRCW060310K0FKEA	3	Y	0603
Fitted	RES, 1.00k ohm, 1%, 0.1W, 0603	R15	Yageo America	RC0603FR-071KL	1	Y	0603
Fitted	RES, 9.76k ohm, 1%, 0.1W, 0603	R16	Vishay-Dale	CRCW06039K76FKEA	1	Y	0603
Fitted	RES, 53.6k ohm, 0.1%, 0.125W, 0805	R17	Susumu Co Ltd	RG2012P-5362-B-T5	1	Y	0805
Fitted	RES, 100k ohm, 1%, 0.1W, 0603	R18, R31	Vishay-Dale	CRCW0603100KFKEA	2	Y	0603
Fitted	RES, 21.5k ohm, 1%, 0.1W, 0603	R19	Vishay-Dale	CRCW060321K5FKEA	1	Y	0603
Fitted	RES, 30k ohm, 5%, 0.1W, 0603	R20, R52	Vishay-Dale	CRCW060330K0JNEA	2	Y	0603
Fitted	RES, 280k ohm, 1%, 0.1W, 0603	R21	Vishay-Dale	CRCW0603280KFKEA	1	Y	0603
Fitted	RES, 10 ohm, 5%, 0.1W, 0603	R23, R27, R61, R62	Vishay-Dale	CRCW060310R0JNEA	4	Y	0603
Fitted	RES, 0 ohm, 5%, 0.1W, 0603	R24, R26, R32, R63, R64, R65	Vishay-Dale	CRCW0603000Z0EA	6	Y	0603
Fitted	RES, 10.0k ohm, 1%, 0.25W, 1206	R25, R29, R34	Vishay-Dale	CRCW120610K0FKEA	3	Y	1206
Fitted	RES, 43.2k ohm, 1%, 0.1W, 0603	R30	Vishay-Dale	CRCW060343K2FKEA	1	Y	0603
Fitted	RES, 1.00Meg ohm, 1%, 0.1W, 0603	R35	Vishay-Dale	CRCW06031M00FKEA	1	Y	0603
Fitted	RES, 10k ohm, 0.01%, 0.063W, 0603	R36, R51	Stackpole Electronics Inc	RNCF0603TKY10K0	2	Y	0603
Fitted	RES, 1.0k ohm, 5%, 0.1W, 0603	R42, R43, R44, R70	Vishay-Dale	CRCW06031K00JNEA	4	Y	0603
Fitted	RES, 1.00k ohm, 1%, 0.25W, 1206	R45, R46	Vishay-Dale	CRCW12061K00FKEA	2	Y	1206
Fitted	RES, 510 ohm, 0.1%, 0.1W, 0603	R47	Susumu Co Ltd	RG1608P-511-B-T5	1	Y	0603
Fitted	RES, 22 ohm, 5%, 0.25W, 1206	R53, R54, R55, R56, R57, R58, R59, R60	Vishay-Dale	CRCW120622R0JNEA	8	Y	1206
Fitted	RES, 47k ohm, 5%, 0.125W, 0805	R66	Panasonic	ERJ-6GEYJ473V	1	Y	0805
Fitted	RES, 470 ohm, 5%, 0.1W, 0603	R69	Vishay-Dale	CRCW0603470RJNEA	1	Y	0603
Fitted	Transformer 475uH SMD	T1	Würth Electronics Midcom	760390015	1	Y	10.05mm L x 6.73mm W
Fitted	Test Point, O.040 Hole	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	STD	STD	40		

Table 11. Bill of Materials (continued)

Fitted	Description	Designator	Manufacturer	Part Number	Quantity	RoHS	Package Reference
Fitted	2.7V, 15.6mV/°C, Temperature Sensor, 3-pin SOT-23	U1	National Semiconductor	LM62BIM3	1	N	MF03A
Fitted	IC, ISOLATED RS-485 PROFIBUS TRANSCEIVER	U2	TI	ISO1176DW	1		SO-16
Fitted	IC, 300-mA 40-V LOW-DROPOUT REGULATOR WITH 25- $\mu$ A QUIESCENT CURRENT	U3	TI	TPS7A6533QKVURQ1	1		PFM
Fitted	100V, 600mA Constant On-Time Synchronous Buck Regulator, DDA0008B	U4	Texas Instruments	LM5017MRE/NOPB	1	Y	DDA0008B
Fitted	IC, DC-DC Converter	U5	TI	TPS55010RTE	1		QFN-16
Fitted	Zero-Drift Programmable Gain Amplifier with MUX	U6	Texas Instruments	PGA11xAIPW	1	Y	TSSOP-20 PW
Fitted	IC, Dual Differential Comparators, 2-36 Vin	U7	TI	LM293AD	1		SO-8
Fitted	IC, Micropower Shunt Voltage Reference 100 ppm/°C, 45 $\mu$ A-12mA, Adjustable	U8	TI	LM4041BIDBZ	1		SOT23
Not Fitted	Header, Male 3-pin, 100mil spacing,	J2	Sullins	PEC03SAAN	0		0.100 inch x 3
Not Fitted	MOSFET, N-CH, 30V, 22A, SON 2X2 MM	Q2, Q3, Q4	TEXAS INSTRUMENTS	CSD17571Q2	0	Y	DQK
Not Fitted	RES, 1.00k ohm, 1%, 0.125W, 0805	R2	Vishay-Dale	CRCW08051K00FKEA	0	Y	0805
Not Fitted	RES, 300 ohm, 5%, 0.1W, 0603	R38, R39, R40	Vishay-Dale	CRCW0603300RJNEA	0	Y	0603
Not Fitted	RES, 22 ohm, 5%, 0.25W, 1206	R48, R49, R50	Vishay-Dale	CRCW120622R0JNEA	0	Y	1206
Not Fitted	RES, 0 ohm, 5%, 0.1W, 0603	R67, R71	Vishay-Dale	CRCW0603000Z0EA	0	Y	0603

## 8 PCB Layout

This design is implemented in 2 layers PCB. For optimal performance of this design follow standard PCB layout guidelines: including proper decoupling capacitors close to all ICs and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC and EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low impedance, low-inductance traces should be used along the output signal path and protection elements. When possible, copper pours are used in place of traces.

### 8.1 Layout Recommendations

In order to achieve a high performance, the following layout guidelines are recommended:

1. Ensure that protection elements such as TVS diodes and capacitors are placed as close to connectors as possible.
2. Use large and wide traces to ensure a low-impedance path for high-energy transients.
3. Place the decoupling capacitors close to supply pin of IC.
4. Use multiple vias for power and ground for decoupling caps.
5. Place the reference capacitor close to the voltage reference.

## 9 Layout Prints

Figure 26 through Figure 33 illustrate the layout prints and some mechanical layout information for the zero drift analog front end PGA and peripherals for MCCB.

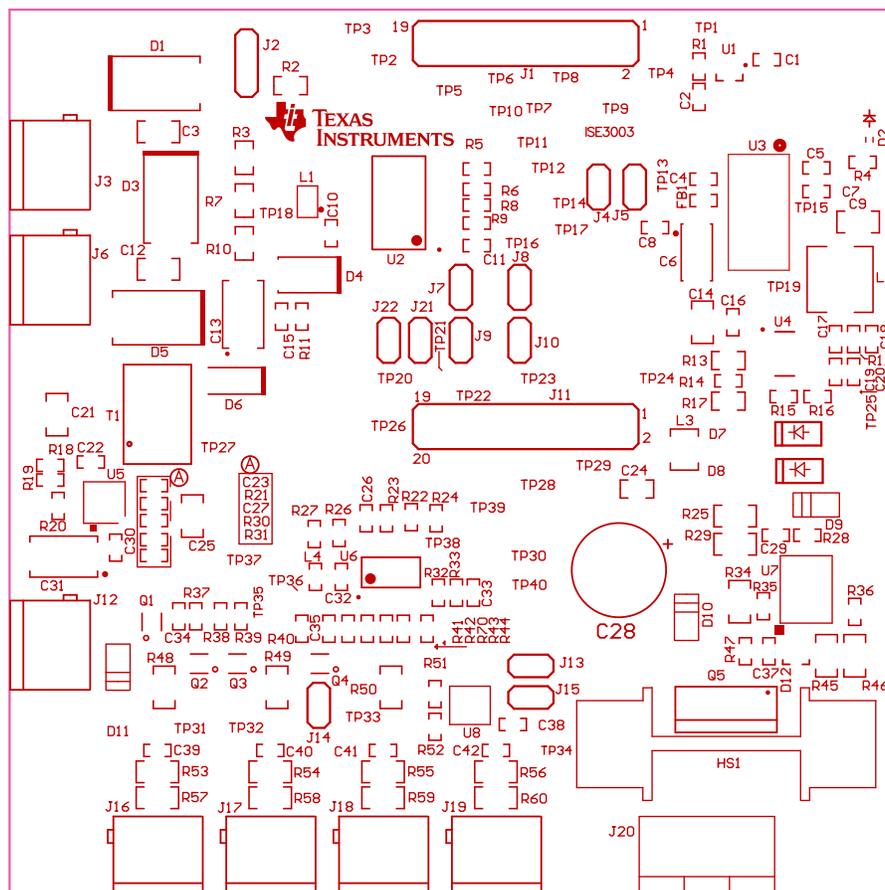


Figure 26. Top Silk Screen

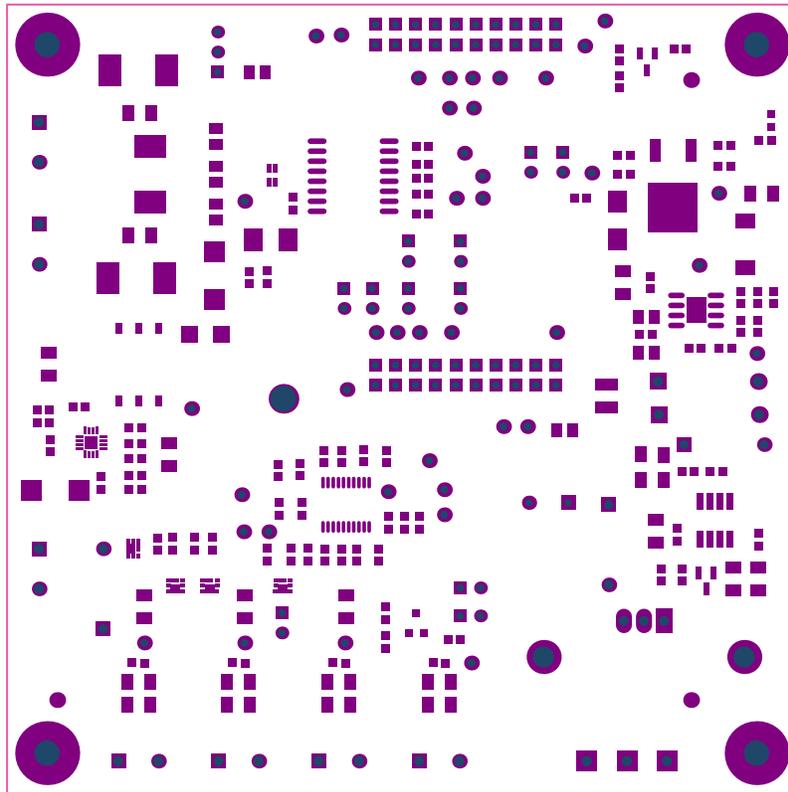


Figure 27. Top Solder Mask

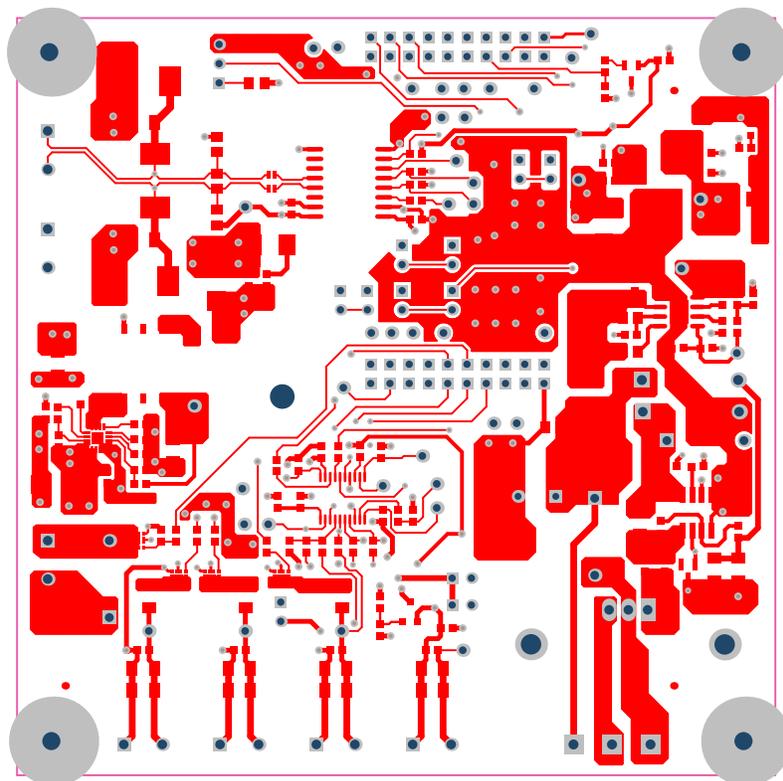
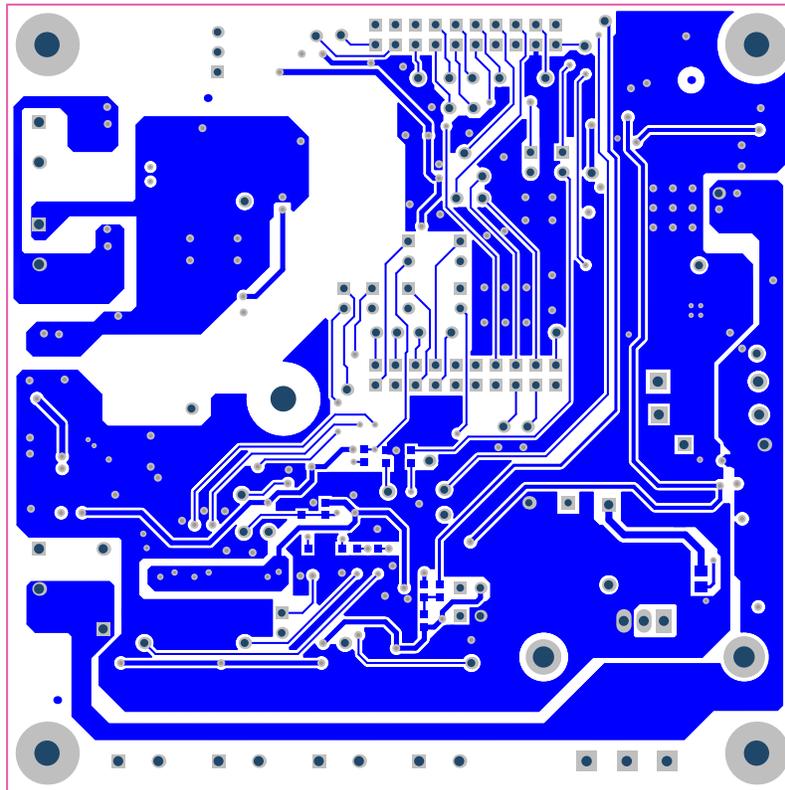
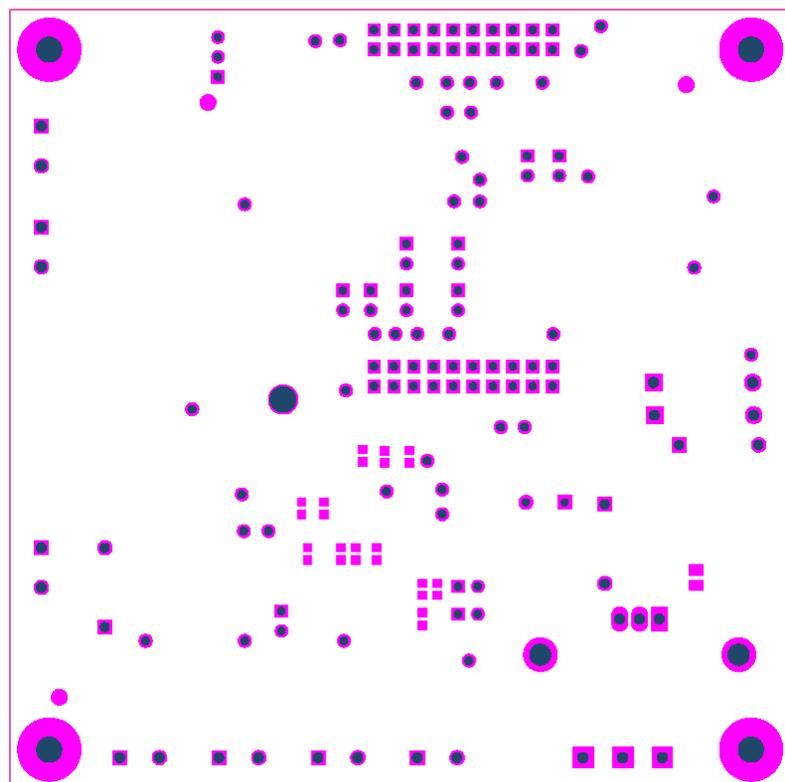


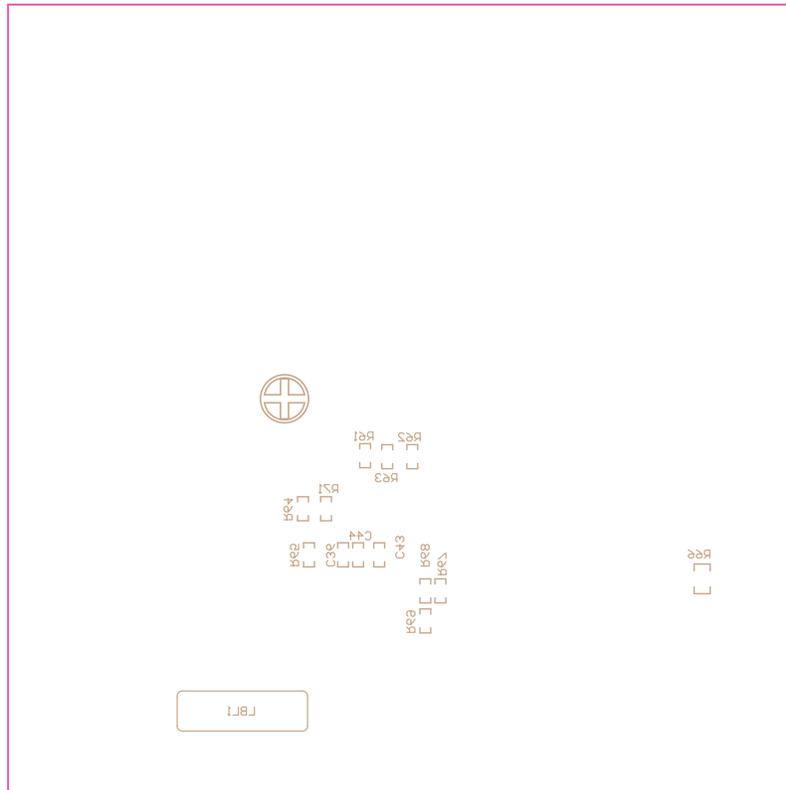
Figure 28. Top Layer



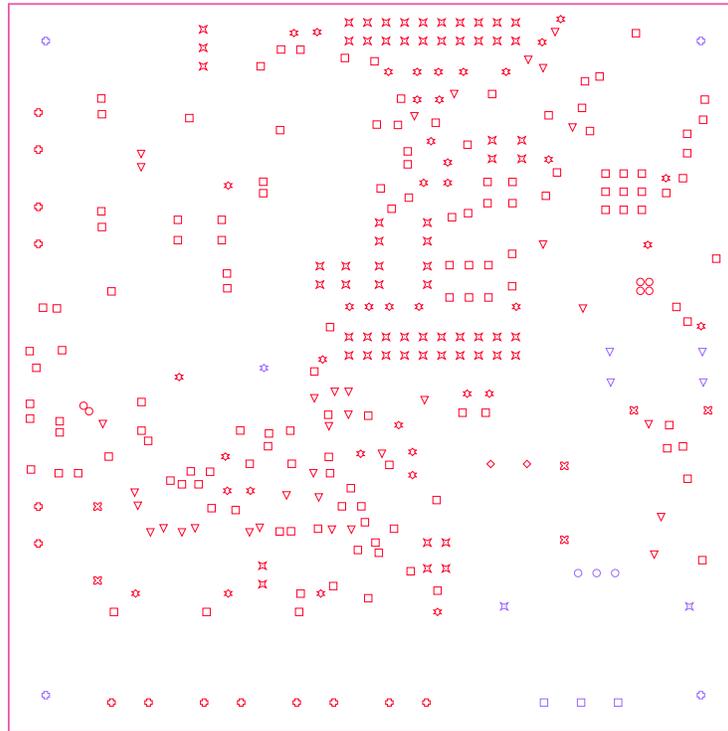
**Figure 29. Bottom Layer**



**Figure 30. Bottom Solder Mask**



**Figure 31. Bottom Silk Screen**

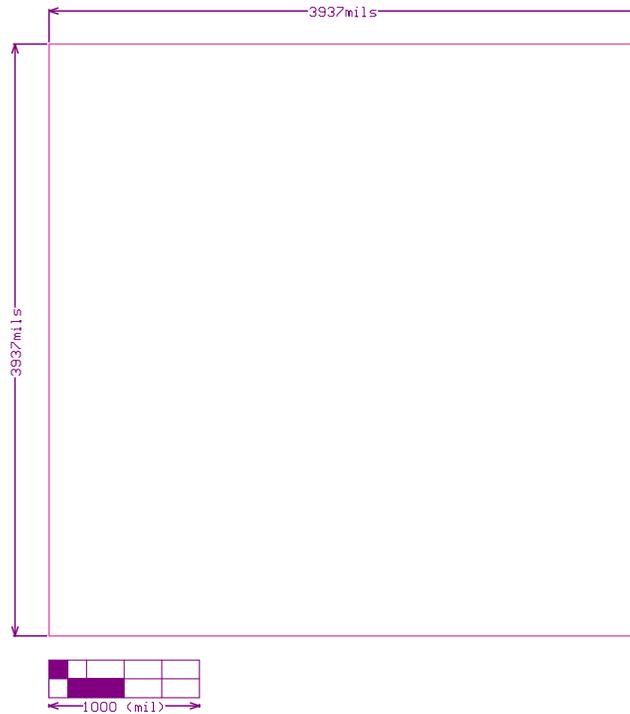


Symbol	Hit Count	Tool Size	Plated	Hole Type
○	6	12mil (0.305mm)	PTH	Round
▽	34	16mil (0.406mm)	PTH	Round
□	134	20mil (0.508mm)	PTH	Round
◇	2	36mil (0.914mm)	PTH	Round
⊠	65	38mil (0.965mm)	PTH	Round
☆	40	40mil (1.016mm)	PTH	Round
⊠	6	45.276mil (1.15mm)	PTH	Round
⊕	14	49.213mil (1.25mm)	PTH	Round
○	3	50mil (1.27mm)	PTH	Round
▽	4	51mil (1.295mm)	PTH	Round
□	3	52mil (1.321mm)	PTH	Round
⊠	2	106.5mil (2.705mm)	PTH	Round
⊕	4	125.984mil (3.2mm)	PTH	Round
☆	1	128mil (3.251mm)	NPTH	Round
	318 Total			

Drill Table

DRILL TOLERANCES: FOR PTH +/-3MILS  
FOR NPTH +/-2MILS

**Figure 32. Drill Drawing**



**Figure 33. Mechanical Dimensions**

**10 Altium Project**

To download the Altium Project files for the board, see the design files at: [www.ti.com/tool/TIDA-00130](http://www.ti.com/tool/TIDA-00130).

**11 Gerber files**

To download the Gerber files for the board, see the design files at: [www.ti.com/tool/TIDA-00130](http://www.ti.com/tool/TIDA-00130).

## Revision History

<b>Changes from Original (March 2014) to A Revision</b>	<b>Page</b>
• Added one bullet to the end of the design features list.....	1
• Deleted last column from <i>Comparison of Different Op Amps and PGAs with Critical Characteristics</i> table. ....	5
• Changed entire title and contents of Offset Variation over Temperature table, now titled DC offset Drift with Reference to 25°C.....	16

## IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

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