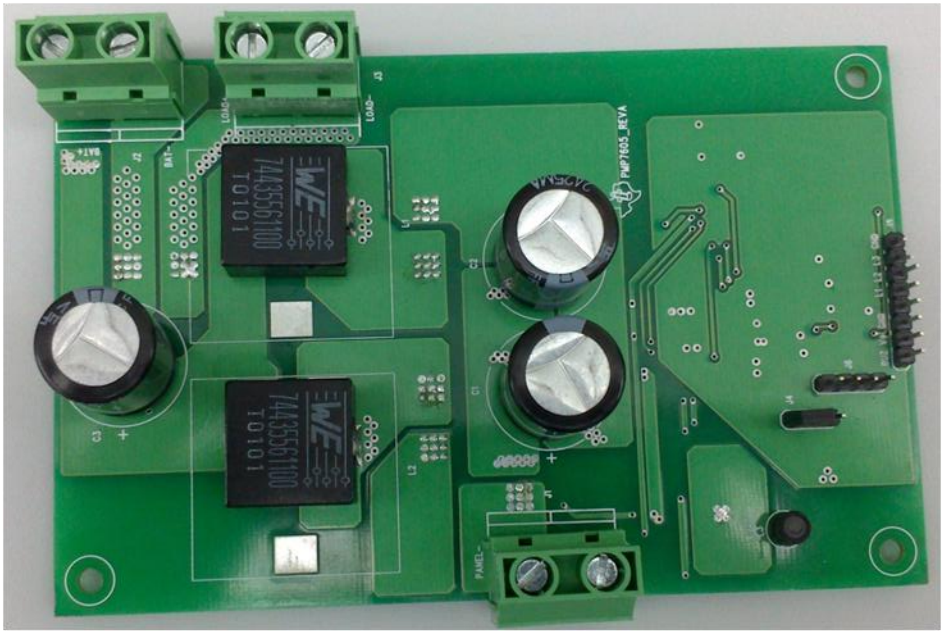
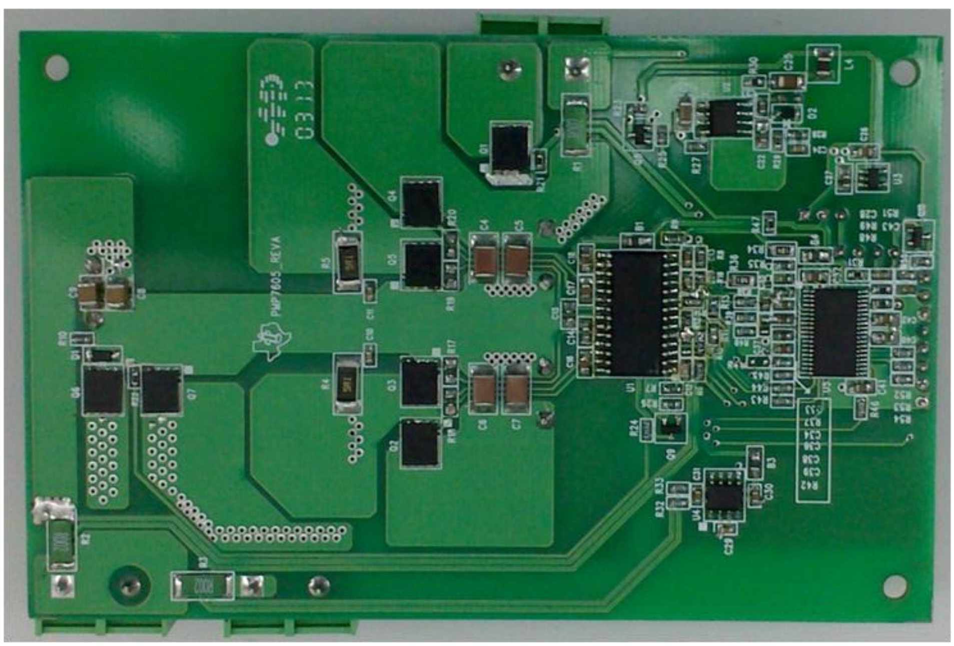
TEST REPORT OF MPPT CHARGE CONTROLLER

PMP 7605





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I. INTRODUCTION

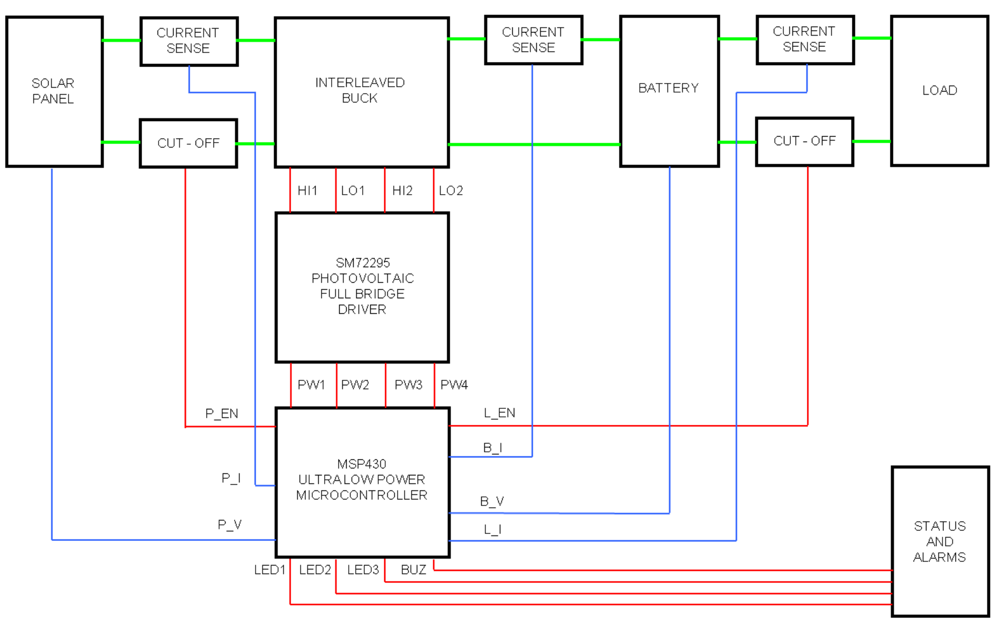
The following document is a compilation of test results of the PMP7605 reference design, a 20A MPPT solar charge controller. The test results are taken with simulated solar panel input corresponding to 12V and 24V panels.

II. DESCRIPTION

The PMP7605 is developed around the MSP430F5132 controller IC. The design is targeted for small and medium power solar charger solutions. The present design is capable of operating with 12V/24V panels and 12V/24V batteries with up to 20A output current. However, it can be easily adapted to 48V systems by just changing the MOSFETs to 100V rated parts. Also, it is possible to increase the current to 40A by using TO-220 package version of the same MOSFETs used in the design. The design has an operating efficiency of above 97% at full load in a 24V system. For 12V systems the efficiency is above 96%. This efficiency figure includes the losses in battery reverse protection MOSFET and panel reverse flow protection MOSFET, which are part of the design. The high efficiency is the result of the low gate charge MOSFETs from TI used in the design, and the interleaved buck topology used. The interleaved buck topology reduces the component stresses by a great extent. Another feature is the relatively small sized components used, possible due to the high operating frequency (~200 KHz per stage). The design has built-in battery charge profiles for 12V and 24V Lead acid batteries. The circuit takes only under 10mA of standby current while operating from battery. There is also a provision to connect a load to the battery with overload and short circuit cut-off built in. The design presently uses 'perturb and observe' algorithm for MPP tracking. This gives fast acquisition of MPP operation. Software programmable alarms and indications are provided in hardware, but are left non-configured.

Surge protection and EMI filtering components are not present on this design, and has to be added depending upon required specification levels.

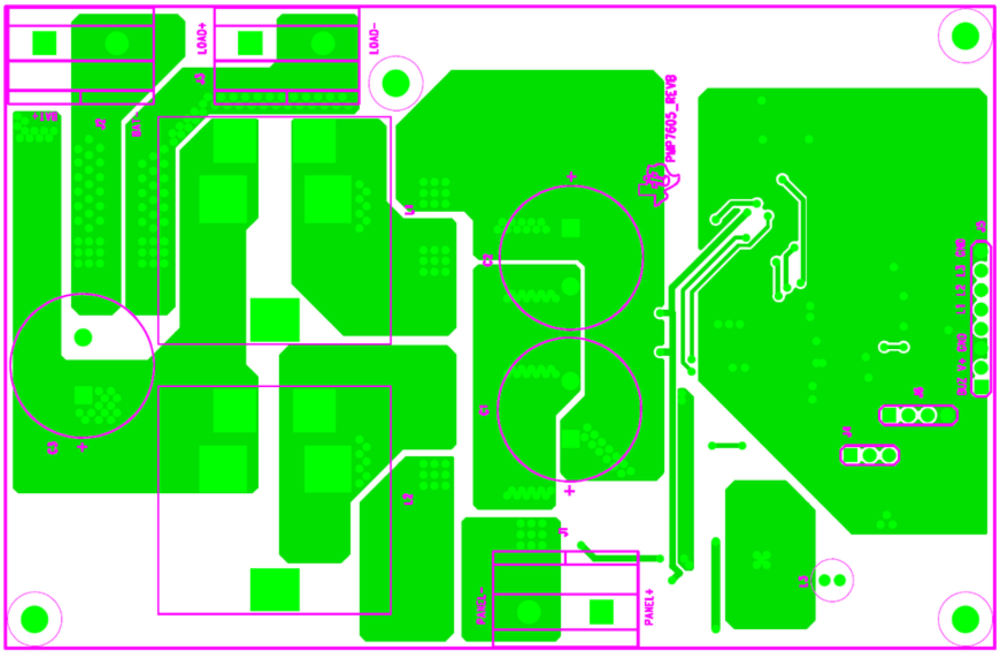
III. BLOCK DIAGRAM

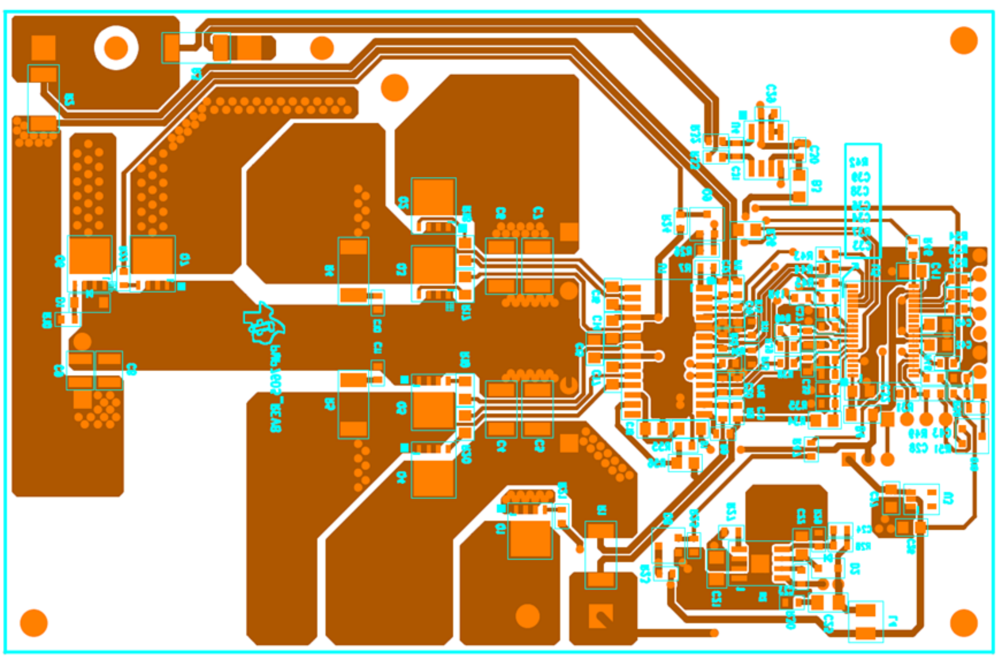


IV. SPECIFICATIONS

Input Voltage Range: 15VDC - 44VDC
Output: 12V or 24V battery
Output Current: 20A max.
Board Form Factor: 130 mm x 84 mm x 22 mm
Expected efficiency: >95%

V. BOARD LAYOUT AND ASSEMBLY





VI. TEST SETUP

Input conditions:
Panel input: 15VDC to 22VDC for 12V system or 30VDC to 44VDC for 24V system
Set current limit to the short circuit current of panel when DC source is used instead of panel

Output:
Electronic load in CV mode to simulate battery or 12/24V battery

Equipment Used:
1. Current limited DC source simulating solar panel
2. Digital Oscilloscope
3. Multimeters
4. Electronic load

Procedure:
1. Connect appropriate battery or electronic load in CV mode to the BAT+ and BAT- terminals of the PMP7605 reference board, maintaining correct polarity.
2. Connect panel or current limited DC source to PANEL+ and PANEL- terrminals, maintaining correct polarity.
3. Set the output voltage of DC source to slightly above the MPP voltage of the panel being simulated (if DC source is used instead of panel) and turn on.
4. Observe for gradual build-up of output current.

VII. TEST DATA

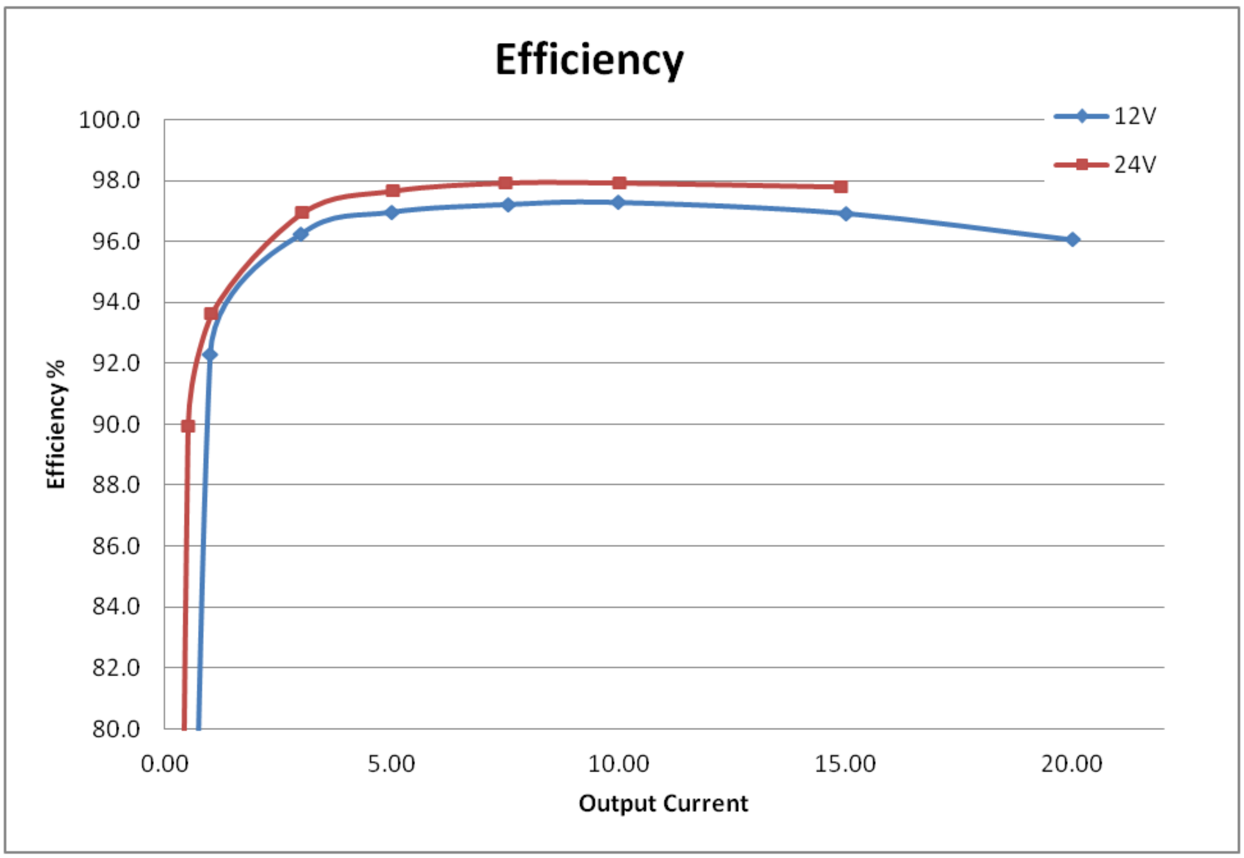
a. 12V SYSTEM PERFORMANCE

Vi (V)	Ii (A)	Vo (V)	Io (A)	Pi (W)	Po (W)	Efficiency (%)
17.70	0.01	0.00	0.00	0.14	0.00	0.0
17.01	0.76	12.01	0.99	12.93	11.93	92.3
17.16	2.19	12.05	3.00	37.58	36.17	96.2
17.27	3.61	12.09	5.00	62.34	60.46	97.0
17.52	5.40	12.15	7.57	94.61	91.98	97.2
17.42	7.20	12.20	10.00	125.42	122.03	97.3
17.33	11.00	12.32	15.00	190.63	184.79	96.9
17.19	15.06	12.44	20.00	258.88	248.70	96.1

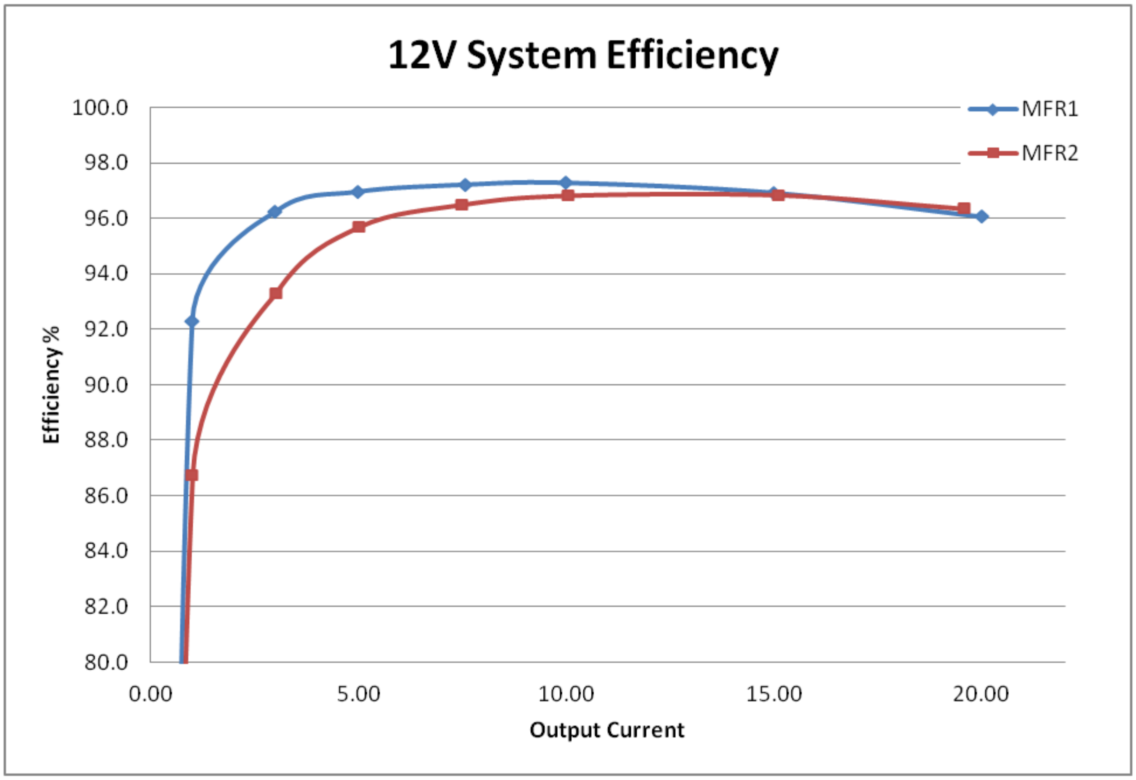
b. 24V SYSTEM PERFORMANCE

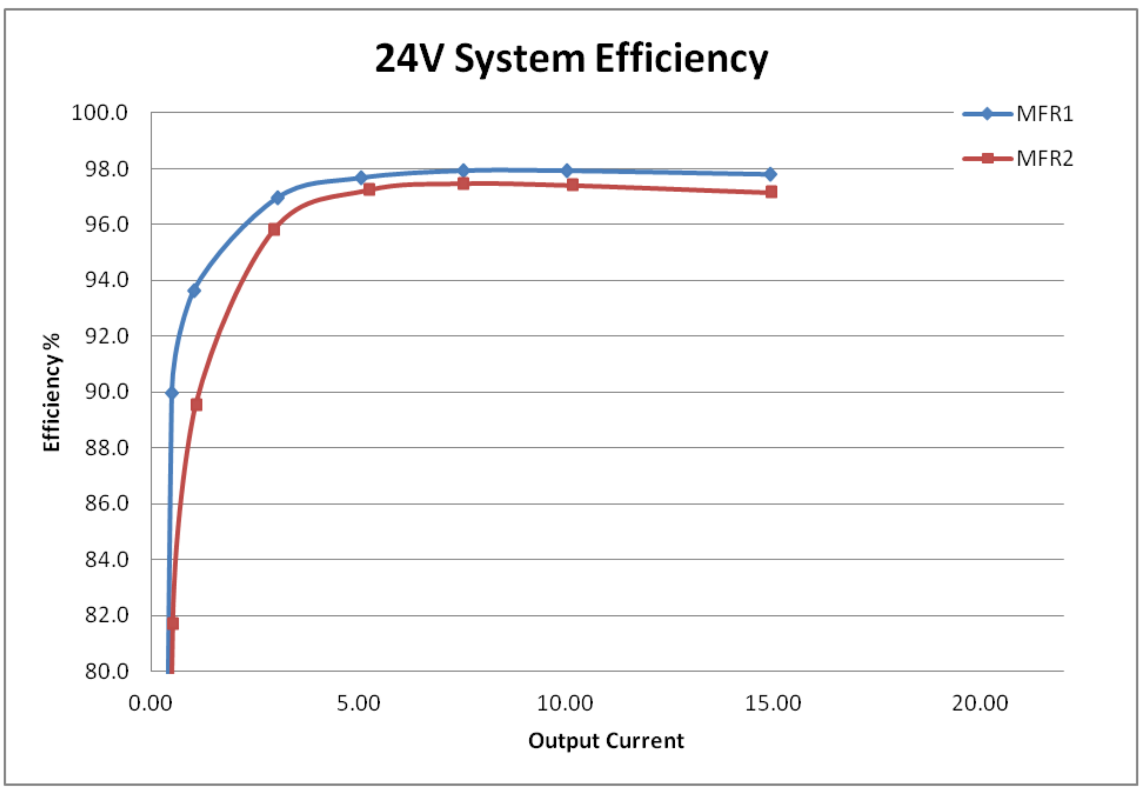
31.50	0.01	0.00	0.00	0.16	0.00	0.0
31.40	0.43	24.00	0.51	13.50	12.14	89.9
31.44	0.84	24.01	1.03	26.41	24.73	93.6
31.36	2.40	24.05	3.03	75.26	72.96	96.9
31.34	3.97	24.09	5.04	124.42	121.52	97.7
31.29	5.92	24.15	7.51	185.24	181.40	97.9
31.23	7.93	24.20	10.02	247.65	242.52	97.9
31.10	11.92	24.32	14.91	370.71	362.55	97.8

c. PLOTS



Efficiency can be dependent on the type of inductor used. The following plots indicate efficiency change with inductor type:

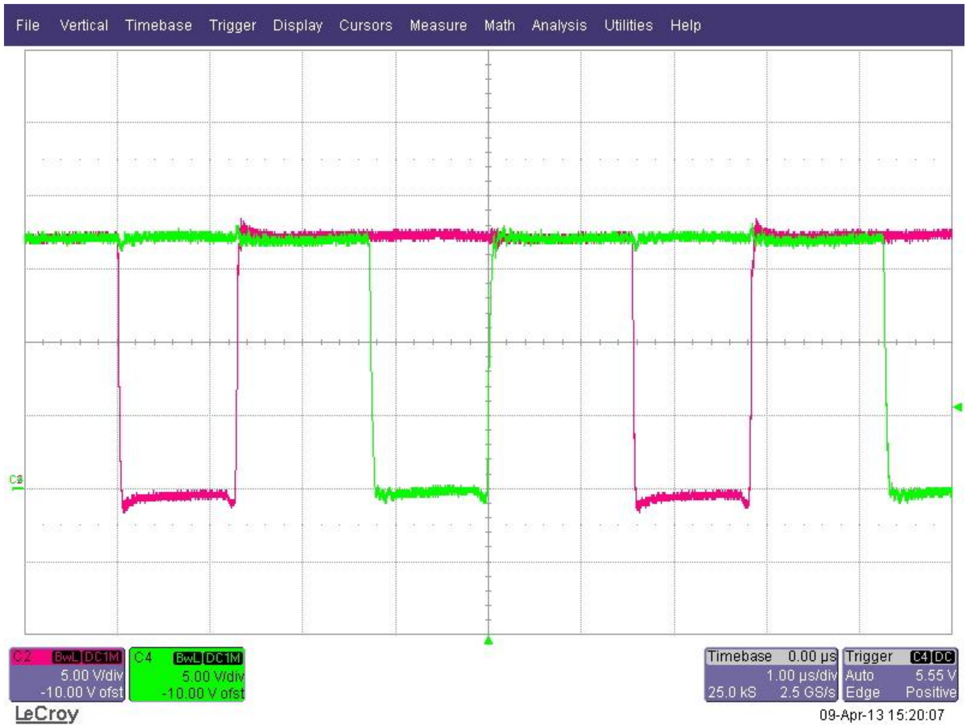

12V System Efficiency
Efficiency %
100.0
98.0
96.0
94.0
92.0
90.0
88.0
86.0
84.0
82.0
80.0
0.00
5.00
10.00
15.00
20.00
Output Current
MFR1
MFR2


24V System Efficiency
Efficiency %
100.0
98.0
96.0
94.0
92.0
90.0
88.0
86.0
84.0
82.0
80.0
0.00
5.00
10.00
15.00
20.00
Output Current
MFR1
MFR2

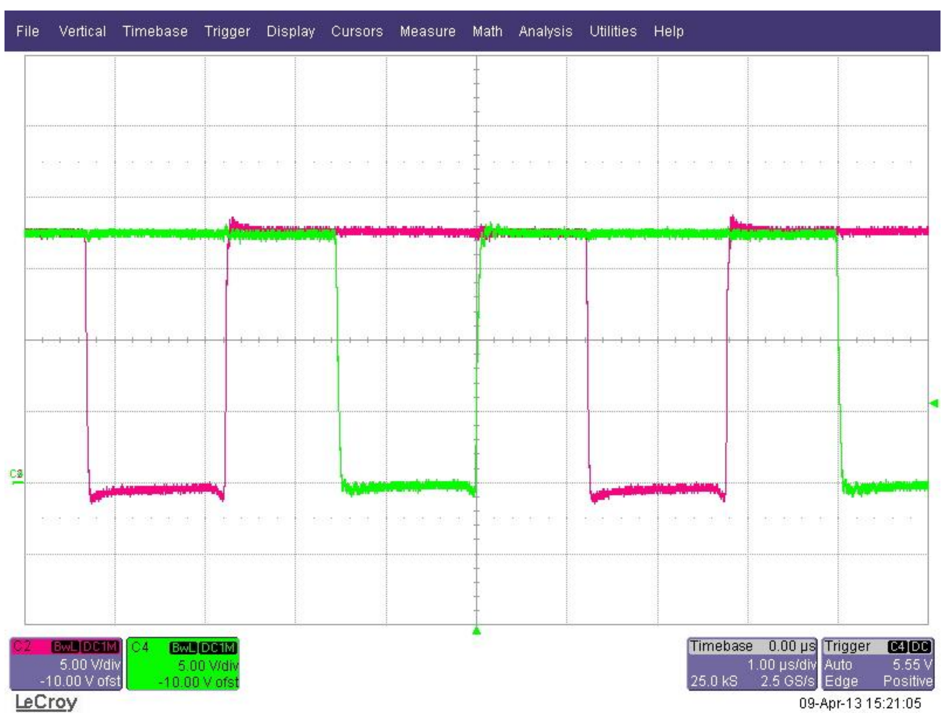
VIII. WAVEFORMS

a. Switching Node Waveforms

12V System, 20A Load. Individual channel switch nodes show interleaved operation



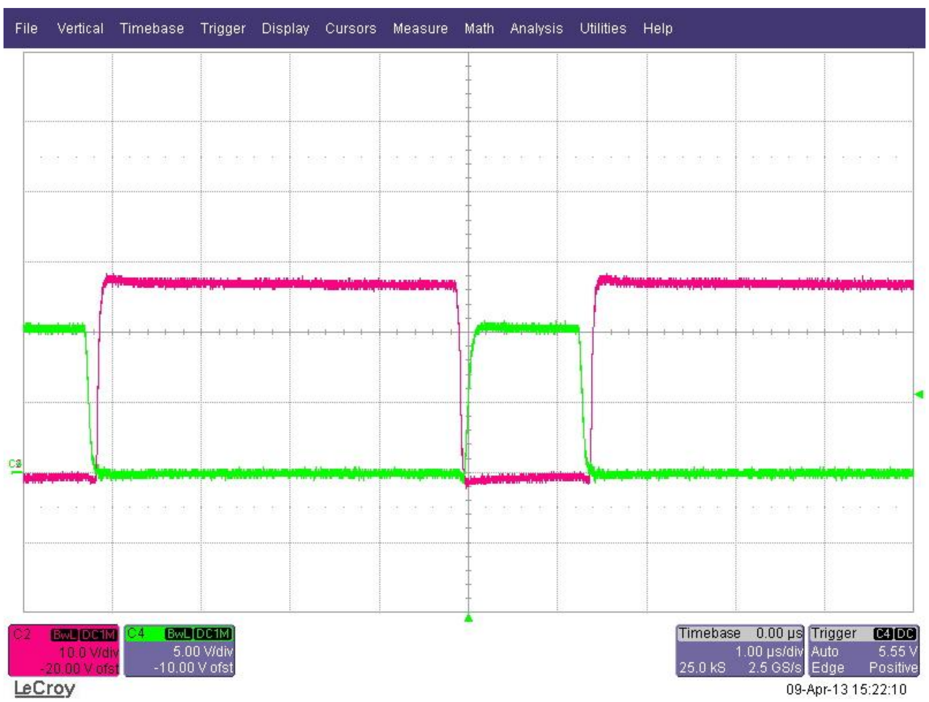
12V System, 10A Load. Individual channel switch nodes show interleaved operation



24V System, 15A Load. Individual channel switch nodes show interleaved operation

b. Gate waveforms

12V System, 20A Load. Top and bottom gate waveforms show dead-time implementation

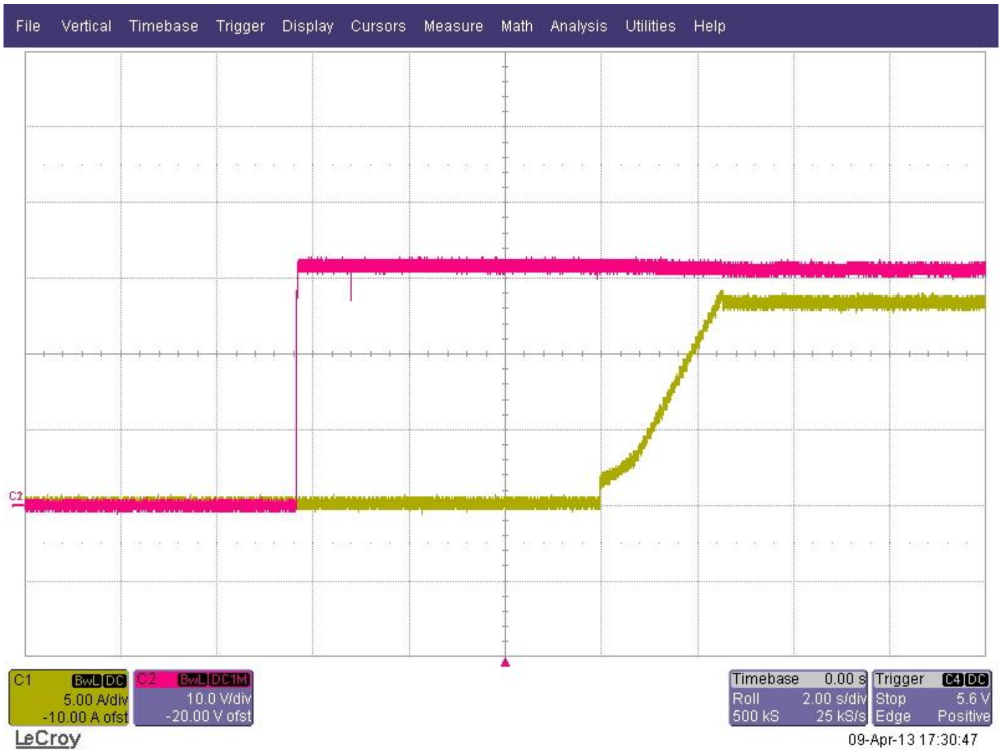


24V System, 15A Load. Top and bottom gate waveforms show dead-time implementation

c. MPP Acquisition

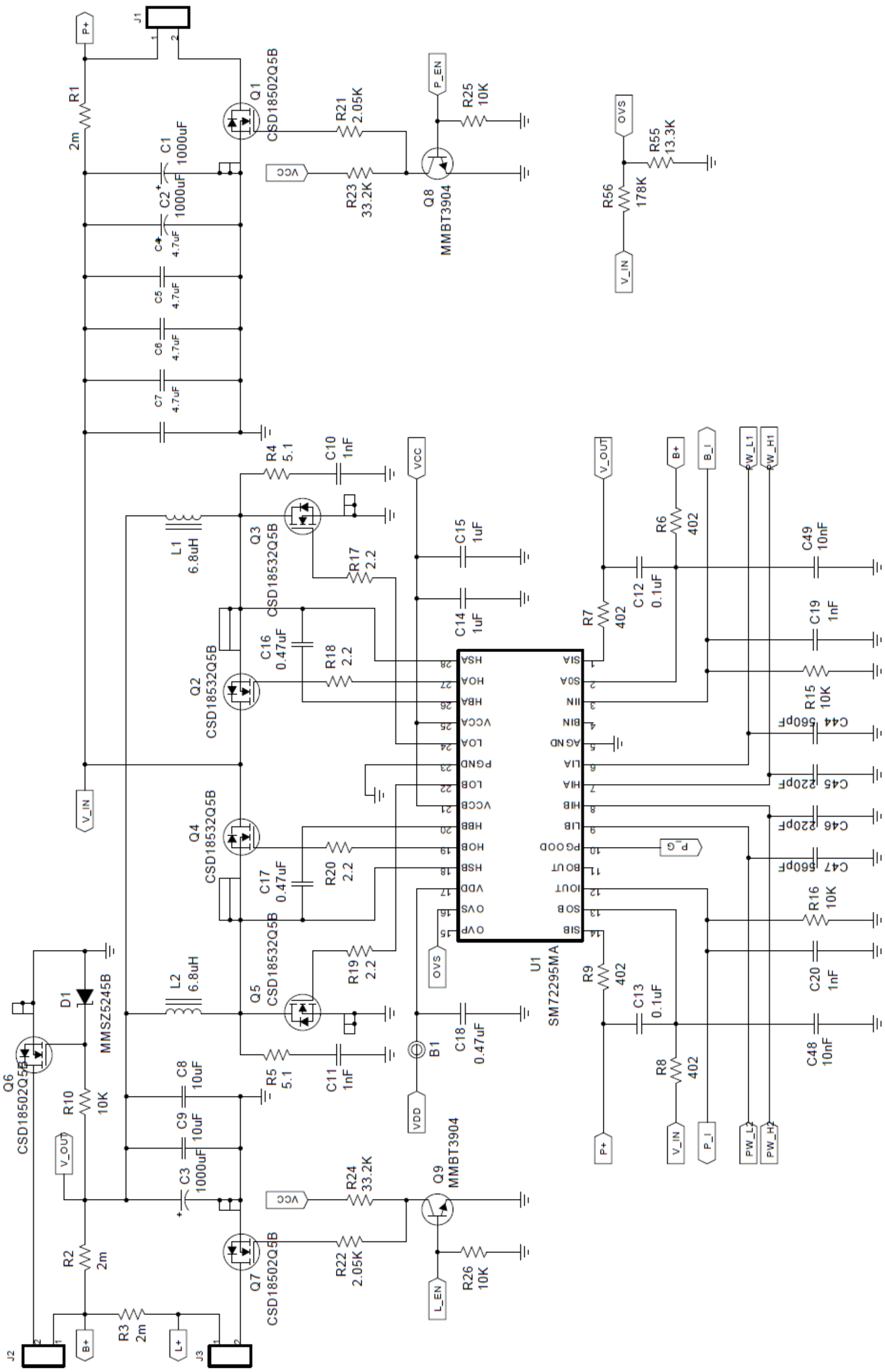
12V System, 20A Load. Red: Input voltage, Yellow: Output current

24V System, 15A Load. Red: Input voltage, Yellow: Output current

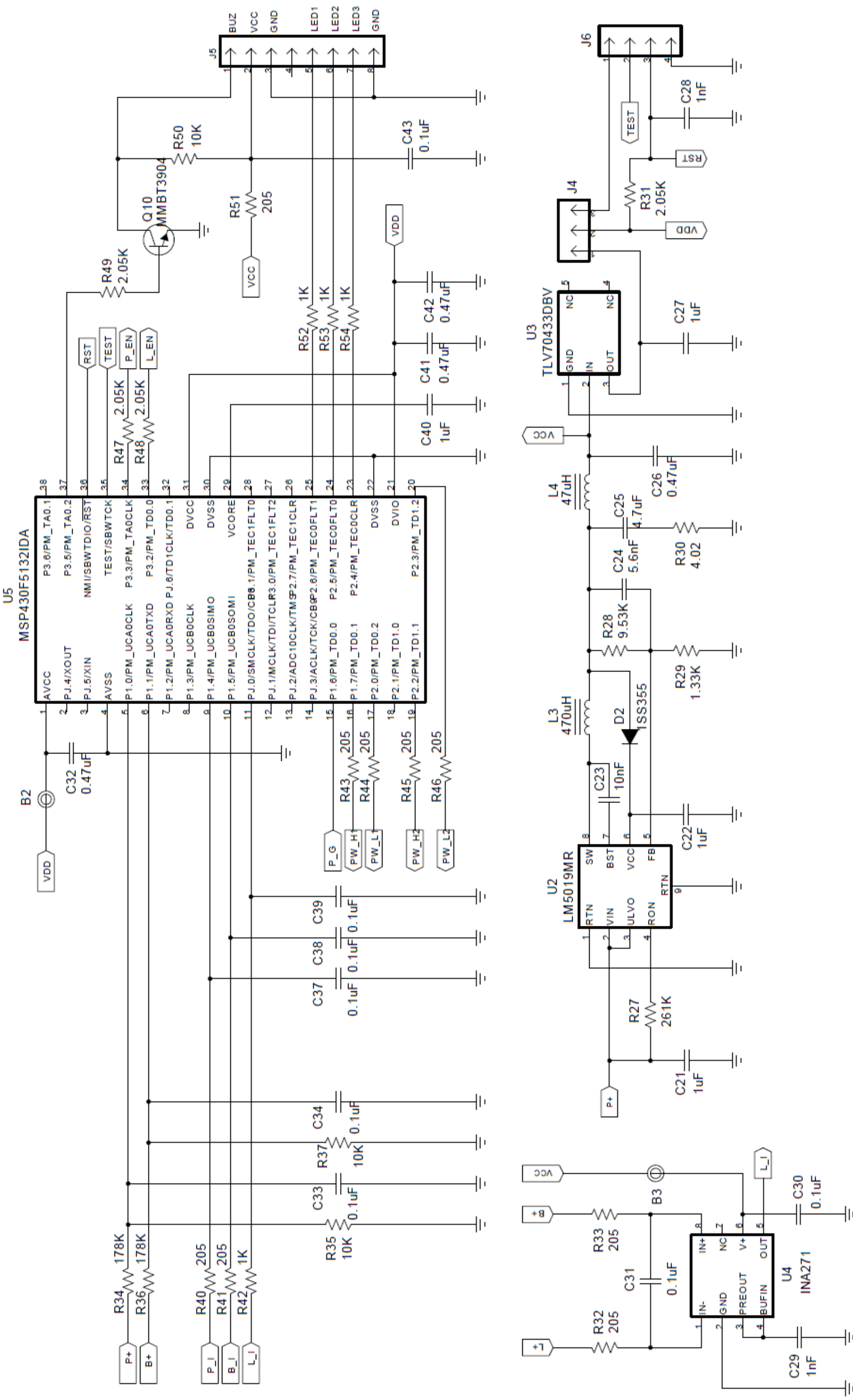


IX. SCHEMATIC

a. Power Stage



b. Controller and Bias Supply



X. BILL OF MATERIALS

(All non-TI parts' costs (except Coilcraft) from DigiKey, TI parts from ti.com)

PMP7605 BOM Revision C										
Item	Qty	Reference	Value	Description	Part Number	Manufacturer	Part_Number	Size	1K Web Price	Total (US$)
1	3	B1, B2, B3		Bead, Ferrite, 500mA		Bourns	MU2029-301Y	805	0.017	0.050
2	3	C1, C2, C3	1000uF	Capacitor, 50V, Low ESR, ±20%		Nichicon	UHE1H102MHD3	18 x 20 mm	0.567	1.701
3	4	C4, C5, C6, C7	4.7uF	Capacitor, Ceramic Chip, 100V, X7S, ±10%		TDK	C4532X7S2A475M230K	1812	0.525	2.100
4	2	C8, C9	10uF	Capacitor, Ceramic, 50V, X7R, 20%		Taiyo-Yuden	UMK325AB7106MM-T	1210	0.208	0.416
5	6	C10, C11, C19, C20, C28, C29	1nF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	603	0.003	0.020
6	10	C12, C13, C30, C31, C33, C34, C37, C38, C39, C43	0.1uF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	603	0.005	0.050
7	5	C14, C15, C22, C27, C40	1uF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	805	0.018	0.089
8	7	C16, C17, C18, C26, C32, C41, C42	0.47uF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	805	0.021	0.147
9	1	C21	1uF	Capacitor, Ceramic Chip, 100V, ±10%		Taiyo-Yuden	HMK316B7105KL-T	1206	0.110	0.110
10	3	C23, C48, C49	10nF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	603	0.002	0.006
11	1	C24	5.6nF	Capacitor, Ceramic, 50V, X7R, 5%		Std	Std	603	0.004	0.004
12	1	C25	4.7uF	Capacitor, Ceramic Chip, 50V, ±10%		Taiyo-Yuden	UMK316AB7475KL-T	1206	0.059	0.059
13	2	C44, C47	560pF	Capacitor, Ceramic, 50V, NPO, 1%		Std	Std	603	0.014	0.028
14	2	C45, C46	220pF	Capacitor, Ceramic, 50V, NPO, 1%		Std	Std	603	0.003	0.007
15	1	D1	MMSZ5245B	Diode, Zener, 500mW, 15-V		Diodes	MMSZ5245B-7-F	SOD123	0.042	0.042
16	1	D2	1SS355	Diode, Switching, 90V, 225 mA Ifm, High speed		Rohm	1SS355	SOD-323	0.040	0.040
17	3	J1, J2, J3	OSTT7020150	Terminal Block, 2-pin, 32-A, 9.5mm		OST	OSTT7020150	0.75 x 0.49 inch	0.576	1.728
18	1	J4	S1012E-36-ND	Header, Male 3-pin, 100mil spacing, (36-pin strip)		Sullins	S1012E-36-ND	0.100 inch x 3	0.063	0.063
19	1	J5	S1012E-36-ND	Header, Male 8-pin, 100mil spacing, (36-pin strip)		Sullins	S1012E-36-ND	0.100 inch x 8	0.168	0.168
20	1	J6	S1012E-36-ND	Header, Male 4-pin, 100mil spacing, (36-pin strip)		Sullins	S1012E-36-ND	0.100 inch x 4	0.084	0.084
21	2	L1, L2	10uH	Inductor, SMT Power, 20A, 1.5 milliohm		Coilcraft	SER2915L-103KL	1.100 x 1.100 inch	1.930	3.860
22	1	L3	470uH	Inductor, Radial , ±10%		Bourns	RLB0608-471KL	0.354 x 0.480 inch	0.095	0.095
23	1	L4	47uH	Inductor, 110mA, 0.95ohm		Taiyo-Yuden	CB2518T470K	0.150 x 0.150 inch	0.077	0.077
24	3	Q1, Q6, Q7	CSD18502Q5B	MOSFET, N-Chan, 40V, 100A, 2.3 milli-ohm		Texas Instruments	CSD18502Q5B	QFN-8 POWER	1.010	3.030
25	4	Q2, Q3, Q4, Q5	CSD18532Q5B	MOSFET, N-Chan, 60V, 100A, 3.2 milli-ohm		Texas Instruments	CSD18532Q5B	QFN-8 POWER	1.010	4.040
26	3	Q8, Q9, Q10	MMBT3904	Bipolar, NPN, xx-V, yy-mA, zz-W		On Semi	MMBT3904LT1	SOT23	0.022	0.066
27	3	R1, R2, R3	2m	Resistor, 2 milliOhm, 3W, 1%		Riedon	CSR2512C-0R002F1	2512	0.183	0.550
28	2	R4, R5	5.1	Resistor, 5.1 Ohm, 1W, 5%		Std	Std	2512	0.054	0.108
29	4	R6, R7, R8, R9	402	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.011
30	8	R10, R15, R16, R25, R26, R35, R37, R50	10K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.021
31	4	R17, R18, R19, R20	2.2	Resistor, Chip, 1/10W, 1%		Std	Std	805	0.004	0.017
32	6	R21, R22, R31, R47, R48, R49	2.05K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.016
33	2	R23, R24	33.2K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.005
34	1	R27	261K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.003
35	1	R28	9.53K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.003
36	1	R29	1.33K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.003
37	1	R30	4.02	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.004	0.004
38	9	R32, R33, R40, R41, R43, R44, R45, R46, R51	205	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.002	0.021
39	3	R34, R36, R56	178K	Resistor, Chip, 1/10W, 1%		Std	Std	805	0.004	0.011
40	4	R42, R52, R53, R54	1K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.002	0.010
41	1	R55	13.3K	Resistor, Chip, 1/16W, 1%		Std	Std	603	0.003	0.003
42	1	U1	SM72295MA	IC, Photovoltaic Full Bridge Driver		TI	SM72295MA	SO	1.900	1.900
43	1	U2	LM5019MR	IC, 100 V, 100 mA Constant On-Time Synchronous Buck Regulator		TI	LM5019MR	PSOP-8	1.250	1.250
44	1	U3	TLV70433DBV	IC, 24-V Input, 150 mA, Utralow IQ LDO Regulator		TI	TLV70433DBV	SOT-23	0.250	0.250
45	1	U4	INA271	IC, Voltage Output, Unidirectional Current-Shunt Monitor		TI	INA271AID	SO-8	0.500	0.500
46	1	U5	MSP430F5132IDA	IC, Mixed Signal Microcontroller		TI	MSP430F5132IDA	MSOP-38	1.250	1.250
							Total EBOM @1K (US$)			24.013

XI. CONCLUSION

The board is tested for the given specifications and found to meet them. Further optimization of software can be done depending on specific system requirements.

XII. APPENDIX

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

For Feasibility Evaluation Only, in Laboratory/Development Environments. The EVM is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

Certain Instructions. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output ranges are maintained at nominal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be indentified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate TI components for possible use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.