

TI Designs

8-Channel Digital Input Module for Programmable Logic Controllers (PLCs)



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Design Resources

TIDA-00017	Design Folder
TIDA-00123	IO Controller Design Files
SN65HVS885	Product Folder
ISO7141CC	Product Folder
ISO7131CC	Product Folder
LM5017	Product Folder
TPS71533	Product Folder
LM5069	Product Folder
CSD18537NQ5A	Product Folder



Design Features

- 8 channel digital input module
- Voltage Inputs: 24-VDC range, limited to 2 mA per channel
- Input protection circuitry and integrated 15-kV ESD protection
- Tested to IEC61000-4 for ESD, EFT, and Surge
- Integrated over-temperature indicator to disconnect inputs when fault conditions occur
- Onboard isolated power supplies
- Galvanic isolation on data and SPI data up to 4242-volts peak
- Pluggable to IO Controller for easy evaluation ([TIDA-00123](#))
- Slim form factor 95 x 50x 10mm (LxWxH)

Featured Applications

- Programmable Logic Controllers digital input modules
- Distributed Control Systems
- Motor drive digital inputs

Block Diagram

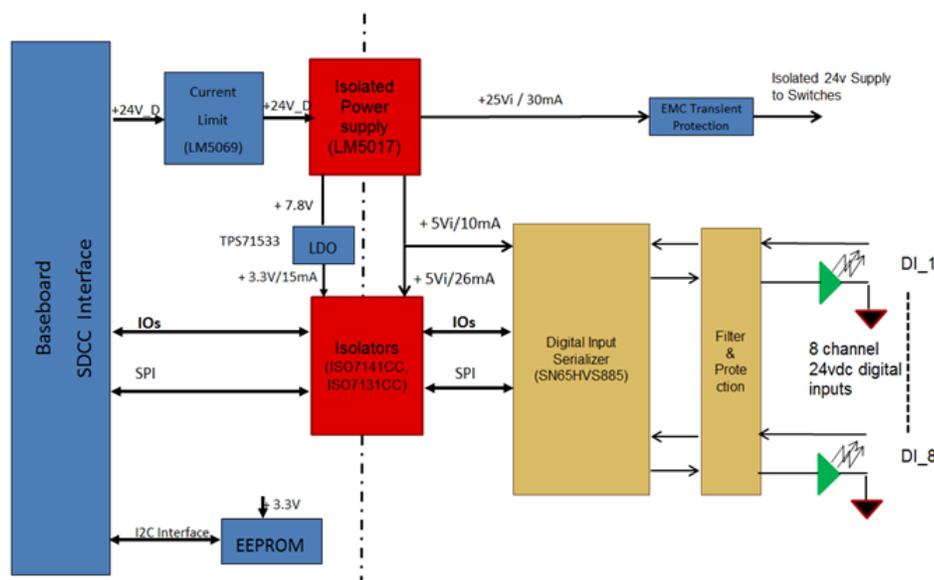


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1 System Description

1.1 Introduction

This TI Design provides a complete Programmable Logic Controller (PLC) 8-channel digital input module front-end reference design. TI has designed and fully tested this controller to meet IEC61000-4 EMC and surge requirements for industrial automation systems. The design serializes 8 digital inputs, up to 34 volts each, minimizing the number of isolation channels and GPIO pins required of the host interface. The design provides LEDs for each input indicating valid input connections. Each input acts as a current controlled sink limited to 2 mA. Each input implements an integrated debounce filter of 3 ms to ensure that spurious noise on the digital inputs do not impact the integrity of the data latched into the shift register. An engineer can program both the current limit and debounce filter duration with external components. The design galvanically isolates serialized data and control signals from the PLC using TI's high-speed, 4242-volt peak, digital isolator technology. The design also includes an over-current protected, isolated power supply providing all necessary module voltages. This design provides an integrated over-temperature indicator, allowing an engineer to place the inputs into a high impedance state if fault conditions exist. The design includes ESD protection and input filters as well. Full documentation, test results, design files, and all the necessary firmware are also available for this design.

2 Design Features

- 8 digital inputs, capable of connecting to input voltages up to 36 volts, serialized to a single output to minimize isolation components and use of GPIO pins
- Fully tested to comply with IEC61000-4 for ESD, EFT, and Surge
- Designed with input protection circuitry and integrated 15-kV ESD protection
- 8 input-status LEDs indicating valid input connections
- Each input implements a user-programmable current limit of 2 mA to protect from over current, while limiting power consumption
- Selectable debounce filters of 3ms implanted for each input ensuring valid input levels are latched into the shift register and output to the PLC host
- High-speed, galvanic isolated SPI interface capable of speeds up to 20 MHz
- Serialized data and SPI control interface galvanically isolated up to 4242-volts peak
- Integrated over-temperature indicator to disconnect inputs when fault conditions occur
- On-board isolated, multi-rail Fly-Buck™ power supply with inrush current protection provides necessary voltage rails to the isolated field side from the host PLC 24-volt power supply
- Slim form factor 95 x 50x 10mm (LxWxH)
- Compatible with TI's SmartIO™ Evaluation Platform

EMC

Test	Levels
IEC61000-4-2: Electro Static Discharge	4kV, Criteria B
IEC61000-4-4 : Electrical Fast Transients	2kV, Criteria B
IEC61000-4-5 : Surge	1kV, Criteria B

3 Block Diagram

The Digital Input Module has the following Block level design:

1. Protection and Filter at Field Inputs
2. Digital Input Serializer
3. Isolated Power and Communication Interface
4. Hot swap controller
5. Nonisolated 3.3-V power supply
6. Isolated 25-V and 5-V power supply

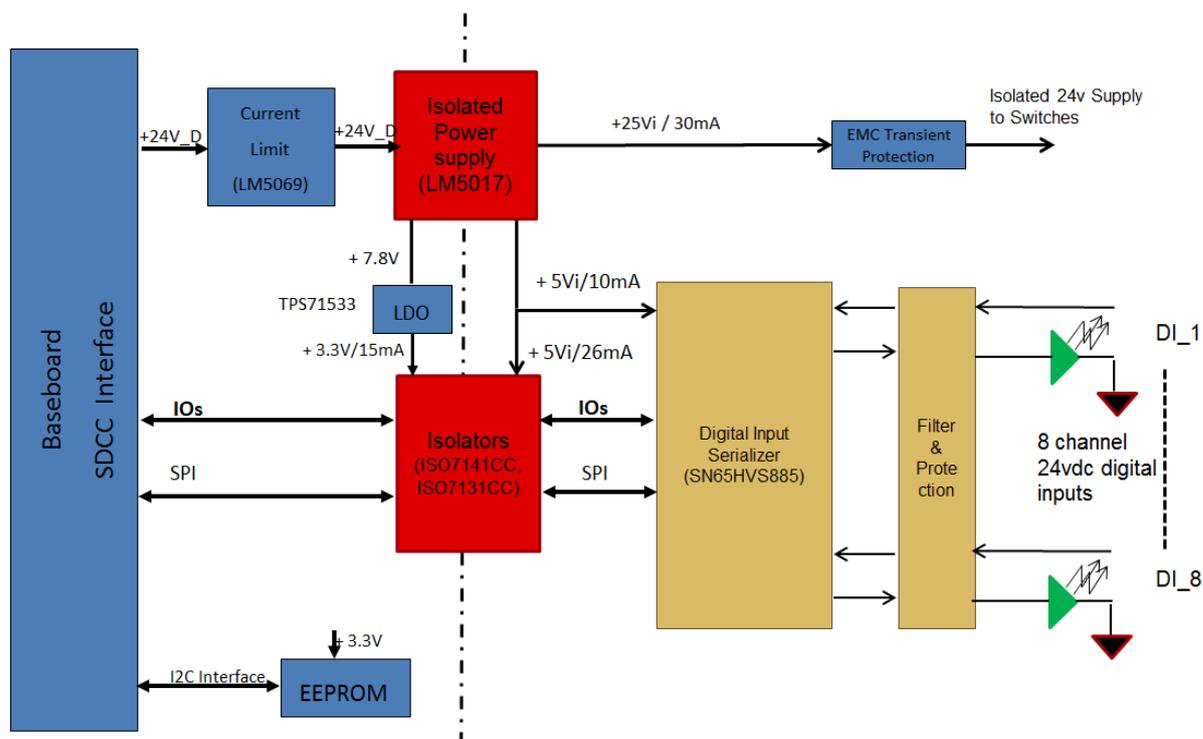


Figure 1 Block Level Design

The Digital Input Module utilizes TI's SN65HVS885 as the digital input serializer and signal conditioner. The SN65HVS885 features per-channel current limiting and input validation by internal debounce filters, to ensure the field input signals are correctly digitized.

The design isolates the digital section interface from the field devices using Digital Isolators ISO7141CC and ISO7131CC.

Fly-Buck converter technology generates onboard the required voltage rails for nonisolated and isolated sections. The field-card base board supplies +24 V that is converted into the various local voltage rails.

The SN65HVS885 serializer and both digital isolators (ISO7141CC and ISO7131CC) require an isolated 5V voltage rail to function. The LM5017 Fly-Buck circuit provides the 5-V voltage rail. The EEPROM and primary-side of both digital isolators require a nonisolated 3.3-V voltage rail. The LM5017 circuit also provides the nonisolated 3.3-V voltage rail.

4 Circuit design and Component Selection

4.1 Design based on SN65HVS885

This design employs the field input serializer and conditioner SN65HVS885. This 8-channel digital-input serializer device accepts input voltages of up to 34 V, as well as limits the current of the input signal and validates the input signal via internal debounce filters. The current-limiting capabilities of the SN65HVS885 device combined with input resistors yield a maximum field input voltage of 36 V. The Block Diagram is shown in Figure 2.

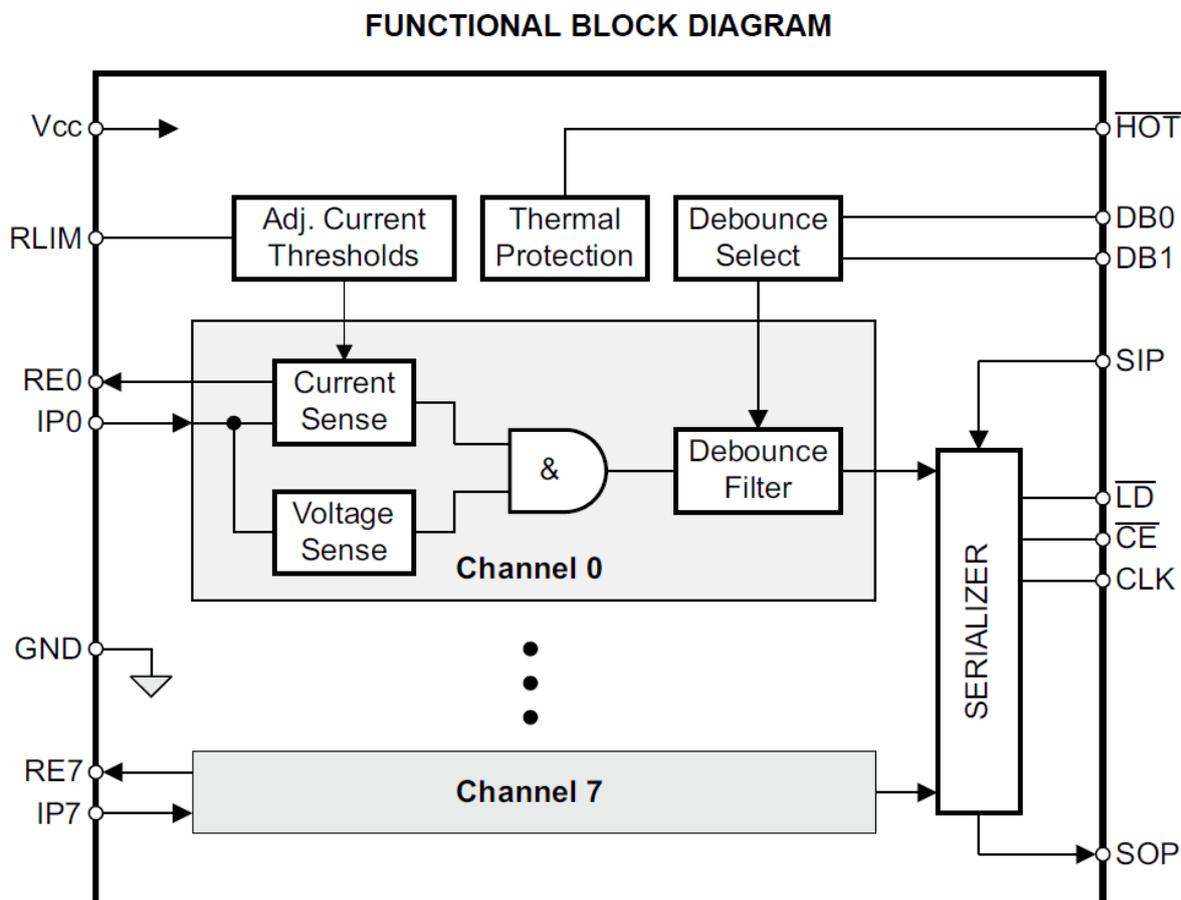


Figure 2 Serializer Block Diagram

4.1.1 Digital Input Current Limiting

The Digital Input Module design, limits each field input to 2 mA to reduce power consumed by the system. The 2 mA current-limit fulfills the switching characteristics for IEC61131-2 Type 1 and Type 3 proximity switches.

In the SN65HVS885, an external register, R_{LIM} , sets this field input current limit according to the following equation:

$$R_{LIM} = 90V / I_{IN-LIM}$$

4.1.2 Digital Input Voltage Thresholds

The design uses input resistors in series with each field input to select the field input voltage threshold with respect to the SN65HVS885's input voltage threshold. The following equation relates the field input voltage threshold to the device voltage threshold and the user selectable current limit on each input:

$$V_{IN-ON} = V_{IP-ON} + R_{IN} * I_{IN-LIM}$$

The SN65HVS885 has $V_{IP-ON} = 5.2$ V, and since $I_{IN-LIM} = 2$ mA for this Digital Input Module, $V_{IN-ON} = 5.2 + R_{IN} * 2$ mA. For the Digital Input Module, V_{IN-ON} is 7.6V ($R_{IN} = 1.2k\Omega$), which satisfies the IEC61131-2 switching characteristics for Type 1 and Type 3 proximity switches. R_{IN} also prevents a fire hazard in the case of an input short, in accordance with UL standards.

Note: V_{IN-ON} represents the rising voltage threshold; the Test Results section gives the voltage threshold values for the Digital Input Module.

4.1.3 Digital Input Level Determination

The SN65HVS885 performs three checks on each field input, to determine the digital level:

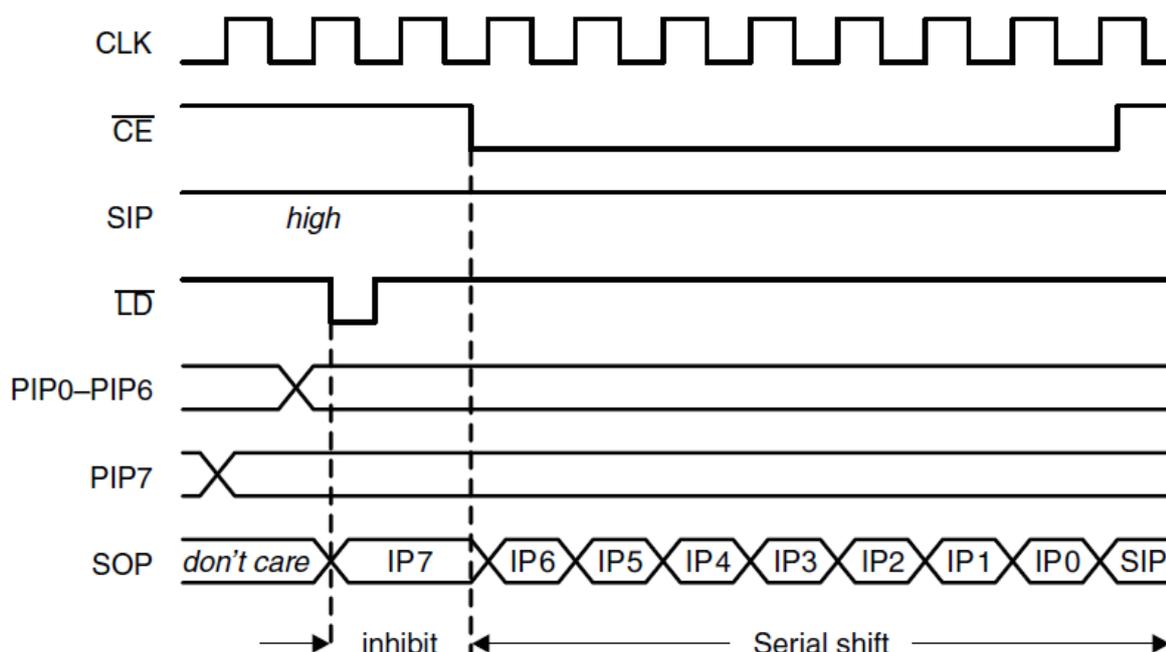
1. Is the input current greater than the leakage threshold (half of I_{IN-LIM})?
2. Is the input voltage at the device greater than 5.2 V (Field voltage greater than 7.6 V for the Digital Input Module configuration)?
3. When both the input current and voltage pass the above two requirements, do both the input current and the input voltage last longer than the debounce filter time?

As described in Sections 4.1.1 and 4.1.2, the engineer can adjust both the field input current and field voltage threshold. The debounce filter has three options: 3 ms, 1 ms, and 0 ms. The engineer can configure the Digital Input Module for various input switch configurations.

4.1.4 SPI Control and Daisy-Chaining Options

A versatile four-wire serial interface (CLK, SOP, \sim CE, and \sim LD) controls the SN65HVS885 serializer. This serial interface can operate at clock rates of up to 100 MHz. The serializer interface is compatible with SPI and interfaces to a wide variety of standard microcontrollers.

The engineer can daisy chain together several SN65HVS885 devices to produce a digital input module with 16, 24, or 32 inputs. However, in this Digital Input Module reference design, only 8 inputs are required. Shown below is the timing diagram for the SN65HVS885 serializer.



4.1.5 Filter and Protection

The goal of protection circuitry is to direct any sort of external transient electrical energy as quickly and directly as possible to earth ground. Shunting this energy to earth ground will avoid damaging any of the circuitry in the Digital Input Module, particularly the SN65HVS885 serializer.

The design uses the field-facing connections to withstand 8-kV ESD, 1-kV EFT, and 1-kV Surge. The voltage surge has the highest energy. Therefore, the protection can withstand this energy. A Transient Voltage Suppressor (TVS) diode is used to clamp the surge voltage to safer limits. In addition, there are high-voltage capacitors in strategic locations to shunt transient energy to earth ground more directly and quickly.

Design for Surge

An RC network designed to reduce transient signals protects every input channel. The capacitor has a voltage rating of 2 kV, and the network has a time constant of 1.2 μ s. A TVS diode SMCJ33CA protects the 24-V voltage rail provided to external switches or other field devices. The TVS diode SMCJ33CA clamps an external 1-kV surge voltage to 36.7 V with a maximum current rating of 28.1 A. In addition, a 1-kV rated diode, BYM10-1000, also protects the 24-V voltage rail against reverse polarity connections.

The internal ESD protection diodes in the SN65HVS885 can withstand \pm 15-kV electrostatic discharges. There are also high-voltage rated capacitors located near the TVS device to create a “faster” path to earth ground.

Design for ESD

An optimized filter as described in the section above protects ESD at the schematic level.

Design for EFT

An optimized filter protects EFT at the schematic level. The PCB layout should be very robust in EFT tests. Therefore, TI recommends using the PCB layout already set in this reference design.

4.2 Power Supply

The PLC base-board supplies a 24-V voltage rail for the Digital Input Module.

The LM5069 positive hot swap controller provides intelligent control of the power supply connections during insertion and removal of circuit module from a live system base board. The LM5069 provides inrush current limiting during turn-on. The LM5069 also provides monitoring of the load current for faults during normal operation. Additional functions include Under-Voltage Lock-Out (UVLO) and Over-Voltage Lock-Out (OVLO) to ensure the LM5069 supplies to the load only when the system input voltage is within a specified range.

The inrush current of the Digital Input Module is limited to 150 mA.

The SN65HVS885 serializer and isolated side of the ISO7141CC and ISO7131CC design supplies a 5 V, derived from the Fly-Buck DC-DC converter (LM5017).

The Fly-Buck DC-DC converter design gives 25 V and 5 V with a ripple of <50-mV peak. The design implements a soft-start feature to the LM5017 to limit the inrush current.

4.3 Isolation

4.3.1 Power Isolation

The LM5017 based Fly-Buck Isolated Power supply provides the Galvanic Isolation to the Base Board with a 24-VDC Power Bus. The Base Board requires this isolation to protect from any unexpected overvoltage on the Digital Input's field connections. Thus, the isolation protects the Base Board and PLC from damaging effects of such overvoltages.

The level of isolation depends on the Fly-Buck transformer specification. This design uses a transformer with a dielectric rating of 1500 VAC for 1 second.

4.3.2 Digital Isolation

The High Speed Digital Isolator ISO7141CC and ISO7131CC connect the SPI Host to the serializer SPI. With these digital isolators, the Host Processor on the Base Board maintains 2.5 kVrms of galvanic isolation for 1 minute from any high voltage condition appearing at the Digital Input Module from the field side.

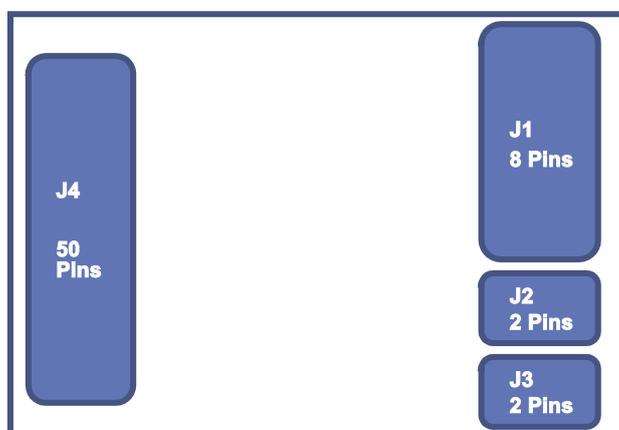
The isolated signals are: CLK, SOP, ~CE, ~LD, DB0, DB1, and nSDRDY.

A low-pass filter with a cutoff frequency of ~40 MHz is located physically close to the source side of each isolated signal. This filter reduces reflections and other undesired high-frequency effects.

4.4 Connectors

The Digital Input Board has been designed with following connectors:

1. J1: 8 Pin Screw Terminal type 2.54mm Pitch connectors for interfacing digital inputs
2. J2: 2 Pin Screw Terminal type 2.54mm Pitch connectors for supplying 24 V to external switches
3. J3: 2 Pin Screw Terminal type 2.54mm Pitch connectors for connecting Earth Reference
4. J4: 50 Pin High Speed Connector for SPI/ Power Supply interface to the Base Board



5 Software Description

The SN65HVS885 has only one set of options to configure via software. Set the debounce setting for the field input filters to 3 ms, 1 ms, or 0 ms, depending on the levels of DB0 and DB1. This design configures DB0 and DB1 with standard GPIO pins, which connect to the PLC base board. If no active selection is made, pull-up resistors installed on the Digital Input module set the default debounce time to 3 ms. The table below shows the appropriate settings for DB0 and DB1 to achieve the desired debounce time.

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (Filter bypassed)
GND	GND	Reserved

Engineers should configure all other software for reading the data from the SN65HVS885 on the PLC baseboard. See the procedure above in section 4.1.4 for reading the serialized data with the timing diagram.

6 Test Setup

6.1 Hardware Test Setup

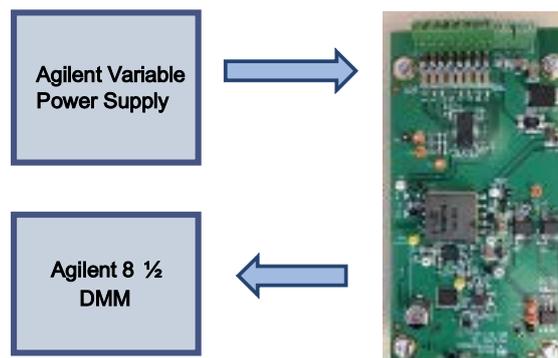


Figure 3 Functional Test Setup

For pre-compliance testing, the design mounts the Digital Input Module on the SmartIO Evaluation Platform in Slot 1. Half of the digital inputs are held high with the following sequence: 10101010.

6.2 Software Test setup

The functional testing phase requires no software support. All functional testing was done with hardware and test equipment only.

The pre-compliance testing setup uses a GUI based Test Setup. The GUI on the PC connects to the SmartIO Evaluation Platform through USB communication. The SmartIO Evaluation Platform then controls the Digital Input Card via SPI interface, to read the digital input levels as connected via external jumper wires.

The SmartIO Evaluation Platform has test firmware coded to expect an input pattern of 10101010, which is what the pre-compliance test setup specifies. As each pre-compliance test is performed on the Digital Input Module, the SmartIO Evaluation Platform compares the expected data value to the actual value returned. If there is any error, an LED glows on the SmartIO Evaluation Platform, and the platform turns off one second after the error clears.

7 Test Results

7.1 Functional Testing

The Digital Input Module was tested for functionality, primarily in two main areas:

- Power Rails and Current Consumption
- Field Input Parameters

The test procedure for functional testing is listed below:

1. Connect 24 V from the Agilent power supply to TP18, and GND to TP17 (power the entire board).
2. Measure the rails of the LM5017 power supply, both isolated and nonisolated with Agilent DMM.
3. Apply voltage to each field digital input with the external Agilent power supply, varying the DC level to determine V_{IL} and V_{IH} (hysteresis of field inputs).
4. Provide 24 V from Digital Input Module to the field inputs, verify power rails, and ensure correct field input LED status.

7.1.1 Results Summary at 25°C (TBD)

The results indicate that the Digital Input Module performs to expected values. The expected and actual voltage rails are shown in Table 1, and the expected and actual V_{IL} and V_{IH} values for each of the 8 field inputs are shown in Table 2.

Table 1: Measurement Results - Voltage Rails

Voltage Net name	Ideal Voltage (V)	Actual Voltage (V)	Note
24 V_LIMIT	24	23.581	Post-current limit voltage
Vpri	7.8	7.893	Pre-regulated primary-side voltage
3V3	3.3	3.3068	Regulated primary-side voltage
5V_ISO	5	5.0238	Regulated isolated voltage
24 V_FIELD	24	24.039	Regulated isolated voltage, $I_{LOAD}=16mA$

Table 2: Measurement Results - Input Thresholds

Field Input #	Designed V_{IH} (V)	Actual V_{IH} (V)	Actual V_{IL} (V)	Note
1	7.6	7.603	6.718	
2	7.6	7.590	6.678	
3	7.6	7.572	6.645	
4	7.6	7.534	6.674	
5	7.6	7.611	6.712	
6	7.6	7.590	6.676	
7	7.6	7.530	6.666	
8	7.6	7.634	6.687	
All Inputs	7.6	7.641	6.675	All inputs wired to external Agilent power supply

As described in section 4.1.2, the design of the field input thresholds meet the IEC61131-2 switching characteristics for Type 1 and Type 3 proximity switches. The design limits each input to 2 mA, and the threshold voltage falls within the specified switching region for digital input modules, as described in IEC61131-2.

7.2 Pre compliance Testing

The design of the Digital Input Module meets standard EMC requirements for Industrial PLC application.

The tests conducted to check the performance are:

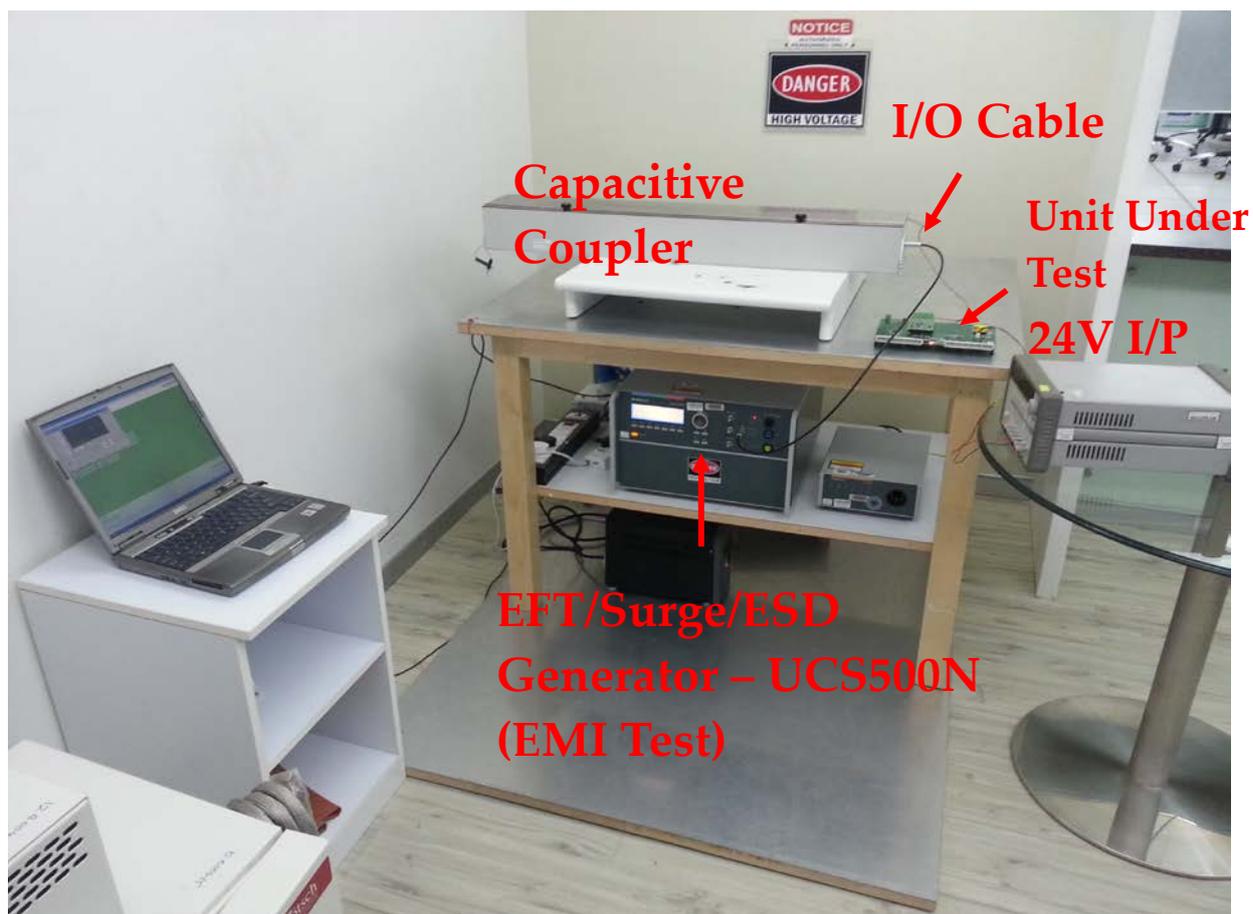
1. Electro Static Discharge as per IEC61000-4-2
2. Electrical Fast Transients as per IEC61000-4-4
3. Surge as per IEC61000-4-5

Criteria and performance as per IEC61131-2:

Criteria	Performance (Pass) Criteria
A	The Digital Input Module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the Digital Input Module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the Digital Input Module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

The next sections explain the test setup, procedures, and observations.

7.2.1 Test Set-Up



Follow these steps to monitor:

1. Connect the EUT as shown in the Test Setup.
The shield pin connects to the Local Earth, the same as the Test Generator.
2. Power on the EUT.
The test software expects an input of 10101010, and if the module detects an error, then the base board LED turns on.
The module checks the respective channel before and after the test.
The module performs the ESD test using test levels listed in the table below.
3. After performing the ESD test, to check the degradation, conduct a performance test.

Results

Generic Test Standard	Test Level	Performance Result (Pass Criteria)
ESD immunity IEC 61000-4-2	2 kV contact discharges – Level 2	Criteria A (Monitored before and after the test)
ESD immunity IEC 61000-4-2	4 kV contact discharges – Level 2	Criteria B (Monitored before and after the test)

Functionality checked before and after the test.

7.2.3 Electric Fast Transients test: EFT – IEC61000-4-4

Test Level and Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

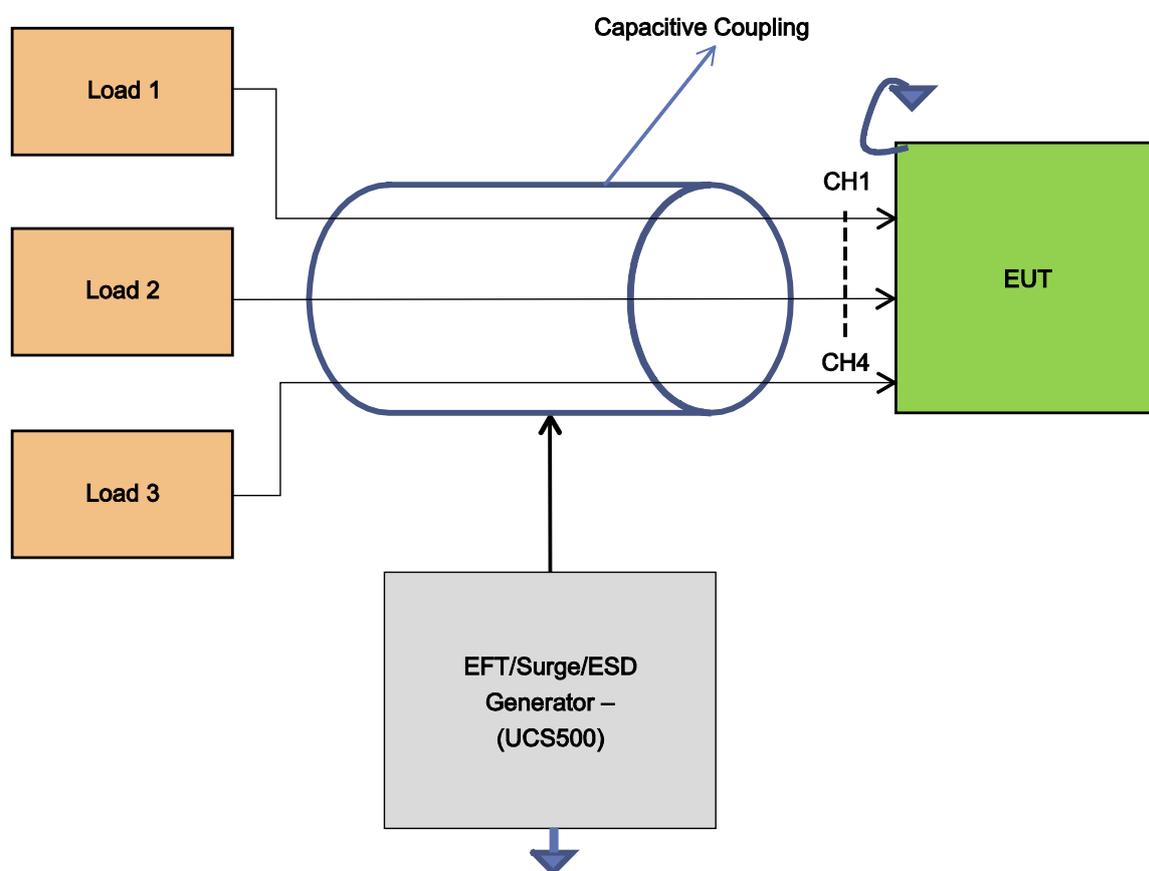
Generic Test Standard	Test Level	Performance (Pass Criteria)
EFT/B immunity IEC 61000-4-4	± 2 KV at 5 KHz, 100KHz on signal ports	Criteria B (Monitored before and after the test)

Description

Setup:

With reference to IEC610004-4:

The module injects the burst signal on all cables together using a Capacitive Coupling Clamp. Unshielded cables connect the EUT to auxiliary sources. The design sets the lengths of the cables to 3 m and places the cables 10 cm above the reference plane. The module carries out the test with the EUT placed 10 cm above the reference plane on insulating material, and with the EUT placed on the reference plane.



Follow these steps to monitor:

1. Connect the EUT as shown in the Test Setup.
The shield pin connects to the Local Earth, the same as the Test Generator.
2. Power on the EUT.
The test software expects an input of 10101010, and if the module detects an error, then the base board LED turns on.
The module checks the respective channel before and after the test.
The module performs the ESD test using test levels listed in the table below.
3. After performing the ESD test, to check the degradation, conduct a performance test.

Results

Test No	Test Mode	Observation*
1	+ 0.5 kV , 5kHz	PASS, Criteria A
2	- 0.5 kV , 5kHz	PASS, Criteria A
3	+ 1 kV , 5kHz	PASS, Criteria A
4	- 1 kV , 5kHz	PASS, Criteria A
5	+ 2 kV , 5kHz	PASS, Criteria B
6	- 2 kV , 5kHz	PASS, Criteria B
7	+ 0.5 kV , 100kHz	PASS, Criteria A
8	- 0.5 kV , 100kHz	PASS, Criteria A
9	+ 1 kV , 100kHz	PASS, Criteria A
10	- 1 kV , 100kHz	PASS, Criteria A
11	+ 2 kV , 100kHz	PASS, Criteria B
12	- 2 kV , 100kHz	PASS, Criteria B

Functionality checked before and after the test.

7.2.4 SURGE- IEC61000-4-5

Test Level and Expected Performance

The module expects the Common-Mode Surge at I/O connectors and the performance criteria as follows:

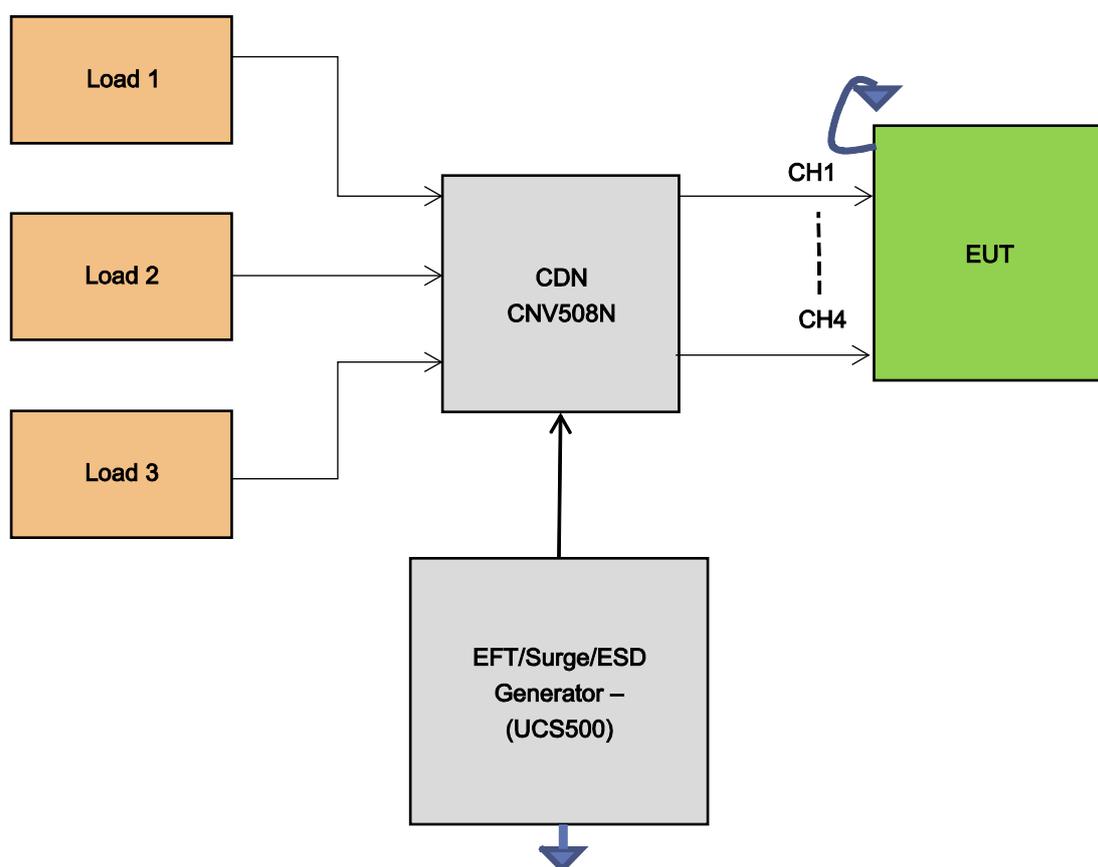
Generic Test Standard	Test Level	Performance (Pass Criteria)
Surge immunity IEC 61000-4-5	± 1 kVCM on signal ports	Criteria B (Monitored before and after the test)

Description

Setup:

With reference to IEC610004-5:

The design places the EUT and the digital input cable on nonconductive support 10 cm above a reference ground plane. Surge was injected into the digital input cable (I/O cable) for testing via the Coupling Decoupling Network. The module monitors the EUT operation before and after the test.



The module monitors EUT operation after the test. The design monitors all eight channels after the test by the Microcontroller (on the SmartIO Evaluation Platform) and compares with a Set Value (equivalent to the external constant voltage or current source). The Error should be within the accuracy mentioned in Section 6.3.1.

Follow these steps to monitor:

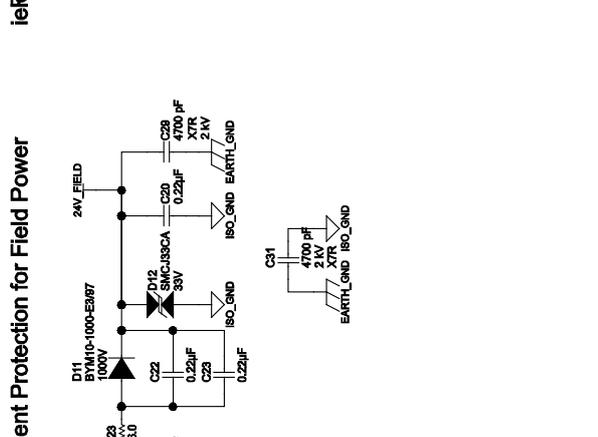
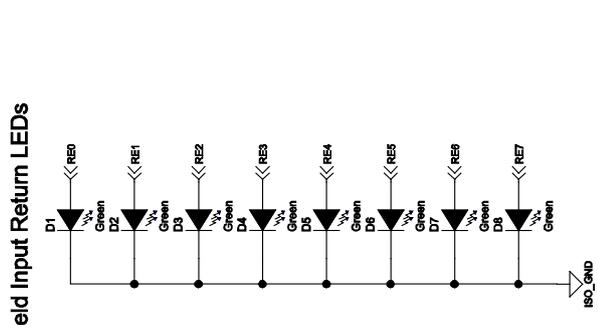
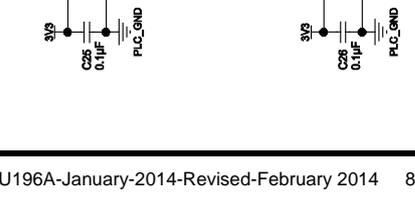
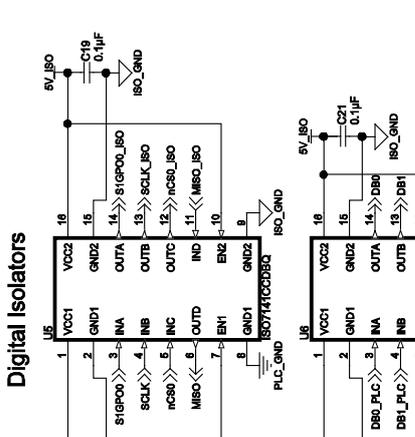
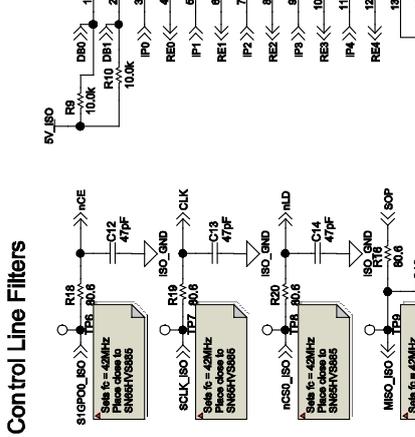
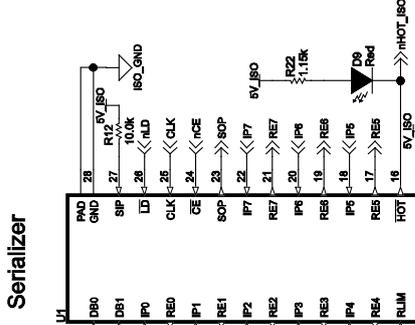
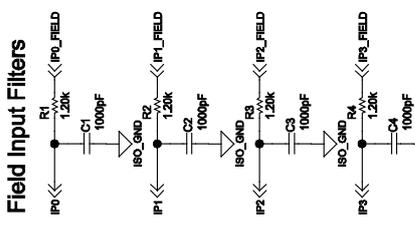
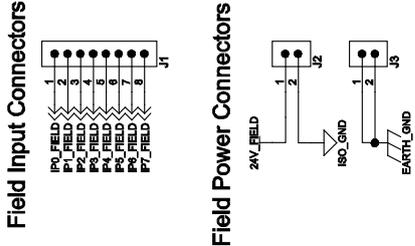
1. Connect the EUT as shown in the Test Setup.
The shield pin connects to the Local Earth, the same as the Test Generator.
2. Power on the EUT.
The test software expects an input of 10101010, and if the module detects an error, then the base board LED turns on.
The module checks the respective channel before and after the test.
The module performs the ESD test using test levels listed in the table below.
3. After performing the ESD test, to check the degradation, conduct a performance test.

Results

Test No	Test Mode	Observation*
1	+ 0.5 kV	PASS, Criteria B
2	- 0.5 kV	PASS, Criteria B
3	+ 1 kV	PASS, Criteria B
4	- 1 kV	PASS, Criteria B

Functionality checked before and after the test.

Note: On Tests 3 and 4, flashover was observed on the 24 V_FIELD lines, indicating an insufficient clearance in those traces on the PCB. The E2 revision of the Digital Input Module corrects this error.



8.2 Bill of Materials

 Bill of Materials TI DESIGNS						
Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
IPCB1	1		Printed Circuit Board		SAT0060	Any
C1, C2, C3, C4, C5, C6, C7, C8	8	1000pF	CAP, CERM, 1000pF, 2KV 10% X7R 1206	1206	202R18W102KV4E	Johanson Dielectrics Inc
C9	1	0.47uF	CAP, CERM, 0.47uF, 16V, +/-5%, X7R, 0805	0805	0805YC474JAT2A	AVX
C10, C11, C19, C21, C25, C26	6	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata
C12, C13, C14, C16	4	47pF	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0402	0402	GRM1555C1H470JZ01	MuRata
C15, C7	2	22uF	CAP, AL, 22uF, 50V, +/-20%, 0.88 ohm, SMD	SMT Radial D	EEE-FK1H220P	Panasonic
C17	1	1uF	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	1206	GRM31CR72A105KA01L	MuRata
C18	1	0.1uF	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	0603	GRM188R72A104KA35D	MuRata
C20, C22, C23, C24	4	0.22uF	CAP, CERM, 0.22uF, 100V, +/-10%, X7R, 0805	0805	GRM21AR72A224KAC5L	MuRata
C27	1	0.01uF	CAP, CERM, 0.01uF, 16V, +/-10%, X7R, 0402	0402	C1005X7R1C103K	TDK
C28	1	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	0603	GRM188R71E104KA01D	MuRata
C29, C31, C32	3	4700 pF	CAP, CERM, xxxF, xxV, (TempCo), xx%, [PackageReference]	Used in PnP output	Used in BOM report	Used in BOM report
C30	1	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	0603	C1608X7R1C105K	TDK
C33	1	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C105KA12D	MuRata
C34	1	1000pF	CAP, CERM, 1000pF, 25V, +/-10%, X7R, 0603	0603	GRM188R71E102KA01D	MuRata
C35	1	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata
C36	1	22uF	CAP, CERM, 22uF, 25V, +/-10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata
C37, C38	2	2.2uF	CAP, CERM, 2.2uF, 25V, +/-10%, X7R, 0805	0805	GRM21BR71E225KA73L	MuRata
C39	1	1000pF	CAP, CERM, 1000pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A102KA01D	MuRata
D1, D2, D3, D4, D5, D6, D7, D8	8		LED GREEN 0.2MM 13MCD 0402 SMD	0402 (1005 Metric)	SML-P12PTT86	Rohm Semiconductor
D9	1		LED RED 0.2MM 60MCD	0402 (1005 Metric)	SML-P12VTT86	Rohm Semiconductor
D10	1	45V	Diode, Schottky, 45V, 0.1A,	SOD-523	SDM10U45-7-F	Diodes Inc.
D11	1	1000V	Diode, P-N, 1000V, 1A,	2.67x5.2mm	BYM10-1000-E3/97	Vishay-Semiconductor
D12	1	33V	Diode, TVS, Bi, 33V, 1500W,	SMC	SMCJ33CA	Boums
D13, D17	2	200V	Diode, Schottky, 200V, 1A,	PowerDI123	DFLS1200-7	Diodes Inc.
D14	1	60V	Diode, Schottky, 60V, 1A,	SOD-123F	PMEG6010CEH,115	NXP Semiconductor
FID1, FID2,	3		Fiducial mark. There is	Fiducial	N/A	N/A
H1, H2, H5,	4		Screw Pan Head M3	Screw M3	29311	Keystone
J1	1		Terminal Block, 8x1, 2.54 mm,	8POS Terminal Block	1725711	Phoenix Contact
J2, J3	2		Header, 2 Pos, 6A, 63V, TH	6.2x8.5x5.54 mm	1725656	Phoenix Contact
J4	1		Receptacle, 0.8mm, 25x2,	25x2 Socket Strip	ERF8-025-05-0-L-DV-K-	Samtec
LBL1	1		Thermal Transfer Printable	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
Q1	1	60V	MOSFET, N-CH, 60V, 50A,	SON 5x6mm	CSD18537NQ5A	Texas Instruments
R1, R2, R3,	8	1.20k	RES, 1.20k ohm, 1%, 0.25W,	1.4x3.6mm	MMA02040C1201FB30	Vishay/Beyschlag
R9, R10,	3	10.0k	RES, 10.0k ohm, 1%, 0.063W,	0402	CRCW040210K0FKED	Vishay-Dale
R11	1	44.2k	RES, 44.2k ohm, 1%, 0.063W,	0402	CRCW040244K2FKED	Vishay-Dale
R13	1	47.5k	RES, 47.5k ohm, 1%, 0.063W,	0402	CRCW040247K5FKED	Vishay-Dale
R14, R36	2	0	RES, 0 ohm, 5%, 0.063W,	0402	CRCW0402000Z0ED	Vishay-Dale
R15	1	11.3k	RES, 11.3k ohm, 1%, 0.063W,	0402	CRCW040211K3FKED	Vishay-Dale
R16, R18,	4	80.6	RES, 80.6 ohm, 1%, 0.063W,	0402	CRCW040280R6FKED	Vishay-Dale
R17, R21	2	1.50k	RES, 1.50k ohm, 1%, 0.063W,	0402	CRCW04021K50FKED	Vishay-Dale
R22	1	1.15k	RES, 1.15k ohm, 1%, 0.063W,	0402	CRCW04021K15FKED	Vishay-Dale

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
R23	1	56.0	RES, 56.0 ohm, 1%, 0.4W,	2.2x5.8mm	MMB02070C5609FB20	Vishay/Beyschlag
R24	1	4.64k	RES, 4.64k ohm, 1%, 0.063W,	0402	CRCW04024K64FKED	Vishay-Dale
R25	1	22.6k	RES, 22.6k ohm, 1%, 0.063W,	0402	CRCW040222K6FKED	Vishay-Dale
R26	1	0.3	RES, xxx ohm, x%, xW,	Used in PnP output	Used in BOM report	Used in BOM report
R27	1	100k	RES, 100k ohm, 1%, 0.063W,	0402	CRCW0402100KFKED	Vishay-Dale
R28	1	49.9k	RES, 49.9k ohm, 1%, 0.063W,	0402	CRCW040249K9FKED	Vishay-Dale
R29	1	6.34k	RES, 6.34k ohm, 1%, 0.063W,	0402	CRCW04026K34FKED	Vishay-Dale
R30	1	340k	RES, 340k ohm, 1%, 0.063W,	0402	CRCW0402340KFKED	Vishay-Dale
R31, R33	2	20.0k	RES, 20.0k ohm, 1%, 0.063W,	0402	CRCW040220K0FKED	Vishay-Dale
R32	1	105k	RES, 105k ohm, 1%, 0.063W,	0402	CRCW0402105KFKED	Vishay-Dale
T1	1	50uH	Transformer, 50uH, SMT	17.02x15.49x6.99mm	750342178	Würth Elektronik eiSos
TP1, TP3,	6	Black	Test Point, Miniature, Black,	Black Miniature Testpoint	5001	Keystone
TP2, TP10,	6	White	Test Point, Miniature, White,	White Miniature Testpoint	5002	Keystone
TP4, TP5,	6	Orange	Test Point, Miniature, Orange,	Orange Miniature Testpoint	5003	Keystone
TP14,	2	Yellow	Test Point, Miniature, Yellow,	Yellow Miniature Testpoint	5004	Keystone
U1	1		34 V, Digital-Input Serializer	PWP0028E	SN65HVS885PWP	Texas Instruments
U2	1		Positive High Voltage Hot	MUB10A	LM5069MM-2	Texas Instruments
U3	1		IC, EEPROM, 2KBIT, 1MHZ,	SOIC-8	AT24C02C-SSHM-B	Atmel
U4	1		100V, 600mA Constant On-	NGU0008B	LM5017SD/NOPB	Texas Instruments
U5	1		4242-VPK Small-Footprint and	DBQ0016A	ISO7141CCDBQ	Texas Instruments
U6	1		4242-VPK Small-Footprint and	DBQ0016A	ISO7131CCDBQ	Texas Instruments
U7	1		50 mA, 24 V, 3.2-mA Supply	DCK0005A	TPS71533DCK	Texas Instruments
D15	0	6.2V	Diode, Zener, 6.2V, 500mW,	SOD-123	MMSZ5234B-7-F	Diodes Inc.
D16	0	27V	Diode, Zener, 27V, 500mW,	SOD-123	MMSZ5254B-7-F	Diodes Inc.

Notes:

Unless otherwise noted in the Alternate PartNumber and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.

8.3 PCB Layout

The Digital Input Module is implemented in a 4 layers PCB. The major guidelines for the layout are placement of the power section and routing of the critical analog input lines to the serializer.

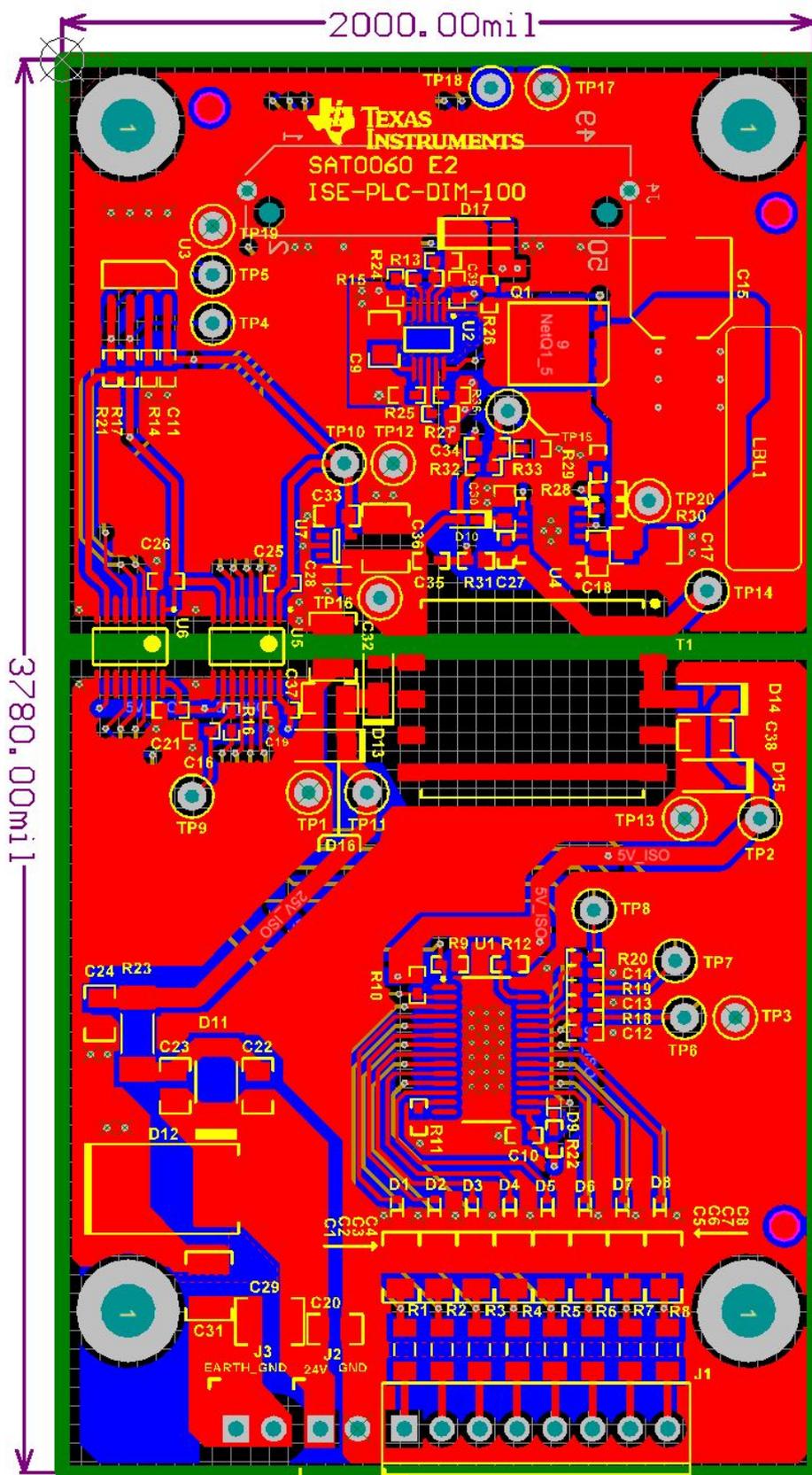
8.3.1 Layout Recommendations

To achieve a high performance from the PCB, the following Layout Guidelines have been followed:

1. Avoid cross-over of digital and analog signals.
2. Route traces on opposite sides of the PCB at right angles.
3. Use continuous ground planes below power planes for better decoupling.
4. Do not split the ground plane: use one solid plane under both the analog and digital sections of the board.
5. Place the decoupling capacitors close to supply pin of the IC.
6. Use multiple vias for power and ground for decoupling caps.
7. Do not split the ground plane: use a continuous plane under both analog and digital sections of the board.
8. All current sense resistors MUST be routed as a Kelvin Sense connection.
9. SPI lines: for signal integrity, place the termination resistances near to the source.
10. Place decoupling capacitors close to the respective pins for each AVDD/AVSS.
11. Place the reference capacitor close to the voltage reference input pin.
12. Place the diversion elements, such as TVS diodes or capacitors, as close to connectors as possible to ensure that return current from high-energy transients does not cause damage to sensitive devices.

Use large and wide traces to ensure a low-impedance path for diverted high-energy transients to flow away from I/O terminals on the SN65HVS885.

8.3.2 Layout Prints



8.4 Altium Project

To download the Altium database, see the design files at: [TIDA-00017](#).

8.5 Gerber files

To download the Gerber artwork, see the design files at: [TIDA-00017](#).

9 About the Author

EVAN D. CORNELL is a Systems Architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Evan brings to this role experience in system-level analog, mixed-signal, and power management design. Evan earned his Master of Electrical and Computer Engineering (MENG) and Bachelor of Science (BS) in Electrical Engineering from the Rose-Hulman Institute of Technology in Terre Haute, IN. Evan is a member of the Institute of Electrical and Electronics Engineers (IEEE).

10 Revision History

Changes from Original (January 2014) to A Revision (February 2014)

- Changed T1 from 750313995 to 750342178 (both Würth brand of transformers)
- Added explanation in Section 4.1 explaining the difference between field input voltage threshold and device input voltage threshold

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