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16-Bit Analog Output Module Reference Design for Programmable Logic Controllers (PLCs)

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Design Resources

TIDA-00119	Input Module Design Files
TIDA-00123	IO Controller Design Files
DAC8760	Product Folder
OPA188	Product Folder
LM5069	Product Folder
LM5017	Product Folder
TPS7A4700	Product Folder
TPS7A1650	Product Folder
TPS7A3001	Product Folder
TPS71533	Product Folder
ISO7141CC	Product Folder
ISO7221	Product Folder

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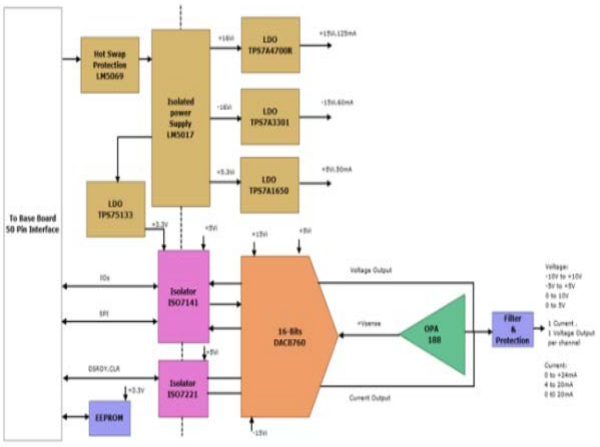
Design Features

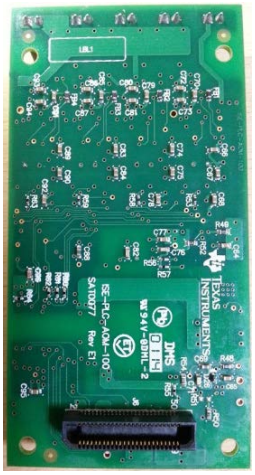
- Designed to comply with IEC61000-4 standards for ESD, EFT and Surge
- 4 Channel, 16 bit DAC based configurable Analog Outputs
- Selectable Voltage Outputs:
  - ± 10V, 0 - 10V, ± 5V, 0 - 5V
  - Voltage Output Accuracy: ±0.2% FSR
- Selectable Current Outputs:
  - 0 - 20 mA, 4 - 20 mA, 0 - 24mA
  - Current Output Accuracy: ±0.2% FSR
- Output filtering, protection circuitry and integrated 15kV ESD protection
- High-speed, galvanic isolated SPI interface capable of speeds up to 20MHz
- Integrated over-temperature, open-line and short circuit protection features
- On-board isolated Flybuck power supply with inrush current protection
- SPI for I/O control interface with digital isolation
- Slim form factor 95 x 50x 10mm (LxWxH)
- Pluggable to IO Controller for easy evaluation (TIDA-00123)

Featured Applications

- PLC current and voltage output modules
- Field Sensors and Process Transmitters

Block Diagram





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1 System Description

Standard industrial analog output (AO) circuits are dedicated to either voltage or current outputs. This reference design using the DAC8760 can output both the standard industrial voltage and current outputs on a single terminal, thus reducing the number of terminals needed from three to two. A combined output succeeds in reducing the wiring cost, connector count, and increasing the versatility of the AO design.

The Smart Analog Output module reference design is intended as an evaluation module for users to develop end-equipment like PLC, field sensors and process transmitters. This design is an Isolated Analog Output Module with Digital isolators for SPI interface and FlyBuck transformer for power supply isolation. On-board EEPROM has been provided to store calibration data and module configuration. Screw type terminals for individual output channels have been provided for easy wiring. LEDs are provided for Power Supply indication.

The reference design provides a complete guide for the design of an Analog Output Module that can be configured for Voltage or Current output, for different output ranges in a slim form factor. This Module has been designed to be pluggable to the IO Controller for quick testing and evaluation. This Module has been designed to comply with EMC standards for Industrial environment. The design files include schematics, BOM, layer plots, Altium files, Gerber Files and an easy-to-use Graphical User Interface (GUI).

The Smart Analog Output Module has been tested for the following:

- Isolated SPI Interface with DACs configures in daisy chain.
- Voltage and Current output functionality and accuracy including over range.
- Surge, EFT & ESD: Pre-compliance testing as per IEC61000-4 standards.

2 Design Specifications

4 Programmable 16 Bit resolution Voltage / Current Analog Outputs with software configurable ranges:

Voltage Outputs *	Current Outputs*
• -10V - 10V • -5V - 5V • 0 - 5V • 0 - 10V	• 0- 20mA. • 0- 25mA. • 4- 20mA.

*Can be programmed for 10% over- range.

Accuracy:

Voltage Range <0.1% Error	Current Range <0.2% Error.

Isolation:

Power Supply : 1500 VAC	Signal : 2500 VAC

EMC:

Test	Levels
IEC61000-4-2: Electro Static Discharge.	+/- 8kV Air Discharge , +/- 4kV Contact Discharge
IEC61000-4-4 : Electrical Fast Transients	+/- 2kV, 5kHz/100kHz.
IEC61000-4-5 : Surge	+/-1kV Common Mode

3 Block Diagram

The Analog output Module has the following Blocks:

1. Digital to Analog Convertor (DAC)
2. Power Supply
3. Isolation
4. Interface

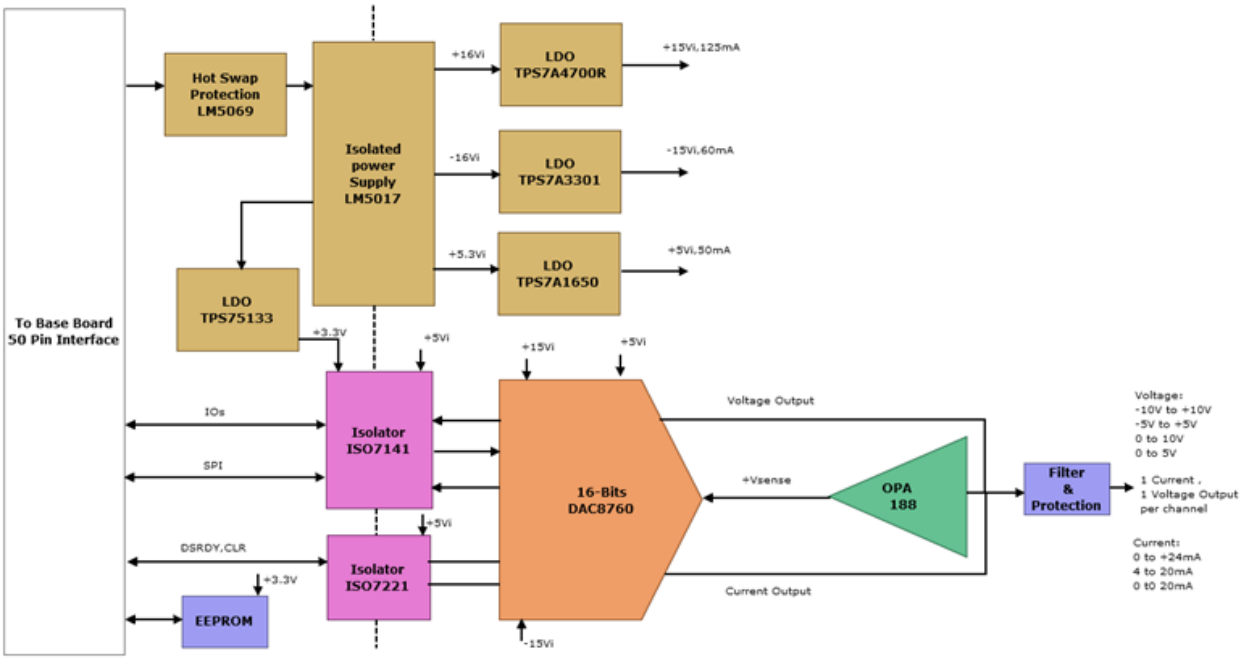

Figure 1 Block Level Design

Digital to Analog Convertor(DAC)

This Module utilizes TI's 16 Bit resolution DAC DAC8760. DAC8760 was chosen for this design for its high level of integration. The DAC8760 features a max 0.1% full-scale range (FSR) total-unadjusted-error (TUE) specification, which includes offset error, gain error, and integral non-linearity (INL) errors at 25°C. The 0.1% FSR TUE is valid for all of the voltage and current output stages providing a baseline for the final system accuracy. The max differential non-linearity (DNL) specification of +/-1 least significant bit (LSB) provides fully monotonic operation for both V_{OUT} and I_{OUT}.

DAC8760 features software-selectable voltage and current ranges, with calibration register for Gain error and Zero error correction. The output slew rate can also be programmed. Four single outputs DAC have been used in this module. The Analog output is configured through SPI interface. The SPI is configured in a daisy chain mode to be able to write to all the four DACs. The Analog Output module has an EEPROM that stores the calibration data and configuration.

Power Supply

The required voltage rails for non-isolated and isolated section are generated onboard using Flybuck converter topology. The voltage rails are derived from +24V from the IO Controller . The DAC and Op Amps need +/-15V power supply. The DAC additionally needs 5V as reference. The power supply section has linear voltage regulator to reduce the ripple.

Isolation

Most AO modules require isolation from the backplane and other AO modules. This is typically accomplished by isolating the digital signals between the host processor/controller and the DAC in the AO circuit. There are many topologies available to achieve the isolation but galvanic (capacitive) isolation has many advantages over other topologies and has been selected for this design. The Power supply isolation is achieved by the use of Flybuck configured transformer.

Interface

The DAC card has one 50-pin connector for interface with IO Controller. Four outputs and the system earth connection, five -2 pin connectors have been provided.

4 Circuit design and Component Selection

4.1 Digital to Analog Convertor

DAC8760 is designed for industrial and process control applications. DAC8760 can provide 4 to 20 mA, 0 to 20mA or 0 to 24 mA current outputs or 0- 5 V, 0-10 V, ±5 V or ±10 voltage outputs with a 10% over range (0 -5.5 V, 0 - 11 V, ±5.5 V, or ±11 V) capability. DAC8760 internal Block Diagram is shown in Figure 2.

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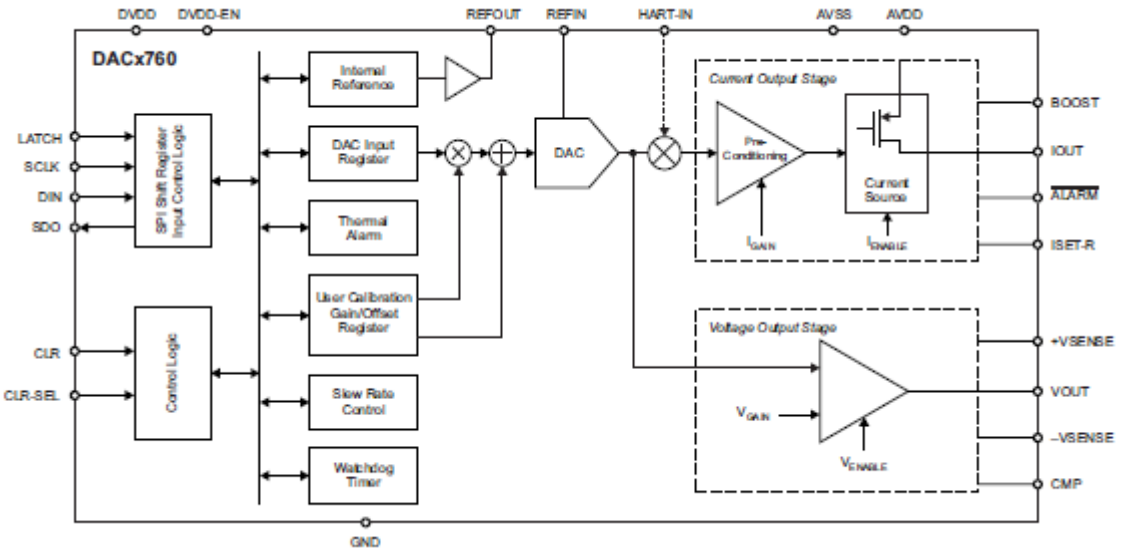


Figure 2 DAC Block Diagram

Notes:

- After Power is applied, by default both the output stages are disabled.
- DAC8760 is capable of providing both current and voltage outputs simultaneously enabled while being controlled by a single data register. This feature cannot be used as the board is configured to provide either current or voltage input only.

4.1.1 Voltage Output

When DAC8760 is configured for voltage output, The max load allowed is 1KΩ Minimum @ 10mA. For voltage output, the module uses +15V and -15V at Power Supply rails thus providing a 5V of headroom for 10mA/1KΩ.

The equation for DAC8760 to generate 16-bit code required Voltage Output is:

For unipolar output mode:

$$VOUT = VREF \cdot GAIN \cdot \frac{CODE}{2^N}$$

For bipolar output mode:

$$VOUT = VREF \cdot GAIN \cdot \frac{CODE}{2^N} - GAIN \cdot \frac{VREF}{2}$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- VREF is the reference voltage; for internal reference, VREF = +5.0 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in Table 1.

4.1.2 Current Output

DAC8760 current output stage consists of a pre-conditioner and a current source. This stage provides current output according to the DAC code. The output range can be programmed as 0- 20mA, 0-24 mA or 4- 20 mA. Optionally an external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals (AV_{DD} – 2.5 V). In single power-supply mode, the maximum AV_{DD} is 36 V, and the maximum compliance voltage is 33.5 V. After power-on, the IOUT pin is in a Hi-Z state, with no output. In the present design an external 15 kΩ 0.1% resistor is connected to the ISET-R pin.
The equation for DAC 16-bit code to Current Output is:

For a 0-mA to 20-mA output range:

$$IOUT = 20mA \cdot \frac{CODE}{2^N}$$

For a 0-mA to 24-mA output range:

$$IOUT = 24mA \cdot \frac{CODE}{2^N}$$

For a 4-mA to 20-mA output range:

$$IOUT = 16mA \cdot \frac{CODE}{2^N} + 4mA$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.

4.1.3 Voltage Sense

+Vsense and – Vsense enable sensing of load. Ideally it is connected to Vout at the terminals. As the Vout and Iout are tied together, when used as current output there will be gain error due to leakage current of the +Vsense pin. This leakage current will be introducing Gain error of -0.36%. This error can be minimized by using high input impedance, low input bias current Op-Amp. In the present design the +Vsense is connected to Vout through buffer OPA188 which has a typical input bias current of 160pA. This reduces the Gain error reducing error to <0.008%.

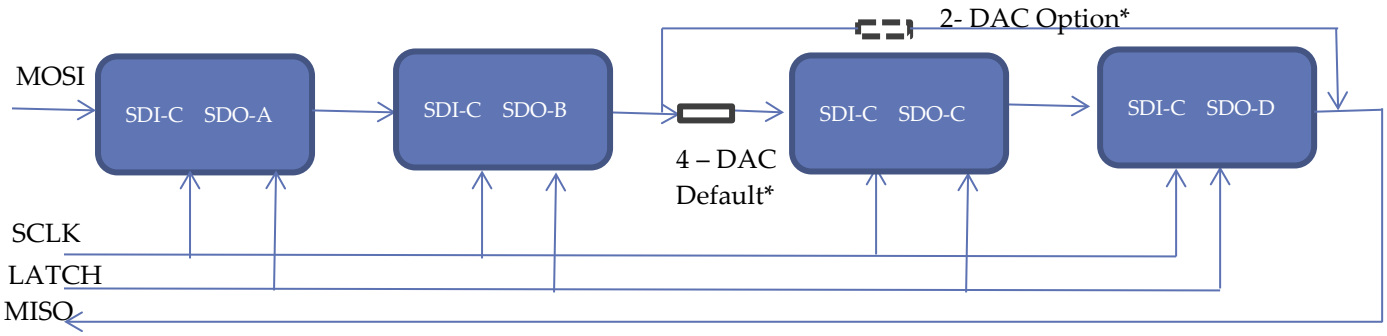
4.1.4 HART Option

The DAC8760 is also provisioned to provide HART output. In this design HART Pins are made available to the user by Test Points. For details on HART utilization refer the DAC8760 datasheet.

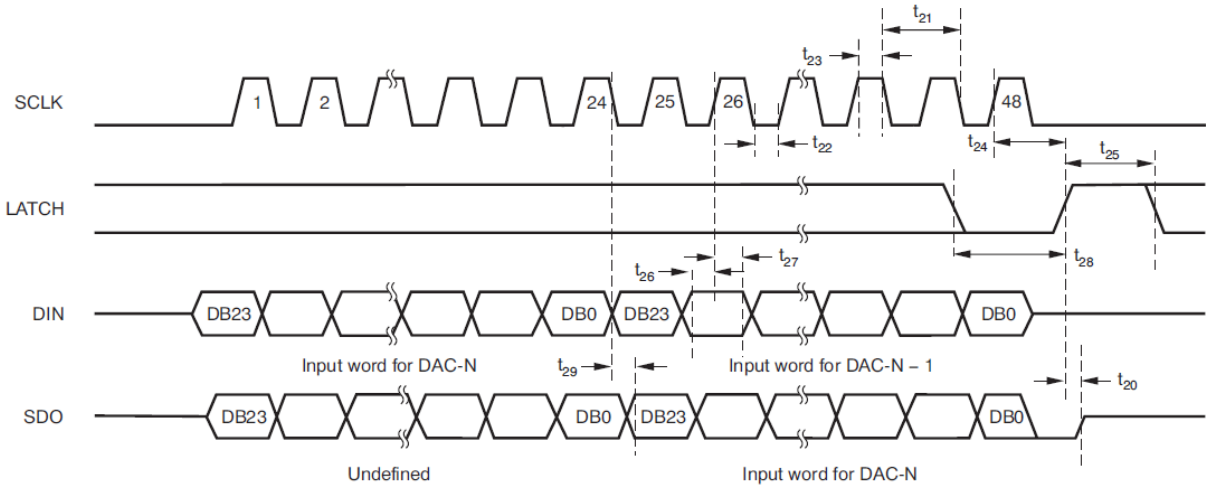
4.1.5 SPI and Daisy chained DACs

DAC8760 is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that can operate at clock rates of up to 31 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. If there are multiple SPI slave devices, DACs can be connected in Daisy chain. Here the four DACs are arranged as shown below.

This reference design can be configured for Two or Four DACs, achievable by a quick configuration of Jumpers on the PCBA. But care must be taken to place only one Jumper at a time.



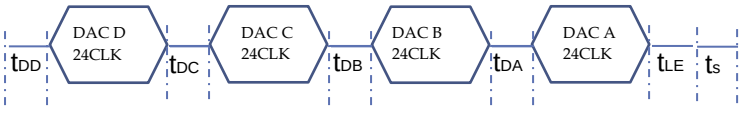
*ONLY one of these two jumpers MUST be placed at any time. Refer the Schematic and BOM for the implementation.



The SDO Pin is used to daisy chain the four devices together. As in a SPI , the rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of WRITE cycle. When the serial transfer to all the devices is complete, LATCH is made HIGH. This action transfers the data from SPI shift registers to the device internal registers of the respective DAC. The number of clocks in each frame depends on the number of devices. Each frame is of Nx24 clocks.

1. 2 DAC Frame size = 48 CLK: First 24clock for DACB and Next 24Clock for DACA.
2. 4 DAC Frame size = 96CLK First 24clock for DACD, Next 24Clock for DACC, Next 24clock for DACB, and Last 24 clock for DACA.

Total Write time estimation for a Four DAC Design:
$T = (24 \times 4 / Fs) + t_{DD} + t_{DC} + t_{DB} + t_{DA} + t_{LE} + t_S$



Where:
Fs = SPI Clock Rate in Hz.
t_{Dx} = Software overhead from host side to load the Next SPI Data for the next DAC.
t_{LE} = Software overhead from host to change the LATCH line status (as an I/O port Pin).
T_s = Analog Output Settling time (Refer Datasheet of DAC8760)

4.1.6 Filter and Protection for Surge, EFT and ESD

The output stage is designed to withstand 8kV ESD, 1kV EFT and 1kV Surge.
Every channel is protected by with TVS SMBJ18CA. This circuit clamps Over-voltage inputs ~25V The ESD protection diodes also protect against overvoltage inputs. Layout guidelines have to be followed to ensure compliance to EMC standards. The protection devices are selected to dissipate the required energy.

4.2 Power Supply

The analog output module uses 24V DC input from the IO Controller.

The LM5069 inrush current controller provides intelligent control of the power supply current during insertion and removal of Pluggable Module from a powered IO Controller. The LM5069 provides in-rush current limiting during turn-on, and monitoring of the load current for faults during normal operation. Additional functions include Under-Voltage Lock-Out (UVLO) and Over-Voltage Lock-Out (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current limit is set to 2.75A.

DAC and Op Amps are supplied by +/- 15V, which is derived from Flybuck DC-DC converter (LM5017) followed by a low noise LDO. The Flybuck DC-DC converter is designed to give +/-15V and 3.3V with a ripple of <50mV peak. A soft-start feature is implemented on LM5017 to limit the inrush current.
For a detailed Flybuck Design, refer AN-2292.

4.3 Isolation

4.3.1 Power Supply Isolation

The LM5017 based Flybuck Isolated Power supply provides the Galvanic Isolation to the IO Controller . This Isolation is required to keep the IO Controller protected from any unexpected overvoltage on the Analog Outputs field connections. The level of isolation depends on the Coupled Inductor's specification. This design utilizes a coupled Inductor of 1500VAC, Isolation.

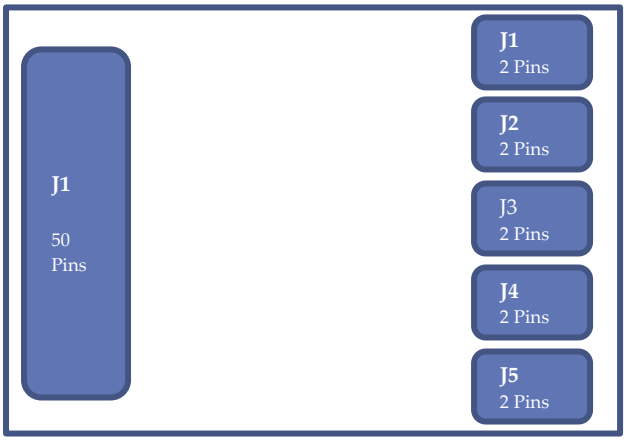
4.3.2 Digital Isolation

In order to maintain isolation from the host controller, these signals are isolated through a digital isolator. The SPI Signals isolated are: SCLK, MISO, MOSI, CSO (Latch), CLR, SDRDY.
The IO Controller is connected to the DAC by the High Speed Digital Isolator ISO7141CC and ISO7221. With this digital isolator the Host Processor on IO Controller maintains 2.5kVrms of galvanic isolation. Ten ohms termination resistance is placed near to the Isolators to maintain good Signal Integrity.

4.4 Interface

The Analog Output module has with following connectors:

1. J1 - J4 : 2 Pin Screw Terminal type 2.54mm Pitch connectors for interfacing external Loads.
2. J5 : 2 Pin Screw Terminal type 2.54mm Pitch connectors for connecting Earth Reference.
3. J6 : 50 Pin High Speed Connector for SPI/ Power Supply interface to the IO Controller .



5 Software Description

The DAC8760 has a number of 16 bit Registers. These need to be Configured / Read/ Written to achieve the desired functionality. A brief overview is as described here. For details refer the datasheet of DAC8760.

REGISTER / COMMAND	READ/WRITE ACCESS	DATA BITS (DB15:DB0)														
		15	14	13	12	11	10:9	8	7	6	5	4	3	2	1	0
Control	R/W	CLRSEL	OVR	REXT	OUTEN	SRCLK			SRSTEP			SREN	DCEN	RANGE		
Configuration	R/W	X(1)					IOUT RANGE	DUAL OUTEN	APD	Reserved	CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC Data(2)	R/W	D15:D0														
No operation(3)	—	X														
Read Operation(3)	—	X									READ ADDRESS					
Reset	W															RESET
Status	R	Reserved										CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC Gain Calibration(2)	RW	G15:G0, unsigned														
DAC Zero Calibration(2)	RW	Z15:Z0, signed														
WATCHDOG TIMER(3)	—	X														

(1) X denotes *don't care* bits.
(2) DAC8760 (16-bit version) shown. DAC7760 (12-bit version) contents are located in DB15:DB4. For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, and *watchdog timer* are commands and not registers.

1. Control and Configuration registers gives users option to select - Output Type, Range (over range), and Slew rate. It also allows user to set the following : Output, Watchdog, HART, Dual Output.
2. DAC Data Register allow user to write the digital equivalent of the desired Analog Output.
3. Read, Status and Watchdog Timer Commands allow the user to monitor the DAC function.
4. Calibration Registers: Allows the user to write the calibration values for Zero Error and Gain Error correction.
5. At power up each of the DAC needs to be initialized using CONTROL and CONFIGURATION Registers.
6. Next the DAC DATA register has to be loaded with relevant values to generate the desired Analog Output.

DAC configuration Examples

Example 1: DAC configured as Voltage Output of 0 to 10V.

To set the Voltage output Range of 0 to 10V , SSI as daisy chained, set Slew rate and Output Enable ,No Overrange the CONTROL register needs to be set as shown

Also the CONFIGURATION registers must be written for NO Dual Output, No HART,10ms Watchdog enabled, No APD , No Calibration.

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1
Configuration	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Example 2: DAC configured as Voltage Output of 0mA to 24mA

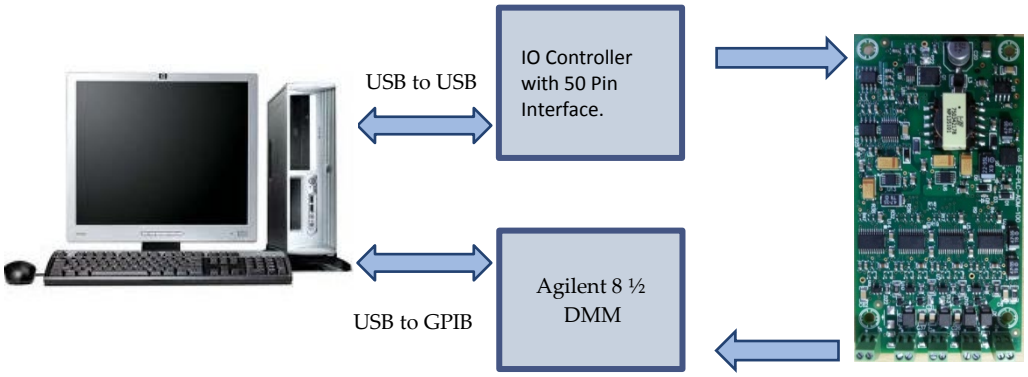
To set the Current output of 0 to 24mA, SSI as daisy chained, set Slew rate and Output Enable ,No Overrange the CONTROL register needs to be set as shown below.

Also the CONFIGURATION registers must be written for NO Dual Output, No HART,51ms Watchdog enabled, No APD , No Calibration.

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1
Configuration	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	1

6 Test Setup

6.1 Hardware Test Setup



Note : For Voltage output the Load Resistance is >10kΩ and For current output the load resistance is 250ohms.

Figure 3 Functional Test Setup

6.2 Software Test setup

The design verification setup uses a GUI based Test Setup. The GUI on the PC connects to the IO Controller through USB communication. The IO Controller then controls the Analog Output Card via SPI interface, to generate Analog Output levels as selected on the GUI. The Analog Output generated is measured by the 8 ½ DMM. The GUI does the computation of results.

The GUI is a LabView based software. It can set the below functionalities:

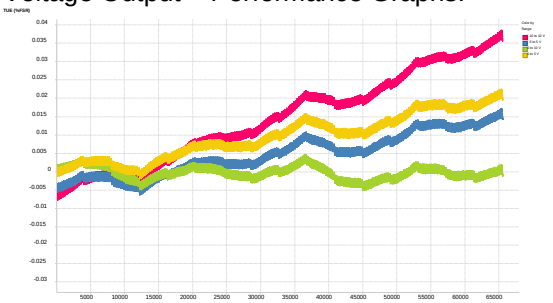
1. Analog Output Channel: There are four channels in each card.
2. Analog output Type: Each Analog Output can be selected as voltage or current type .
3. ZERO Error Correction register:
4. Gain correction Register.
5. Result Options: DNL or INL or TUE. This can be before or after the offset / gain corrections. In the results herewith the errors are not compensated for.

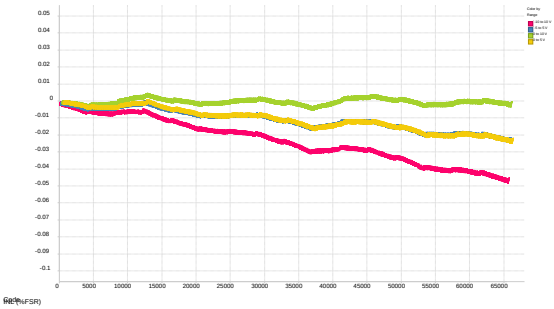
7 Test Results

7.1 Accuracy Testing

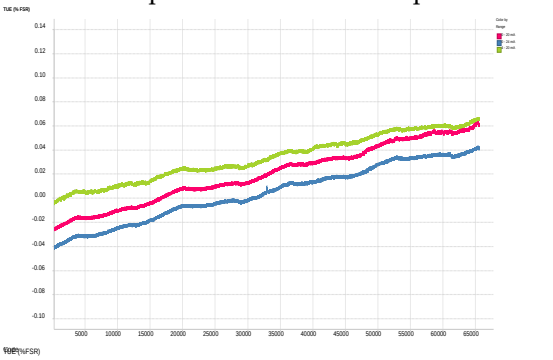
The overall accuracy depends on the performance of the different subsystems. The result below is for the integrated Analog Output Module consisting of the DAC, Power Supply, Filters, and Protections.

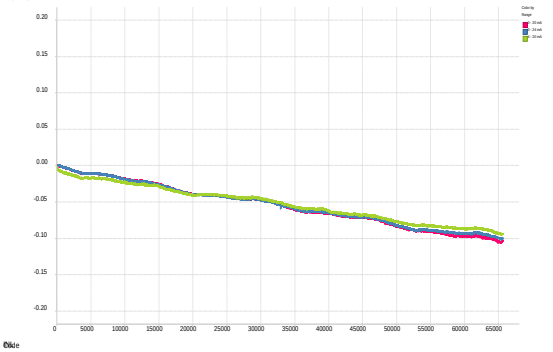
Voltage Output – Performance Graphs:





Current Output - Performance Graphs:





7.1.1 Results Summary at 25°C

The Results indicate that the overall TUE is within the target range of 0.2% FSR (Section 2)
The maximum DNL is within1LSB and the INL is within 0.2 % FSR at 25°C.

Table 1 Measurement Results Summary- Voltage Ranges.

Sr. No.	Parameter	+/-10V	0 to10V	+/- 5V	0 to 5V
1	TUE (%FSR)Max	+0.038	0.035%	0.017%	0.019%
2	TUE (%FSR)Min	-0.0083	-0.0019	-0.0064	-0.005
3	INL(%FSR)Max	-0.00045	0.00851	0.00039	0.0047
4	INL(%FSR)Min	-0.04845	-0.0249	-0.024	-0.0055
5	DNL Max	0.381	0.594	0.415	0.511
6	DNL Min	-0.555	-0.587	-0.473	-0.357

Table 2 Measurement Results Summary- Current Ranges.

Sr. No.	Parameter	4 to 20mA	0 to 20mA	0 to 24mA
1	TUE (%FSR)Max	0.327	0.291	0.257
2	TUE (%FSR)Min	-0.532	-0.309	-0.361
3	INL(%FSR)Max	0	0.0007	0.0009
4	INL(%FSR)Min	-0.106	-0.106	-0.101
5	DNL Max	0.120	0.080	0.078
6	DNL Min	0.024	-0.024	-0.024

By definition, INL for a particular code is the summation of DNL array till that code. DNL is specified in LSB and INL is specified as %FSR.

7.2 Pre compliance Testing

The Analog Output Module has been designed to meet standard EMC requirements for Industrial PLC application.

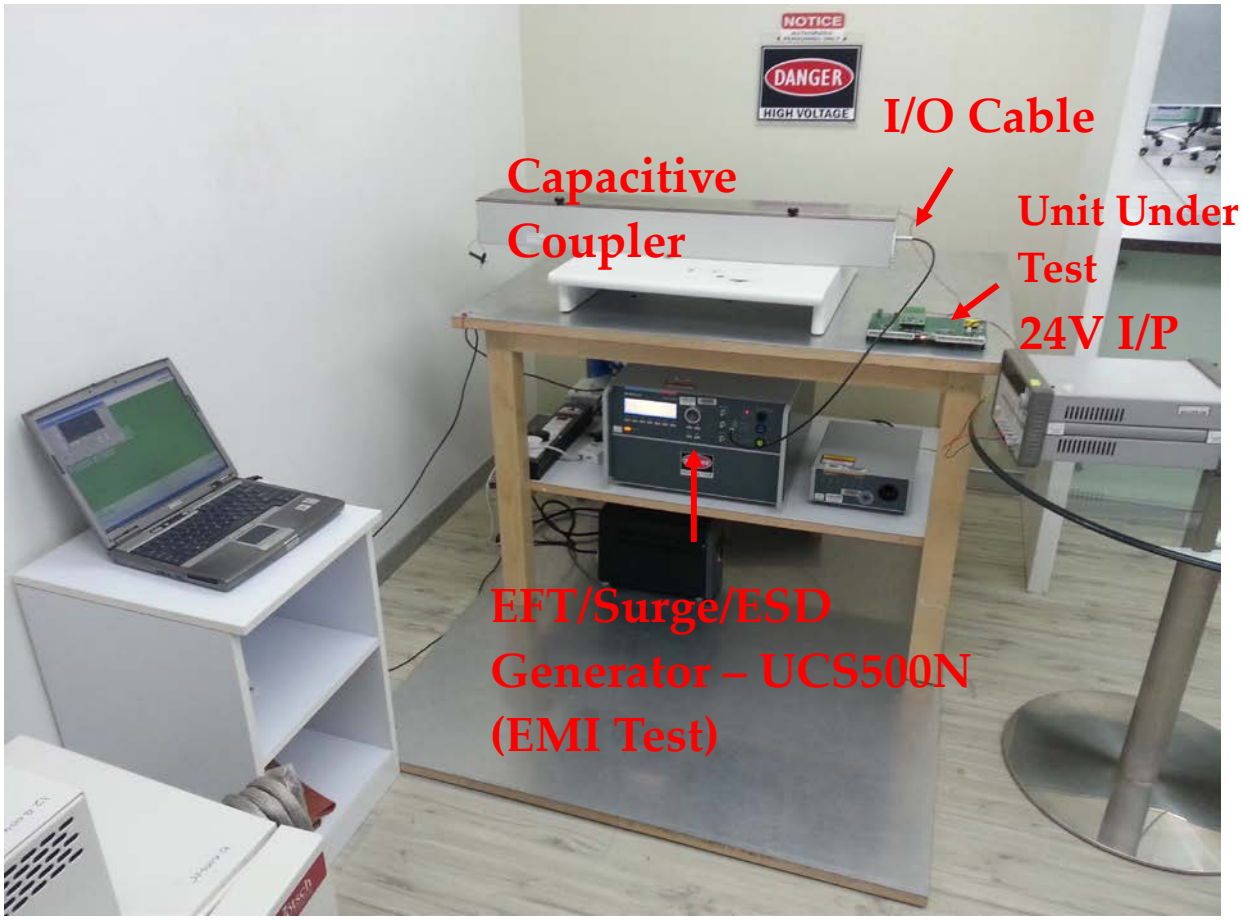
The following EMC tests have been performed

Tests	Standards
Electro Static Discharge	IEC61000-4-2
Electrical Fast Transients	IEC61000-4-4
Surge	IEC61000-4-5

Criteria and performance as per IEC61131-2

Criteria	Performance (Pass) Criteria
A	The Analog Output Module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test Analog Output Module shall continue to operate as intended without manual intervention.
C	During the test loss of functions accepted, but no destruction of hardware or software. After the test Analog Output Module shall continue to operate as intended automatically, after manual restart or power off/power on.

7.2.1 Test Set-Up



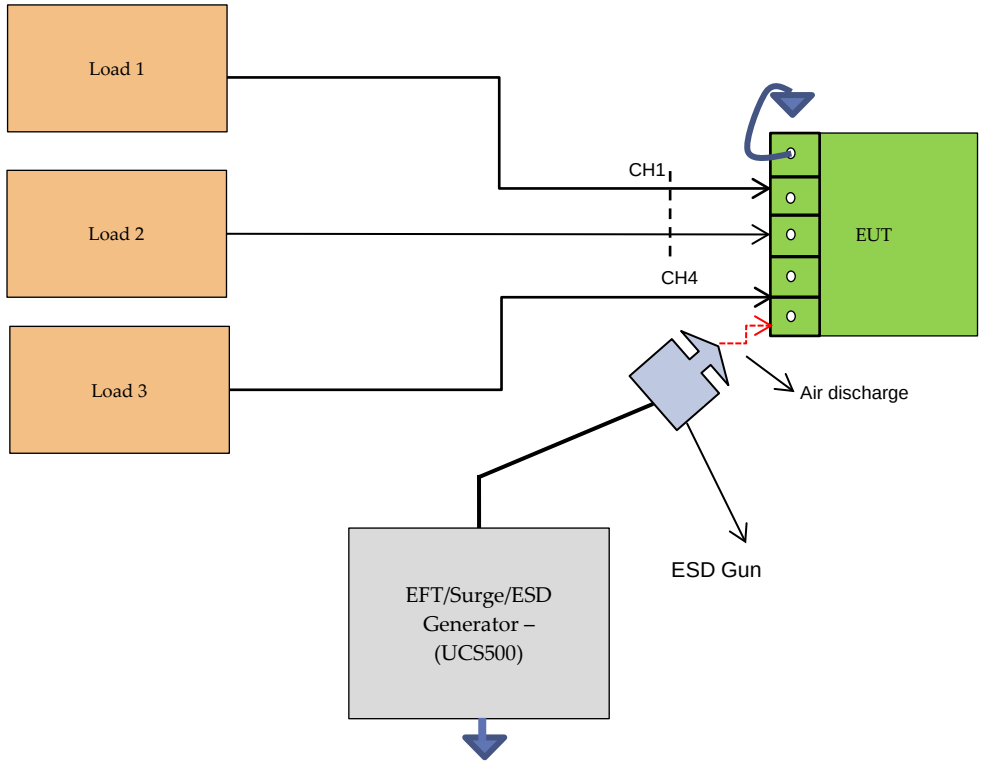
7.2.2 Electro Static Discharge (ESD): IEC61000 -4-2

The ESD level at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance (Pass Criteria)
ESD-IEC 61000-4-2	4 kV contact discharges – Level 2 8 kV air discharges – Level 3	Criteria B (Monitored before and after the test)

Setup Description

The ESD is injected to the EUT as **Contact discharge or Air discharge.**



The EUT is placed on a horizontal coupling plane (HCP) of 160 x 80cm dimensions on top of a wooden table 80cm high and located above ground reference plane. The EUT and its attached cables were isolated from the HCP by a thin insulating support of 0.5mm thickness. Electrostatic discharges were applied using an ESD gun directly (via contact or air discharges) or indirectly (via horizontal coupling plane). EUT operation was monitored after the test. The EUT is tested in active mode using unshielded 3m cables on IO ports.

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test.

Results

Test No	Test Mode	Observation*
1	Air +2kV	PASS
2	Air– 2kV	PASS
3	Air +4kV	PASS
4	Air -4kV	PASS
5	Air +6kV	PASS
6	Air -6kV	PASS
7	Air +8kV	PASS
8	Air -8kV	PASS
9	Contact +1kV	PASS
10	Contact -1kV	PASS
11	Contact +2kV	PASS
12	Contact -2kV	PASS
13	Contact +4kV	PASS
14	Contact -4kV	PASS
15	HCP +2kV	PASS
16	HCP – 2kV	PASS
17	HCP +4kV	PASS
18	HCP -4kV	PASS
19	VCP +2kV	PASS
20	VCP – 2kV	PASS
21	VCP +4kV	PASS
22	HCP -4kV	PASS

*Functionality checked before and after the test.

7.2.3 Electric Fast Transients test: EFT – IEC61000 – 4-4

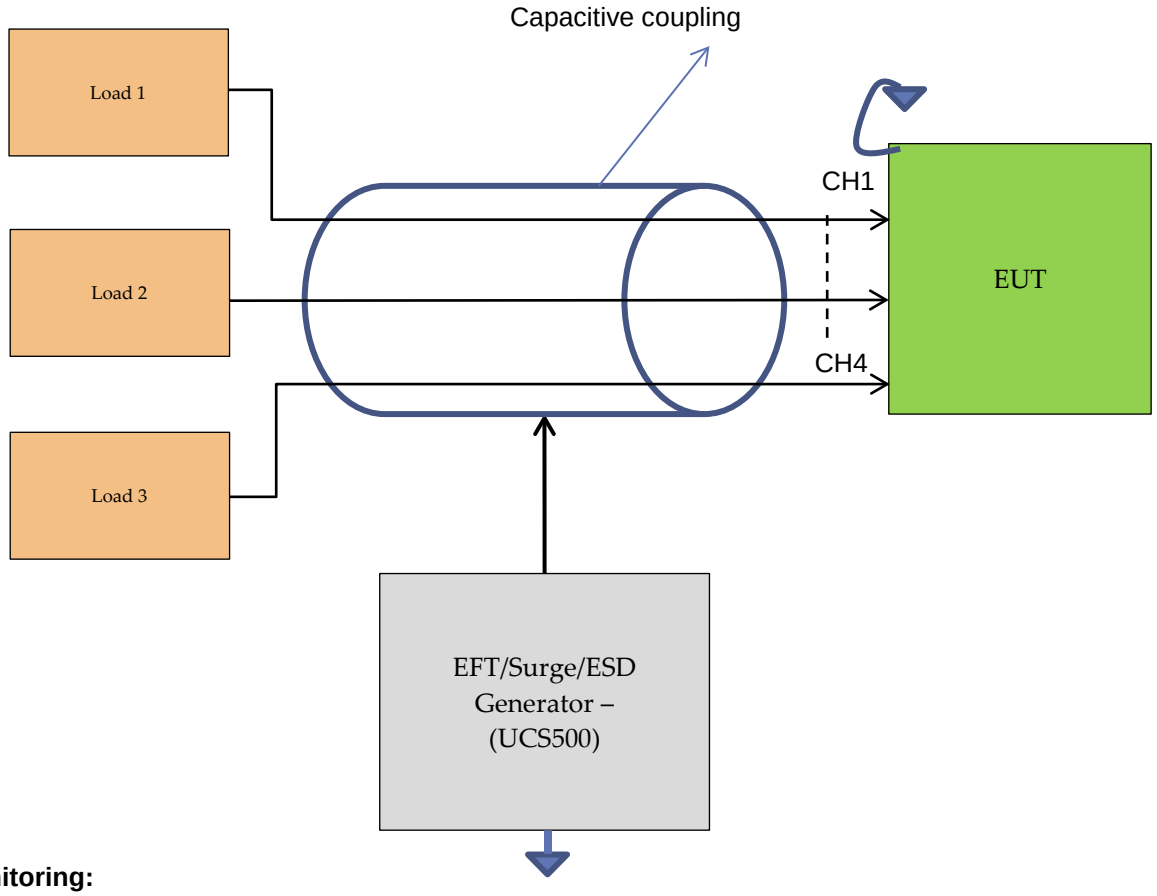
Test Level & Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance (Pass Criteria)
EFT -IEC 61000-4-4	±2 KV at 5 KHz, 100KHz on signal ports	Criteria B (Monitored before and after the test)

Description

Setup:
The EFT is injected on all cables together using a Capacitive Coupling Clamp.
EUT is connected to auxiliary sources by unshielded cables. The lengths of the cables are set to 3m and cables are placed 10cm above the reference plane. The test is carried out with the EUT placed 10cm above the reference plane on insulating material, and with the EUT placed on the reference plane.



Monitoring:

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test.

Results

Result summary to be updated with observations.

Test No	Test Mode	Observation*
1	+ 0.5 kV , 5kHz	PASS
2	- 0.5 kV , 5kHz	PASS
3	+ 1 kV , 5kHz	PASS
4	- 1 kV , 5kHz	PASS
5	+ 1.5 kV , 5kHz	PASS
6	- 1.5 kV , 5kHz	PASS
7	+ 2 kV , 5kHz	PASS
8	- 2 kV , 5kHz	PASS
9	+ 0.5 kV , 100kHz	PASS
10	- 0.5 kV , 100kHz	PASS
11	+ 1 kV , 100kHz	PASS
12	- 1 kV , 100kHz	PASS
13	+ 1.5 kV , 100kHz	PASS
14	- 1.5 kV , 100kHz	PASS
15	+ 2 kV , 100kHz	PASS
16	- 2 kV , 100kHz	PASS

*Functionality checked before and after the test.

7.2.4 SURGE- IEC61000 -4-5

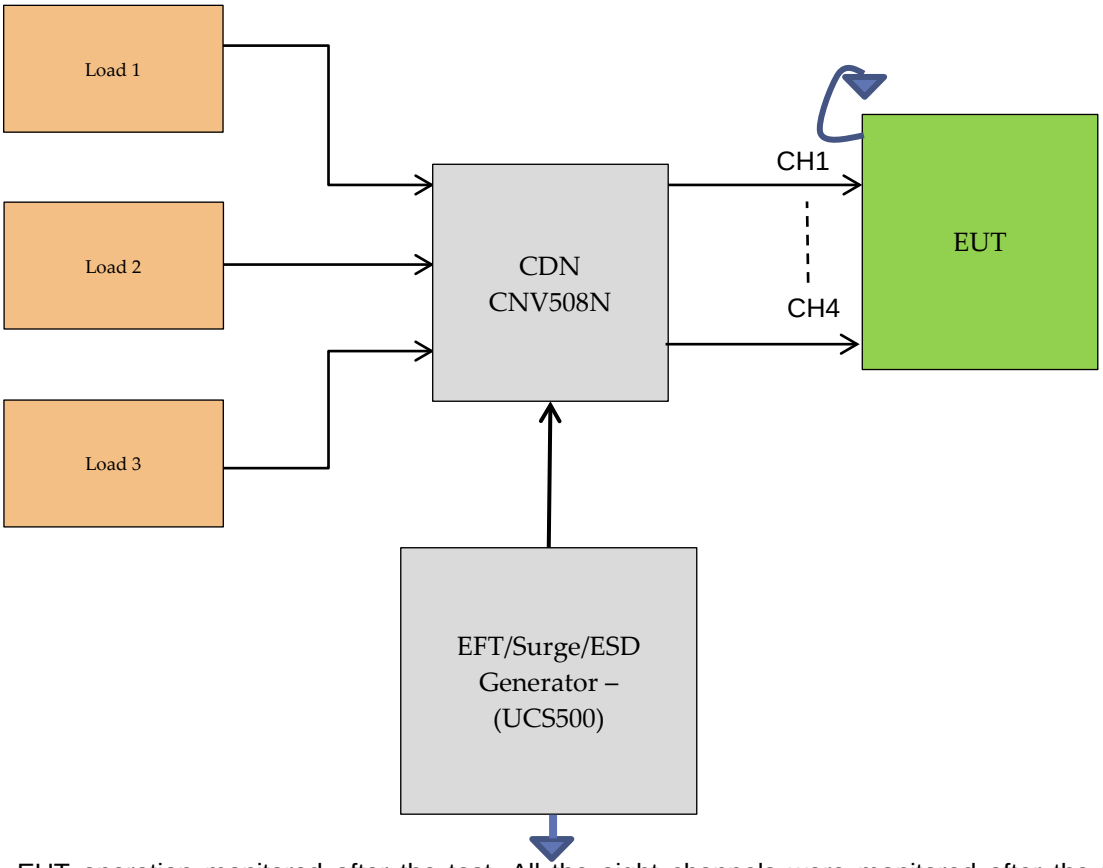
Test Level & Expected Performance

The Common-Mode Surge at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance (Pass Criteria)
Surge IEC 61000-4-5	±1kV CM on signal ports	Criteria B(Monitored before and after the test)

Description

Setup:
The EUT and analog output cable were placed on non-conductive support 10cm above a reference ground plane. Surge was injected into analog output cable (I/O cable) for testing via Coupling Decoupling Network. The EUT operation was monitored before and after the test.



EUT operation monitored after the test. All the eight channels were monitored after the test by the Microcontroller (on IO Controller) and compared with a Set Value (equivalent of the external constant voltage or current source). The Error should be within accuracy as mentioned in Section 6.3.1.
Method of monitoring:

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation - conduct a performance test.

Results

Result summary to be updated with observations.

Test No	Test Mode	Observation*
1	+ 0.5 kV	PASS
2	- 0.5 kV	PASS
3	+ 1 kV	PASS
4	- 1 kV	PASS

*Functionality checked before and after the test.

8 References

1. Texas Instruments Application Report, Noise Analysis in Operational Amplifier Circuits, SLVA043A, 1999
2. Op Amp Noise Theory and Applications Literature Number SLOA082

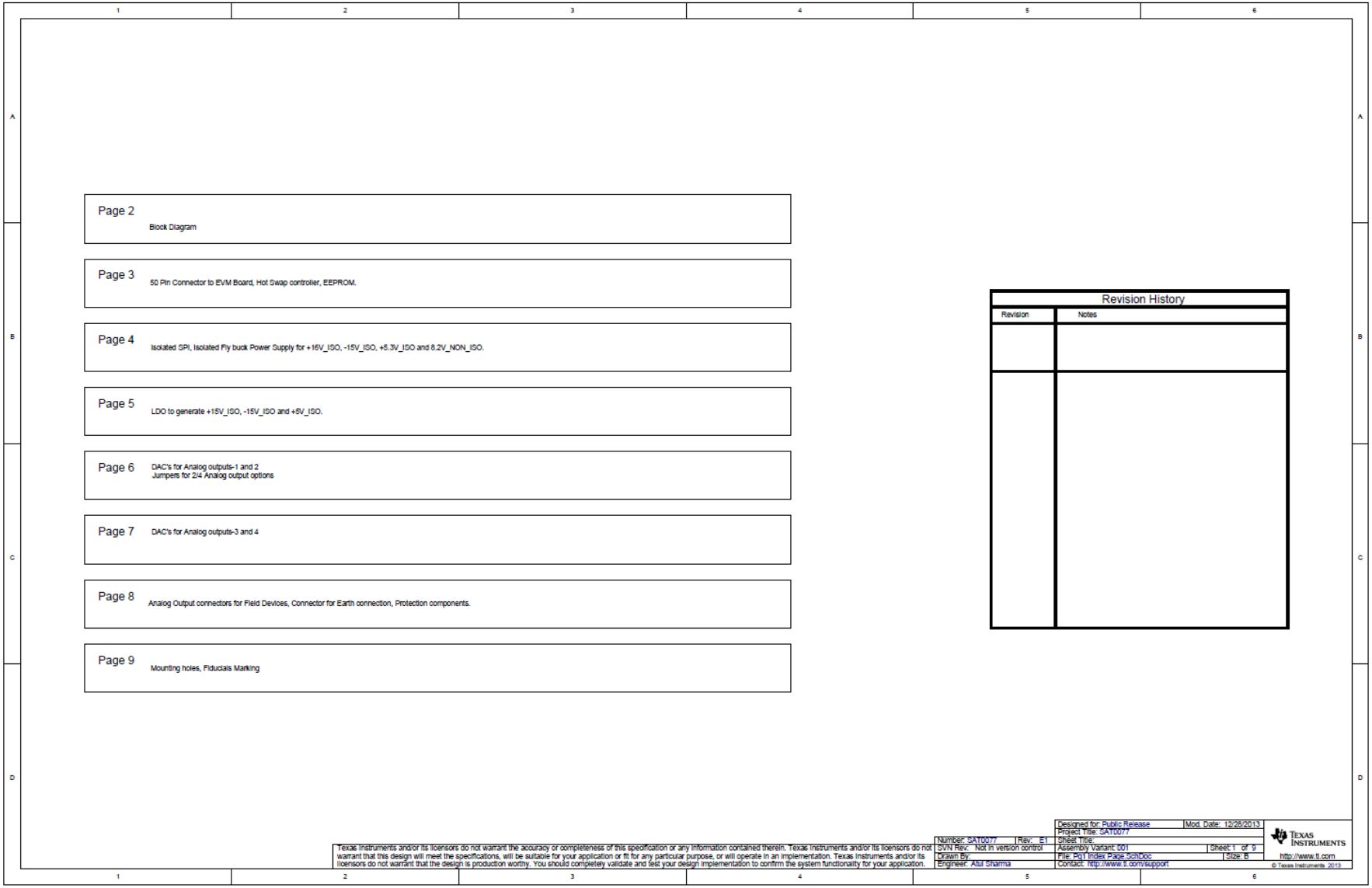
8.1.1 Terminology

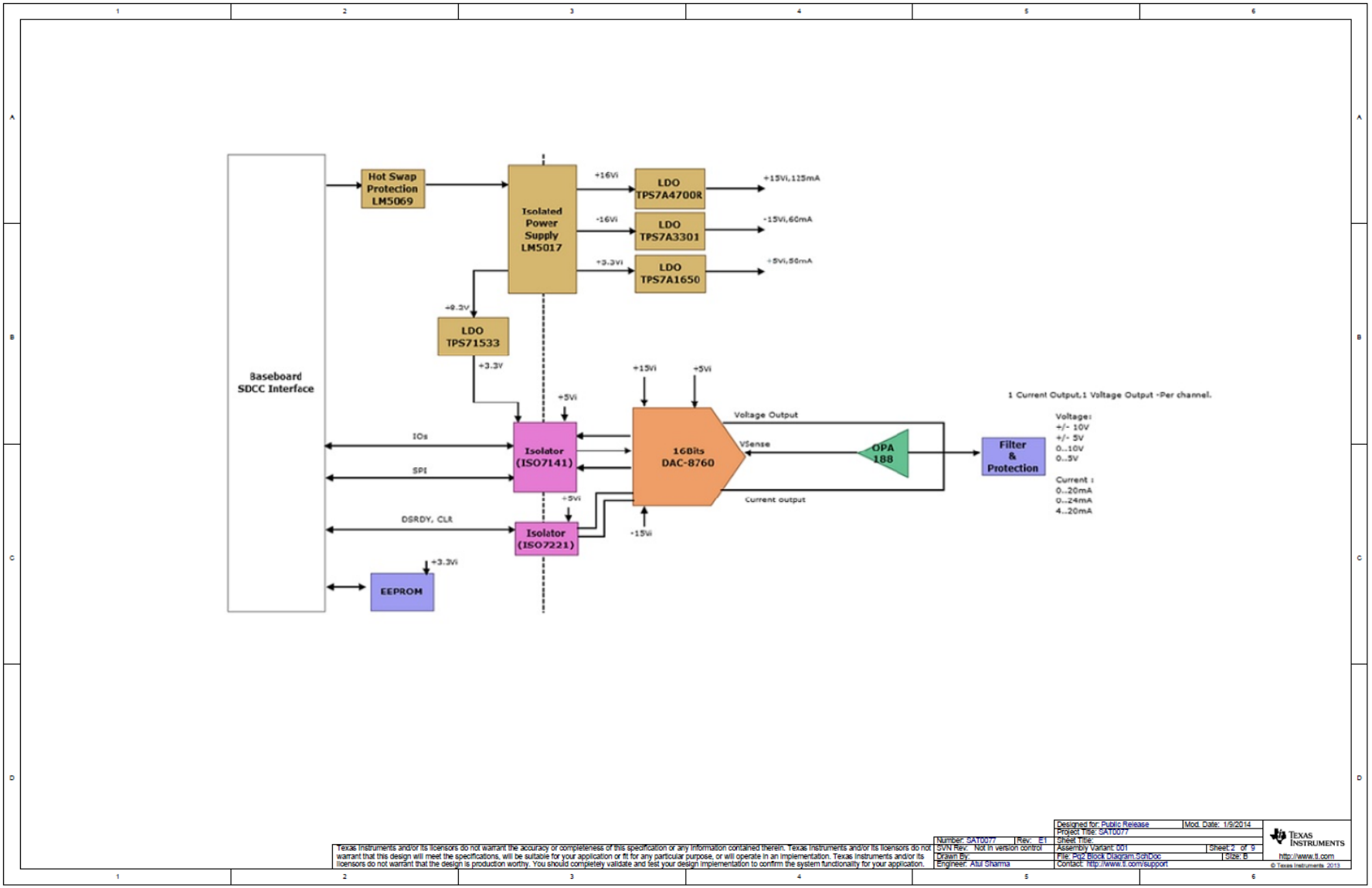
Total Unadjusted Error (TUE)
TUE is measurement error without any gain or offset error compensations. TUE gives an exact measure of the system level inaccuracies. With the right choice of components and proper PCB layout the need for Factory calibration may be avoided. This shall save a lot of time and cost during Mass Production.
TUE = sqrt (sq(Offset Error) + sq(Gain Error) + sq(DNL) + sq(INL)).

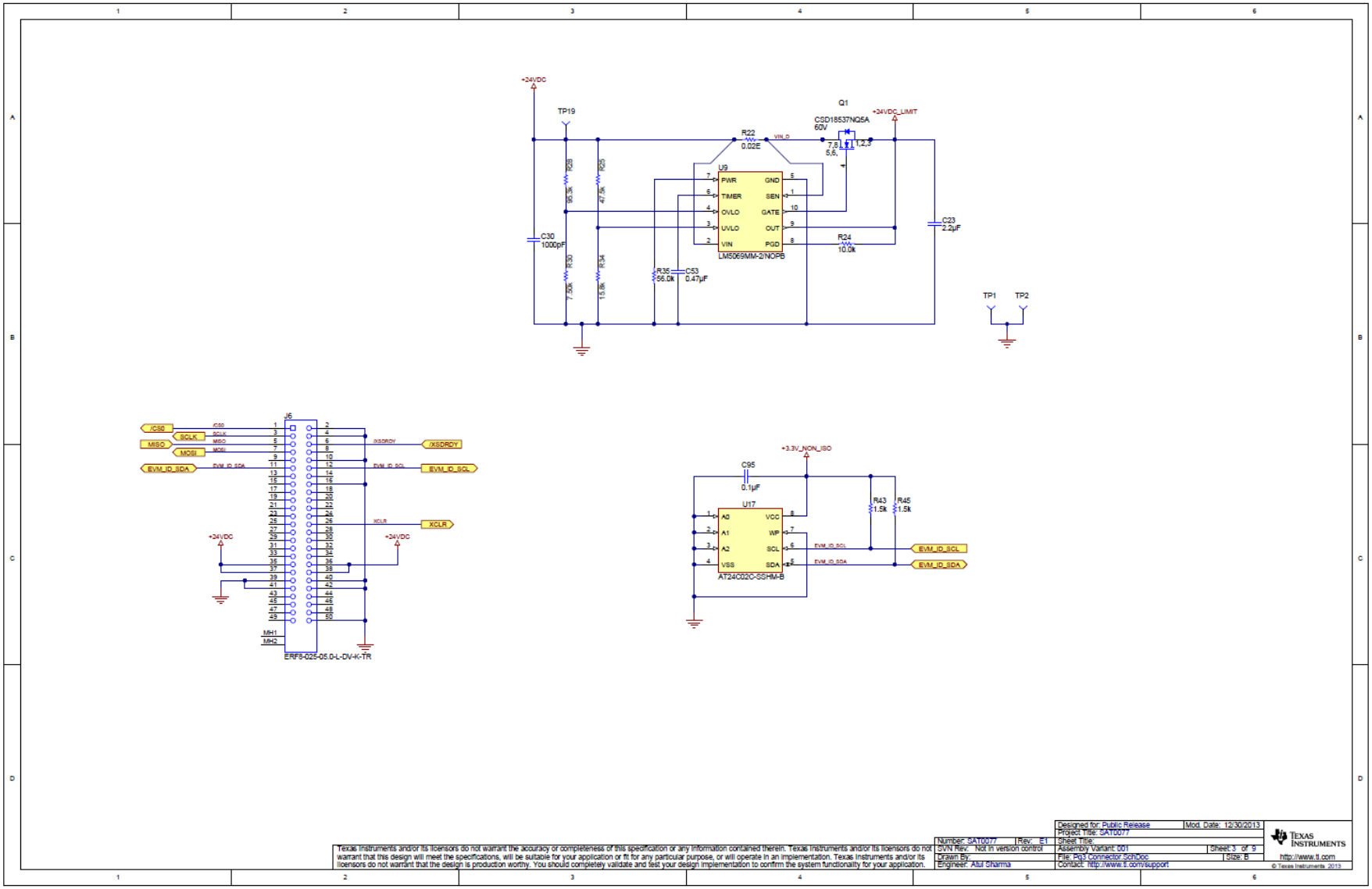
Differential Non Linearity (DNL) and Integral Non Linearity (INL)
DNL is the deviation between two analog values corresponding to adjacent digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the Differential Non-Linearity.

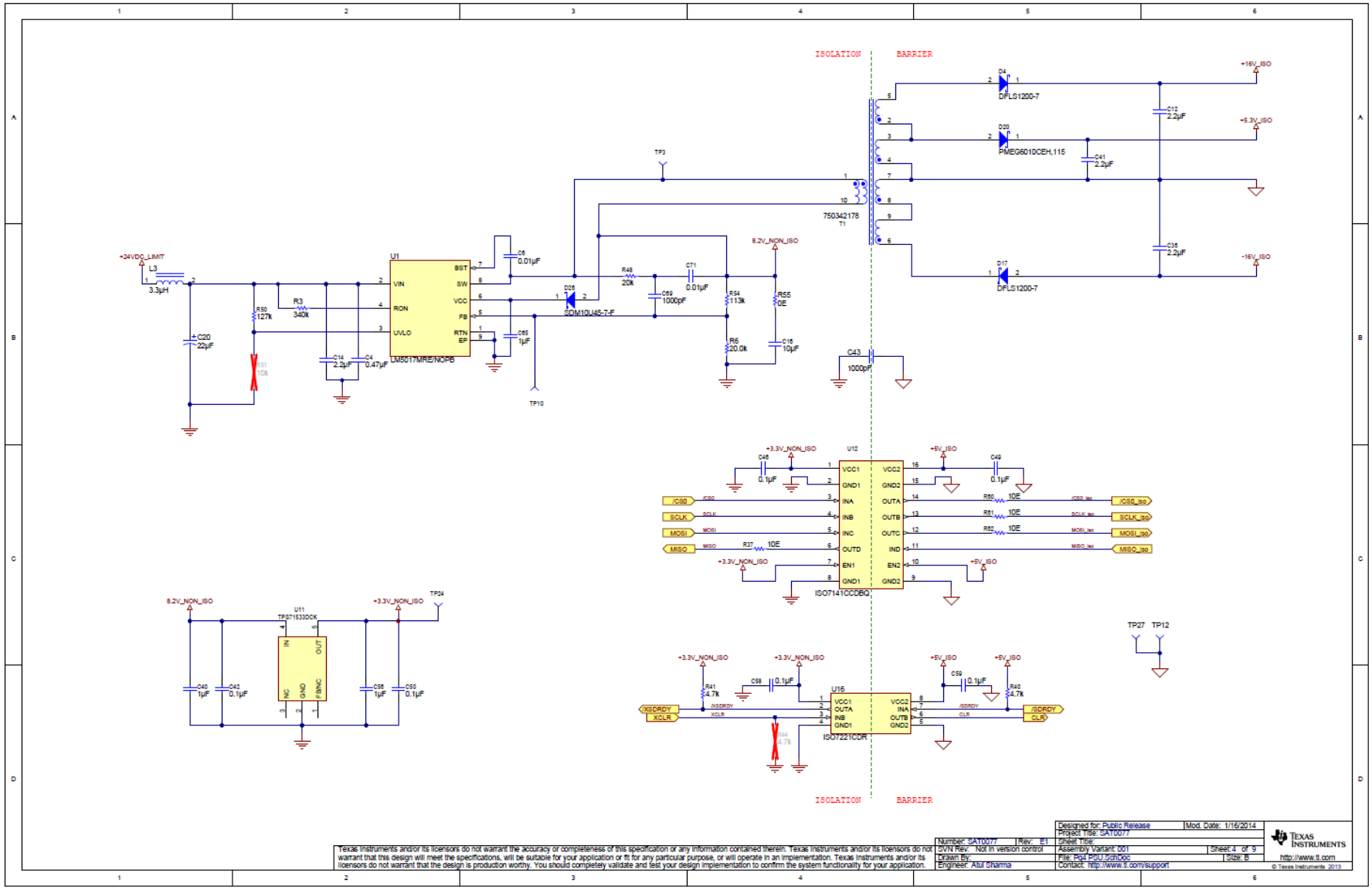
9 Design files

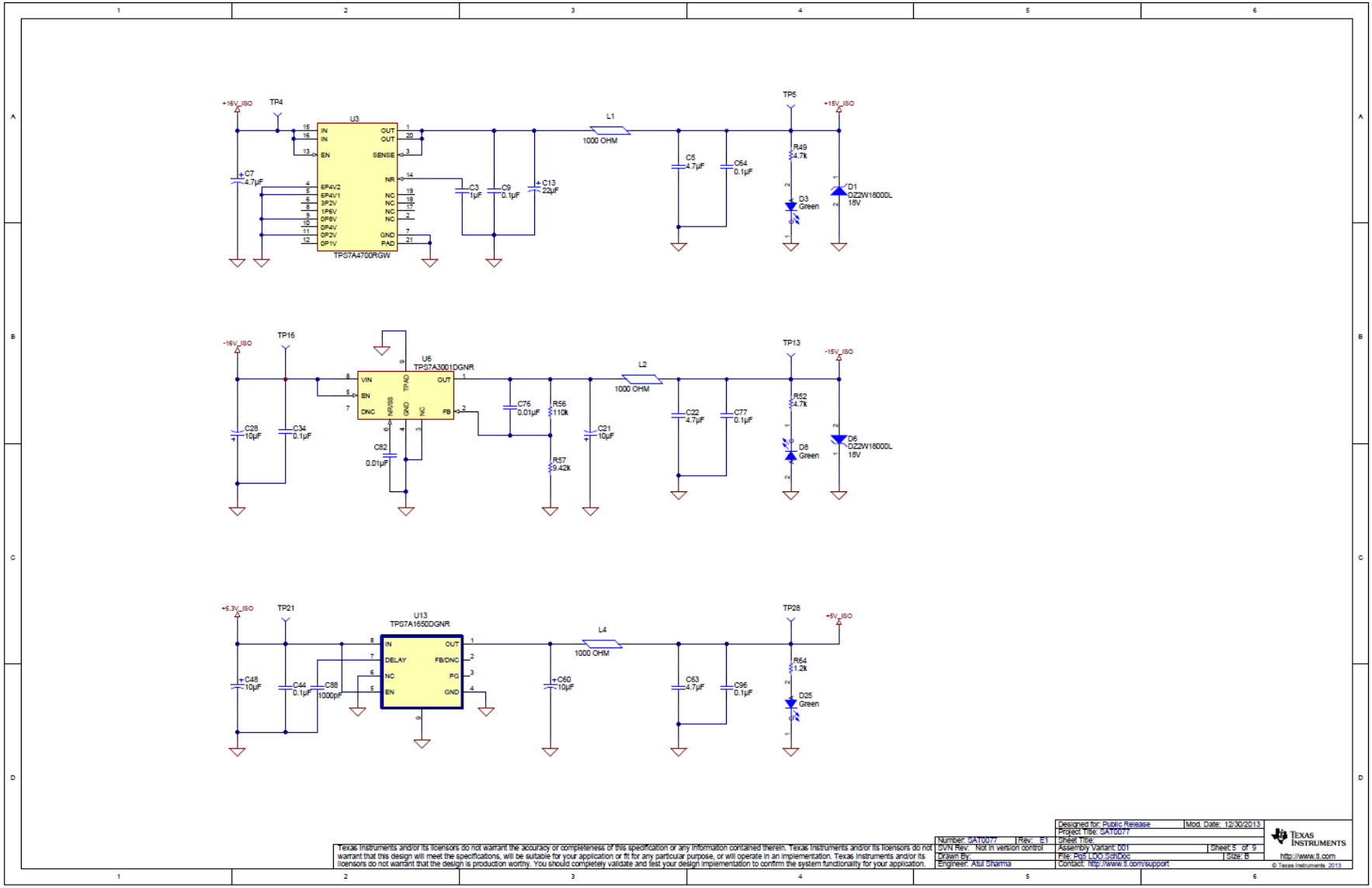
9.1 Schematics

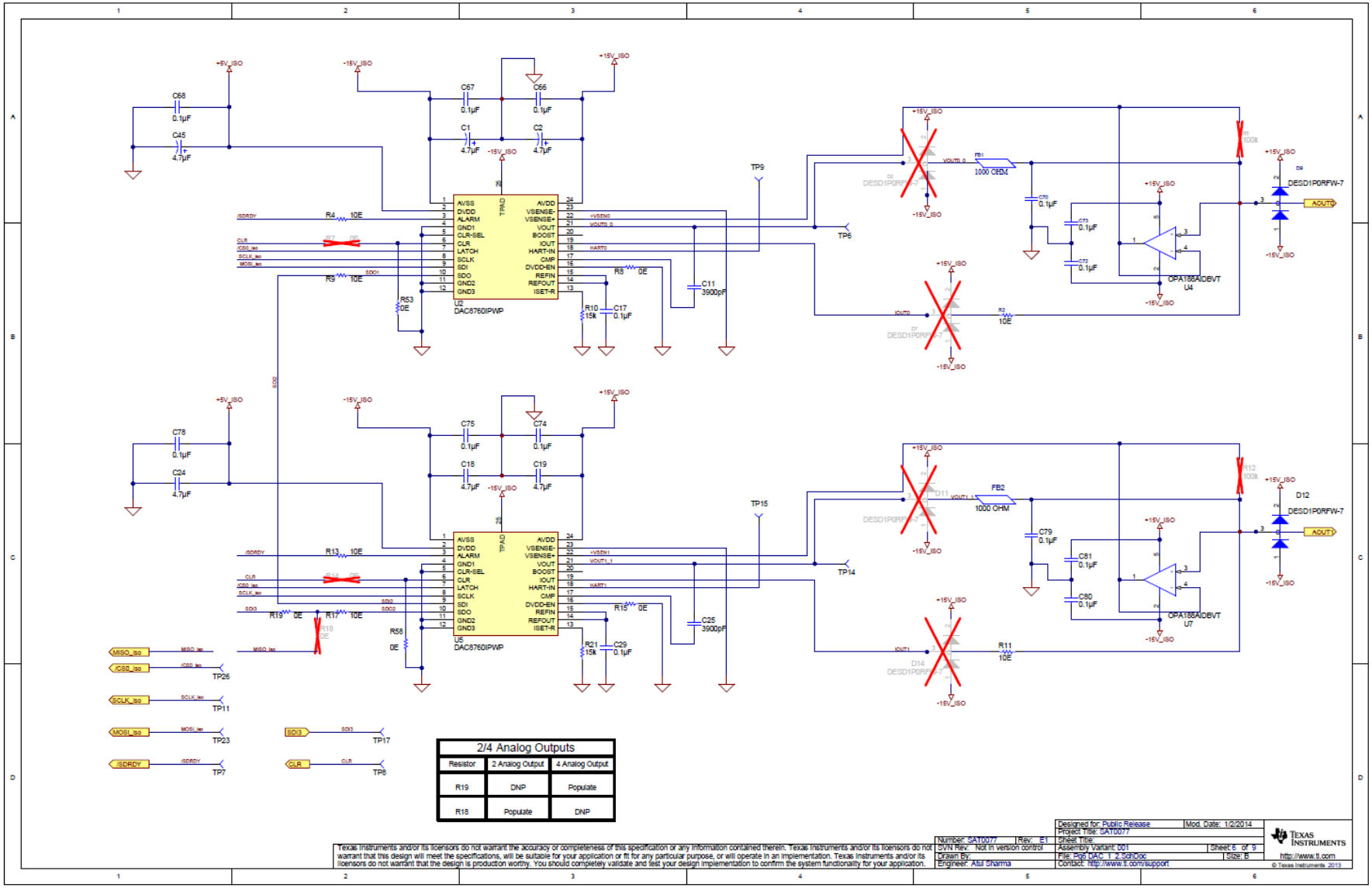


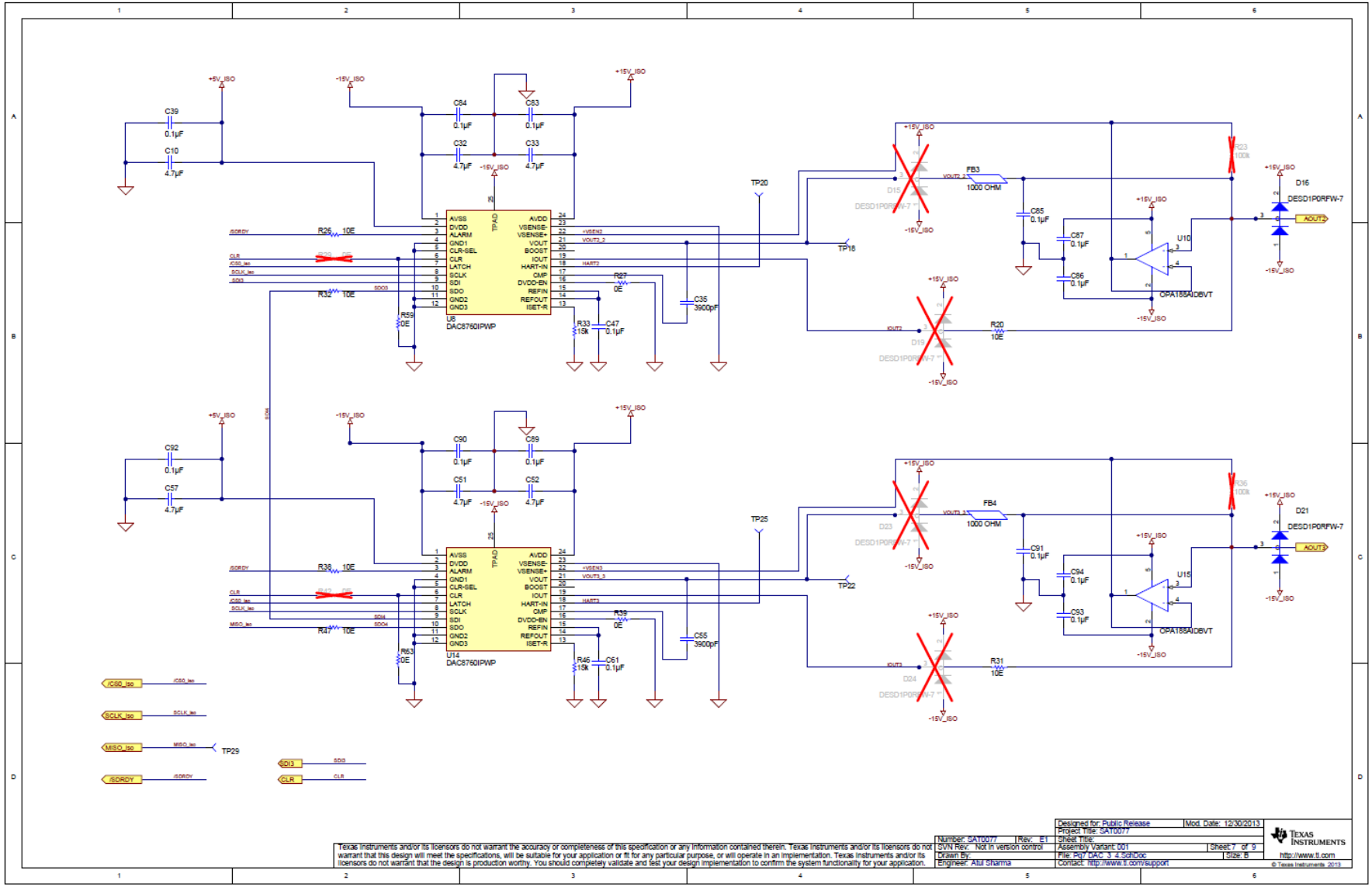


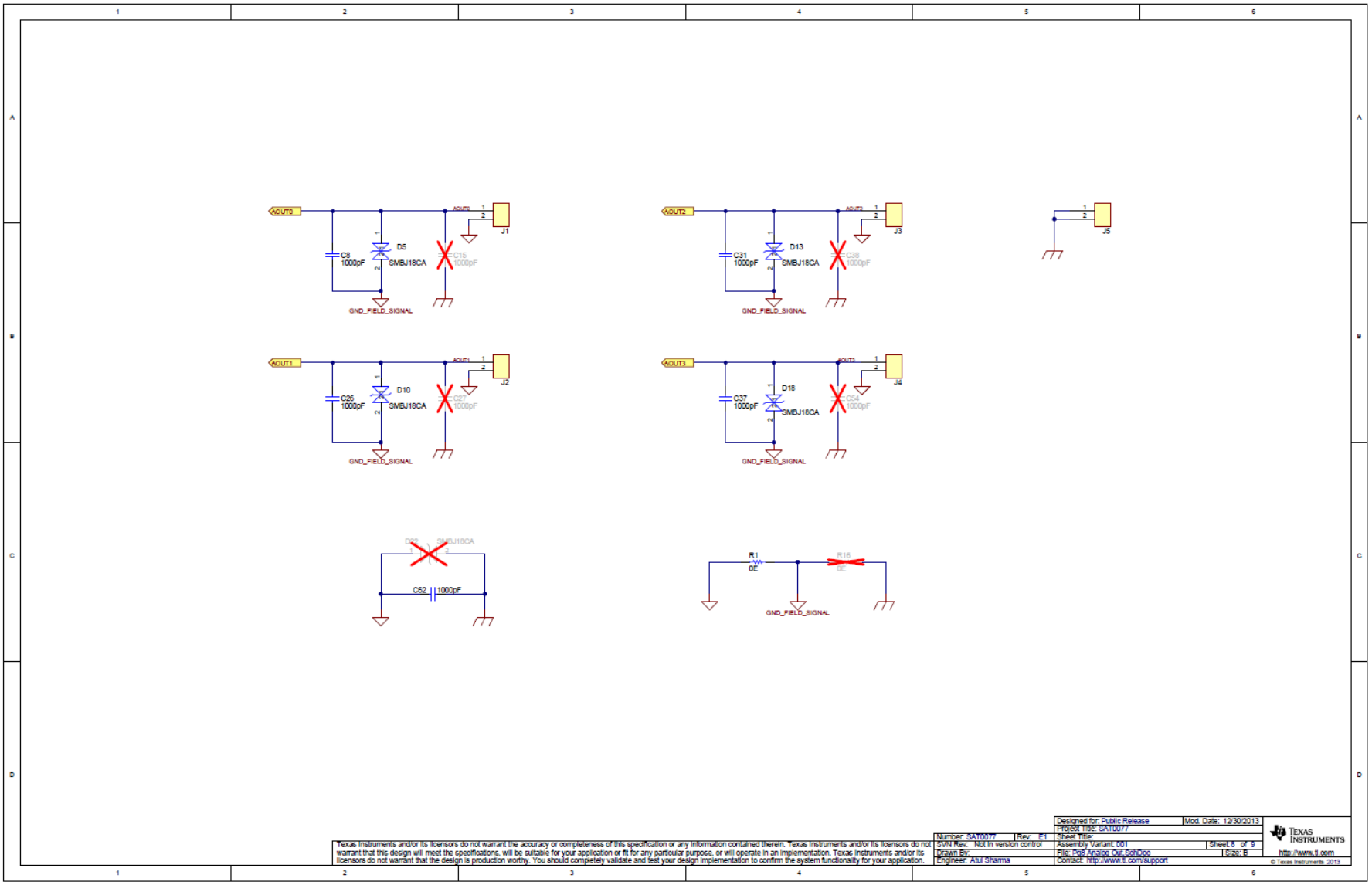


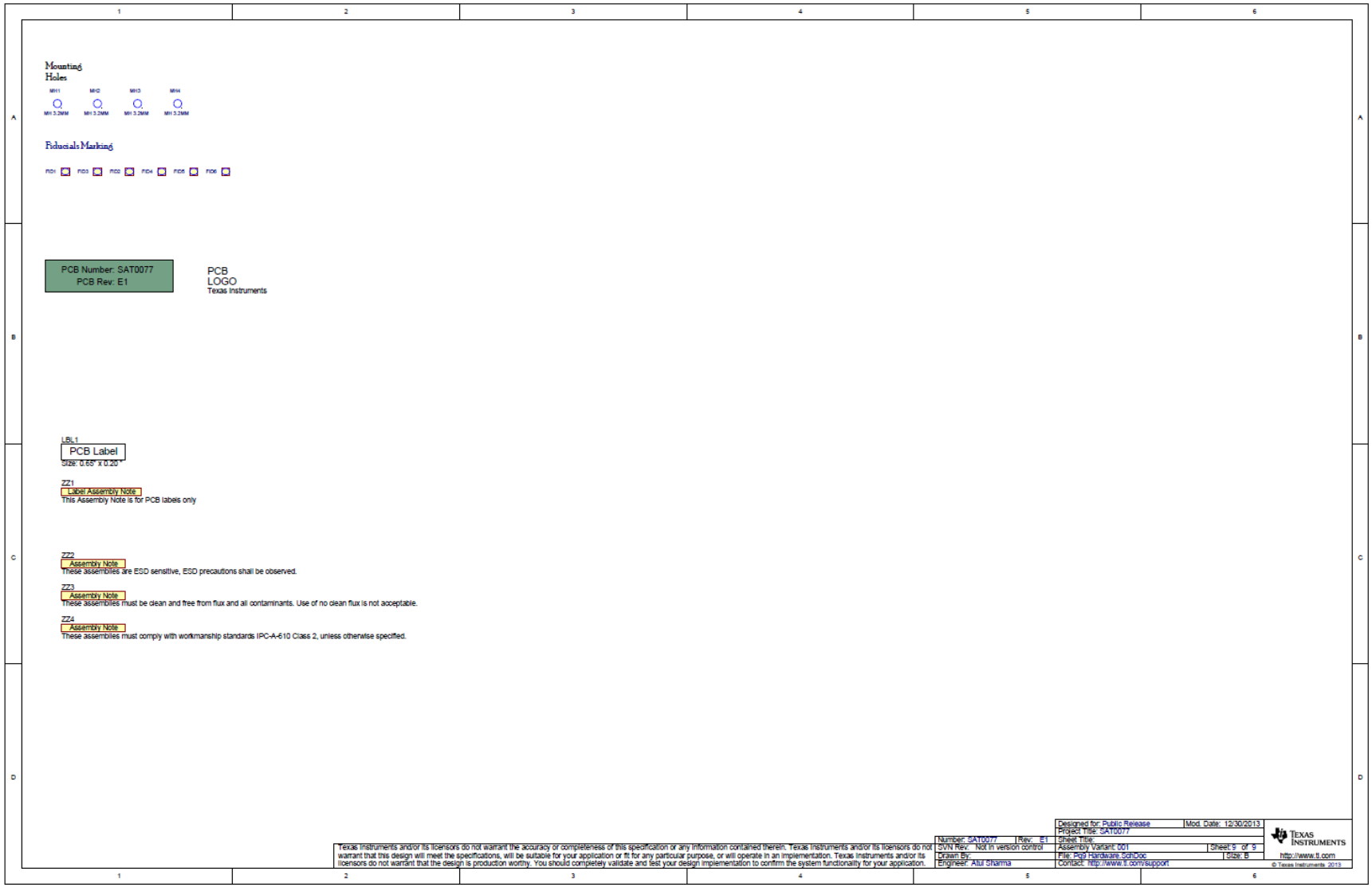












9.2 Bill of Materials

Fitted	Description	Designator	Manufacturer	PartNumber	Quantity	RoHS	Package Reference
Fitted	Printed Circuit Board	!PCB	Any	ISE-PLC-AOM-200	1	O	
Fitted	CAP, TA, 4.7uF, 35V, +/-10%, 1.9 ohm, SMD	C1, C2, C7, C45	Vishay-Sprague	293D475X9035C2TE3	4	Y	6032-28
Fitted	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603	C3, C40, C56, C65	TDK	C1608X7R1E105K080AB	4	Y	0603
Fitted	CAP, CERM, 0.47uF, 100V, +/-10%, X7R, 1206	C4	TDK	C3216X7R2A474K	1	Y	1206
Fitted	CAP, CERM, 4.7uF, 50V, +/-10%, X5R, 0805	C5, C10, C18, C19, C22, C24, C32, C33, C51, C52, C57, C63	TDK	C2012X5R1H475K125AB	12	Y	0805
Fitted	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	C6, C71, C76, C82	AVX	06031C103JAT2A	4	Y	0603
Fitted	CAP, CERM, 1000pF, 2KV 10% X7R 1206	C8, C26, C31, C37, C43, C62	Johanson Dielectrics Inc	202R18W102KV4E	6	Y	1206
Fitted	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	C9, C17, C29, C34, C39, C42, C44, C46, C47, C49, C50, C58, C59, C61, C64, C66, C67, C68, C70, C72, C73, C74, C75, C77, C78, C79, C80, C81, C83, C84, C85, C86, C87, C89, C90, C91, C92, C93, C94, C95, C96	AVX	06035C104KAT2A	41	Y	0603
Fitted	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0805	C11, C25, C35, C55	AVX	08055C392KAT2A	4	Y	0805
Fitted	CAP, CERM, 2.2uF, 25V, +/-10%, X5R, 0805	C12, C36, C41	MuRata	GRM219R61E225KA12D	3	Y	0805
Fitted	CAP, TA, 22uF, 35V, +/-10%, 0.6 ohm, SMD	C13	Vishay-Sprague	293D226X9035D2TE3	1	Y	7343-31
Fitted	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	C14, C23	MuRata	GRM32ER72A225KA35L	2	Y	1210
Fitted	CAP, CERM, 10uF, 16V, +/-20%, X5R, 0805	C16	AVX	0805YD106MAT2A	1	Y	0805
Fitted	CAP, AL, 22uF, 50V, +/-20%, 0.88 ohm, SMD	C20	Panasonic	EEE-FK1H220P	1	Y	SMT Radial D
Fitted	CAP, TA, 10uF, 35V, +/-10%, 1.6 ohm, SMD	C21, C28, C48, C60	Vishay-Sprague	293D106X9035C2TE3	4	Y	6032-28
Fitted	CAP, CERM, 1000pF, 100V, +/-5%, X7R, 0603	C30, C69, C88	AVX	06031C102JAT2A	3	Y	0603
Fitted	CAP, CERM, 0.47uF, 50V, 10%, X5R, 0603	C53	Taiyo Yuden	UMK107ABJ474KA-T	1	Y	0603
Fitted	Diode, Zener, 18V, 1W, SOD-123	D1, D6	Panasonic	DZ2W18000L	2	Y	SOD-123
Fitted	LED SmartLED Green 570NM	D3, D8, D25	OSRAM	LG L29K-G2J1-24-Z	3		0603
Fitted	Diode, Schottky, 200V, 1A, PowerDI123	D4, D17	Diodes Inc.	DFLS1200-7	2	Y	PowerDI123
Fitted	TVS 18 VOLT 600 WATT BI-DIR SMB	D5, D10, D13, D18	Littelfuse Inc	SMBJ18CA	4		SMB
Fitted	Diode, P-N, 70V, 0.2A, SOT-323	D9, D12, D16, D21	Diodes Inc	DESD1P0RFW-7	4	Y	SOT-323
Fitted	Diode, Schottky, 60V, 1A, SOD-123F	D20	NXP Semiconductor	PMEG6010CEH,115	1	Y	SOD-123F
Fitted	Diode, Schottky, 45V, 0.1A, SOD-523	D26	Diodes Inc.	SDM10U45-7-F	1	Y	SOD-523
Fitted	FERRITE CHIP 1000 OHM 300MA 0603	FB1, FB2, FB3, FB4	TDK Corporation	MMZ1608Y102B	4	Y	0603

Fitted	Description	Designator	Manufacturer	PartNumber	Quantity	RoHS	Package Reference
Fitted	[NoValue], [NoValue], [NoValue], [NoValue], [NoValue], [NoValue], Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm	FID1, FID2, FID3, FID4, FID5, FID6, MH1, MH2, MH3, MH4			10		
Fitted	Terminal Block, 4x1, 2.54mm, TH	J1, J2, J3, J4, J5	On Shore Technology Inc	OSTVN02A150	5	Y	TERM_BLK, 2pos, 2.54mm
Fitted	Receptacle, 0.8mm, 25x2, SMT	J6	Samtec	ERF8-025-05.0-L-DV-K-TR	1	Y	25x2 Socket Strip
Fitted	FERRITE CHIP 1000 OHM 300MA 0603	L1, L2, L4	TDK Corporation	MMZ1608B102C	3	Y	0603
Fitted	Inductor, Chip, ±10%	L3	Panasonic	ELJ-EA3R3MF	1		1210
Fitted	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	Brady	THT-14-423-10	1	Y	PCB Label 0.650"H x 0.200"W
Fitted	MOSFET, N-CH, 60V, 50A, SON 5x6mm	Q1	Texas Instruments	CSD18537NQ5A	1	Y	SON 5x6mm
Fitted	RES, 0 ohm, 5%, 0.25W, 1206	R1	Vishay-Dale	CRCW12060000Z0EA	1	Y	1206
Fitted	RES, 10 ohm, 5%, 0.25W, 1206	R2, R11, R20, R31	Vishay-Dale	CRCW120610R0JNEA	4	Y	1206
Fitted	RES, 340k ohm, 1%, 0.1W, 0603	R3	Vishay-Dale	CRCW0603340KFKEA	1	Y	0603
Fitted	RES, 10 ohm, 5%, 0.063W, 0402	R4, R9, R13, R17, R26, R32, R37, R38, R47, R60, R61, R62	Vishay-Dale	CRCW040210R0JNED	12	Y	0402
Fitted	RES, 20.0k ohm, 1%, 0.1W, 0603	R6	Yageo America	RC0603FR-0720KL	1	Y	0603
Fitted	RES, 0 ohm, 5%, 0.063W, 0402	R8, R15, R19, R27, R39, R53, R55, R58, R59, R63	Vishay-Dale	CRCW04020000Z0ED	10	Y	0402
Fitted	RES, 15k ohm, 1/10W 0.1% 0603	R10, R21, R33, R46	Vishay-Dale	RT0603BRB0715KL	4	Y	0603
Fitted	RES, 0.02 ohm, 1%, 1W, 1206	R22	Susumu Co Ltd	PRL1632-R020-F-T1	1	Y	1206
Fitted	RES, 10.0k ohm, 1%, 0.1W, 0603	R24	Vishay-Dale	CRCW060310K0FKEA	1	Y	0603
Fitted	RES, 47.5k ohm, 1%, 0.1W, 0603	R25	Vishay-Dale	CRCW060347K5FKEA	1	Y	0603
Fitted	RES, 95.3k ohm, 1%, 0.1W, 0603	R28	Vishay-Dale	CRCW060395K3FKEA	1	Y	0603
Fitted	RES, 7.50k ohm, 1%, 0.1W, 0603	R30	Vishay-Dale	CRCW06037K50FKEA	1	Y	0603
Fitted	RES, 15.8k ohm, 1%, 0.1W, 0603	R34	Vishay-Dale	CRCW060315K8FKEA	1	Y	0603
Fitted	RES, 56.0k ohm, 0.1%, 0.1W, 0603	R35	Susumu Co Ltd	RG1608P-563-B-T5	1	Y	0603
Fitted	RES, 4.7k ohm, 5%, 0.1W, 0603	R40, R41, R49, R52	Vishay-Dale	CRCW06034K70JNEA	4	Y	0603
Fitted	RES, 1.5k ohm, 5%, 0.063W, 0402	R43, R45	Vishay-Dale	CRCW04021K50JNED	2	Y	0402
Fitted	RES, 20k ohm, 5%, 0.1W, 0603	R48	Vishay-Dale	CRCW060320K0JNEA	1	Y	0603
Fitted	RES, 127k ohm, 1%, 0.1W, 0603	R50	Vishay-Dale	CRCW0603127KFKEA	1	Y	0603

Fitted	Description	Designator	Manufacturer	PartNumber	Quantity	RoHS	Package Reference
Fitted	RES, 113k ohm, 1%, 0.1W, 0603	R54	Vishay-Dale	CRCW0603113KFKEA	1	Y	0603
Fitted	RES, 110k ohm, 1%, 0.063W, 0402	R56	Vishay-Dale	CRCW0402110KFKED	1	Y	0402
Fitted	RES, 9.42k ohm, 1%, 0.063W, 0402	R57	Vishay-Dale	TNPW04029K42BEED	1	Y	0402
Fitted	RES, 1.2k ohm, 5%, 0.063W, 0402	R64	Vishay-Dale	CRCW04021K20JNED	1	Y	0402
Fitted	Transformer, 50uH, SMT	T1	Wurth Elektronik eiSos	750342178	1	Y	17.75x12.7x13.46mm
Fitted	Test Point, O.040 Hole	TP1, TP2, TP12, TP19, TP27	Standard	Standard	5		
Fitted	Test Point 40mil pad 20mil drill	TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP13, TP14, TP15, TP16, TP17, TP18, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP28, TP29	STD	STD	24		
Fitted	100V, 600mA Constant On-Time Synchronous Buck Regulator, DDA0008B	U1	Texas Instruments	LM5017MRE/NOPB	1	Y	DDA0008B
Fitted	1-Channel, 16-Bit, Programmable Current/Voltage Output DAC for 4-20mA Current Loop Applications	U2, U5, U8, U14	Texas Instruments	DAC8760IPWP	4	Y	HTSSOP (PWP) 24
Fitted	36-V, 1-A, 4.17-µVRMS, RF LDO Voltage Regulator, RGW0020A	U3	Texas Instruments	TPS7A4700RGW	1	Y	RGW0020A
Fitted	Precision, Low Noise, Rail-to-Rail Output, 36V Zero-Drift Operational Amplifier	U4, U7, U10, U15	Texas Instruments	OPA188AIDBVT	4	Y	SOT-23 (DBV) 5
Fitted	-36V, -200mA, Ultralow-Noise, Negative Linear Regulator	U6	Texas Instruments	TPS7A3001DGNR	1	Y	MSOP-PowerPAD (DGN) | 8
Fitted	Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	U9	National Semiconductor	LM5069MM-2/NOPB	1	Y	MUB10A
Fitted	50 mA, 24 V, 3.2-mA Supply Current Low-Dropout Linear Regulator, DCK0005A	U11	Texas Instruments	TPS71533DCK	1	Y	DCK0005A
Fitted	4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	U12	Texas Instruments	ISO7141CCDBQ	1	Y	DBQ0016A
Fitted	IC, 60-V, 6-A IQ, 100-mA, LDO Voltage Regulator with Enable and Power-Good Functions	U13	TI	TPS7A1650DGNR	1		HTSSOP8
Fitted	25 Mbps Dual Channels, 1 / 1, Digital Isolator, 3.3 V / 5 V, -40 to +125 degC, 8-pin SOIC (D), Green (RoHS & no Sb/Br)	U16	Texas Instruments	ISO7221CDR	1		D0008A
Fitted	IC, EEPROM, 2KBIT, 1MHZ, SOIC-8	U17	Atmel	AT24C02C-SSHM-B	1	Y	SOIC-8
Not Fitted	CAP, CERM, 1000pF, 2KV 10% X7R 1206	C15, C27, C38, C54	Johanson Dielectrics Inc	202R18W102KV4E	0	Y	1206
Not Fitted	Diode, P-N, 70V, 0.2A, SOT-323	D2, D7, D11, D14, D15, D19, D23, D24	Diodes Inc	DESD1P0RFW-7	0	Y	SOT-323
Not	TVS 18 VOLT 600 WATT BI-DIR SMB	D22	Littelfuse Inc	SMBJ18CA	0		SMB

Fitted	Description	Designator	Manufacturer	PartNumber	Quantity	RoHS	Package Reference
Fitted							
Not Fitted	RES, 100k ohm, 1%, 0.125W, 0805	R5, R12, R23, R36	Vishay-Dale	CRCW0805100KFKEA	0	Y	0805
Not Fitted	RES, 0 ohm, 5%, 0.063W, 0402	R7, R14, R18, R29, R42	Vishay-Dale	CRCW04020000Z0ED	0	Y	0402
Not Fitted	RES, 0 ohm, 5%, 0.25W, 1206	R16	Vishay-Dale	CRCW12060000Z0EA	0	Y	1206
Not Fitted	RES, 4.7k ohm, 5%, 0.1W, 0603	R44	Vishay-Dale	CRCW06034K70JNEA	0	Y	0603
Not Fitted	RES, 10k ohm, 5%, 0.1W, 0603	R51	Yageo America	RC0603JR-0710KL	0	Y	0603

9.3 PCB Layout

The Analog Output module is implemented in 4 layers PCB. For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low impedance, low-inductance traces should be used along the output signal path and protection elements. When possible copper pours are used in place of traces. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions

9.3.1 Layout Recommendations

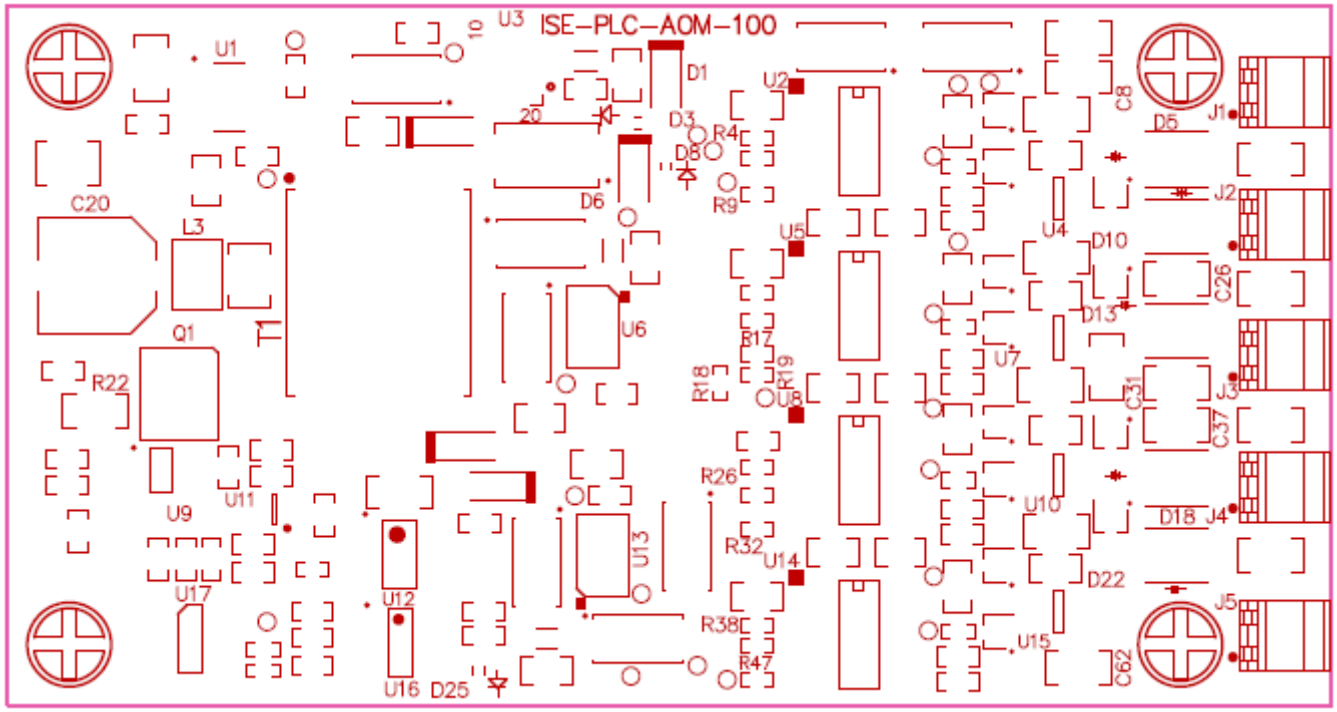
In order to achieve a high performance, the below Layout Guidelines are recommended

1. Ensure that protection elements such as TVS diodes, capacitors are placed as close to connectors as possible to ensure that return current from high-energy transients does not cause damage to sensitive devices. Further use large and wide traces to ensure a low-impedance path for high-energy transients.
2. Place the decoupling capacitors close to supply pin of IC.
3. It is recommended to use multiple vias for power and ground for decoupling caps.
4. Current sense resistor must be routed as Kelvin Sense connection.
5. SPI lines: For signal integrity the termination resistances should be placed near to the source.
6. Each AVDD/AVSS should have decoupling capacitors placed close to the respective pins.
7. The reference capacitor should be placed close to the voltage reference input pin.

9.3.2 Layout Prints

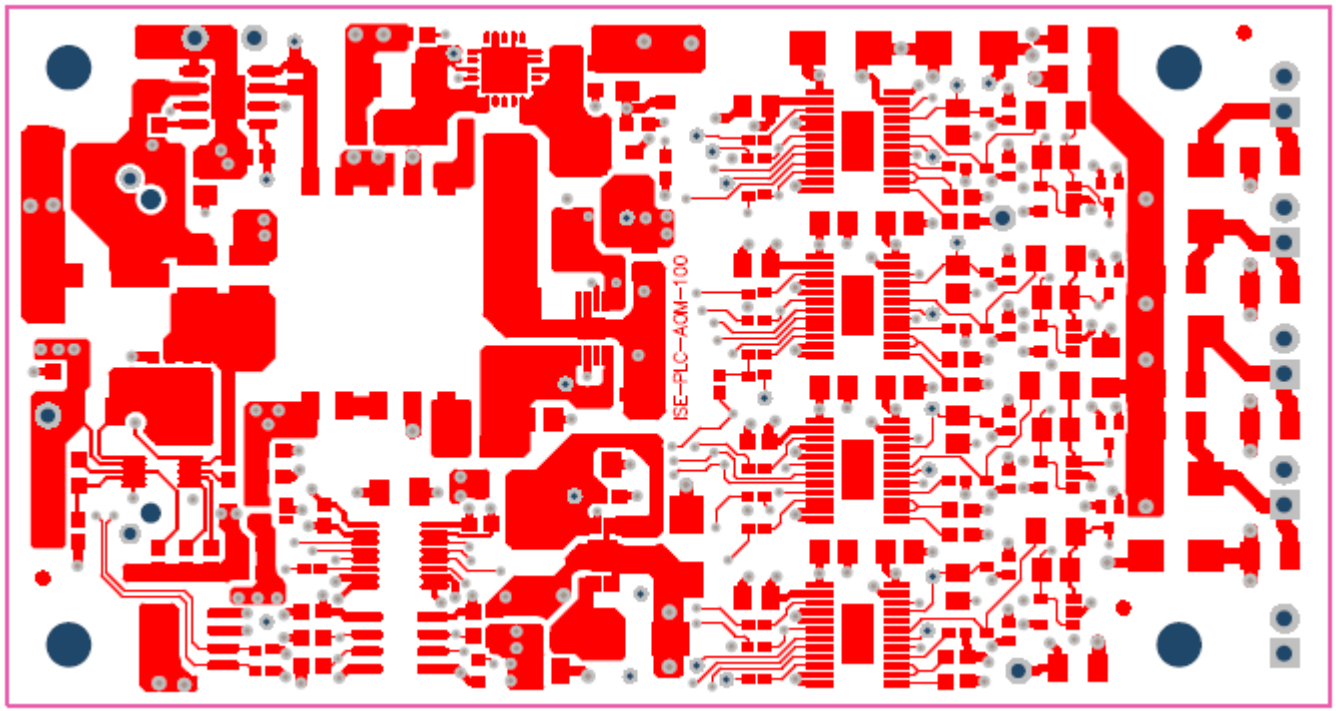
To download the layer plots of the board, see the design files at: www.ti.com/tools/TIDA-00118

Top Overlay

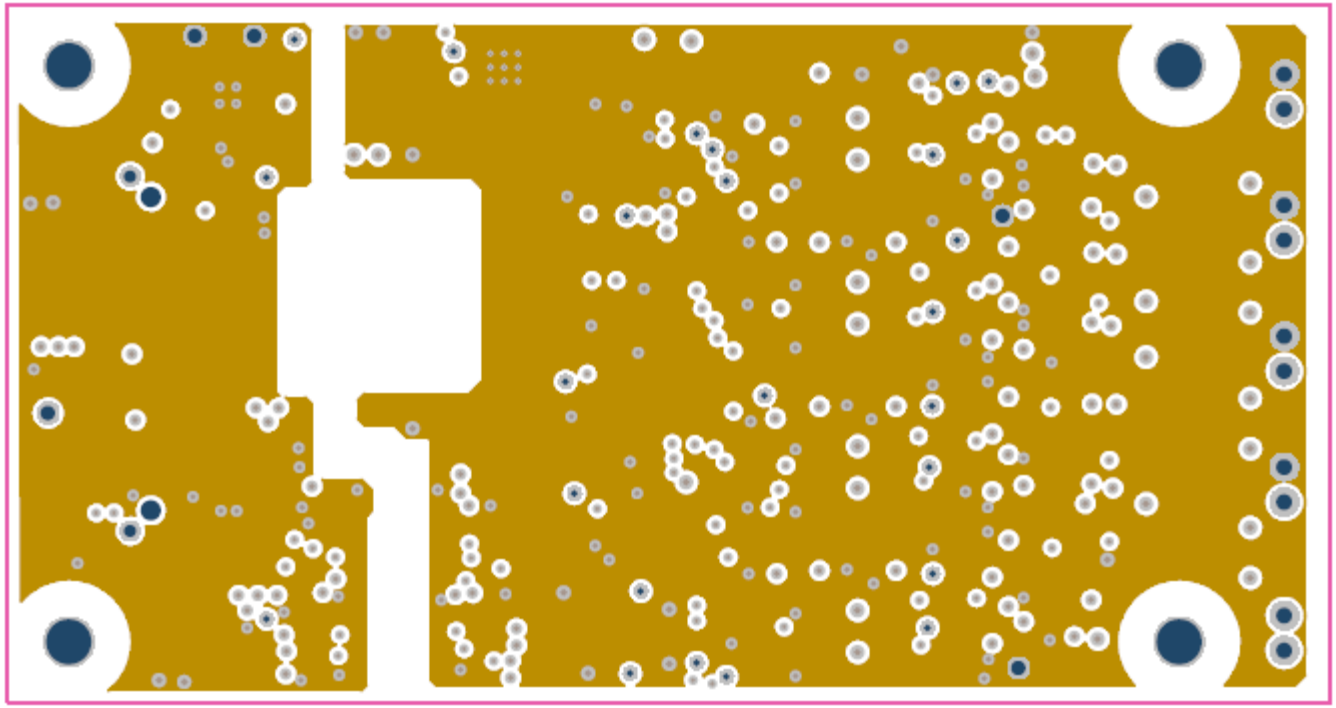


Top Solder

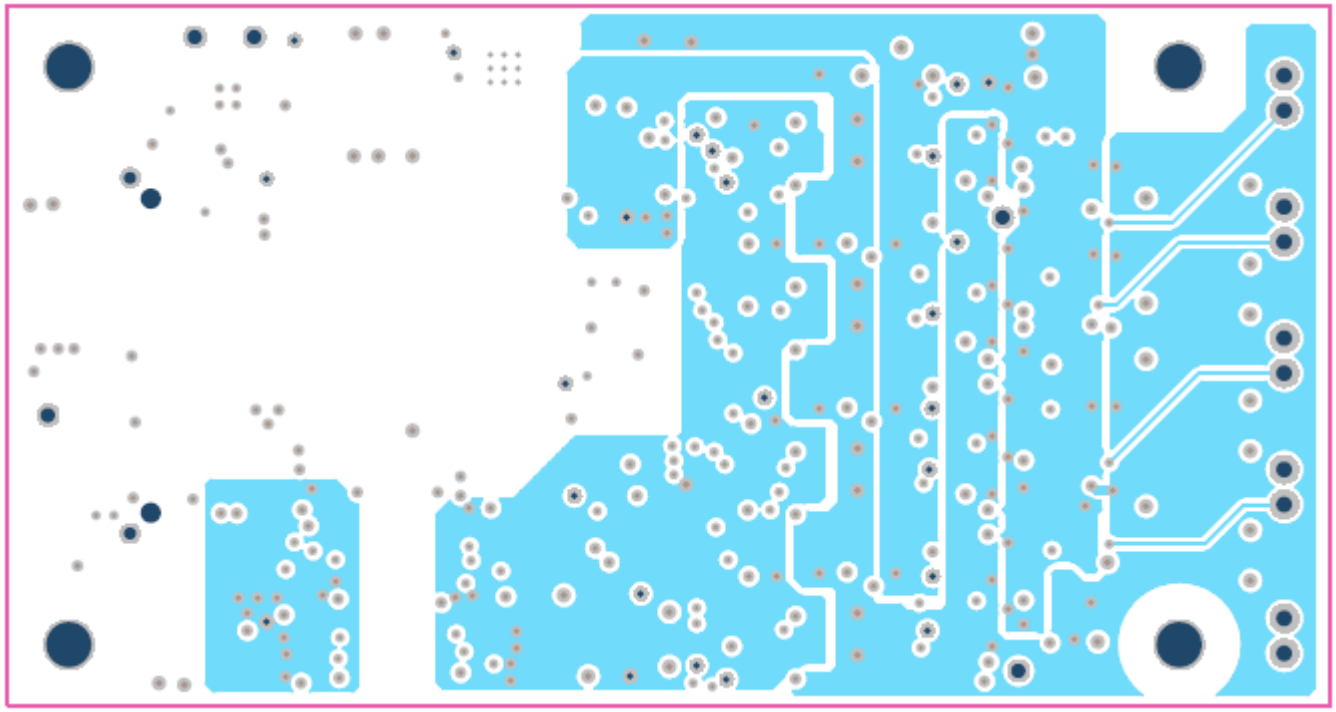
Top Layer



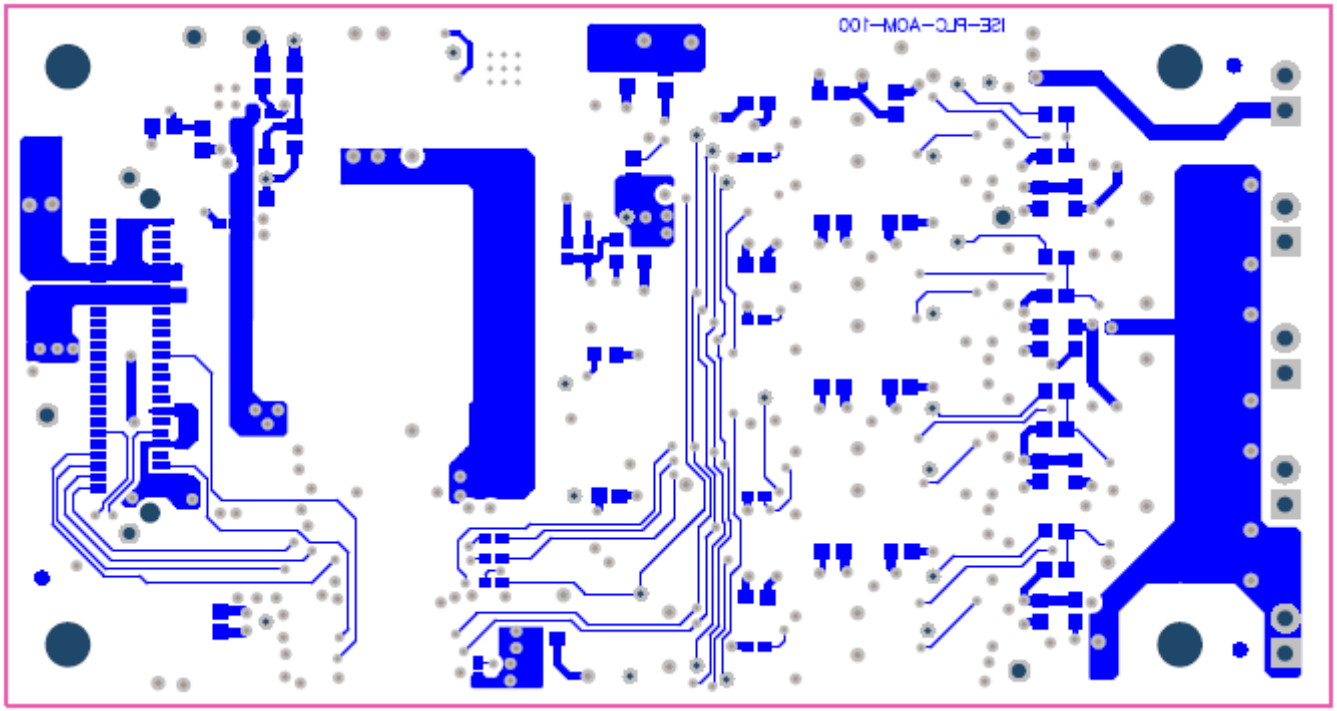
Inner Layer 1 Ground Plane



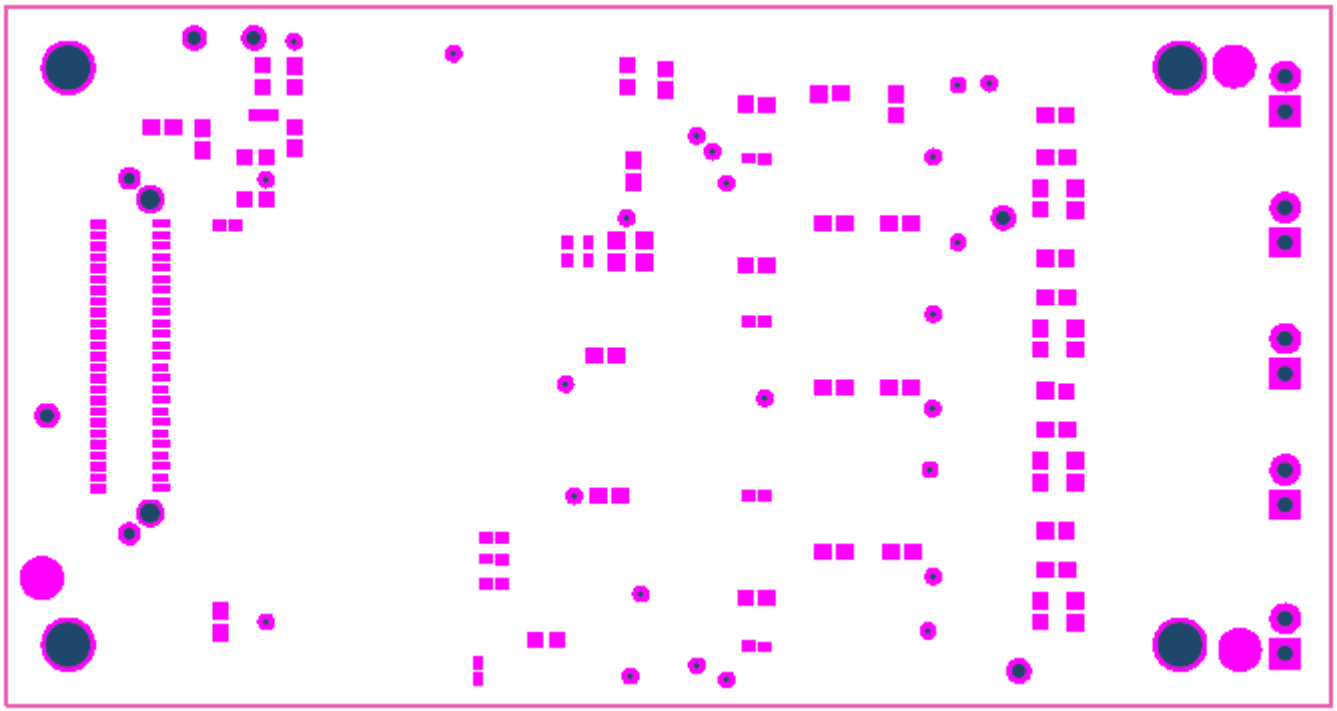
Inner Layer 2 Power Plane



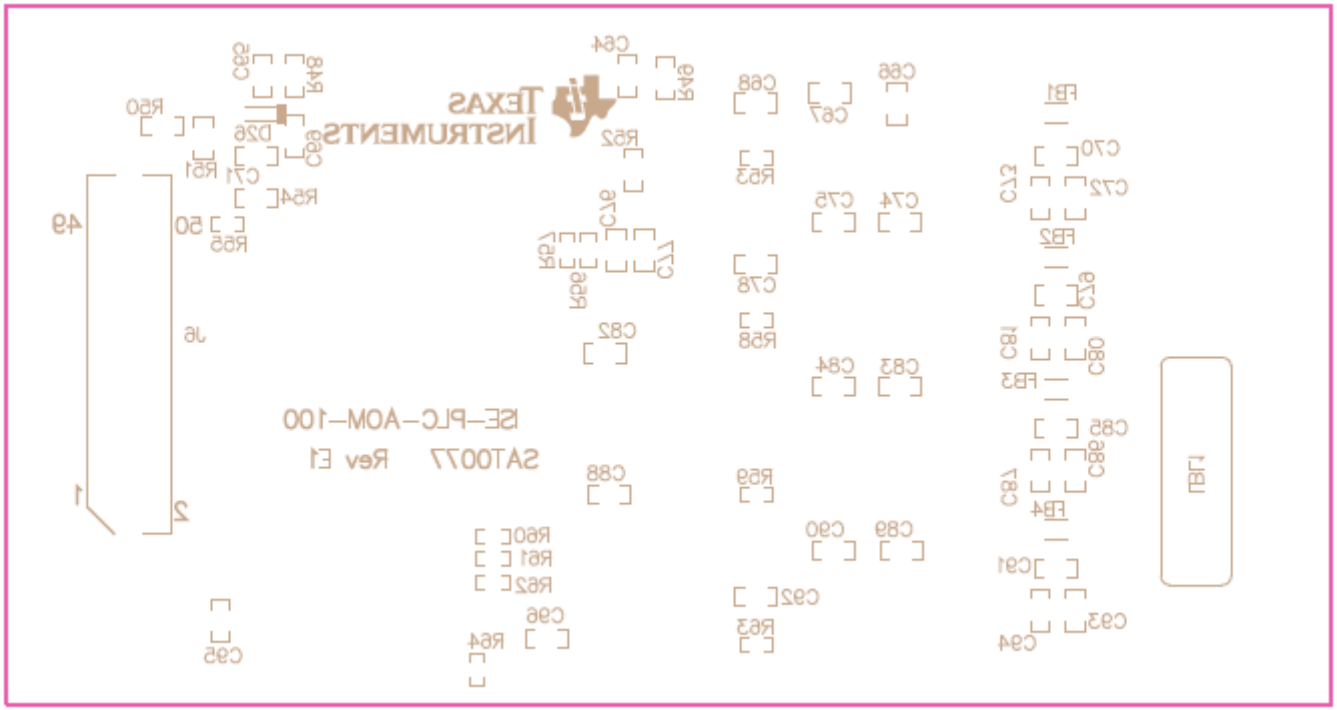
Bottom Layer



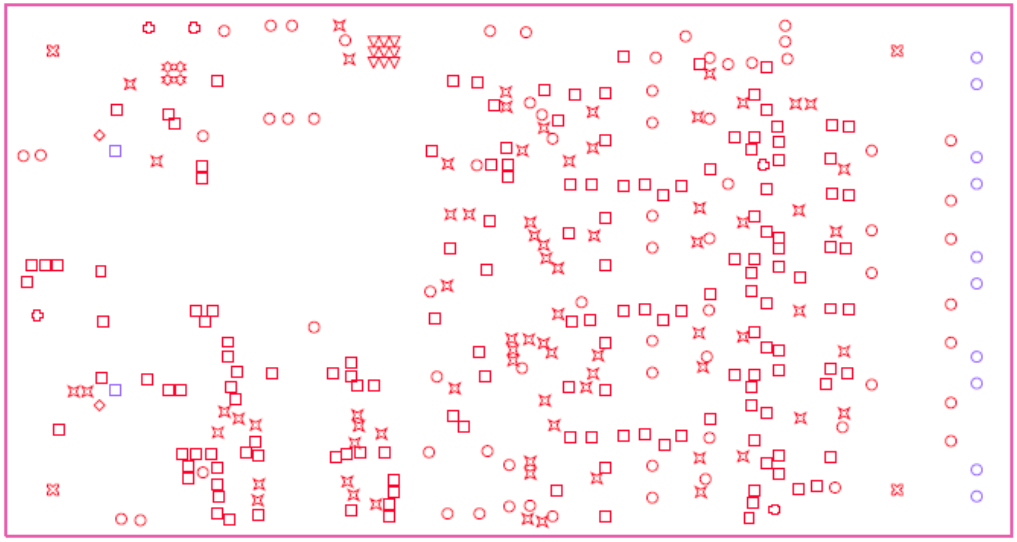
Bottom Solder



Bottom Overlay



Drill Drawing



Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	9	7.874mil (0.2mm)	PTH	Round
⌑	75	12mil (0.305mm)	PTH	Round
☆	4	12.992mil (0.33mm)	PTH	Round
□	159	16mil (0.406mm)	PTH	Round
○	68	20mil (0.508mm)	PTH	Round
◇	2	33mil (0.838mm)	PTH	Round
⌑	5	40mil (1.016mm)	PTH	Round
○	10	44mil (1.118mm)	PTH	Round
□	2	57.087mil (1.45mm)	NPTH	Round
⊠	4	128mil (3.251mm)	NPTH	Round
	338 Total			

Drill Table

Mechanical Layer

9.4 Altium Project

To download the Altium Project files for the board, see the design files at : www.ti.com/tools/TIDA-00118

9.5 Gerber files

To download the Gerber files for the board, see the design files at: www.ti.com/tools/TIDA-00118

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