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TI Designs High Speed
Quad-Channel 250-Msps Digitizer with Variable Gain Amplifier

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Design Resources

Design Files	Simulations, PCB, Gerber, BOM
TINA Spice	SPICE Simulator
LMH6881	Product Folder
ADS4449	Product Folder

Design Overview

A quad-channel wide input range digitizer can be created by pairing the quad channel, 14-bit, 250-Msps ADS4449 with the LMH6881 programmable differential amplifier. This combination can maintain a minimum SNR of 6 dB over an input voltage range of approximately 1 Vpp to 100 uVpp (4 dBm to -75 dBm) due to a programmable gain range of 6 dB to 26 dB. The focus of this reference design is on the use and performance of the LMH6881 amplifier to drive the ADS4449. Different options for common-mode voltages, power supplies, and interfaces are discussed and measured, including AC-coupling and DC-coupling, to meet the requirements of a variety of digitizer applications including scientific sensor applications, medical imaging, and automated test systems.

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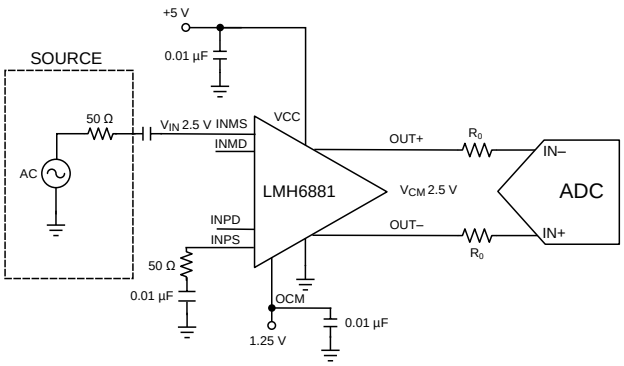

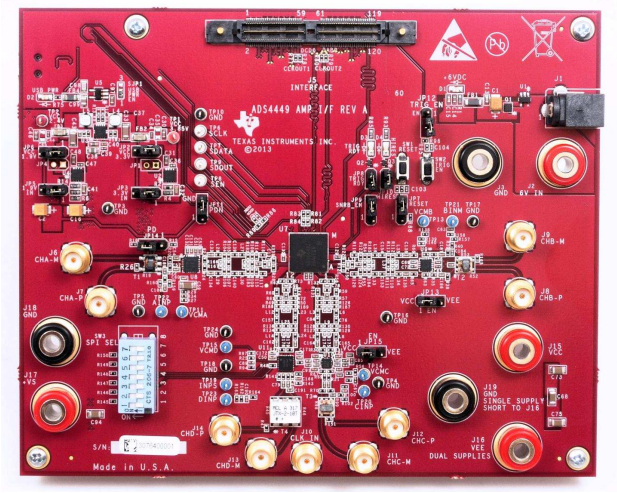

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1 Introduction

This reference design focuses on the use of the LMH6881 programmable differential amplifier and ADS4449 quad-channel, 14-bit, 250-Msps ADC. These devices can be combined to form a quad channel, 14-bit, 250-Msps digitizer with wide input range. This combination allows an input voltage range of approximately 1 Vpp to 100 uVpp (4 dBm to -75 dBm) while maintaining a minimum SNR of 6 dB. The maximum voltage can be increased even further by using an external programmable attenuator in front of the amplifier and the minimum voltage can be increased by placing additional low noise gain front of the amplifier. Note that the LMH6882, dual channel programmable differential amplifier, can be used instead of the LMH6881 to create a smaller overall solution. A printed-circuit board was developed in order to test different setups. This document includes the general considerations when driving an ADC with an amplifier, such as common-mode voltages, power supplies, AC-coupling and DC-coupling, and filter interfaces. This document also includes a discussion of the measured performance based on different circuit topologies.

2 General Considerations

2.1 Single-Ended Input to Differential-Output Operation

Many applications require a single-ended source to drive a differential-input ADC. In general, transformers are used to provide single-to-differential conversion, but these transformers are inherently band-pass in nature and cannot be used for DC-coupled applications. As a result, a common solution is to use a high-speed amplifier in order provide differentiation to enable DC-coupling without affecting ADC performance at higher frequencies. Op-amps offer a flexible and cost-effective solution when the application requires gain, a flat pass-band with low ripple, DC-level shifts, or a DC-coupled signal path.

2.1.1 AC-Coupled Configuration

AC-coupling is the recommended configuration if the application does not require signals down to DC. Figure 1 shows a typical AC-coupled configuration where an LMH6881 device is used to produce a balanced differential output signal from a single-ended source. Although not shown, the amplifier to ADC interface is also typically AC coupled such that each can maintain optimal bias points for best distortion performance.

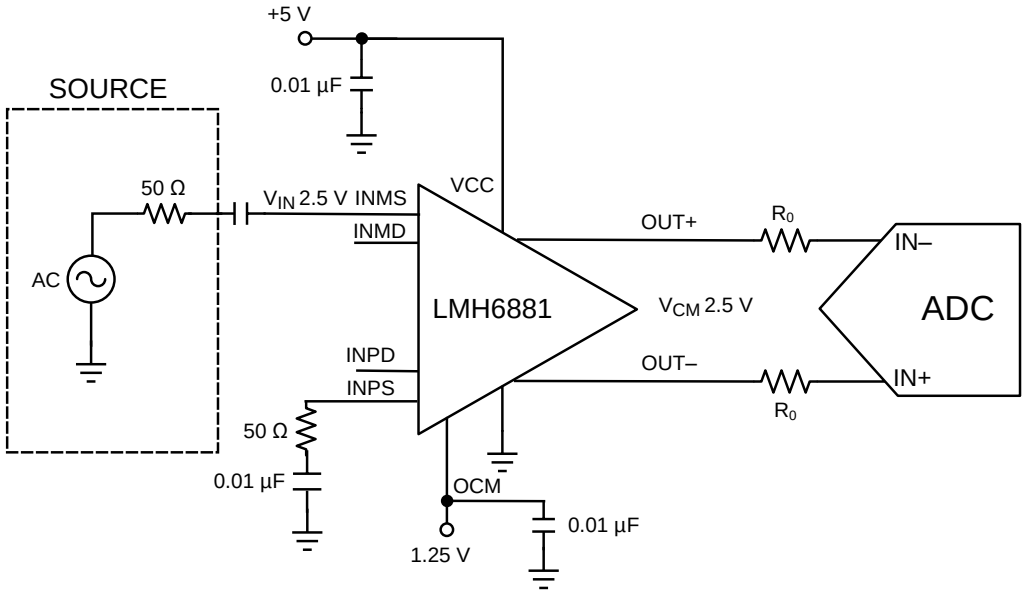


Figure 1. Single-Ended Input With Differential Output

This circuit shows a configuration where a 50-Ω source is used. A 50-Ω resistor is also placed on the negative input to balance the amplifier. Since the LMH6881 device is a programmable differential amplifier the device requires no external gain-setting components. The gain range of the LMH6881 is 6 dB to 26 dB and is controllable through either a serial or parallel interface.

2.1.2 DC-Coupled Configuration

In order to successfully implement a DC-coupled signal chain the common-mode voltage requirements of every stage must be met. This requires careful planning and, in some cases, may require signal swing, system gain, or termination trade-offs to optimally interface the parts.

Figure 2 shows a typical DC-coupled configuration of the LMH6881 device. Note that the input common mode must be set to 2.5 V at each input pin to maintain best distortion performance although the input pins can be externally biased to a wider common mode voltage range. If the source is DC-coupled with an offset voltage outside of the LMH6881 input common mode range then a level-shifting amplifier is likely needed to shift the DC level up to 2.5 V.

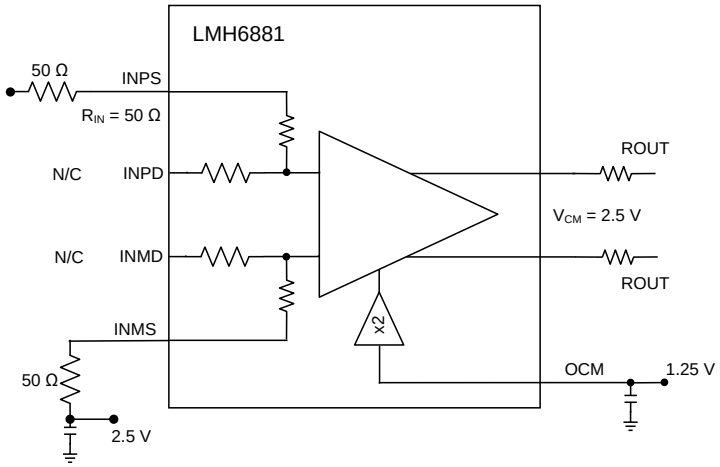


Figure 2. DC-Coupled Configuration

2.2 Common-Mode Level Consideration

For most ADCs the common-mode voltage must be set to a particular value to realize full dynamic range without much flexibility. Differential amplifiers typically have more flexibility in setting the output common mode which can be set independently from the input. By changing the common mode voltage the amplifier outputs will swing closer to the power supply rails and may introduce distortion if set too high or low. The optimal setting is at the midpoint of the power supply rails.

The output common-mode level of the LMH6554 device is set at the V_{CM} pin. The drive at the V_{CM} pin can be one of the following:

- A resistive divider circuit that uses the existing supply voltages (generally ¼V_+)
- A reference level defined by an ADC output pin
- A dedicated voltage reference

NOTE: The LMH6881 device uses a times-2 multiplier to set the output common-mode voltage as two times the voltage applied to the OCM pin.

2.3 Power Supply Consideration

The LMH6881 device was designed to operate with a 5-V power supply. The voltage range for VCC is 4.75 V to 5.25 V. Power-supply accuracy of 5% or better is advised. The advantage of AC-coupling over DC-coupling is to offer easier interfacing in order to properly bias each stage. In AC-coupling configuration, the common mode of the op-amp can be easily set at the optimal 2.5 V by either letting the amplifier self-bias or by providing 1.25 V at the OCM pin. Then the ADC common mode can be set to the optimal voltage by using AC coupling capacitors between the amplifier and ADC and using the V_{CM} output of the ADC to bias the input pins (see Figure 3).

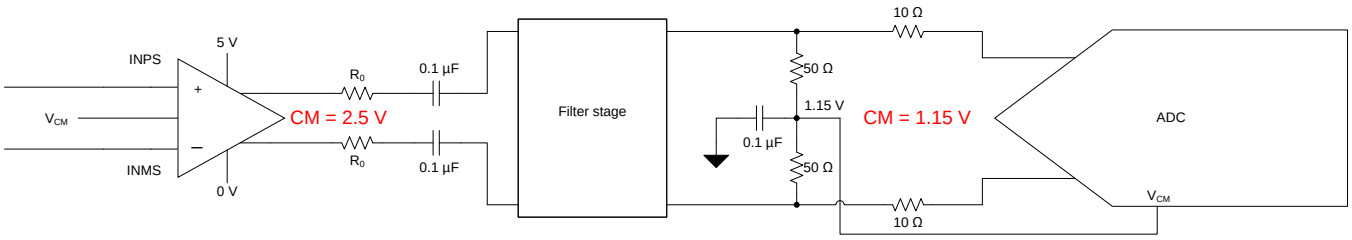


Figure 3. Interfacing With AC-Coupled Configuration

In DC coupled cases, shifting the amplifiers common mode level to match the common mode of the ADC is possible while maintaining the amplifier's optimal output common mode voltage (see Figure 4). The appropriate common mode is set by using the voltage divider between R_0 and R_1. Unfortunately, this method results in lower gain and may require the op-amp to drive a larger voltage to overcome the attenuation of the voltage divider formed by R0 and R1, which may result in degraded performance. Alternatively, the amplifier's output common mode can be lowered by setting a lower voltage on the OCM pin. This would require a smaller voltage divider at the output allowing the recovery of some of the gain. Ultimately the performance of each method should be evaluated to determine which provides the best performance to gain performance.

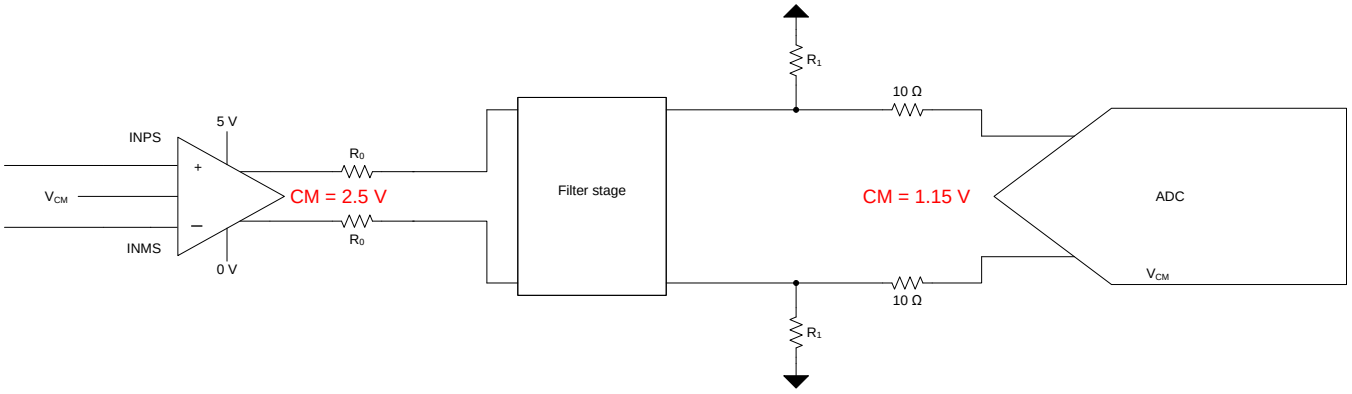


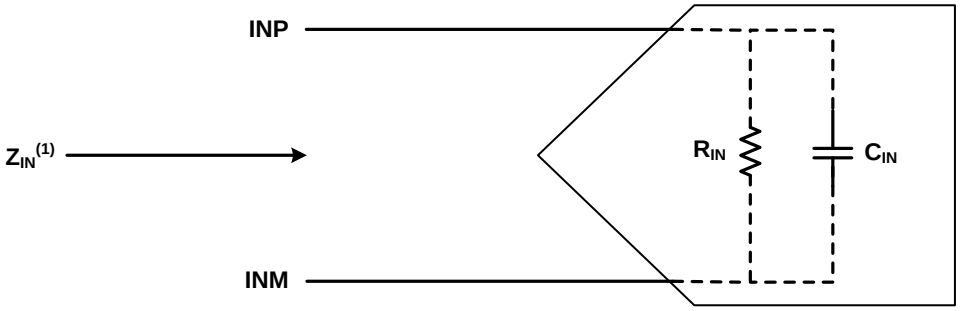
Figure 4. Interfacing With DC-Coupled Configuration

NOTE: This example shows a voltage division in order to get 1.15 V from 2.5 V. Another solution is to use the V_{CM} of the ADC at 1.15 to feed the V_{CM} input of the op-amp. Thus, the output CM is set at 2.3 V which is still within the specification without adding too much distortion. A final simple division by 2 with R_0 and R_1 provides 1.15-V CM to the ADC.

2.4 Connecting the Amplifier to the ADC

Analog-to-digital converters (ADCs) often present challenging load conditions. ADCs typically have high impedance inputs with variable capacitive components. Current spikes associated with a switched capacitor or sample-and-hold circuits can also occur. These characteristics result in an ADC input that is a challenge to drive. Using an amplifier provides value to the design because the output stage of a differential amplifier improves tolerance to glitches by providing a low-impedance, fast-settling source for accurate sampling.

The first aspect to consider is the ADC-equivalent input impedance. Figure 5 shows that the input of the ADS4449 can be represented by a differential resistor (R_{IN} ≈ 700 to 1000 Ω for the first two Nyquist zones, 0 to 250 MHz) and capacitor (C_{IN} ≈ 3.5 pF) in parallel. The ADS4449 device does not have a buffered input so the driving circuit will see glitches from the sampling capacitor.



(1) $Z_{IN} = R_{IN} || (1 / j\omega C_{IN})$.

Figure 5. ADS4449 Equivalent-Input Impedance

The interface between the op-amp and the ADC must be optimized to achieve best performance. Figure 6 shows a typical circuit for driving an ADC. The two R_0 resistors isolate the capacitive loading of the ADC from the amplifier to ensure stability. The resistors form part of a low-pass filter with L_1 and C_1, which helps to provide anti-alias and noise reduction functions. The two C_1 capacitors can also help to smooth the glitches associated with the internal switching circuits of the ADC. Note that the ADC input capacitance must be factored into the frequency response of the input filter. A 5 to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. The input circuit (and notably these resistors) must be optimized in the lab because up to a 4-dB SFDR and 2-dB SNR improvement has been observed with various values of resistors.

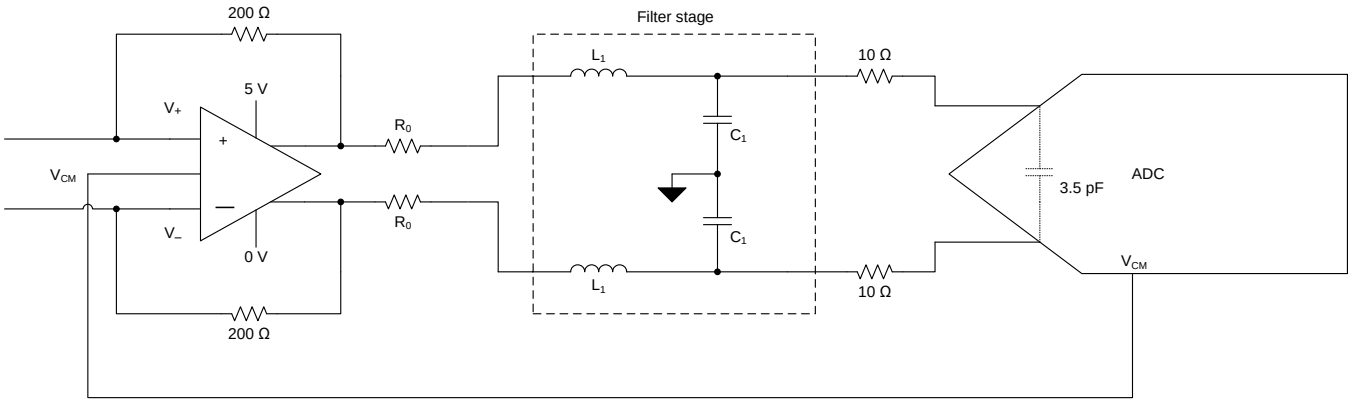


Figure 6. Typical Interface Circuit Driving an ADC

2.5 Layout Considerations

Board layout is critical for high-speed circuits. To achieve a proper layout, TI recommends the following:

- The amplifier and ADC should be located as close together as possible to reduce effects of impedance mismatch and minimize inductance.
- Both the amplifier and the ADC require that the filter components be located in close proximity.
- The ADC digital outputs must be well isolated from the ADC input as well as from the amplifier inputs.
- The amplifier input and output pins should not be placed over power or ground planes to reduce parasitic capacitance for stability reasons.
- Power-supply bypass capacitors should be low ESR and placed within 2 mm of the associated pins.
- When vias are used, using multiple vias is recommended. This includes placing ground vias near vias on the signal traces.

2.5.1 Board Layout

Figure 7, Figure 8, and Figure 9 show the board and board layout.

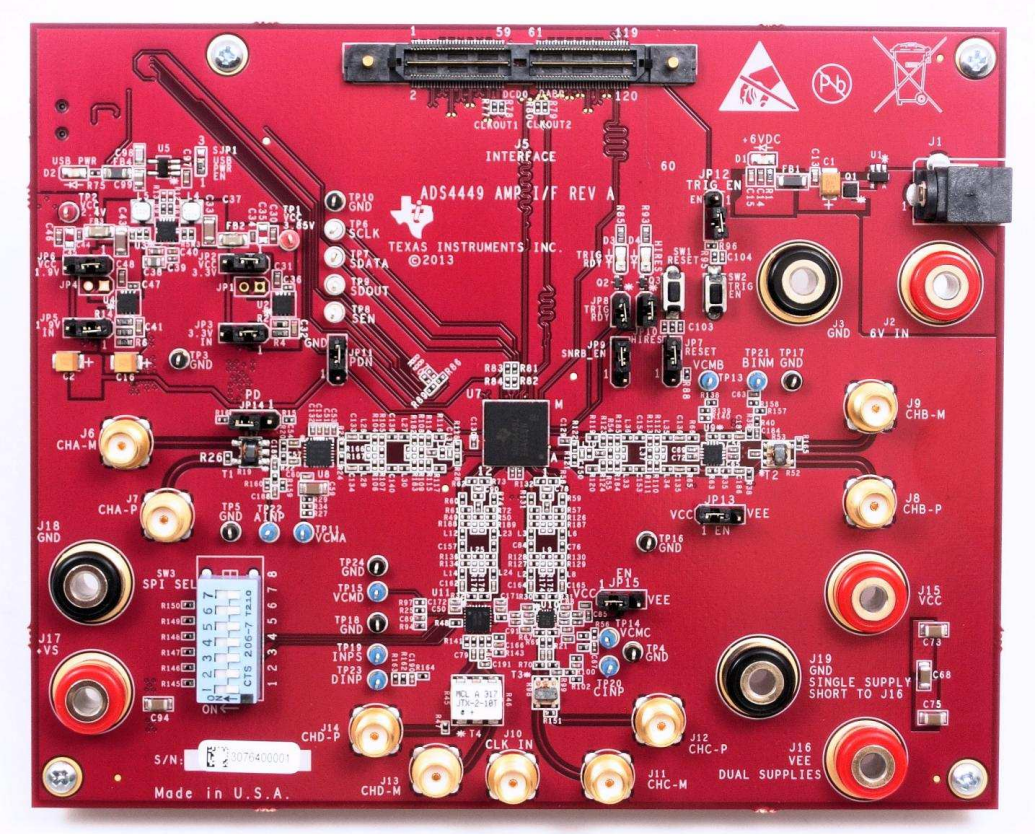


Figure 7. LMH6881 and ADS4449 Test Board

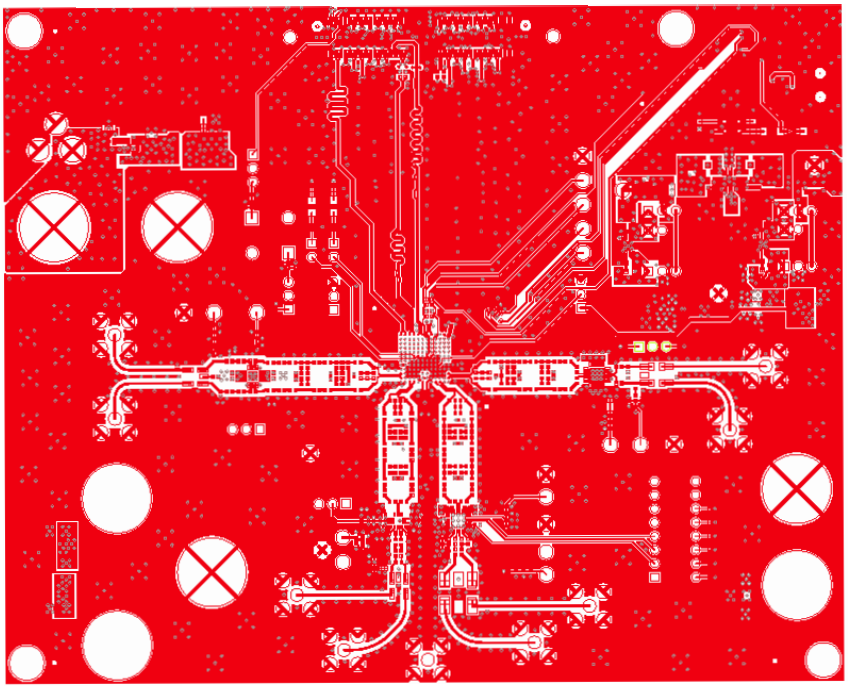


Figure 8. Top-Side Layer

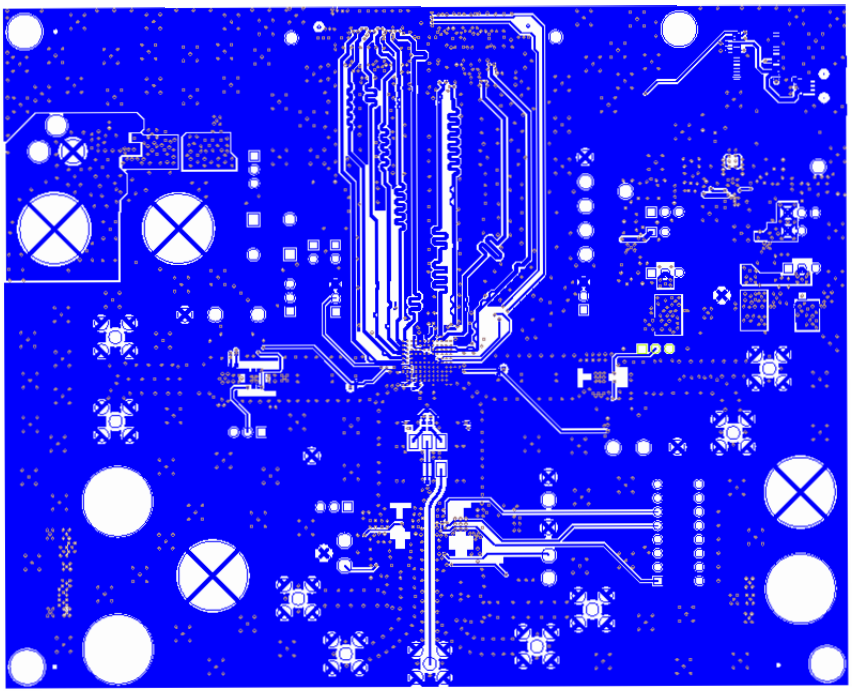


Figure 9. Bottom-Side Layer

3 Tests and Measurements

Two design options have been explored and optimized: AC-coupling and DC-coupling for signals in the first Nyquist zone. The schematics of the circuits, and the SNR and SFDR measurement results are presented in this section.

3.1 Test setup

The board used for these measurements is the ADS4449 amplifier I/F which was specifically created for these tests. The board comprises an ADS4449 ADC and LMH6881 amplifier. All SNR and SFDR measurements are taken at –1 dBFS. The clock used for all these measurements is set at 245.76 MHz with a 10-dBm amplitude.

3.2 AC-Coupled Scenario

Figure 10 shows the circuit used in the AC-coupled scenario.

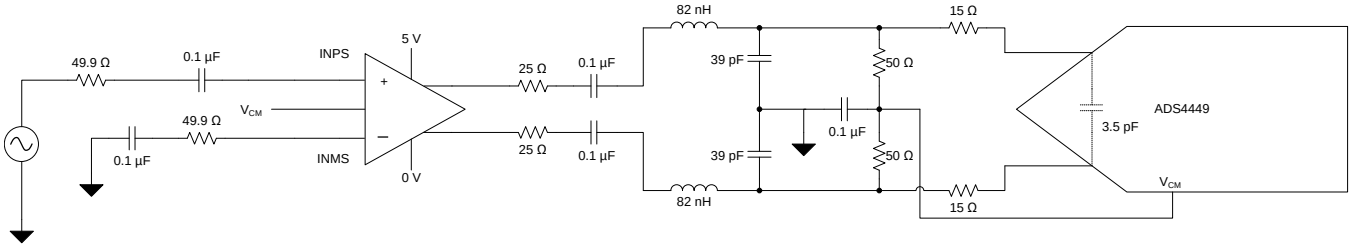


Figure 10. Circuit Used for the AC-coupled Measurements

An LC filter was designed as a second-order low-pass filter to attenuate noise and distortion outside of the first Nyquist zone. Figure 11 shows the measured filter response. The corner frequency is located at 105 MHz.

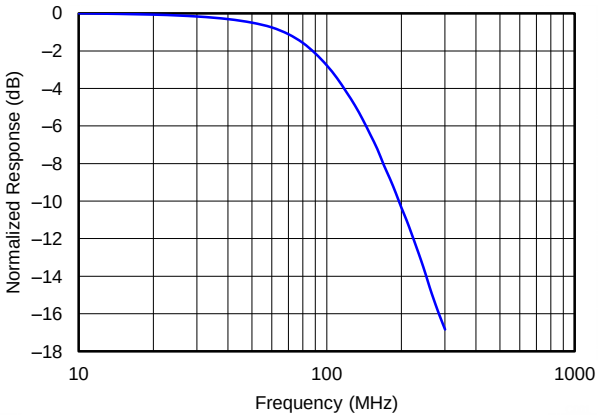


Figure 11. Normalized Gain Response — AC-Coupled

Table 1 and Table 2 list the SNR and SFDR results at a gain of 6-dB.

Table 1. SNR Result — AC-Coupled (6-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	64.46	68.92
90	64.5	68.94
80	64.49	68.96
70	64.58	69.02
60	64.53	69.15
50	64.57	69.15
40	64.63	69.11
30	64.61	69.17
20	64.59	69.21
10	64.65	69.22

Table 2. SFDR Result — AC-Coupled (6-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	60.04	66.6
90	63.39	70.4
80	65.73	70.86
70	69.6	70.56
60	80.62	73.09
50	78.76	78.35
40	76.2	81.65
30	77.38	85.59
20	72.74	81.65
10	72.03	77.14

Table 3 and Table 4 list the SNR and SFDR results at a gain of 16-dB.

Table 3. SNR Result — AC-Coupled (16-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	61.3	67.52
90	61.28	67.62
80	61.25	67.66
70	61.36	67.77
60	61.43	67.77
50	61.41	67.77
40	61.43	67.81
30	61.39	67.77
20	61.39	67.82
10	61.52	67.78

Table 4. SFDR Result — AC-Coupled (16-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	60.76	64.14
90	61.31	64.57
80	65.06	65.89
70	75.95	66.8
60	77.9	69.27
50	75.1	71.34
40	79.64	73.99
30	74.02	86.76
20	68.42	85.38
10	72.04	87.37

Table 5 and Table 6 list the SNR and SFDR results at a gain of 26-dB.

Table 5. SNR Result — AC-Coupled (26-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	55.95	62
90	55.97	62.01
80	55.95	62.05
70	55.97	62.08
60	56	62.06
50	56.03	62.1
40	56.05	62.05
30	56.04	62.1
20	56.08	62.07
10	56.1	62.08

Table 6. SFDR Result — AC-Coupled (26-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	56.64	53.98
90	60.53	55.64
80	67.31	56.6
70	75.06	57.6
60	78.06	59.45
50	72.47	61.91
40	70.85	64.55
30	73.94	73.66
20	72.77	73.27
10	71.16	82.07

3.3 DC-Coupled Scenario

Figure 12 shows the circuit used for the DC-coupled scenario.

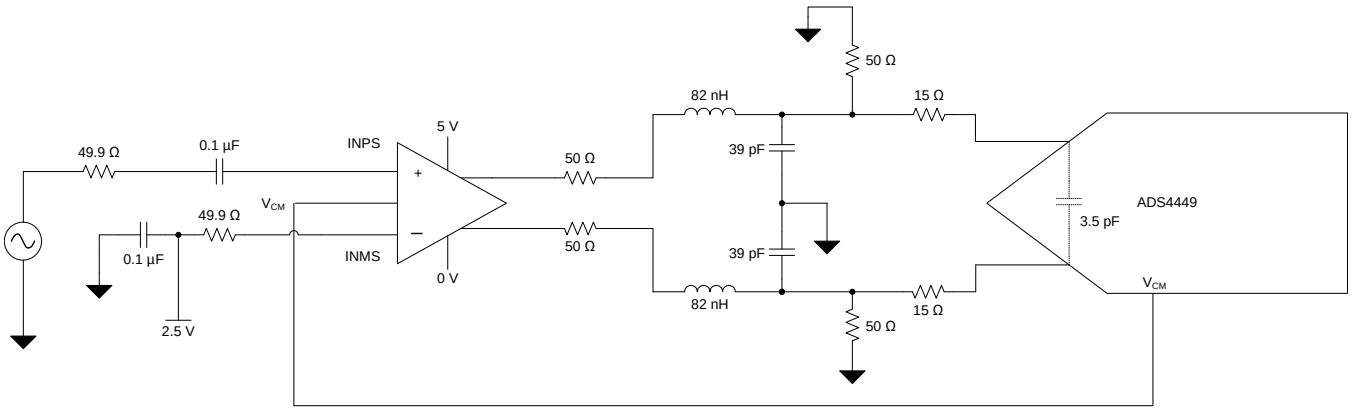


Figure 12. Circuit Used for the DC-Coupled Measurements

NOTE: For this design, a fully DC-coupled solution could not be evaluated because a DC-coupled solution would require an additional op-amp after the source to shift the DC-level to 2.5 V. Therefore, a 50-Ω AC-source is still used in this configuration, however, the interface between the op-amp and the ADC is DC-coupled. The solution of using the V_{CM} from the ADC at 1.15 V has been selected which provides the op-amp with an output CM of 2.3 V which is then easily divided by 2 to match the 1.15 V CM required by the ADS4449 device.

The DC coupled measurements used the same LC filter that was used for the AC coupling case. Figure 13 shows the measured filter response. The corner frequency is located at 110 MHz.

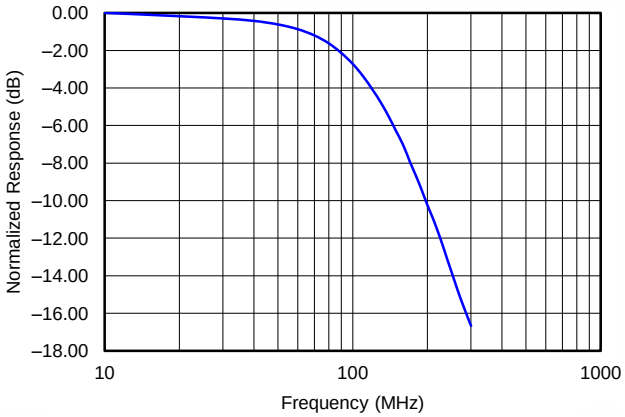


Figure 13. Normalized Gain Response — DC-Coupled First Nyquist Zone

Table 7 and Table 8 list the SNR and SFDR results at a gain of 6-dB.

Table 7. SNR Result — DC-Coupled (6-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	66.14	69.48
90	66.23	69.6
80	66.3	69.72
70	66.34	69.76
60	66.39	69.84
50	66.42	69.88
40	66.51	69.89
30	66.56	69.95
20	66.61	70.01
10	66.31	70.0

Table 8. SFDR Result — DC-Coupled (6-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	58.46	66.19
90	62.92	68.54
80	65.39	70.14
70	67.31	70.47
60	73.8	73.26
50	76.46	79.6
40	71.43	76.45
30	74.23	77.35
20	70.38	77.15
10	69.34	74.65

Table 9 and Table 10 list the SNR and SFDR results at a gain of 16-dB.

Table 9. SNR Result — DC-Coupled (16-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	64.03	68.41
90	64.06	68.5
80	64.11	68.36
70	64.13	68.56
60	64.24	68.43
50	64.25	68.62
40	64.29	68.64
30	64.27	68.79
20	64.27	68.78
10	64.36	68.92

Table 10. SFDR Result — DC-Coupled (16-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	61.76	67.6
90	64.78	67.2
80	69.26	67.32
70	72.13	69.65
60	77.15	74.74
50	82.89	76.11
40	81.3	78.04
30	79.8	84.57
20	76.27	89.74
10	77.58	89.63

Table 11 and Table 12 list the SNR and SFDR results at a gain of 26-dB.

Table 11. SNR Result — DC-Coupled (26-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	57.23	63.71
90	57.26	63.84
80	57.31	63.87
70	57.33	63.83
60	57.42	63.93
50	57.45	63.96
40	57.48	63.96
30	57.46	63.91
20	57.49	63.91
10	57.55	64.02

Table 12. SFDR Result — DC-Coupled (26-dB gain)

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
100	56.23	57.35
90	59.65	58.54
80	65.27	60.09
70	73.61	61.87
60	76.34	64.77
50	75.71	67.22
40	70.12	70.3
30	73.86	78.77
20	72.08	79.41
10	69.84	83.43

3.4 Comparison Between Op-Amps and Raw ADC Performance

Table 13 and Table 14 list a general summary of the performance measured with this setup and additional amplifiers with the ADS4449. These tables include measurements using the THS4509 device, the LMH6881 device, and the LMH6554 device to drive the ADS4449 device. For additional information on how to drive high-speed ADC using the THS4509 device and the LMH6554 device, please see TIDU173 and TIDU172 (respectively). Typical values from the ADS4449 datasheet (SBAS603) are shown as a benchmark.

Table 13. Performance Measured in AC-Coupling Configuration

	Frequency (MHz)	THS4509	LMH6881 (6-dB gain)	LMH6554	ADS4449
SNR (dBFs)	40	71.65	69.11	72.02	71.1
	70	71.49	69.02	71.84	71
	130	68.12	N/A	68.74	69.5
	170	67.89	N/A	68.5	69
	230	67.9	N/A	68.42	68.5
SFDR (dBFs)	40	84.03	81.65	84.65	84
	70	78.55	70.56	82.63	87
	130	71.03	N/A	82.21	85
	170	69.24	N/A	82.02	86
	230	75.34	N/A	80.12	84

Table 14. Performance Measured in DC-Coupling Configuration

	Frequency (MHz)	THS4509	LMH6881 (6-dB gain)	LMH6554	ADS4449
SNR (dBFs)	40	70.83	70.39	71.11	71.1
	70	70.66	70.21	70.99	71
SFDR (dBFs)	40	88.55	75.86	84.25	84
	70	80.1	69.32	83.66	87

4 Conclusion

The measured results show that the LMH6881 device is a good solution to drive a high-speed ADC such as the ADS4449 device for high speed, wide input voltage range digitizer applications. The LMH6881 device can be set in either DC-coupled or AC-coupled configuration. An important consideration is proper common-mode biasing. One difficulty with the DC-coupling case is the need to provide the optimal common-mode voltage at the amplifier output pins and the ADC input pins. Another challenge with DC coupling is the need to level shifted the DC source to the amplifier's input common mode voltage.

In terms of SNR and SFDR, the performance can be improved if time is spent to optimize the interface circuit and filtering, likely further than what is shown in this document. The limitation in terms of SFDR performance is the second harmonic coming from the LMH6881 device when driven by a single-ended source at higher input frequencies. However, at lower frequencies the SFDR performance is very good. At higher frequencies, the HD_2 performance can be improved by using a balun in front of the amplifier to do the conversion from single-ended to differential, however this can only be used when AC coupling is allowed. An additional high speed differential amplifier could also be used in front of the LMH6881 to provide DC level shifting and single-ended to differential conversion. Lastly, the LMH6881 device is a programmable differential amplifier, and as shown in this document, results from 6-dB to 26-dB gains are consistent.

5 References

1. *LMH6881 DC to 2.4GHz, High Linearity, Programmable Differential Amplifier*, SNOSC72
2. ADS4449, *Quad-Channel, 14-Bit, 250-MSPS, Low-Power ADC*, SBAS603
3. *Driving High-Speed Analog-to-Digital Converters: Circuit Topologies and System-Level Parameters*, SLAA416
4. *AN-1393 Using High Speed Differential Amplifiers to Drive Analog-to-Digital Converters*, SNOA461
5. *AN-2177 Using the LMH6554 as an ADC Driver*, SNOA565

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