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TI Designs High Speed: Verified Design
TSW1266 Wideband RF-to-Digital Complex Receiver-Feedback Signal Chain

TI Designs High Speed

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Design Resources

Design Zip File	Simulations, PCB, Gerber, BOM
ADS5402	Product Folder
LMH6521	Product Folder
TSW1400EVM	Tool Folder
LMK04800	LMK0480x Family Datasheet

Design Description

The TSW1266EVM is a wideband complex-receiver reference design and evaluation platform that is ideally suited for use as a feedback receiver for transmitter digital predistortion. The EVM signal chain is ideal for high intermediate-frequency (IF) complex-feedback applications and contains a complex demodulator, TI's LMH6521 dual-channel DVGA and ADS5402 12-bit 800-MSPS dual-channel ADC. By modifying the onboard filter components, the signal chain is configurable for a variety of frequency plans. The EVM also includes TI's LMK04808 dual-PLL clock jitter cleaner and generator to provide an onboard low-noise clocking solution. The LMH6521 DVGA gain is controlled through the GUI or alternatively through the high speed connector with an FPGA.

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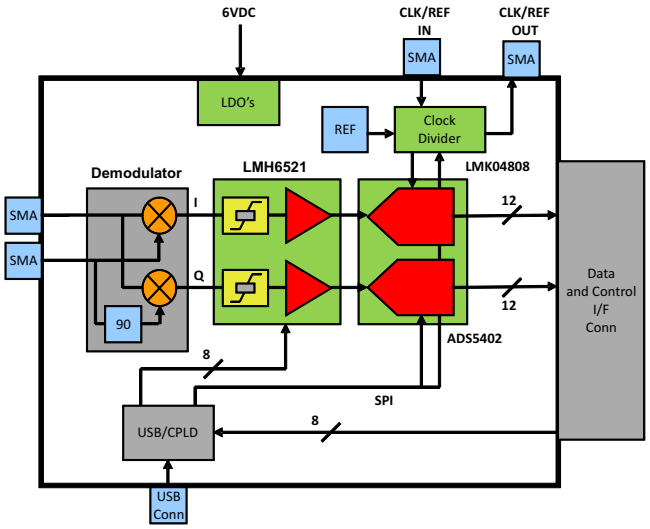

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1 Introduction

1.1 Overview

The TSW1266EVM evaluation module is a wideband, complex receiver reference design and evaluation platform. The signal chain is ideal for high intermediate frequency (IF) complex feedback applications. The signal chain has a wideband complex demodulator, the LMH6521 dual-channel, digitally controlled variable gain amplifier (DVGA), and the ADS5402 12-bit 800-MSPS analog-to-digital converter (ADC). The TSW1266EVM also includes the LMK04800 dual-PLL clock jitter cleaner and generator to provide an onboard low-noise clocking solution. A provided software GUI allows for configuration of the ADS5402 and LMK04800. Either the GUI or an FPGA using the high-speed connector can control the gain of the LMH6521 DVGA. The EVM mates with the TSW1400 pattern capture and generation card to capture data from the ADS5402. Then, the High Speed Data Converter Pro software tool can perform signal analysis. The TSW1266EVM product folder on the TI web site contains the EVM schematic, bill of materials, and layout files (http://www.ti.com/tool/tsw1266evm).

The default configuration of the board allows for an RF frequency of 1880 MHz to 2390 MHz and an LO frequency around 2600 MHz. The IF portion of the board, starting at the output of the demodulator to the ADC input, is set for a center frequency of 460.8 MHz and a 3-dB bandwidth of 500 MHz. Modification of both the RF and IF frequency ranges is possible.

A software GUI allows for configuring the ADS5402 and LMK04800. The GUI, or alternatively through the high-speed connector with an FPGA, can control the gain of the LMH6521 DVGA. The EVM mates with the TSW1400 pattern capture and generation board to capture data from the ADS5402. The High Speed Data Converter Pro software tool then can perform signal analysis. The TSW1400 and High Speed Data Converter Pro greatly simplify the evaluation process by providing the hardware and software necessary for pattern capture and analysis.

1.2 Block Diagram

Figure 1 shows the block diagram of the TSW1266EVM.

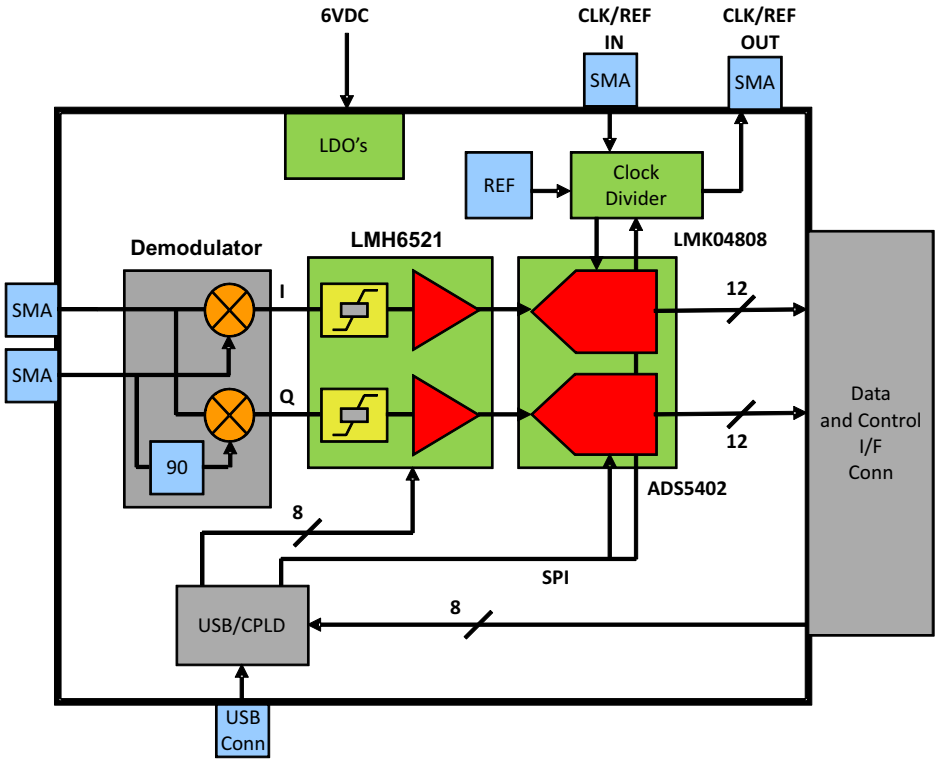

Figure 1. TSW1266EVM Block Diagram

2 Software Control

This section provides installation instructions and explanations of the TSW1266 GUI.

2.1 Installation Instructions

1. The software can be downloaded from the TSW1266EVM production page on www.ti.com. Find the page by searching for *TSW1266EVM*. The software appears under the *Related Products* section on the *TI Software* tab.
2. Extract the files from the zip file named *TSW1266 GUI vXpY Installer.zip* where *XpY* represents the version number.
3. Run *setup.exe*, and follow the installation prompts.
4. Start the GUI by going to
   Start Menu → All Programs → Texas Instruments ADCs → TSW1266 GUI.
5. When plugging the board into the computer for the first time through the USB cable, you are prompted to install the USB drivers.
   - Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the TSW1266 GUI, Windows 7 should automatically be able to install the drivers for the TSW1266EVM with no input from the user.

2.2 Software Operation

The TSW1266 GUI allows the user to program the ADS5402, LMH6521, and LMK04800 for proper operation. The controls for each device are split between different tabs for a simplified interface. Detailed descriptions for each tab are below.

2.2.1 ADS5402 Control Tab

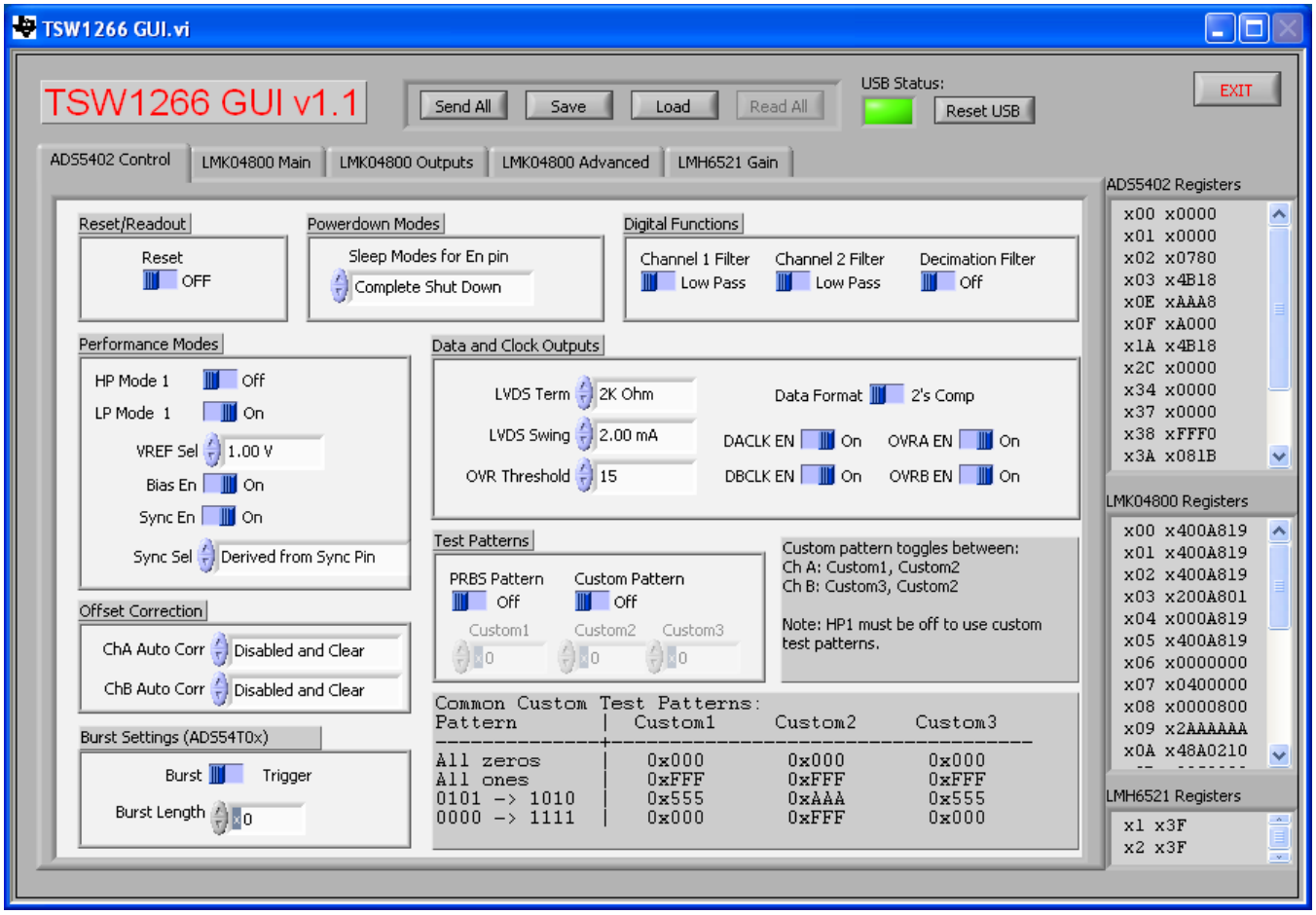

Figure 2. ADS5402 Control Tab

Table 1. ADS5402 Control Tab Section Descriptions

Section	Description
Reset/Readout	Allows software reset of the ADS5402 registers. The device should be reset on startup.
Powerdown Modes	Control the Enable pin functionality.
Digital Functions	Enable the decimation filters and set the filter type.
Performance Modes	Control performance modes of the ADS5402. HP Mode 1 should be on for proper operation.
Data and Clock Outputs	Control the LVDS data lines and data format, also control the overrange functionality.
Offset Correction	Enable or disable automatic interleaving correction.
Burst Settings	Configure the high resolution burst mode. Only applicable to the ADS54T0x family.
Test Patterns	Enable and set test patterns to verify the digital interface.

2.2.2 LMK04800 Main Tab

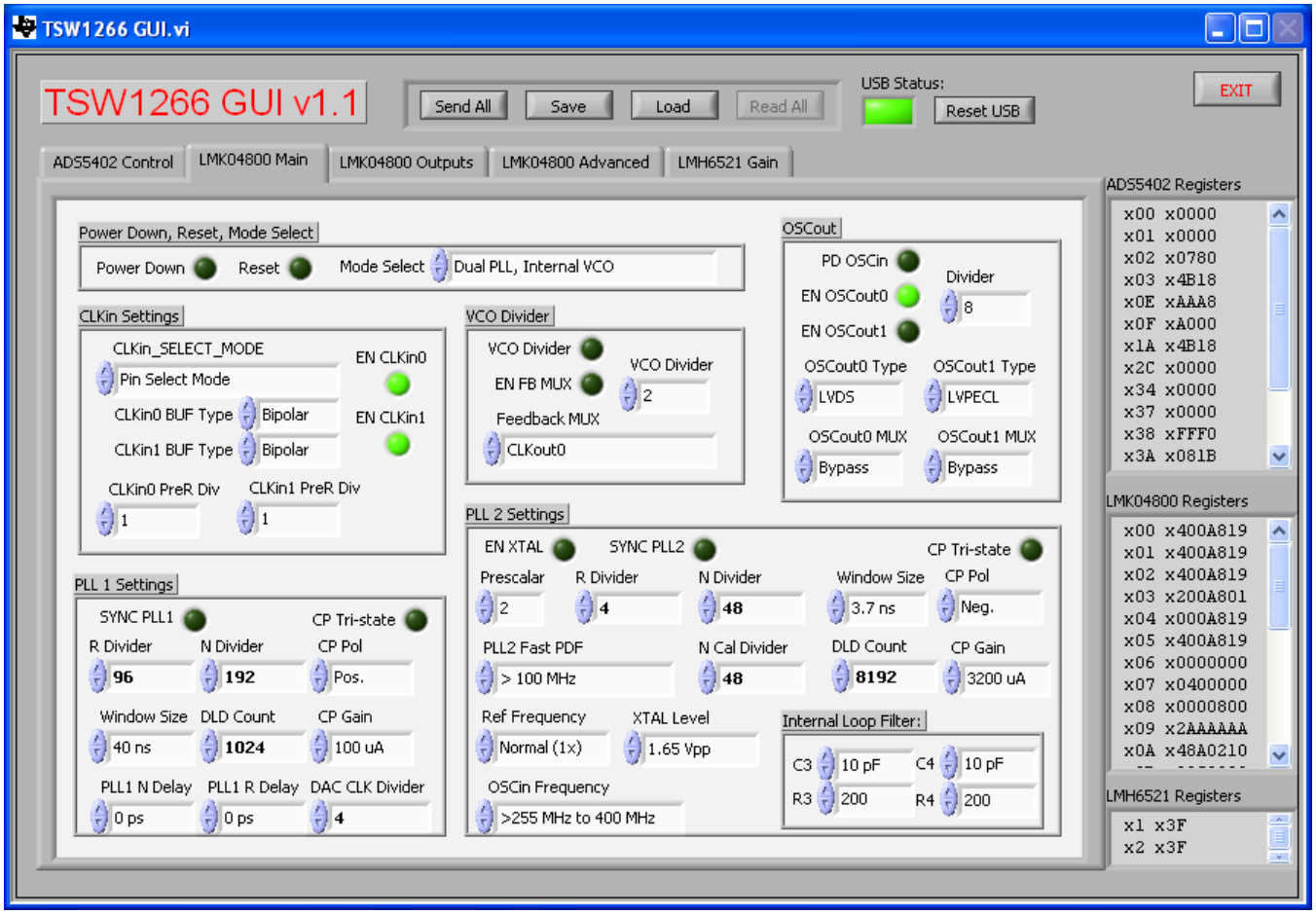

Figure 3. LMK04800 Main Tab

Table 2. LMK04800 Main Tab Section Descriptions

Section	Description
Power Down, Reset, Mode Select	Allows for powering down and resetting the part, also controls the mode of the LMK04800.
CLKin Settings	Enabled and select the input clock source, input buffer types, and dividers.
VCO Divider	Set the VCO divider to reduce the frequency on the clock distribution path. It is recommended to use the VCO directly.
OSCout	Control power to the OSCin port, also enable and change parameters of the OSCout pins.
PLL 1 Settings	Configure PLL 1 settings when using the dual PLL mode.
PLL 2 Settings	Configure PLL 2 settings for both dual and single PLL mode.

2.2.3 LMK04800 Outputs Tab

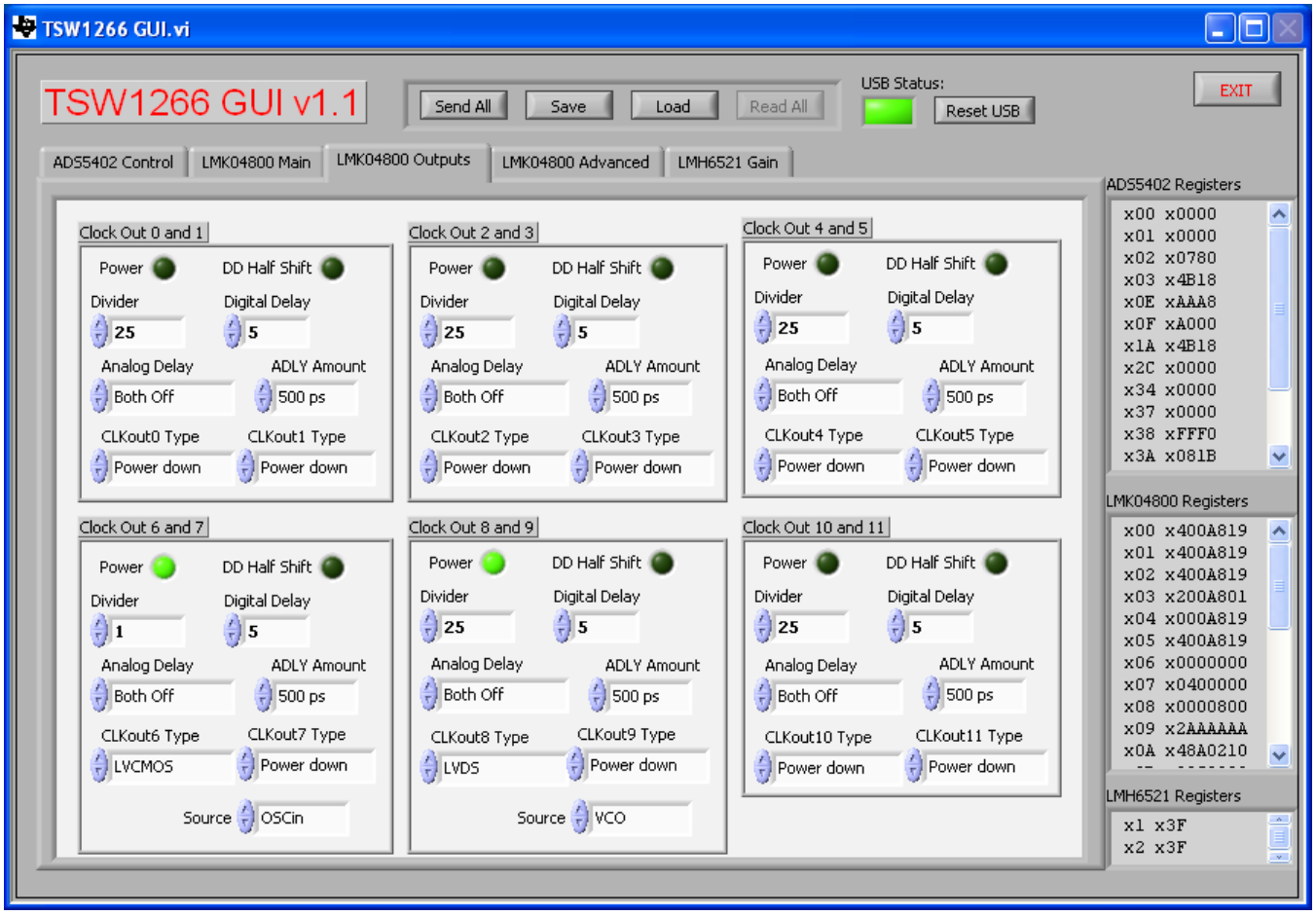

Figure 4. LMK04800 Outputs Tab

Table 3. LMK04800 Outputs Tab Section Descriptions

Section	Description
Clock Out 0 and 1	Configure Clock Out 0 and 1 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 2 and 3	Configure Clock Out 2 and 3 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 4 and 5	Configure Clock Out 4 and 5 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 6 and 7	Configure Clock Out 6 and 7 outputs. Enable the outputs and set the divider, delay, and output buffer, also select the source for the output.
Clock Out 8 and 9	Configure Clock Out 8 and 9 outputs. Enable the outputs and set the divider, delay, and output buffer, also select the source for the output.
Clock Out 10 and 11	Configure Clock Out 10 and 11 outputs. Enable the outputs and set the divider, delay, and output buffer.

2.2.4 LMK04800 Advanced Tab

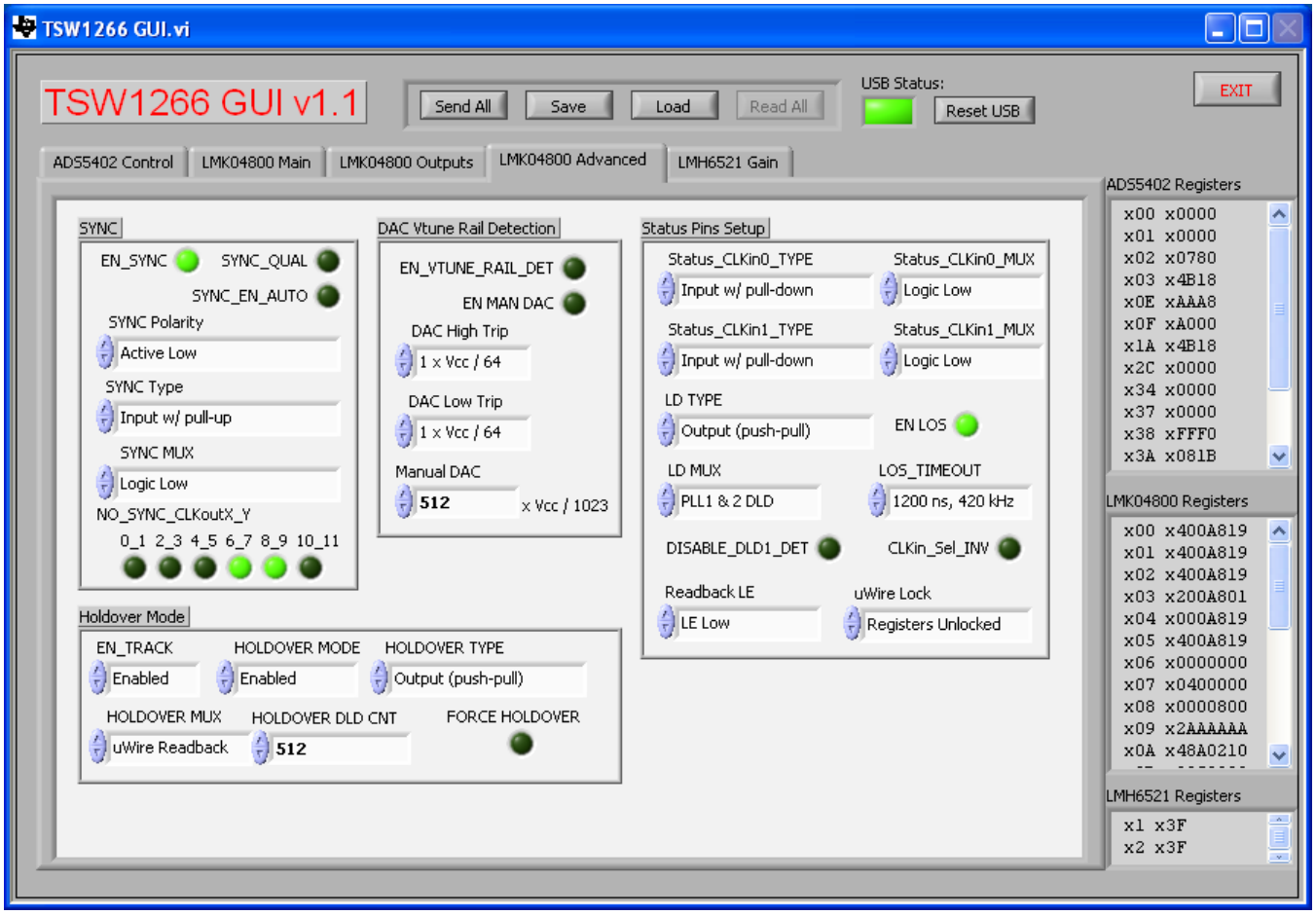

Figure 5. LMK04800 Advanced Tab

Table 4. LMK04800 Advanced Tab Section Descriptions

Section	Description
SYNC	Enable and configure the sync functionality.
DAC Vtune Rail Detection	Enable and control the internal DAC settings.
Status Pins Setup	Setup the status pins for various outputs as well as control some miscellaneous functions.
Holdover Mode	Enable and configure holdover mode.

2.2.5 LMH6521 Gain Tab

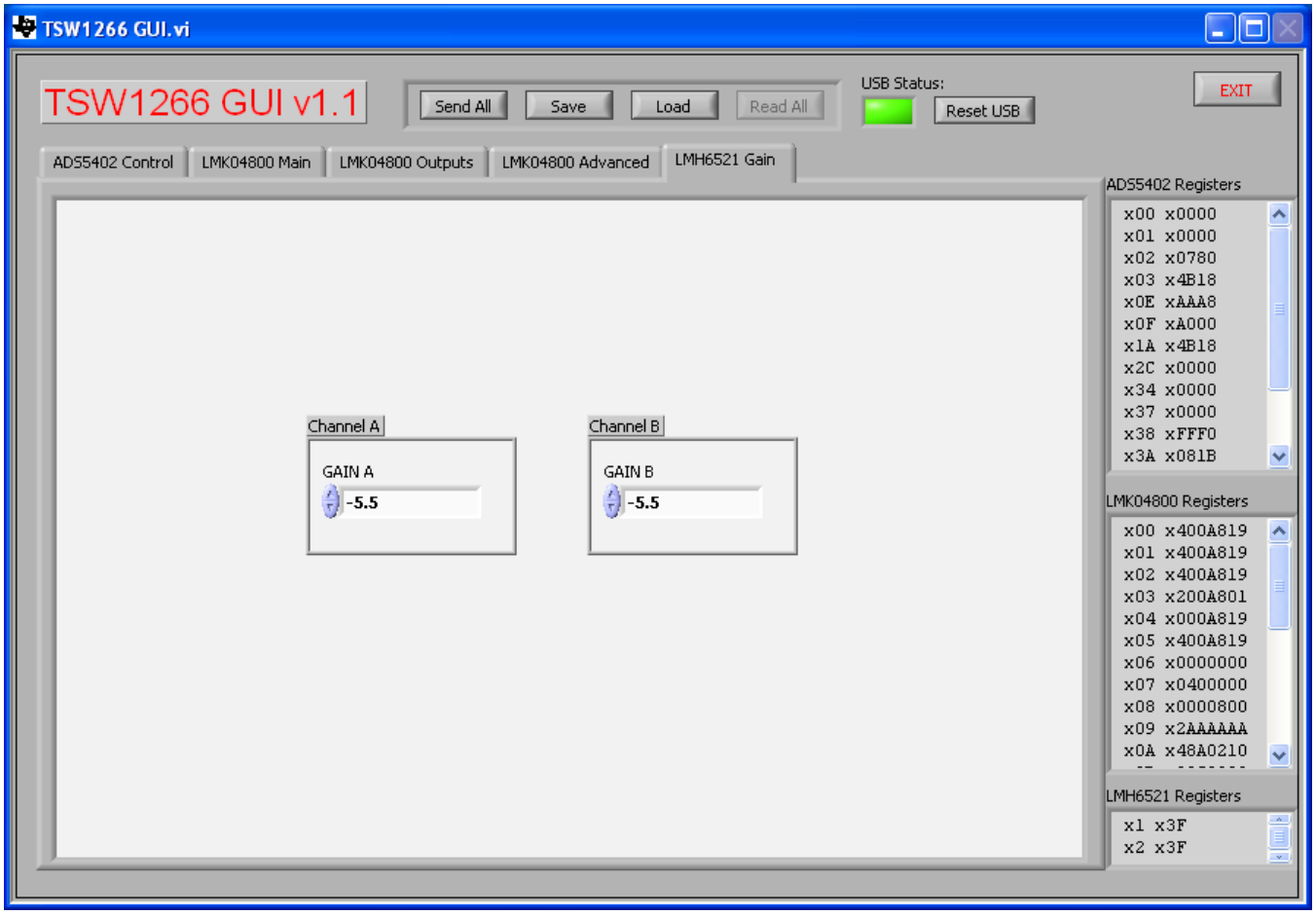

Figure 6. LMH6521 Gain Tab

Table 5. LMH6521 Gain Tab Section Descriptions

Section	Description
Channel A	Set the gain for channel A of the LMH6521.
Channel B	Set the gain for channel B of the LMH6521.

2.2.6 Send All, Save, Load, Read All

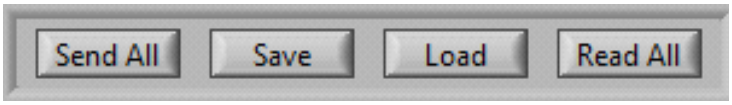

Figure 7. Send All, Save, Load, and Read All

Table 6. Send All, Save, Load, and Read All Descriptions

Section	Description
Send All	Click to send all the registers for all devices. Press a few times if the board does not seem to be responding correctly.
Save	Save the register settings in a text file. Can be reloaded later to set the GUI and devices to a known state.
Load	Load a saved configuration.
Read All	This function is not currently enabled on the TSW1265 GUI.

2.2.7 USB Status

The indicator shows the status of the USB connection. The indicator is lit when the USB connection is valid. If the computer is not connected to the board, click the **Reset USB** button.

2.2.8 Exit

Click to exit the GUI. Note that the *X* in the upper right corner of the window has been disabled to ensure that the USB connection is closed properly.

3 Basic Test Procedure

3.1 TSW1400 Setup

See the TSW1400 User's Guide (SLWU079) for a more detailed explanation of the TSW1400 setup and its features. This document assumes that the High Speed Data Converter Pro software and the TSW1400 pattern capture and generation board are both installed and functioning properly. This information can be found at http://www.ti.com/tool/tsw1400evm.

3.2 Quick-Start Procedure

3.2.1 TSW1400 Data Capture Card

1. Connect a 5-V power supply to connector J12 of the TSW1400. Flip switch SW7 to the *ON* position.
2. Insert a USB cable into the USB port on the TSW1400. Connect the other end to the PC.

3.2.2 TSW1266EVM

1. Connect a 6-V power supply to either the banana jacks or the barrel connector. If using the banana jacks, connect the positive end to J17 and the negative end to J16.
2. Connect a USB cable between the TSW1266 board and the PC.
3. Connect a 10-MHz reference (such as the one from the back of the signal generator) to the CLKIN SMA connector on the TSW1266. If a 10-MHz reference is not available, it is still possible to use the onboard clocking solution.
4. Connect an LO source to the SMA connector labeled *LO*. Set the LO source to 2600 MHz and 0 dBm.
5. Connect an RF source to the SMA connector labeled *RF*. Because the DVGA may come up with an unknown gain, set the amplitude of the RF input to –30 dBm to prevent overdriving the ADC on start-up. Set the frequency to 2140.9 MHz.
6. Connect the TSW1266 to the TSW1400 by connecting J1 on the TSW1266 to the ADC Interface connector on the bottom of the TSW1400.

3.2.3 TSW1266 GUI

1. Start the TSW1266 GUI by going to
   Start Menu → All Programs → Texas Instruments ADCs → TSW1266 GUI.
2. Make sure the green indicator is lit indicating that the TSW1266 board has been successfully connected to the PC. If not, click the **Reset USB** button. If it still is not lit, check the USB connection. If the USB connection is correct, unplug the USB cable, wait five seconds and then plug it back in. Repeat these steps if necessary.
3. Click on the ADS5402 tab and toggle the *RESET* switch a few times. Repeat this step for the LMK04800 tab as well. The LMK04800 and ADS5402 need to be RESET for proper operation.
4. Click the **Load** button. If a 10-MHz reference was plugged into the CLKIN connector, select the file named *LMK04808_614p4M_Dual_Loop_10M_Ref.txt*. If a 10-MHz reference was not available, select the file named *LMK04808_614p4M_Single_Loop.txt*. Click *Ok*. The file is located in the TSW1266 GUI installation directory in the folder named *Configuration Files*.
5. Click *Send All*. At this point, the LED labeled *D1* on the TSW1266 should be lit indicating a PLL lock. If it is not lit, click *Send All* again.

3.2.4 High Speed Data Converter Pro

1. Start the High Speed Data Convert Pro software tool by going to Start Menu → All Programs → Texas Instruments ADCs → High Speed Data Converter Pro.
2. When it prompts for the serial number of the board, select the serial number that represents the TSW1400 that has been connected to the TSW1266. This number should be on a sticker on the TSW1400.
3. In the *Select ADC* drop-down box select *ADS5402*. If it asks to download the firmware select *Yes*. Multiple LEDs will light up on the TSW1400 once the firmware has finished downloading.
4. Select *Single Tone* from the *Test Selection* drop-down menu.
5. At the bottom left corner, enter *614.4M* into the *ADC Sampling Rate (Fs)* box. Enter *459.1M* into the *ADC Input Target Frequency* box. Press the *Enter* key.
6. All boards and software are now set up. Click the **Capture** button. Once the capture is complete, adjust the input source amplitude and LMH6521 gain as needed. The LMH6521 gain can be changed on the *LMH6521* Gain tab of the TSW1266 GUI. An example of a –1-dBFS plot is shown in the figure below.

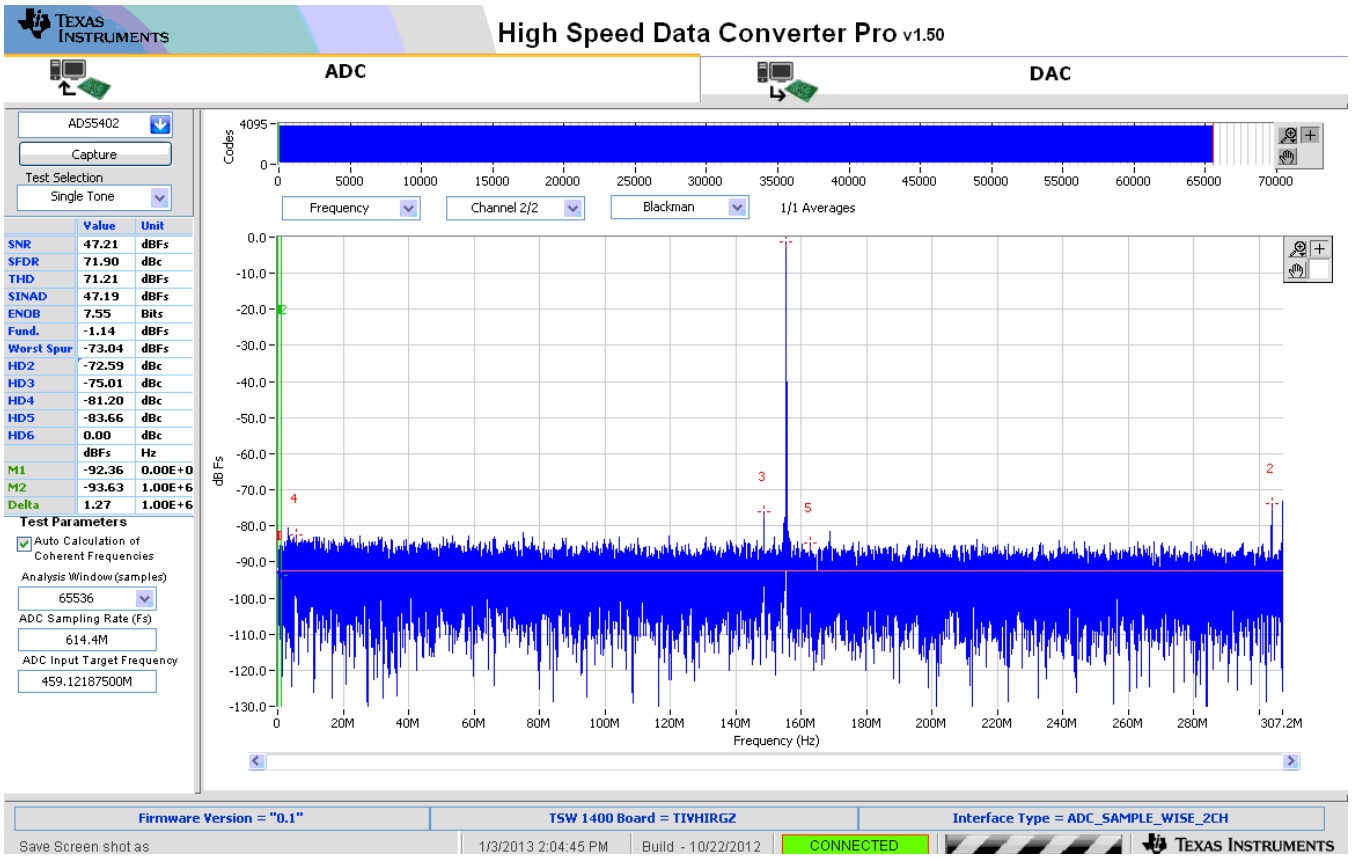

Figure 8. TSW1266 Sample Capture using the TSW1400

3.3 Optional Features and Configurations

3.3.1 Clocking

The TSW1266EVM allows for multiple clocking configurations by using the LMK04800 clock jitter cleaner and generation chip. The board comes preinstalled with a 122.88-MHz VCXO which can be used to generate the sampling clock. A 10-MHz reference can be applied to the CLKIN connector to synchronize the onboard clock with the signal sources. Otherwise, the onboard VCXO can be used to generate a non-synchronous clock or clock distribution mode can be used.

The TSW1266 board comes preinstalled with the LMK04808 which has an internal VCO frequency range of 2750 MHz to 3072 MHz. If the desired clock cannot be derived from this frequency range using integer dividers, then this device can be swapped out for another LMK04800 with a different VCO range. Consult the LMK04800 datasheet (SNAS489) to determine which LMK04800 will provide the correct VCO range for the needed clocking frequency.

The LMK04800 can be setup in clock distribution mode or as a clock generator using single or dual PLL mode. The different modes of operation are discussed below.

- **External Clock Mode:** The LMK04800 can be setup in clock distribution mode to allow the use of an external clock source. This can be used for coherent sampling by provided a clock that is synchronized to the RF and LO signal sources. The TSW1266 GUI includes a configuration file for the external clock mode. This file is located in the TSW1266 GUI installation directory in the folder *Configuration Files* and is named *external_clock.txt*. The file can be loaded by clicking the **Load** button, navigating to the correct folder, selecting the file, and clicking *Ok*. Click *Send All* a few times to make sure the board is configured properly. The user provides an external clock through the *CLKIN1* SMA connector on the TSW1266 board.

- **Onboard Clock using Single PLL Mode:** In this mode, the 122.88-MHz VCXO is used to generate other frequencies by using the single PLL mode of the LMK04800. The 122.88-MHz VCXO acts as the reference for the PLL and the divided down internal VCO acts as the clock source. There is an included configuration file that will setup the LMK04800 in single PLL mode and generate a 614.4-MHz sampling clock for the ADS5402. This file is located in the TSW1266 GUI installation directory in the folder *Configuration Files* and is named *LMK04808_614p4M_Single_Loop.txt*. The file can be loaded by clicking the **Load** button, navigating to the correct folder, selecting the file, and clicking *Ok*. Click *Send All* a few times to make sure the board is configured properly. The LED labeled *D1* on the board will light up indicating that the PLL is locked.
- **Onboard Clock using Dual PLL Mode:** This mode of operation allows the user to provide a low frequency reference through the CLKIN1 connector to generate a synchronized sampling clock. The reference can come from any source, such as a 10-MHz reference from a piece of test equipment. This allows for synchronization between all signal sources and for coherent sampling. There is an included configuration file that will setup the LMK04800 in dual PLL mode and generate a 614.4-MHz sampling clock for the ADS5402. This file is located in the TSW1266 GUI installation directory in the folder *Configuration Files* and is named *LMK04808_614p4M_Dual_Loop_10M_Ref.txt*. The file can be loaded by clicking the **Load** button, navigating to the correct folder, selecting the file, and clicking *Ok*. Click *Send All* a few times to make sure the board is configured properly. The LED labeled *D1* on the board will light up indicating that both PLLs are locked. For other output or reference frequencies, use the Clock Design Tool (http://www.ti.com/tool/clockdesigntool) to design the PLL settings.

3.3.2 Changing the RF and LO Frequencies

The default RF frequency range is 1880 MHz to 2390 MHz. The default LO frequency range is around 2600 MHz. These ranges are set by the matching networks on the RF and LO inputs of the demodulator. These matching networks can be changed based on the data sheet of the part.

3.3.3 Changing the IF Frequency

The IF frequency of the TSW1266 is fixed due to the LC filters on the board. There is a filter between the demodulator and the LMH6521 and a filter between the LMH6521 and the ADS5402. These filters provide an overall 3-dB bandwidth of 500 MHz centered at 460.8 MHz. To change the IF frequency of the TSW1266, the user must change the filters that are implemented on the board. There are many tools available for download online that will calculate a filter design based on frequency and ripple requirements. Use these tools to get a starting point for the filter design. Due to parasitic capacitance and inductance on the board, the user must interactively tune the filter to achieve the desired response. Once the filter has been designed for one channel, it can be implemented on the other channel as well.

3.3.4 Using the High-Speed Connector to Set the DVGA Gain

The high-speed connector (J1) on the TSW1266 board has connections that allow a user to change the gain of the LMH6521 quickly. Pins 105, 107, 109, 111, 113, 115, 117, and 119 on the connector can be used to pass the gain and latch signals from an FPGA to the DVGA. To use this feature, the jumper JP9 needs to be moved between pins 2 and 3. This configures the CPLD to route the gain from the connector rather than from the USB connection.

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