User's Guide
SLUU410–February 2010

bq24600/20/40 EVM (HPA421) Multi Cell Synchronous Switch-Mode Charger

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PowerPAD is a trademark of Texas Instruments.

1 Introduction

1.1 EVM Features

- Evaluation Module for bq24600/bq24620/bq24640
- High Efficiency Synchronous Buck Charger
- User-programmable up to 26V Battery Voltage
- AC Adapter Operating Range 5V–28V
- LED Indication for Control and Status Signals.
- Test Points for Key Signals Available for Testing Purpose. Easy Probe Hook-up.
- Jumpers Available. Easy to Change Connections.

1.2 General Description

The bq24600 is a highly integrated Li-ion or Li-polymer switch-mode battery charge controller. The bq24620 is highly integrated switch-mode battery charge controller designed specifically to charge Lithium Phosphate battery chemistries. The bq24640 is highly integrated super capacitor switch-mode charge controller.

The devices offer a constant-frequency synchronous PWM controller with high accuracy charge current and voltage regulation, adapter current regulation, termination, charge preconditioning, and charge status monitoring, The bq24600/bq24620 charges the battery in three phases: preconditioning, constant current, and constant voltage. Charge is terminated when the current reaches a minimum user-selectable level. A programmable charge timer provides a safety backup for charge termination.

The bq24600/bq24620 automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage.

For details, see bq24600 (SLUS891); BQ24620 (SLUS893) and bq24640 data sheet.

1.3 I/O Description

Table 1. I/O description

Jack	Description
J1 – ACPWR	AC adapter, positive output
J1 – GND	AC adapter, negative output
J2 – BATDRV_EXT	External BATDRV signal
J2 – ACDRV_EXT	External ACDRV signal
J2 – GND	Ground
J3 – VSYS	Connected to system
J3 – VBAT	Connected to battery pack
J3 – GND	Ground
J3 – TS	Temperature Qualification Voltage Input
J4 – GND	External power supply, negative output
J4 – ISET1	Charge Current Program Pin
J4 – VEXT	External power supply, positive output
J5 – $\overline{PG}$	Power Good (active low)
J5 – CHGEN	Charge-enable active-HIGH logic input.
J5 – VREF	IC reference voltage VREF
J5 – GND	Ground
JP1 – BATDRV_EXT	External BATDRV signal
JP1 – BATDRV	BATDRV net
JP1 – BATDRV_IN	Internal BATDRV signal
JP2 – ACDRV_EXT	External ACDRV signal

Table 1. I/O description (continued)

Jack	Description
JP2 – ACDRV	ACDRV net
JP2 – ACDRV_IN	Internal ACDRV signal
JP3 – VEXT	External power supply from J4
JP3 – PULLUP	Pull-up voltage source
JP3 – VREF	IC reference voltage VREF
JP4 – CHGEN	Charge-enable signal
JP4 – GND	Ground
JP5 – LEDPWR	LED Pull-up power line
JP5 – VPULLUP	Pull-up voltage source from JP3

1.4 Controls and Key Parameters Setting

Table 2. Controls and Key Parameters Setting

Jack	Description	Factory Setting
JP1	BATDRV setting Connect BATDRV to external signal BATDRV_EXT Connect BATDRV to internal signal BATDRV_IN	Connect BATDRV to BATDRV_IN
JP2	ACDRV setting Connect ACDRV to external signal ACDRV_EX Connect ACDRV to internal signal ACDRV_IN	Connect ACDRV to ACDRV_IN
JP3	VPULLUP setting 1-2 : Connect VPULLUP to VREF 2-3 : Connect VPULLUP to VEXT	Jumper On 1-2 (VPULLUP and VREF)
JP4	CHGEN is pulled high and the output is enabled when Jumper is on.	Jumper Off
JP5	The pull-up power source supplies the LEDs when on. LED has no power source when off.	Jumper On

Table 3. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
Supply voltage, V_{IN}	Input voltage from ac adapter input	5	24	28	V	
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J5	2.1	21	26	V	
Supply current, I_{AC}	Maximum input current from ac adapter input	0		4.5	A	
Charge current, I_{chrg}	Battery charge current	2	3	8	A	
Operating junction temperature range, T_J		0		125	°C	

The bq246000/20/40 EVM board requires a regulated supply approximately 0.5 V minimum above the regulated voltage of the battery pack to a maximum input voltage of 28 VDC. R14 and R15 can be changed to regulate output.

$$V_{BAT} = 2.1\ V \times \left[1 + \frac{R14}{R15}\right] \text{ for bq24600/40;} \qquad V_{BAT} = 1.8\ V \times \left[1 + \frac{R14}{R15}\right] \text{ for bq24620}$$

Adjust the input voltage as required. Output set to operate at 21V (bq24600), 18V (bq24620) or 19.8V (bq24640) from the factory.

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA421 evaluation board. On the test procedure the following naming conventions are followed. See the HPA421 schematic for details.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy):	Voltage at internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx):	Voltage at jack terminal Jxx.
V(TP(XXX)):	Voltage at test point "XXX". For example, V(ACDET) means the voltage at the test point which is marked as "ACDET".
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	Internal jumper Jxx terminals are shorted
Jxx OFF:	Internal jumper Jxx terminals are open
Jxx (-YY-) ON:	Internal jumper Jxx adjacent terminals marked as "YY" are shorted
Measure:→A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Equipment

2.2.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 30-V at 5-A is required.
Power Supply #2 (PS#2): a power supply capable of supplying 5-V at 1-A is required.
Power Supply #3 (PS#3): a power supply capable of supplying 30-V at 1-A is required.

2.2.2 LOAD #1

A 30V (or above), 5A (or above) electronic load that can operate at constant current mode

2.2.3 LOAD #2

A Kepco bipolar operational power supply/amplifier, 0 ± 30V (or above), 0 ± 6A (or above).

2.2.4 METERS

Seven Fluke 75 multimeters, (equivalent or better)
Or: Four equivalent voltage meters and three equivalent current meters.
The current meters must be capable of measuring 5A+ current.

2.3 Equipment Setup

(A) Set the power supply #1 for 0V ± 100mVDC, 5 ± 0.1A current limit and then turn off supply.
(B) Connect the output of power supply #1 in series with a current meter (multimeter) to J1 (VIN, GND).
(C) Connect a voltage meter across J1 (VIN, GND).
(D) Set the power supply #2 for 0V ± 100mVDC, 1 ± 0.1A current limit and then turn off supply.
(E) Connect the output of the power supply #2 to J3 (TS, GND).
(F) Connect Load #1 in series with a current meter to J3 (SYS, GND). Turn off Load #1.
(G) Connect Load #2 in series with a current meter to J3 (BAT, GND).Turn off Load #2.
(H) Connect a voltage meter across J3 (BAT, GND).
(I) Connect an oscilloscope's probe across J3 (BAT, GND).
(J) Connect a voltage meter across J3 (SYS, GND).
(K) JP1: Connect to BATDRV_IN, JP2: Connect to ACDRV_IN, JP3 (VPULLUP and VREF): ON, JP4: OFF, JP5: ON.

After the steps above, the test setup for HPA421 is shown in Figure 1.

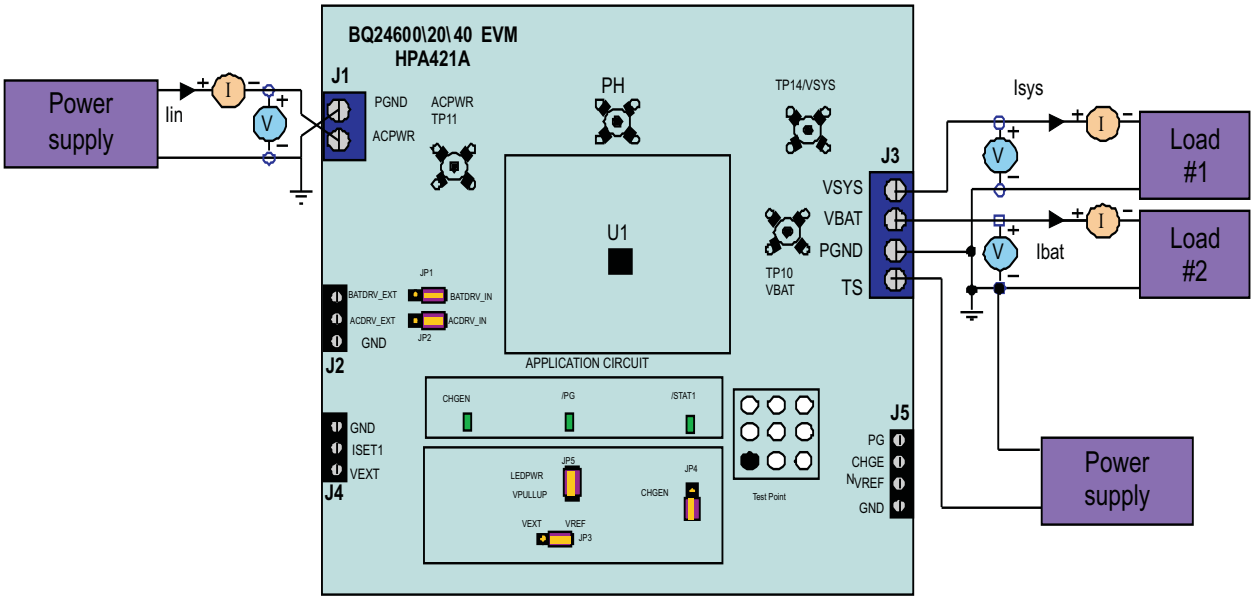

Figure 1. Original Test Setup for HPA421 (bq24600/20/40 EVM)

2.4 Procedure

2.4.1 AC ADAPTER DETECTION THRESHOLD

1. Make sure EQUIPMENT SETUP steps are followed. Turn on PS#2.
2. Turn on PS#1
   Measure → V(J3(SYS)) = 0 ± 500mV
   Measure → V(TP(VREF)) = 0V ± 1000mV
   Measure → V(TP(REGN)) = 0V ± 500mV
3. Increase the output voltage on PS#1 until D6 ($\overline{PG}$) on but do not exceed 5V. Set the power supply #2 to 1.8V ± 100mVDC
   Measure → V(J1(VIN)) = 4.2V ± 0.5V
   Measure → V(J3(SYS)) = 4.2V ± 0.5V
   Measure → V(TP(VREF)) = 3.3V ± 200mV
   Measure → V(TP(REGN)) = 0V ± 500mV
   Observe → D7 (STAT) blink; D6 ($\overline{PG}$) on

2.4.2 CHARGER REGULATION VOLTAGE

1. Increase the voltage of PS#1 until V(J1(VIN)) = 24V ± 0.1V.
   Measure → V(J3(BAT, GND)) = 0V ± 1V
2. Put JP4 on.
   Measure → Peak V(J3(BAT)) = 21V ± 1V (bq24600)
   Peak V(J3(BAT)) = 18V ± 1V (bq24620)
   Peak V(J3(BAT)) = 19.8V ± 1V (bq24640)
   Measure → V(TP(REGN)) = 6V ± 500mV
   Observe → D5(CHGEN) on; D7($\overline{\text{STAT}}$) blink; D6 ($\overline{\text{PG}}$) on. (bq24600/20)
   D5(CHGEN) on; D7($\overline{\text{STAT}}$) on; D6 ($\overline{\text{PG}}$) on. (bq24640)

2.4.3 CHARGE CURRENT

1. Take JP4 off (Disable the charging).
2. Connect the Load #2 in series with a current meter (multimeter) to J3 (BAT, GND). Make sure a voltage meter is connected across J3 (BAT, GND). Turn on the Load #2. Use the constant voltage mode. Set the output voltage to 12V (HPA421 -001) or 2V (HPA421,-002,-003).
3. Connect the output of the Load #1 in series with a current meter (multimeter) to J3 (SYS, GND). Make sure a voltage meter is connected across J3 (SYS, GND). Turn on the power of the Load #1. Set the load current to 1A ±50mA but disable the output. Make sure Ibat = 0A ± 10mA and Isys = 0A ± 10mA.
4. Put JP4 on (Enable the charging).
   Observe → D5 (CHG EN) on
5. *Measure* → Ibat = 300mA ± 200mA (bq24600)
   Ibat = 125mA ± 60mA (bq24620)
   Ibat = 3A ± 300mA (bq24640)
   Observe → D7 (**$\overline{\text{STAT}}$**) on.
6. Set the Load #2 output voltage to 16.5V.
   Ibat = 3000mA ± 300mA
   D7 (**$\overline{\text{STAT}}$**) on.
7. Set the Load #2 output voltage to 22V (bq600/40) or 19V (bq620).
   Measure → Ibat = 0mA ± 300mA
   Observe → D5(CHGEN) on; D6 ($\overline{\text{PG}}$) on. (bq24600/20)
   D5(CHGEN) on; D7($\overline{\text{STAT}}$) blink, D6 ($\overline{\text{PG}}$) on. (bq24640)
8. Set the Load #2 output voltage back to 16.5V.
   Measure → Ibat = 3000mA ± 300mA
   Observe → D5(CHGEN) on; D7($\overline{\text{STAT}}$) on, D6 ($\overline{\text{PG}}$) on.

2.4.4 CHARGER CUT-OFF BY THERMISTOR

1. Slowly increase the output voltage of PS2 until Ibat = 0 ±10mA.
   Measure → V(J3(TS)) = 2.44V ±300mV
   Observe → D7 ($\overline{\text{STAT}}$) blink.
2. Slowly decrease the output voltage of PS2 to 1.4V±0.1V.
   Measure → V(J3(TS)) = 1.4V ±100mV
   Measure → Ibat = 3000mA ± 300mA (bq24600/640)
   Ibat = 375mA ± 150mA (bq24620)
   Observe → D7($\overline{\text{STAT}}$) on.
3. Slowly decrease the output voltage of PS2
   Continue to decrease the output voltage of PS2 slowly until Ibat = 0 ±10mA
   Measure → V(J4(TS)) = 1.14V ±200mV
   Observe → D7($\overline{\text{STAT}}$) blink.
4. Slowly increase the output voltage of PS2 to 1.8V ± 300mV.
   Measure → Ibat = 3000V ± 200mV
   Observe → D7($\overline{\text{STAT}}$) on.

2.4.5 POWER PATH SELECTION

1. Take JP4 off (Disable the charging)
   Observe → D5(CHGEN) off; D7 ($\overline{\text{STAT}}$) blink.
2. Set JP3 Jumper On 2-3 (VPULLUP and VEXT). Connect the output of the power supply #3 to J2(VEXT, GND). Set the power supply #3 for 3.3V ± 200mVDC, 1 ± 0.1A current limit.
3. Set Load #2 at 16.5V ± 500mV.
   Measure → V(J3(SYS)) = 24V ±1mV (adapter connected to system)
   Measure → ACDRV = 9V ± 2V; BATDRV = 24V ± 1V
   Observe → D6($\overline{\text{PG}}$) on.
4. Turn off PS#1
5. *Measure* → V(J3(SYS)) = 16.5V ± 0.5mV (battery connected to system)
   Measure → ACDRV = 16V ± 1V; BATDRV = 1.5V ± 1V
6. *Observe* → D6($\overline{\text{PG}}$) off.
7. Turn off power supply #2 and #3. Set JP3 on 1-2 (VPULLUP and VREF).

3 PCB Layout Guideline

1. It is critical that the exposed PowerPAD™ on the backside of the bq24600/20/40 package be soldered to the PCB ground. Make sure there are sufficient thermal vias right underneath the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. Charge current sense resistor must be connected to SRP, SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. Decoupling capacitors for DCIN, VREF, VCC, REGN should make the interconnections to the IC as short as possible.
5. Decoupling capacitors for BAT must be placed close to the corresponding IC pins and make the interconnections to the IC as short as possible.
6. Decoupling capacitor(s) for the charger input must be placed very close to Q4 drain and Q5 source.

4 Board Layout

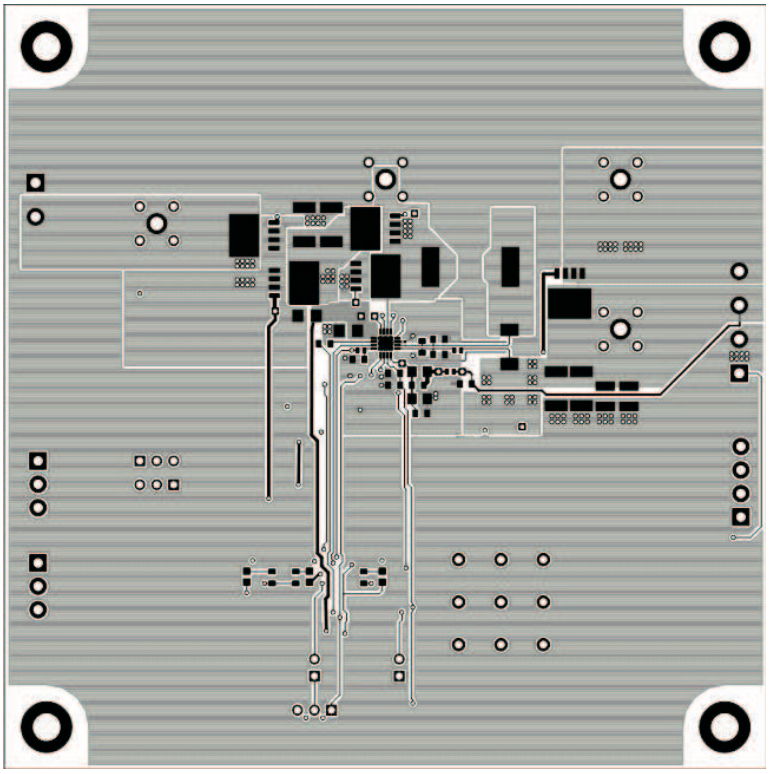

Figure 2. Top Layer

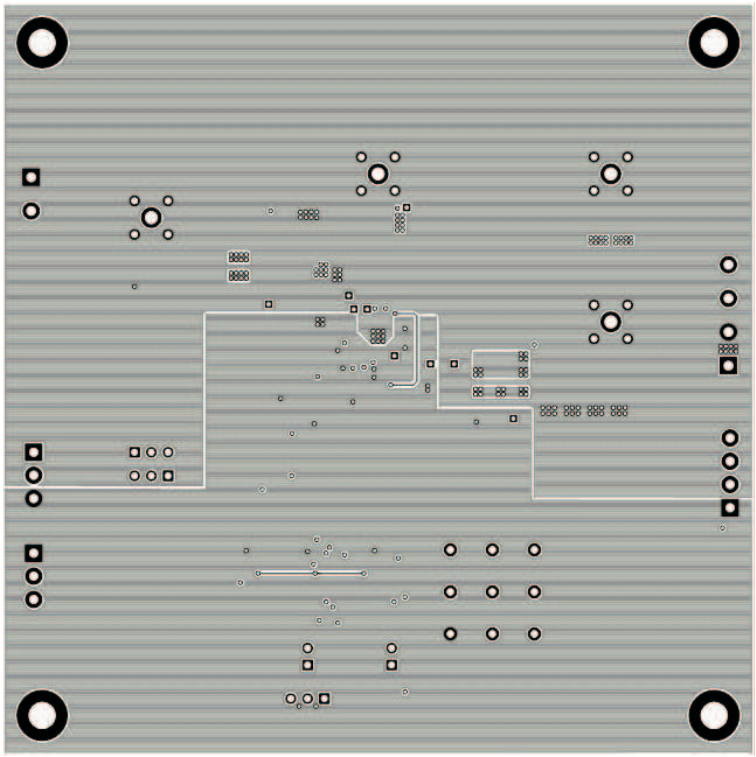

Figure 3. 2nd Layer

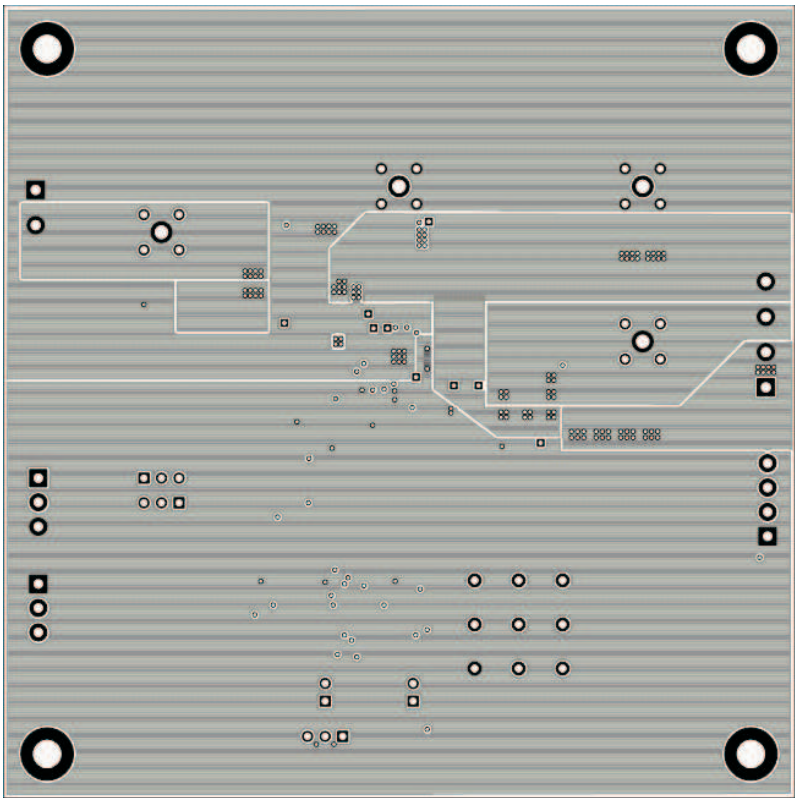

Figure 4. 3rd Layer

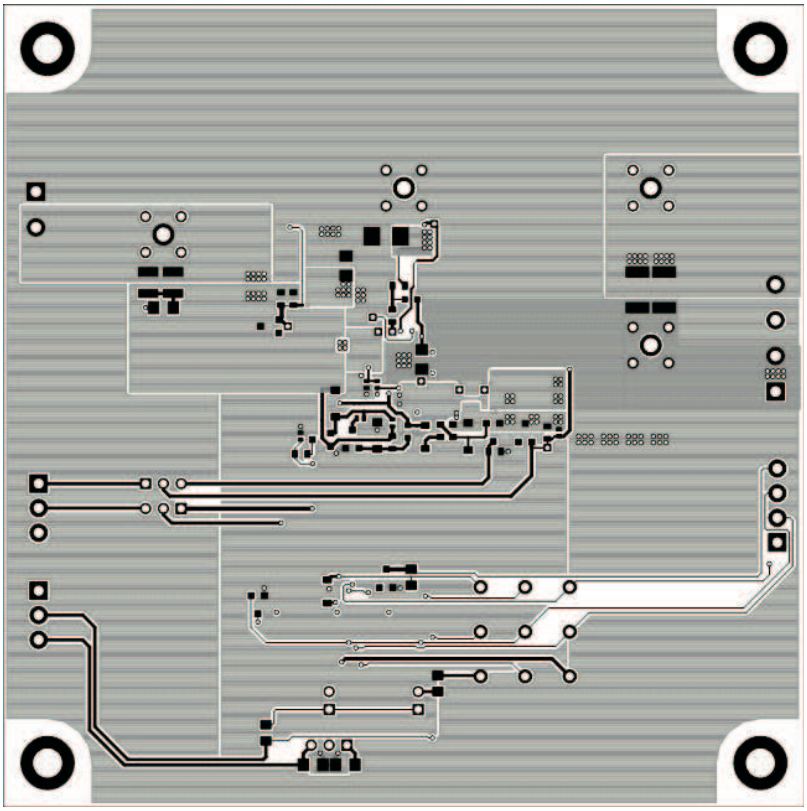

Figure 5. Bottom Layer

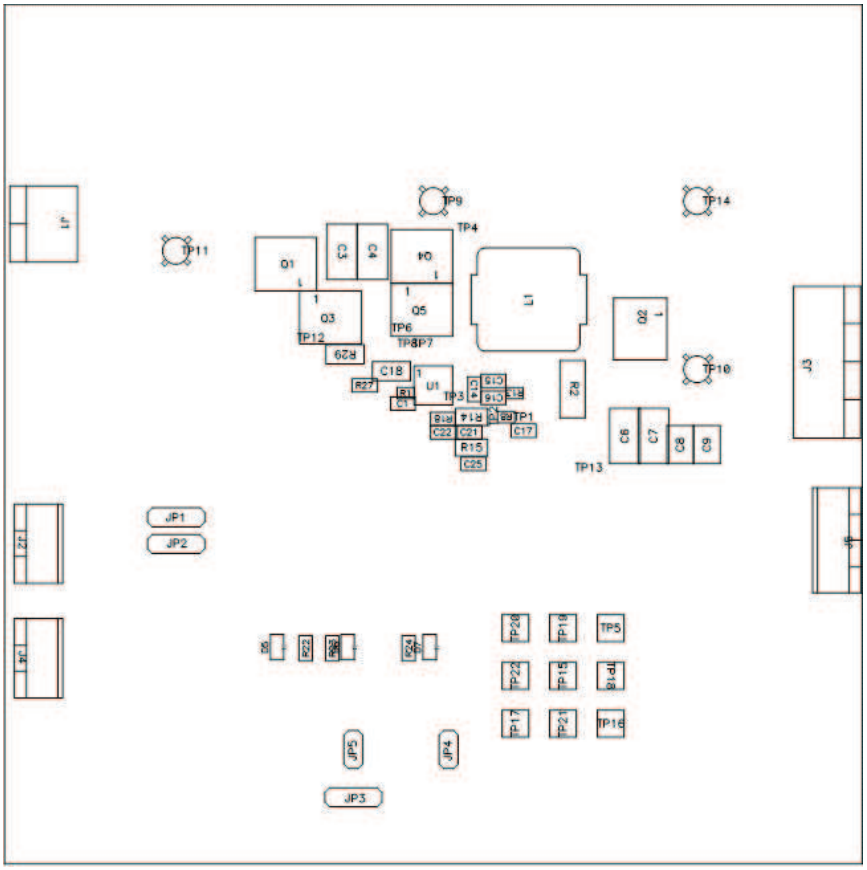

Figure 6. Top Assembly

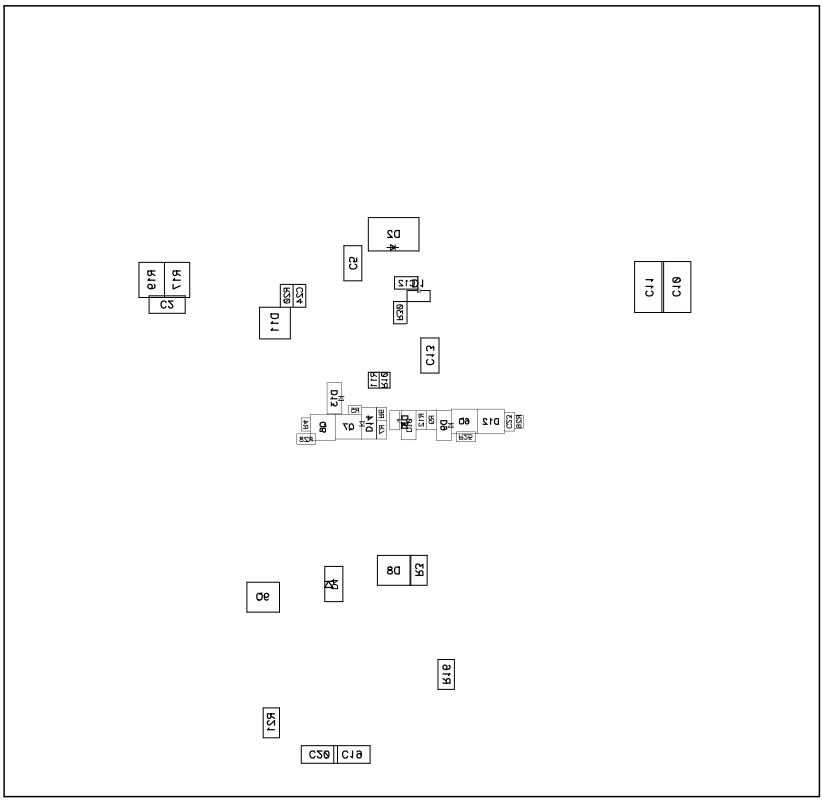

Figure 7. Bottom Assembly

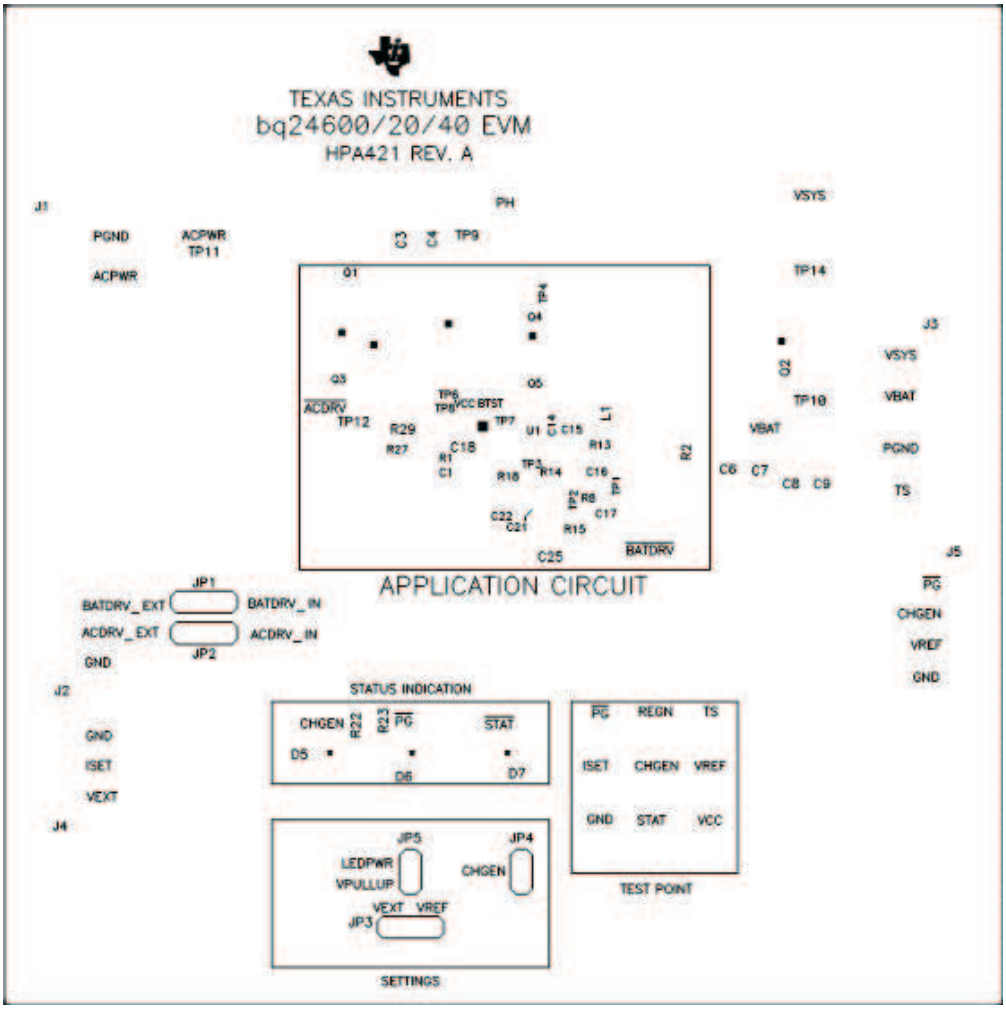

Figure 8. Top Silkscreen

5 Schematics

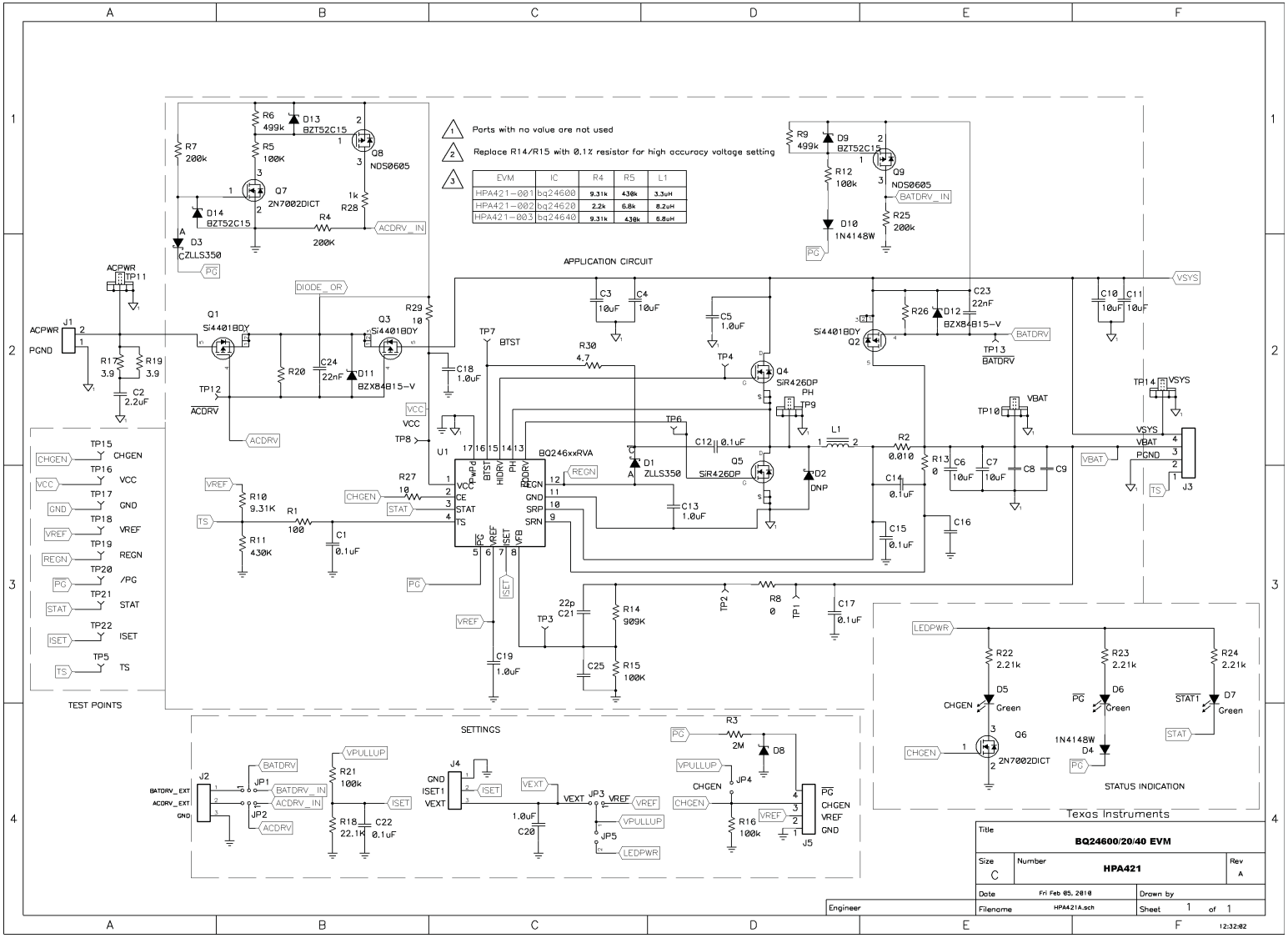

Figure 9. bq246xx EVM Schematic (Sheet 1 of 1)

6 Bill of Materials

Table 4. Bill of Materials

bq24600 -001	bq24620 -002	bq24640 -003	RefDes	Value	Description	Size	Part Number	MFR
1	0	0	U1	BQ24600RVA	IC, 28V Synchronous Switchmode Charge Management	QFN16[RVA]	BQ24600RVA	TI
0	1	0	U1	BQ24620RVA	IC, 28V Synchronous Switchmode Charge Management	QFN16[RVA]	BQ24620RVA	TI
0	0	1	U1	BQ24640RVA	IC, 28V Synchronous Switchmode Charge Management	QFN16[RVA]	BQ24640RVA	TI
6	6	6	C1,C12,C14,C15 ,C17,C22	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1H104K	TDK
2	2	2	C23, C24	22nF	Capacitor, Ceramic, 50V, X7R, 10%	603	Std	TDK
1	1	1	C21	22p	Capacitor, Ceramic, 50V, X7R, 10%	603	Std	TDK
0	0	0	C16	DNP	Capacitor, Ceramic, 50V, X7R, 10%	603	Std	TDK
0	0	0	C25	DNP	Capacitor, Ceramic, 50V, X7R, 10%	603	Std	TDK
5	5	5	C5,C13,C18,C19 ,C20	1.0uF	Capacitor, Ceramic, 50V, X7R, 10%	1206	C3216X7R1H105K	TDK
1	1	1	C2	2.2uF	Capacitor, Ceramic, 50V, X7R, 10%	1206	C3216X7R1H225K	TDK
0	0	0	C8,C9	DNP	Capacitor, Ceramic, 50V, X5R, 20%	1210	Std	Vishay
6	6	6	C3,C4,C6,C7,C1 0,C11	10uF	Capacitor, Ceramic, 50V, X5S, 20%	1812	UMK432C106MM-T	Taiyo Yuden
2	2	2	D4,D10	1N4148W	Diode, Signal, 300-mA, 75-V, 350-mW	SOD-123	1N4148W	Diodes
3	3	3	D9,D13,D14	BZT52C15	Diode, Zener, Planar Power, 15V	SOD-123	BZT52C15	Diodes
2	2	2	D11,D12	BZX84B15-V	Diode, Zener, 15-V, 300-mW	SOT-23	BZX84B15-V	Diodes
0	0	0	D8	DNP	Diode, Zener, xx-V, 300-mW	SOT-23	BZX84Bxx-x	Diodes
0	0	0	D2	DNP	Diode, Schottky, 1A, 30V	SMB	MBRS130TR	IR
2	2	2	D5,D7	Green	Diode, LED, Green, 2.1V, 20mA, 6mcd	603	LTST-C190GKT	Lite On
1	1	1	D6	Red	Diode, LED, Red, 1.8V, 20mA, 20mcd	603	LTST-C190CKT	Lite On
2	2	2	D1,D3	ZLLS350	Diode, Schottky, 1.16A, 40-V	SOD-523	ZLLS350	Zetex
0	1	0	L1	8.2uH	Inductor, IHLP5050EZERxxxM01	0.51 x 0.52 inch	IHLP5050EZERxxxM01	Vishay
1	0	0	L1	3.3uH	Inductor, IHLP5050EZERxxxM01	0.51 x 0.52 inch	IHLP5050EZERxxxM01	Vishay
0	0	1	L1	6.8uH	Inductor, IHLP5050EZERxxxM01	0.51 x 0.52 inch	IHLP5050EZERxxxM01	Vishay
2	2	2	JP4,JP5	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
3	3	3	JP1–JP3	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
5	5	5	SJ1–SJ5	929950-00	Shorting jumpers, 2-pin, 100mil spacing,		929950-00	3M/ESD
2	2	2	R8,R13	0	Resistor, Chip, 1/16W, 5%	402	Std	Std

Table 4. Bill of Materials (continued)

bq24600 -001	bq24620 -002	bq24640 -003	RefDes	Value	Description	Size	Part Number	MFR
1	0	1	R10	9.31K	Resistor, Chip, 1/16W, 1%	402	Std	Std
0	1	0	R10	2.2K	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	0	1	R11	430K	Resistor, Chip, 1/16W, 1%	402	Std	Std
0	1	0	R11	6.8K	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R1	100	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R5	100K	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R4	200K	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R6	499k	Resistor, Chip, 1/16W, 1%	402	Std	Std
0	0	0	R26	DNP	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	R28	1k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R30	4.7	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R27	10	Resistor, Chip, 1/16W, 1%	603	Std	Std
3	3	3	R22–R24	2.21k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R18	22.1K	Resistor, Chip, 1/16W, 1%	603	Std	Vishay
1	1	1	R12	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std
2	2	2	R7,R25	200k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R9	499k	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	0	0	R20	DNP	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	R3	2M	Resistor, Chip, 1/10W, 1%	805	Std	Std
3	3	3	R15,R16,R21	100K	Resistor, Chip, 1/10W, 1%	805	Std	Std
1	1	0	R14	909K	Resistor, Chip, 1/10W, 1%	805	Std	Std
0	0	1	R14	845K	Resistor, Chip, 1/10W, 1%	805	Std	Std
1	1	1	R29	10	Resistor, Metal Film, 1/4 watt, 5%	1206	Std	Std
2	2	2	R17,R19	3.9	Resistor, 1/2W, 5%	1210	Std	Std
1	1	1	R2	0.01	Resistor, Chip, 1/2W, 1%	2010	WSL2010R0100FEA	Vishay, Dale
2	2	2	J2,J4	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
1	1	1	J5	ED1516	Terminal Block, 4 pin, 6A, 3.5mm	0.55 x 0.25 inch	ED1516	OST
1	1	1	J1	ED1609-ND	Terminal Block, 2 pin, 15A, 5.1mm	0.40 x 0.35 inch	ED1609	OST
1	1	1	J3	ED2227	Terminal Block, 4 pin, 15A, 5.1mm	0.80 x 0.35 inch	ED2227	OST
1	1	1	TP17	GND	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
0	0	0	TP1–TP4, TP6–TP8, TP12, TP13		Test Point, 0.020 Hole			

Table 4. Bill of Materials (continued)

bq24600 -001	bq24620 -002	bq24640 -003	RefDes	Value	Description	Size	Part Number	MFR
8	8	8	TP5, TP15, TP16, TP18–TP22	CHGEN,ISET,REGN ,STAT,TS,VCC,VRE F,~PG	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
4	4	4	TP9–TP11,TP14	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.200 inch	131-4244-00	Tektronix
1	1	1	Q7	2N7002DICT	MOSFET, N-ch, 60-V, 115-mA, 1.2-Ω	SOT23	2N7002DICT	Vishay-Liteon
1	1	1	Q6	2N7002DICT	MOSFET, N-ch, 60V, 115mA, 1.2Ω	SOT23	2N7002DICT	Vishay-Liteon
2	2	2	Q8, Q9	NDS0605	MOSFET,P-ch, -60 V, 180-mA, 5 Ω	SOT-23	NDS0605	Vishay
3	3	3	Q1–Q3	Si4401BDY	MOSFET, PChan, –40V, –8.7A, 21mΩ	PWRPAK S0-8	Si4401BDY	Vishay
1	1	1	Q4, Q5	SiR426DP	MOSFET, NChan, 40V, 30A, 12.5 mΩ	PWRPAK S0-8	SiR426DP	Vishay
4	4	4			6-32 NYL nuts	NY HN 632	H620-ND	Building Fasteners
4	4	4	ST1–ST4	4816	STANDOFF M/F HEX 6-32 NYL 0.500"	sf_thvt_325_rnd	4816	Keystone
1	1	1	PCB	HPA421	4x4.25 inch 4 layer 2oz. PCB	4x4.25 inch	PCB	

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 18 V to 22 V and the output voltage range of 0 V to 18 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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