Ian Williams

TI Precision Designs: Verified Design

10 µA-100 mA, 0.05% Error, High-Side Current Sensing

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
PGA281	Product Folder
TPS7A4101	Product Folder

Circuit Description

This split-supply, high-side current sensing solution accurately detects load currents from 10 µA to 100 mA. The linear range of the differential voltage output is from -4.9V to +4.9 V. An instrumentation amplifier with pin-programmable gain was selected in order to measure the four-decade load current range.

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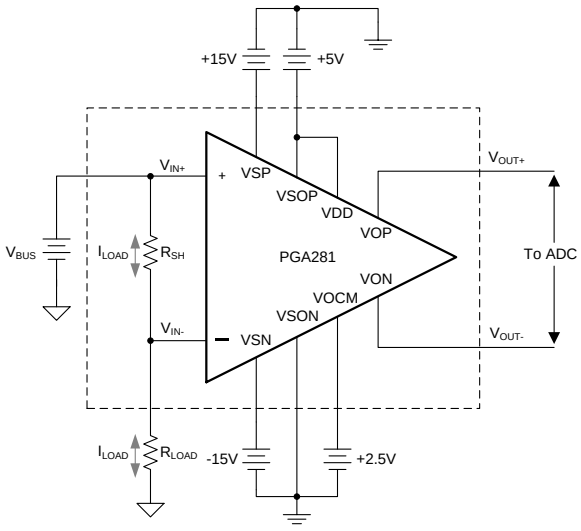

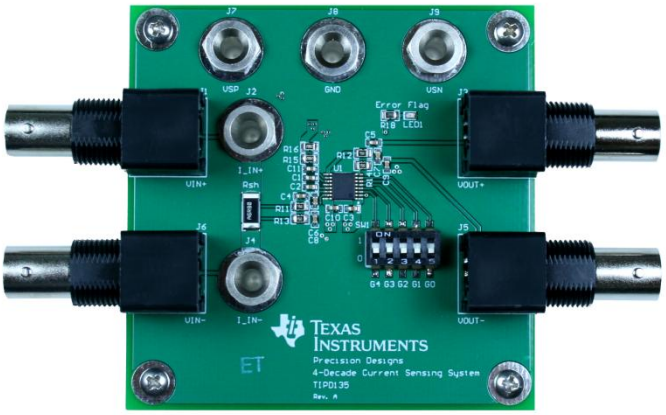

1 Design Summary

The design requirements are as follows:

- Supply Voltage: ±15 V
- Input: 10 µA – 100 mA (bidirectional)
- Output: ± 4.9 V (differential)
- Maximum Shunt Voltage: 700 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Error (%FSR$_{error}$)	0.05%	0.002%	0.0481%
Relative Error (I_{LOAD} = 10 µA, G = 176)	35.0%	30.47%	33.16%
Relative Error (I_{LOAD} = 100 µA, G = 176)	5%	3.13%	3.15%
Relative Error (I_{LOAD} = 1 mA, G = 176)	1%	0.31%	0.31%
Relative Error (I_{LOAD} = 10 mA, G = 5.5)	0.1%	0.09%	0.09%
Relative Error (I_{LOAD} = 100 mA, G = 5.5)	0.01%	0.01%	0.01%

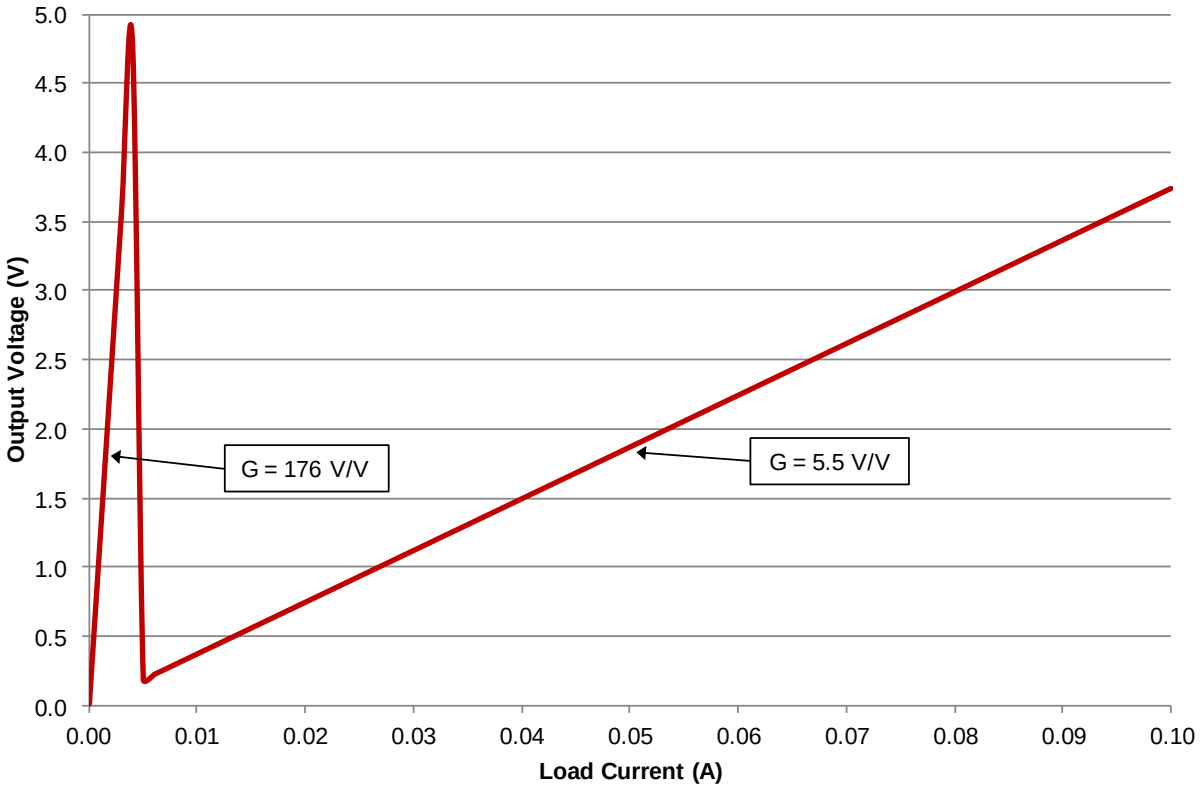

Figure 1: Measured Transfer Function

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The transfer function of the circuit is based on the relationship between the load current I_{LOAD}, the shunt resistance R_{SH}, and the gain blocks inside the PGA281 which are controlled by the switch SW_1. In this high-side current sense application, a power supply V_{BUS} is connected to the load represented by R_{LOAD}. R_{LOAD} draws current I_{LOAD} from V_{BUS} which flows through R_{SH}, developing a voltage drop across R_{SH} as defined by Ohm's Law. This differential voltage is filtered and applied to the input of the PGA, where it is amplified and output differentially with a common-mode voltage equal to half of its output stage supply voltage, or VSOP/2.

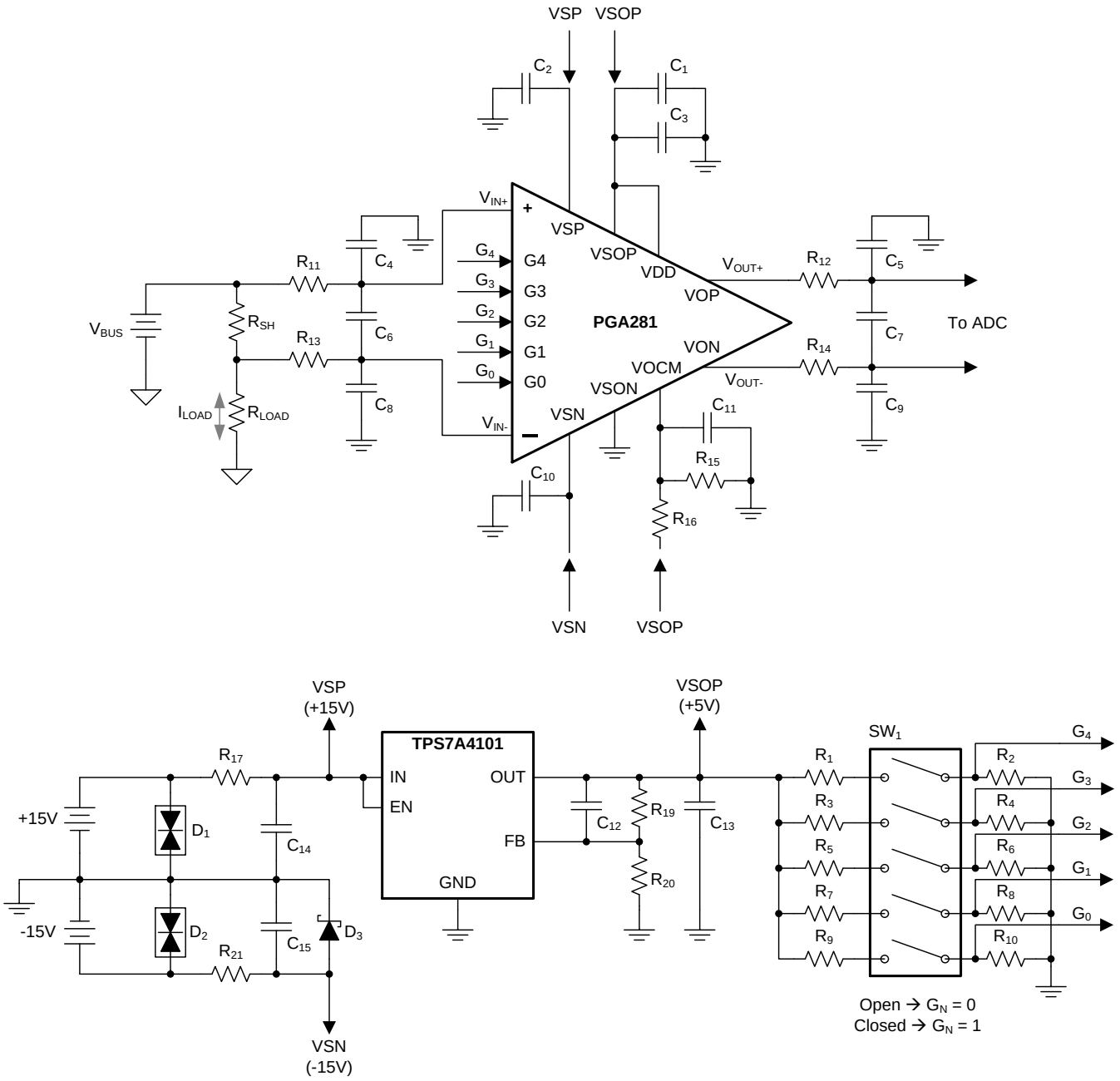

Figure 2: Complete Circuit Schematic

The transfer function for this design is defined by the following equation:

$$V_{OUT} = V_{OUT+} - V_{OUT-} = I_{LOAD} * R_{SH} * Gain_{PGA} \quad (1)$$

2.1 High-Side Current Sensing

In high-side current sensing applications, the sense resistor is placed between the supply voltage V_{BUS} and the load R_{LOAD}. High-side sensing is desirable in that it directly monitors the current delivered by the supply, which allows for the detection of load shorts. The most common challenge when using this topology is that the amplifier's input common-mode voltage range must include the load's supply voltage, or V_{BUS}. With ±15 V supplies the PGA281 can accept common-mode voltages of ±12.5 V, making it a suitable choice for high-side current sensing as long as V_{BUS} falls within the common-mode voltage range.

Figure 3 depicts a typical high-side current sensing scenario.

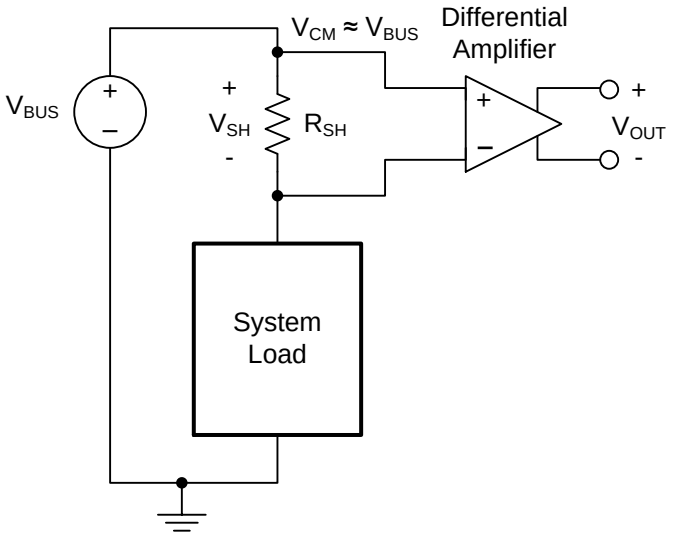

Figure 3: High-Side Current Sensing Topology

As shown in Figure 3, the value of V_{SH} is the voltage drop across the shunt resistor R_{SH}. If the value of V_{SH} is too large, then the voltage actually delivered to the load may not meet the load's minimum requirements. Therefore it is important to limit the voltage drop across the shunt resistor. Equation 2 can be used to calculate the maximum value of R_{SH}.

$$R_{SH(max)} = \frac{V_{SH(max)}}{I_{LOAD(max)}} = \frac{0.7\ V}{100\ mA} = 7\ \Omega \quad (2)$$

It is recommended to use the maximum shunt resistance to minimize relative error at minimum load current. Relative error is discussed in Section 4.4. Based on the availability of resistors at major distributors, a value of 6.8 Ω was chosen for R_{SH}.

The gain(s) required for this design depend on the maximum output swing of the amplifier, shunt resistor, and the load current range. It is recommended to use the maximum gain to ensure full utilization of the linear operating range of the device. Equation 3 shows how to calculate the maximum gain for the maximum load current.

$$G_{I\_LOAD(max)} = \frac{V_{OUT(max)}}{V_{SH(max)}} = \frac{V_{OUT(max)}}{R_{SH(max)} * I_{LOAD(max)}} = \frac{4.9\ V}{6.8\ \Omega * 100\ mA} = 7.21\ \frac{V}{V} \quad (3)$$

The closest available gain setting on the PGA281 (without exceeding the maximum) is 5.5 V/V.

To determine if the design requires more than one gain, the minimum load current that can be measured given $G_{I\_LOAD(max)}$ and $V_{OUT(min)}$ must be calculated as shown in Equation 4 and Equation 5.

$$V_{SH(min)} = \frac{V_{OUT(min)}}{G_{I\_LOAD(max)}} \quad (4)$$

$$I_{LOAD(min)} = \frac{V_{SH(min)}}{R_{SH}} = \frac{V_{OUT(min)}}{G_{I\_LOAD(max)} * R_{SH}} = \frac{10\ mV}{5.5\ \frac{V}{V} * 6.8\ \Omega} = 267.38\ \mu A \quad (5)$$

Since $I_{LOAD(min)}$ does not meet the minimum load current specification of 10 µA, a second gain is required. It is recommended to now calculate the maximum gain for the minimum load current ($G_{I\_LOAD(min)}$) as shown in Equation 6.

$$G_{I\_LOAD(min)} = \frac{V_{OUT(min)}}{V_{SH(min)}} = \frac{V_{OUT(min)}}{R_{SH} * I_{LOAD(min)}} = \frac{10\ mV}{6.8\ \Omega * 10\ \mu A} = 147.06\ \frac{V}{V} \quad (6)$$

The closest available gain setting on the PGA281 is 176 V/V. Equation 7 and Equation 8 show how to calculate the maximum load current that can be measured given $G_{I\_LOAD(min)}$.

$$V_{SH(max)} = \frac{V_{OUT(max)}}{G_{I\_LOAD(min)}} \quad (7)$$

$$I_{LOAD(max)} = \frac{V_{SH(max)}}{R_{SH}} = \frac{V_{OUT(max)}}{G_{I\_LOAD(min)} * R_{SH}} = \frac{4.9\ V}{176\ \frac{V}{V} * 6.8\ \Omega} = 4.09\ mA \quad (8)$$

Since the minimum load current that can be measured when G = 5.5 V/V overlaps with the maximum load current for G = 176 V/V, only two gains are required to measure the entire load current range.

2.2 Input and Output Filtering

In order to minimize noise at the input of the PGA281, a low-pass filter network is placed between the sense resistor and the PGA281 input pins. Figure 4 shows the input filter schematic.

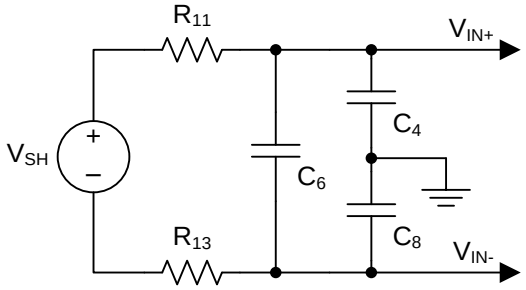

Figure 4: Input Filter Schematic

The input filter has both a common-mode component and a differential component. Since the shunt voltage signal is dc, the cutoff frequencies of this filter can be set very low in order to attenuate any ac noise which may be present. However, this system can also be used as a universal differential gain block for signals up to 10 kHz, so the differential cutoff frequency is set to 10 kHz.

The cutoff frequency of the filter is defined by the following equations:

$$R_{11} = R_{13};\ C_4 = C_8;\ C_6 = 10 * C_4 \tag{9}$$

$$f_{C\_DIFF} = \frac{1}{2 * \pi * 2R_{11} * (10C_4 + \frac{1}{2}C_4)} = \frac{1}{42 * \pi * R_{11} * C_4}\ \text{Hz} \tag{10}$$

$$f_{C\_CM} = \frac{1}{2 * \pi * R_{11} * C_4}\ \text{Hz} \tag{11}$$

The desired cutoff frequencies for this filter are f_{C_DIFF} = 10 kHz and f_{C_CM} = 200 kHz. A simple way to calculate the required passive component values is to pick a common value for C_4 and solve for R_{11}. By rearranging the terms of the equations above, the required value of R_{11} for each filter is defined as:

$$R_{11\_DIFF} = \frac{1}{42 * \pi * C_4 * f_{C\_DIFF}} \tag{12}$$

$$R_{11\_CM} = \frac{1}{2 * \pi * C_4 * f_{C\_CM}} \tag{13}$$

Substituting C_4 = 10 nF, f_{C_DIFF} = 10 kHz and f_{C_CM} = 200 kHz in the equations above yields the following values for R_1:

$$R_{11_{DIFF}} = 75.8\ \Omega$$

$$R_{11\_CM} = 79.6\ \Omega$$

Given these ideal values, 75 Ω was selected as the nearest 1% standard value which satisfies both requirements. Using the final circuit values of R_{11} = 75 Ω and C_4 = 10 nF, the final cutoff frequencies of the filter are:

$$f_{C\_DIFF} = 10.11\ \text{kHz}$$

$$f_{C\_CM} = 212.21\ \text{kHz}$$

The filter at the output of the PGA281 follows the same topology, however the desired cutoff frequencies are one decade higher (f_{C_DIFF} = 100 kHz and f_{C_CM} = 2 MHz). The same design equations as above can be used to calculate the required resistor and capacitor values, yielding the following result:

$$R_{12} = R_{14} = 75\ \Omega$$

$$C_5 = C_9 = 1\ \text{nF}$$

$$C_7 = 10\ \text{nF}$$

3 Component Selection

3.1 Instrumentation Amplifier Selection

In high-side current sensing applications, the sense resistance is placed between the supply voltage V_{BUS} and the load. In this case the instrumentation amplifier's input common-mode voltage range must include V_{BUS}, which can often be greater than the supply voltage range of most single-supply amplifiers. The PGA281 was chosen for this design since it features a wide input voltage range, made possible by its dedicated high-voltage input stage power supplies.

In order to accurately measure a wide range of currents, multiple instrumentation amplifier gain settings must be used. The PGA281 is ideal for this application as it can be easily programmed to multiple gains, from 0.125 V/V to 176 V/V, by applying a logic-level voltage to its gain set pins.

3.2 Power Management Selection

The PGA281 requires three separate power connections: a high-voltage, split-supply for the input stage and single supplies for the output stage and digital logic. In order to simplify the power connections required on the PCB for this design, a linear regulator was used to generate a +5 V rail from the +15 V rail of the split supply. The TPS7A4101 was chosen for this design to meet the input voltage range and output current requirements of this design while allowing for adjustable output voltage and consuming low quiescent current.

3.3 Passive Component Selection

The passive component with the greatest impact on this design is the shunt resistor R_{SH}. This component must accurately convert load current to a differential voltage, while also potentially dissipating a significant amount of power. Selecting an ideal shunt resistor can be difficult, since resistors with very low tolerances typically can't dissipate significant power, and resistors with high power handling typically aren't available in low tolerances. A compromise was found for this design by selecting a 6.8 Ω resistor with ±1% tolerance in a large 2512 package that can dissipate up to 16 W of power - well within the maximum requirement of 1 W.

The resistors and capacitors in the PGA281 input and output filter network also have an impact on the design as they are located within the signal path. However, the cutoff frequencies of the filters do not need to be extremely accurate, so resistor tolerance of ±1% and capacitor tolerance of ±10% are chosen. Select tighter tolerances if required by your application.

Other passive components in this design may be selected for ±1% or greater tolerance as they will not directly affect the transfer function of the system. Ensure that all capacitors selected have sufficient voltage ratings.

3.4 Protection Component Selection

Several additional circuit components provide protection for the system against ESD (electrostatic discharge), EFT (electrical fast transients), and surge (simulates a lightning strike). This protection is provided by a Schottky diode and two TVS (transient voltage suppressor) diodes.

The BAT54-V-GS08 Schottky diode ensures that no current flows through the split supply when the power terminals are connected in reverse polarity. This diode protects against reverse voltages up to 30V, and the small SOT-23 package takes up a minimal amount of PCB area.

Since the split supplies to the PGA281 can reach up to ±18 V, the TVS diodes should have a breakdown voltage slightly higher than 18V. The diodes must also be bidirectional and should have a very fast response time in order to provide sufficient protection against fast transients. Based on these requirements the SMBJ20CA was chosen to provide up to 600 W of protection.

4 Simulation

The TINA-TI™ schematic shown in Figure 5 includes the circuit values obtained in the design process.

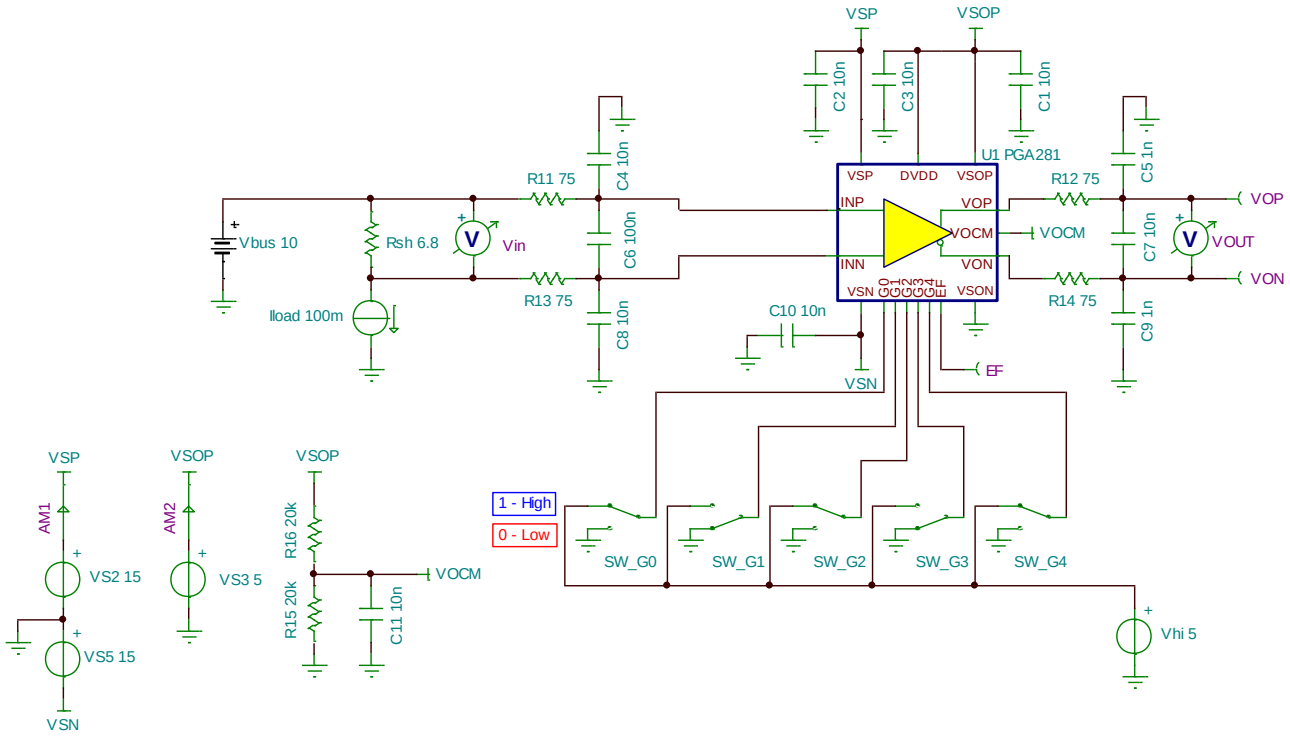

Figure 5: TINA-TI™ Schematic

Note that a series of single pole, double throw (SPDT) switches are used to control the gain of the PGA281. Refer to the gain control table in the PGA281 data sheet for all the possible gain settings. Also note that the power management circuitry in the real system is replaced with discrete power supplies in the simulation schematic.

4.1 Transfer Function

The result of the dc transfer function is shown in Figure 6.

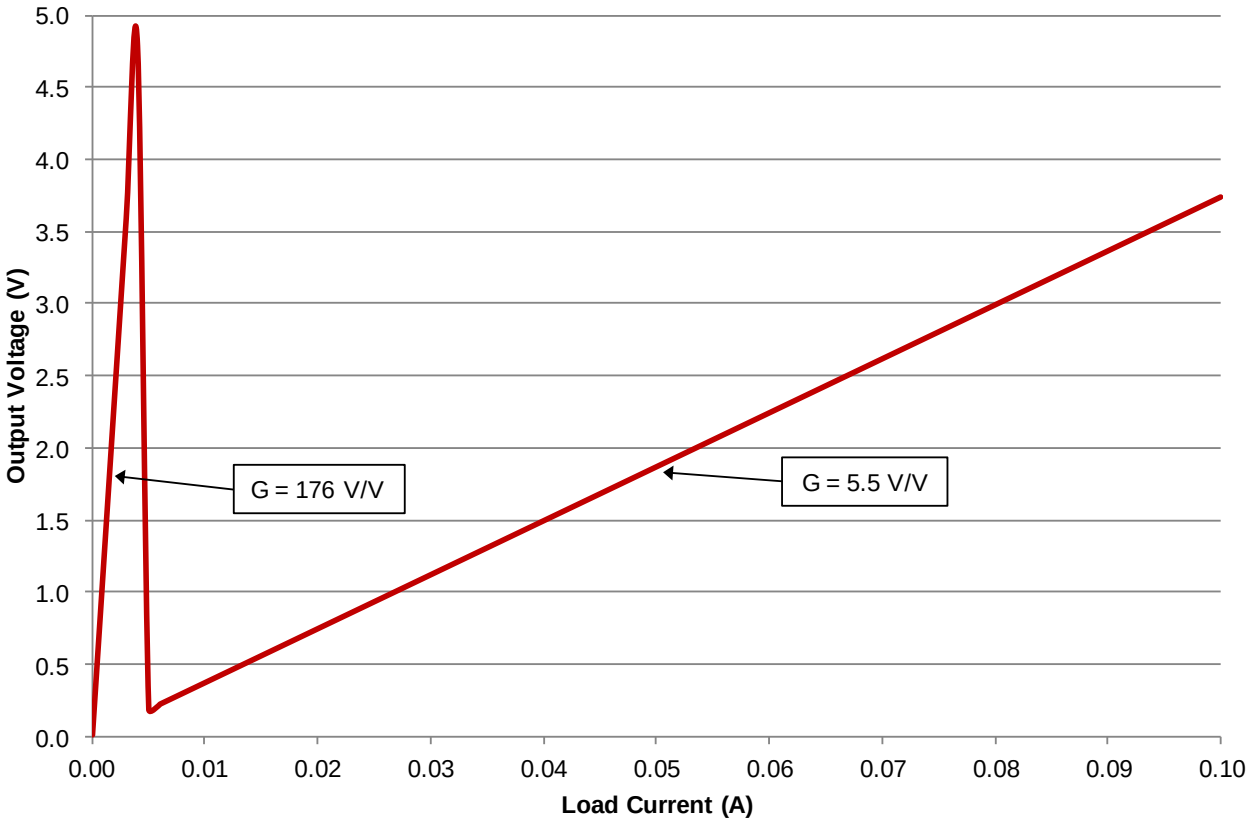

Figure 6: Simulated Transfer Function

4.2 Frequency Response

The circuit shown in Figure 7 was utilized to perform an ac analysis for each gain of the circuit. The simulation results are shown in Figure 8.

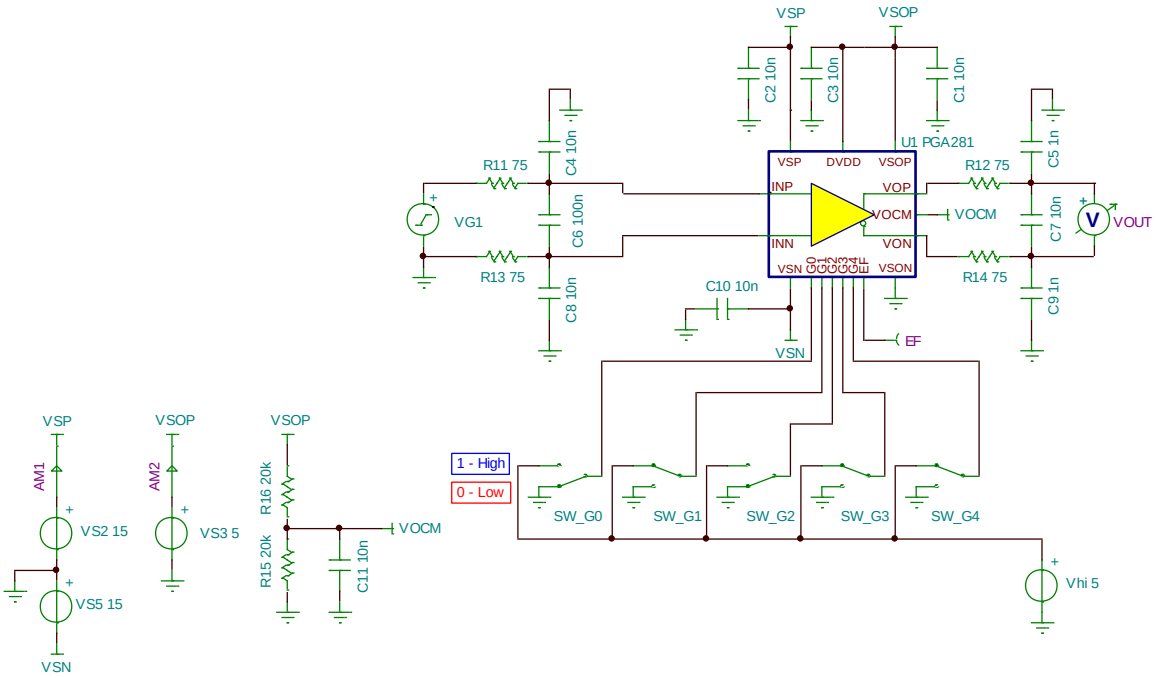

Figure 7: AC Analysis Schematic

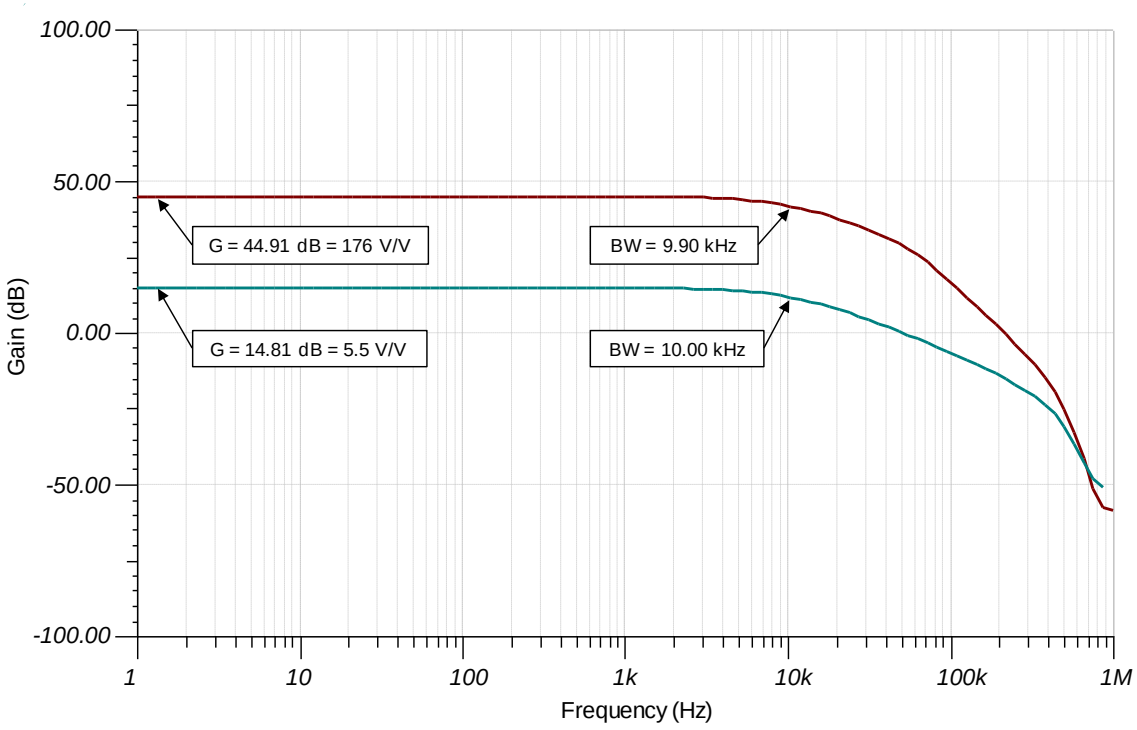

Figure 8: Simulated AC Analysis

The dc gains of the simulation were found to be 44.91 dB and 14.81 dB, which equate to 176.0 V/V and 5.5 V/V, respectively. The -3dB bandwidth of each gain configuration was 9.90 kHz and 10.00 kHz, respectively.

4.3 Full Scale Error

The data from Figure 6 was exported to a spreadsheet in order to calculate the error as a percent of the full-scale range (%FSR_{error}). Equation 14 was used to calculate %FSR_{error}.

$$\%FSR_{error} = \frac{I_{LOAD(simulated)} - I_{LOAD(ideal)}}{I_{LOAD(max)} - I_{LOAD(min)}} * 100 = \frac{\left[\frac{V_{OUT}}{G} * \frac{1}{6.8\Omega}\right] - I_{LOAD(ideal)}}{100mA - 10\mu A} * 100 \quad (14)$$

In order to accurately calculate the error, the gain was switched from 176 V/V to 5.5 V/V once the load current reached 4 mA. Figure 9 shows %FSR_{error} as a function of load current.

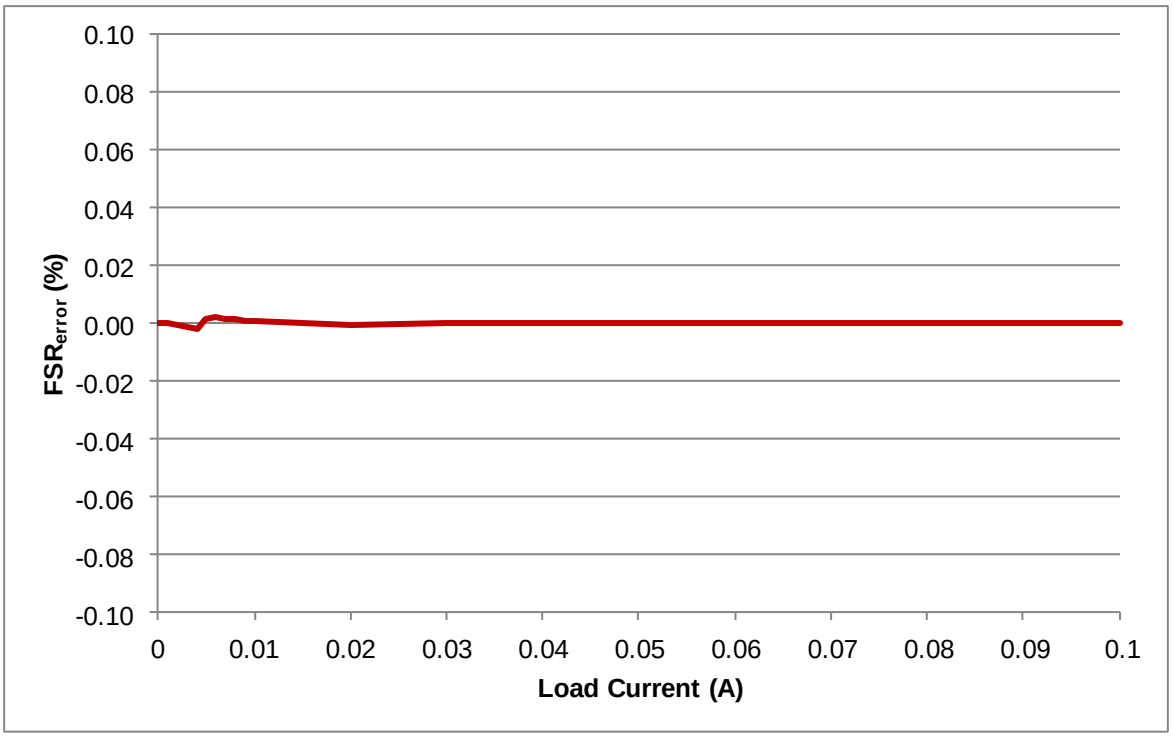

Figure 9: Simulated Full Scale Error

The maximum simulated %FSRerror was found to be 0.002%, which meets our design goal of 0.05%.

4.4 Relative Error

The error relative to the load current (relative error) was also calculated for each load current decade. Equation 15 shows how to calculate relative error.

$$\%\mathrm{Rel}_{\mathrm{error}} = \frac{\mathrm{V}_{\mathrm{OS(max)}}}{\mathrm{V}_{\mathrm{SH}}} * 100 \tag{15}$$

The maximum offset voltage of the PGA281 is calculated using Equation 16.

$$\mathrm{V}_{\mathrm{OS(max)}} = \left(20 + \frac{235}{\mathrm{G}}\right)\ \mu\mathrm{V} \tag{16}$$

The maximum relative error for each decade of load current occurs at the minimum load current for each range (10 µA, 100 µA, 1 mA, 10 mA, and 100 mA). For example, the maximum relative error for a load current of 10 µA is calculated in Equation 17.

$$\%\mathrm{Rel}_{\mathrm{error\_10\mu A}} = \frac{\mathrm{V}_{\mathrm{OS(max)}}}{\mathrm{V}_{\mathrm{SH}}} * 100 = \frac{\left(20 + \frac{235}{176}\right)\mu\mathrm{V}}{6.8\Omega * 10\mu\mathrm{A}} = 31.38\% \tag{17}$$

The maximum relative error for the other load currents can be calculated in a similar manner. Table 2 summarizes the results of the calculations.

Equation 18 calculates the relative error using the simulation data. The output voltage was referred to the input by dividing by the ideal gain (176 V/V or 5.5 V/V).

$$\%\mathrm{Rel}_{\mathrm{error\_sim}} = \frac{\mathrm{V}_{\mathrm{OS(max)}} * \mathrm{G}}{\mathrm{V}_{\mathrm{OUT}}} * 100 \tag{18}$$

4.5 Simulated Results Summary

Table 2 summarizes the simulated performance of the design.

Table 2. Comparison of Design Goals and Simulated Performance

	Goal	Simulated
Error (%FSR$_{error}$)	0.05%	0.002%
Relative Error (I_{LOAD} = 10 µA, G = 176)	35.0%	30.47%
Relative Error (I_{LOAD} = 100 µA, G = 176)	5%	3.13%
Relative Error (I_{LOAD} = 1 mA, G = 176)	1%	0.31%
Relative Error (I_{LOAD} = 10 mA, G = 5.5)	0.1%	0.09%
Relative Error (I_{LOAD} = 100 mA, G = 5.5)	0.01%	0.01%

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The PCB used in this design is a 3” by 3” square. This generous size allows for efficient routing of critical components and the use of larger BNC and banana plug connectors. The high-level approach to this layout was to place the analog signal path components on the top layer, with input connections on the left and output connections on the right, and to place the power management components on the bottom layer.

The load current source is connected at J2 and J4. Large copper areas are used to connect the load current to R_{SH}, ensuring that parasitic trace resistance is minimized. Narrow copper traces running under R_{SH} connect the induced current sense voltage to the PGA281 input filter while minimizing load current leakage. All passive components in the analog signal path are placed and routed very tightly in order to minimize parasitics, and all decoupling capacitors are located very close to their associated power pins. Solid copper areas on the bottom layer provide low-impedance paths for the various power supplies. Solid copper planes on both layers provide an excellent low-impedance path for return currents to ground.

Connections to the split power supply are made at J7, J8, and J9. Connections to the differential output voltage are made at J3 and J5. If a voltage input is used, connections to the input voltage source are made at J1 and J6.

The PCB layout for both layers is shown in Figure 10.

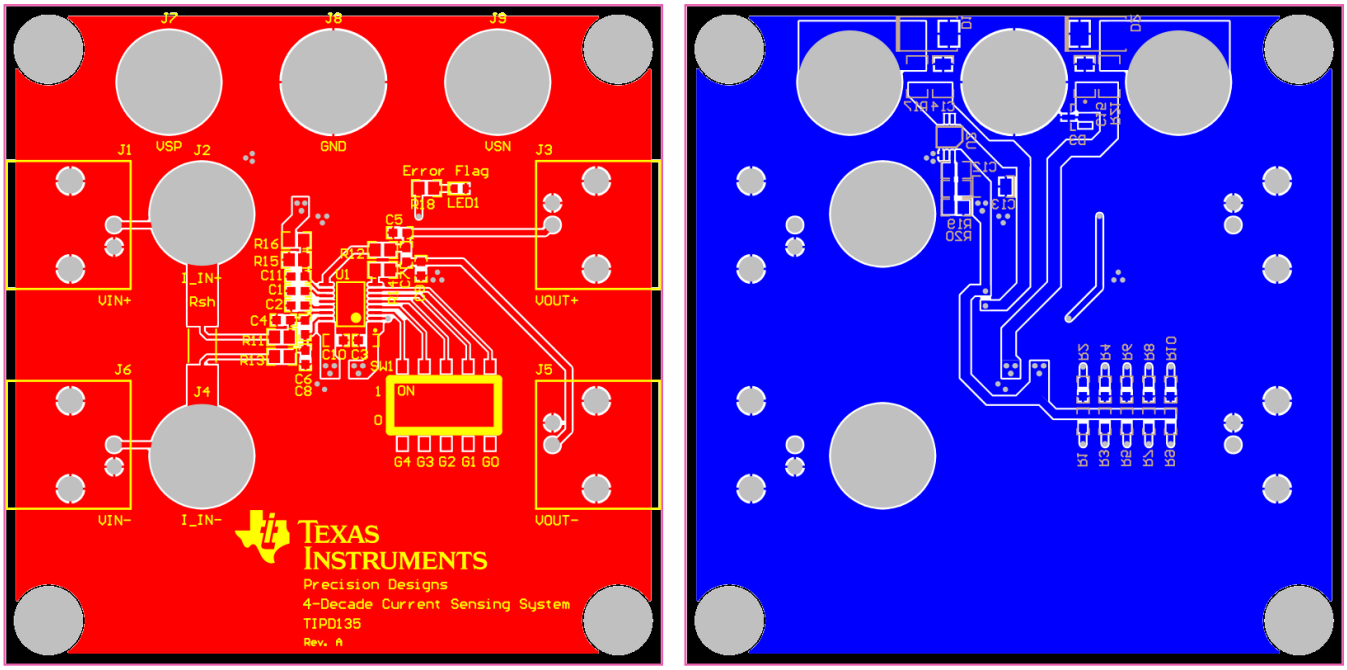

Figure 10: PCB Layout

6 Verification & Measured Performance

6.1 Bench Test Hardware Setup

The circuit defined by this reference design is intended to represent a functional block which, in a real application, would only be part of a greater complete system. Even so, the convenient input and output connectors on the PCB allow the circuit to be easily tested on a bench using standard lab equipment. The test setup used consists of the components listed below. Figure 11 shows the full bench test setup.

1. Precision Current Source/Meter: Provides the load current to the system and sets the load compliance voltage.
2. Digital Multimeter, 6 ½ Digits: Measures the differential output voltage of the system.
3. Triple Output Power Supply: Provides ±15 V power supply rails to the system.
4. Digital Multimeter, 8 ½ Digits: Measures the load current input to the system.

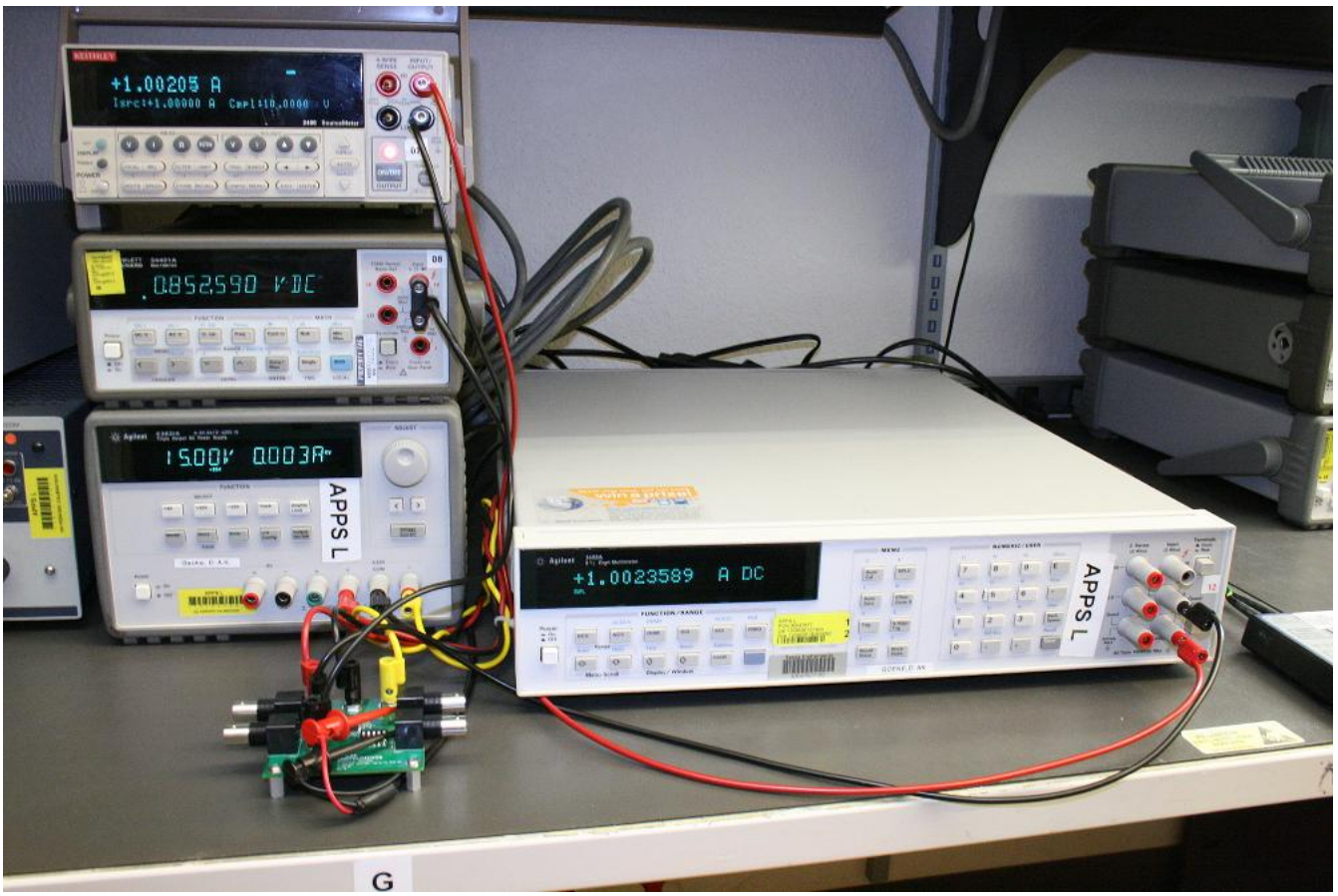

Figure 11: Bench Test Setup

Once the test hardware was connected, a LabVIEW program was used to communicate with the equipment over a GPIB interface and automate the data collection process. This allowed quick and thorough characterization of the system's performance by automatically sweeping the load current and logging the load current and voltage output. This process was repeated for each gain setting of the PGA281.

6.2 Full Scale Error

The logged test data was exported to a spreadsheet in order to calculate the error as a percent of the full-scale range (%FSR_{error}). Equation 14 was used to calculate %FSR_{error}.

In order to accurately calculate the error, the gain was switched from 176 V/V to 5.5 V/V once the load current reached 4 mA. Figure 12 shows %FSR_{error} as a function of load current.

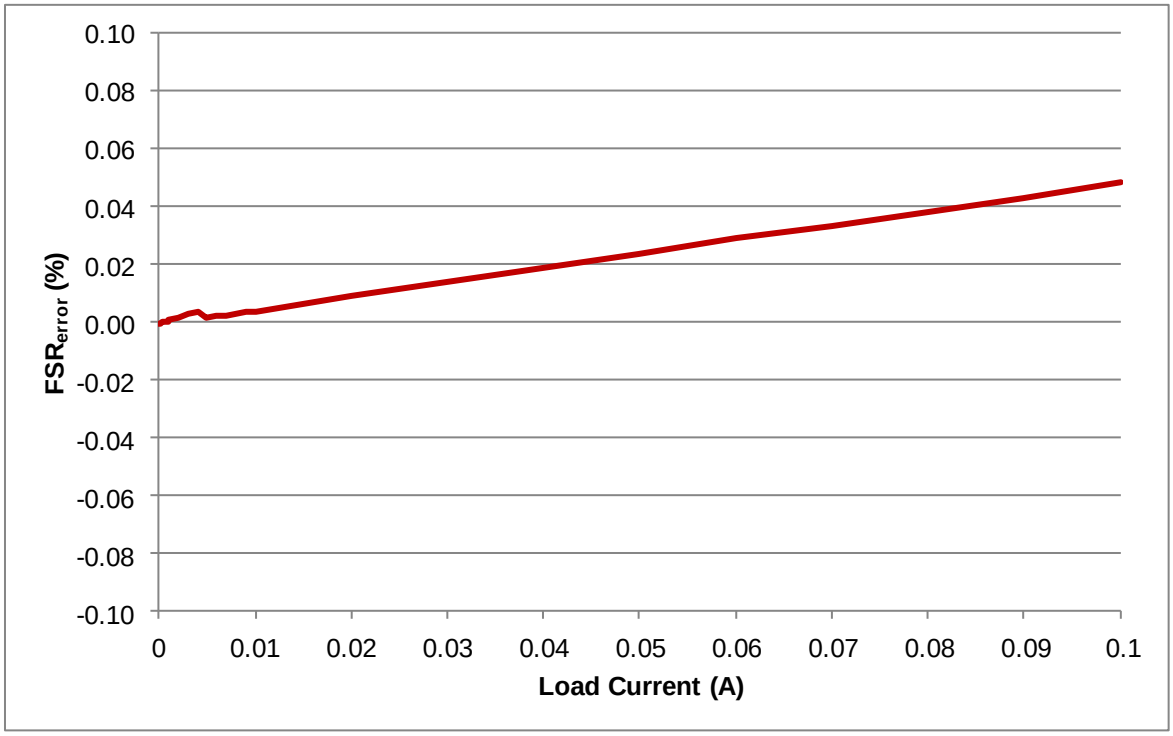

Figure 12: Measured Full Scale Error

The maximum %FSR_{error} was found to be 0.0481%, which meets our design goal of 0.05%.

6.3 Relative Error

The error relative to the load current (relative error) was also calculated for each load current decade. Equation 18 calculates the measured relative error using the logged test data. The output voltage was referred to the input by dividing by the ideal gain (176 V/V or 5.5 V/V).

Table 3 compares the measured and ideal output voltages at the minimum load current of each decade.

Table 3. Measured Output Voltage for Various Load Currents

Load Current	Specified Gain (V/V)	Ideal Output Voltage	Measured Output Voltage
10 µA	176	11.968 mV	11.323 mV
100 µA	176	119.68 mV	119.107 mV
1 mA	176	1.1968 V	1.1974 V
10 mA	5.5	374.00 mV	374.15 mV
100 mA	5.5	3.74 V	3.7419 V

6.4 Measured Results Summary

Table 4 summarizes the measured performance of the design.

Table 4. Comparison of Design Goals and Measured Performance

Load Current	Goal	Measured
Error (%FSR_{error})	0.05%	0.0481%
Relative Error (I_{LOAD} = 10 µA, G = 176)	35.0%	33.16%
Relative Error (I_{LOAD} = 100 µA, G = 176)	5%	3.15%
Relative Error (I_{LOAD} = 1 mA, G = 176)	1%	0.31%
Relative Error (I_{LOAD} = 10 mA, G = 5.5)	0.1%	0.09%
Relative Error (I_{LOAD} = 100 mA, G = 5.5)	0.01%	0.01%

7 Modifications

The components selected for this design were based on the design goals outlined at the beginning of the design process.

The type of resistor selected for R_{SH} was the best overall choice for the 10µA to 100mA current range and the gain settings offered by the PGA281. However, applications which measure lower currents should consider a resistor with lower tolerance in a smaller package. Conversely, applications dealing with higher currents could benefit from specialized current sense resistors in a larger package (such as D2PAK) or a parallel combination of resistors.

Some applications may require or benefit from multiplexing of multiple inputs or more robust diagnostics. The PGA280 is a programmable-gain instrumentation amplifier with the same analog core as the PGA281 but with these additional features included, as well as digital control via SPI™ and seven GPIO pins. Table 5 compares the PGA280 to the PGA281 as a potential PGA for this design.

Table 5. Brief Comparison of PGA281 and PGA280

Instrumentation Amplifier	Error Diagnostics	Number of Differential Inputs	Gain Control	Approx. Price (US$)
PGA281	Error Flag pin, no advanced error reporting	1	Dedicated gain set pins	2.55 / 1ku
PGA280	Error Flag pin, detailed error reporting via registers	2, more possible with GPIO mux control	SPI	2.90 / 1ku

Other programmable-gain instrumentation amplifiers with a wide power supply and analog input range and low offset voltage could also be used in a high-side current sensing application. The PGA204 and PGA205 are suitable choices for this system, with the differences being different gain options, higher quiescent current, lower noise, and higher cost. Table 6 summarizes other potential PGAs for this design as compared to the PGA281.

Table 6. Brief Comparison of Programmable-gain Instrumentation Amplifiers

Instrumentation Amplifier	Gain Options	Offset Voltage (µV, RTI)	Voltage Noise (RTI, 1 kHz)	Quiescent Current	Approx. Price (US$)
PGA281	1/8 to 176	±5 + 45/G	22 nV/√Hz	3 mA	2.55 / 1ku
PGA204	1, 10, 100, 1000	±10 + 20/G	13 nV/√Hz	5.2 mA	8.35 / 1ku
PGA205	1, 2, 4, 8	±10 + 20/G	13 nV/√Hz	5.2 mA	7.25 / 1ku

8 About the Author

Ian Williams (ian@ti.com) is an applications engineer in the Precision Analog – Linear team at Texas Instruments where he supports industrial products and applications. Ian graduated from the University of Texas, Dallas, where he earned a Bachelor of Science in Electrical Engineering with a concentration in Microelectronics.

9 Acknowledgements & References

9.1 Acknowledgements

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9.2 References

1. *P. Semig. (2013, June 18). 10uA-10mA, Single-Supply, Low-Side, Current Sensing Solution. Available: http://www.ti.com/lit/ug/slau504/slau504.pdf*

2. *P. Semig and C. Wells. (2012, February 8). A Current Sensing Tutorial Parts I-IV. Available: http://www.eetimes.com/design/industrial-control*

3. *PGA281EVM User's Guide (SBOU130). Available: http://www.ti.com/lit/ug/sbou130/sbou130.pdf*

Appendix A.

A.1 Electrical Schematic

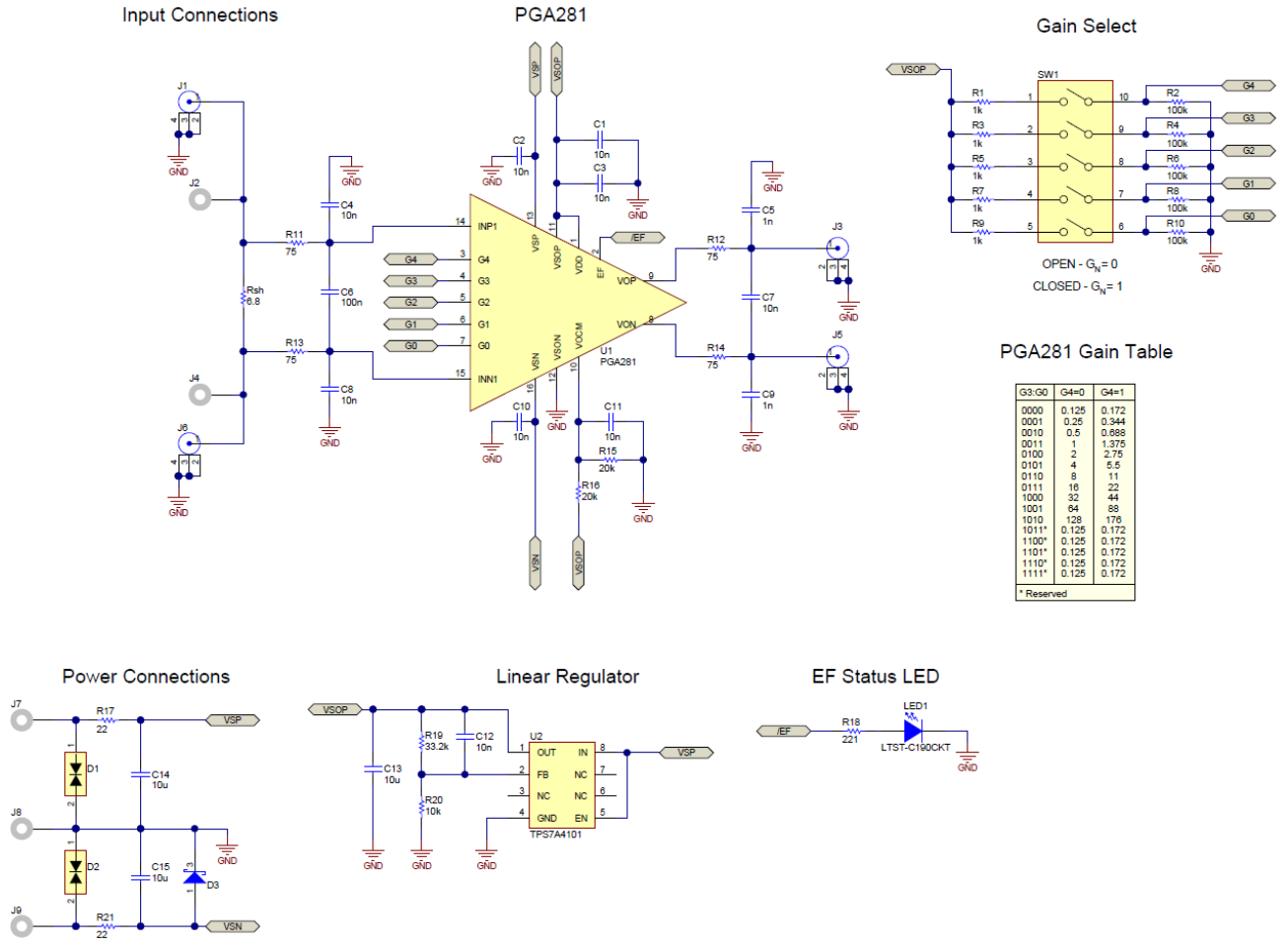

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item #	Quantity	Value	Designator	Description	Manufacturer	Part Number	Supplier Part Number
1	9	10nF	C1, C2, C3, C4, C7, C8, C10, C11, C12	CAP CER 10000PF 50V 10% X7R 0603	Samsung Electro-Mechanics America	CL10B103KB8NNNC	1276-1009-1-ND
2	2	1nF	C5, C9	CAP CER 1000PF 50V 10% X7R 0603	Samsung Electro-Mechanics America	CL10B102KB8NNNC	1276-1018-1-ND
3	1	100nF	C6	CAP CER 0.1UF 50V 10% X7R 0603	Samsung Electro-Mechanics America	CL10B104KB8NNNC	1276-1000-1-ND
4	3	10µF	C13, C14, C15	CAP CER 10UF 25V 10% X7R 1206	Samsung Electro-Mechanics America	CL31B106KAHNNNE	1276-1804-1-ND
5	2	TVS	D1, D2	TVS 20 VOLT 600 WATT BI-DIR SMB	Littelfuse Inc	SMBJ20CA	SMBJ20CALFCT-ND
6	1	SCHOTTKY	D3	DIODE SCHOTTKY 30V 200MA SOT23	Vishay Semiconductor Diodes Division	BAT54-V-GS08	BAT54-V-GS08CT-ND
7	1	LED	LED1	LED RED CLEAR 0603 SMD	Lite-On Inc	LTST-C190CKT	160-1181-1-ND
8	5	1k	R1, R3, R5, R7, R9	RES 1K OHM 1/8W 5% 0805	Stackpole Electronics Inc	RMCF0805JT1K00	RMCF0805JT1K00CT-ND
9	5	100k	R2, R4, R6, R8, R10	RES 100K OHM 1/8W 5% 0805	Stackpole Electronics Inc	RMCF0805JT100K	RMCF0805JT100KCT-ND
10	4	75	R11, R12, R13, R14	RES 75 OHM 1/8W 1% 0805	Stackpole Electronics Inc	RMCF0805FT75R0	RMCF0805FT75R0CT-ND
11	2	20k	R15, R16	RES 20K OHM 1/8W 1% 0805	Stackpole Electronics Inc	RMCF0805FT20K0	RMCF0805FT20K0CT-ND
12	2	22	R17, R21	RES 22.0 OHM .5W 1% 1206 SMD	Vishay Dale	CRCW120622R0FKEAHP	541-22.0UCT-ND
13	1	221	R18	RES 221 OHM 1/8W 1% 0805	Stackpole Electronics Inc	RMCF0805FT221R	RMCF0805FT221RCT-ND
14	1	33.2k	R19	RES 33.2K OHM 1/8W 1% 0805	Stackpole Electronics Inc	RMCF0805FT33K2	RMCF0805FT33K2CT-ND
15	1	10k	R20	RES 10K OHM 1/8W 1% 0805	Stackpole Electronics Inc	RMCF0805FT10K0	RMCF0805FT10K0CT-ND
16	1	6.8	RSH	RES 6.8 OHM 16W 1% 2512 SMD	Susumu	CPA2512Q6R80FS-T10	CPA25Q6.8CT-ND
17	1	SWITCH	SW1	SWITCH DIP 5POS TOP ACT GULLEAD	Omron Electronics Inc-EMC Div	A6S-5104-H	SW1013-ND
18	1	PGA281	U1	PGA281 TSSOP-16 PGA	Texas Instruments	PGA281AIPW	PGA281AIPW
19	1	TPS7A4101	U2	TPS7A4101 ADJUSTABLE LDO	Texas Instruments	TPS7A4101DGN	TPS7A4101DGN
20	4	BNC	J1, J6, J3, J5	CONN BNC JACK R/A 50 OHM PCB	TE Connectivity	1-1634612-0	A97555-ND
21	5	BANANA	J2, J4, J7, J8, J9	CONN JACK BANANA UNINS PANEL MOUNT	Emerson Network Power Connectivity	108-0740-001	J147-ND
22	4	SCREW	Screws	SCREW MACHINE PHILLIPS 4-40X3/8	B&F Fastener Supply	PMS 440 0038 PH	H781-ND
23	4	STANDOFF	Standoffs	STANDOFF HEX 4-40THR ALUM .500"L	Keystone Electronics	2203	2203K-ND

Figure A-2: Bill of Materials

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