

450W Four-Phase Interleave Buck Converter Reference Design



Description

This reference design describes a four-phase interleaved Buck converter. Using LM5137F-Q1 as a controller enables the converter with three options for functional safety: Capable, ASIL B, and ASIL D. The converter operates over a wide range of 6.5V to 36V to deliver 4.5V regular outputs with better than 1% set-point accuracy at load currents up to 42A per output. The converter applies dynamic phase shedding to get 81% efficiency at 15mA per output and also can achieve $\pm 8.3\%$ output voltage vibration when output current jumps from 21A to 86A in 1 μ s.

Resources

PMP41158	Design Folder
LM5137-Q1	Product Folder
LM5137F-Q1	Product Folder



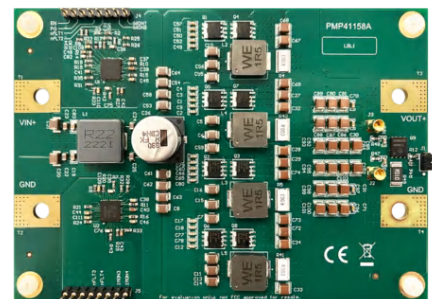
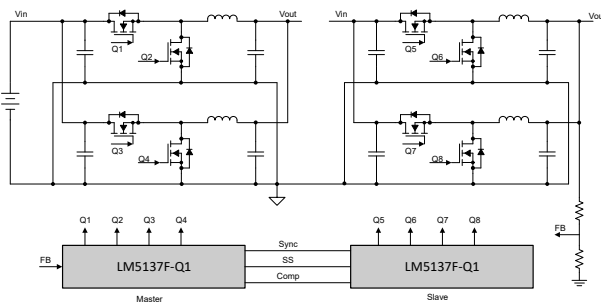
Ask our TI E2E™ support experts

Features

- Four-phase interleave buck converter using LM5137F-Q1 with functional safety
- Dynamic phase shedding (DPS)
- 81.05% efficiency at 13.5V_{in}, 4.5V_{out}, 0.015A load
- 95.5% efficiency at 13.5V_{in}, 4.5V_{out}, 21A load
- 94.1% efficiency at 13.5V_{in}, 4.5V_{out}, 40A load
- $\pm 8.3\%$ output voltage vibration when output current jumps from 21A to 86A in 1 μ s
- 20mV_{pp} ripple at 13.5V_{in}, 4.5V_{out}, 42A load

Applications

- [Advanced driver assistance systems \(ADAS\)](#)
- [ADAS domain controller](#)
- [Infotainment & cluster](#)



1 System Description

The cabin integration architecture supports both automotive infotainment and intelligent driving features, providing greater integration and flexibility in modular design compared to the traditional cabin discrete architecture. Supports self-driving at L2+ level and above, while meeting both cabin and intelligent drive module capacity requirements. To achieve these features, a high-end processor with more than 400W of power is required. The power rail that powers the processor presents a design challenge, delivering high power while meeting requirements for efficiency, ripple, transient loads, thermal performance and functional safety.

The reference design describes a four-phase interleaved buck converter which can be used in ADAS and IVI application. The converter operates over a wide range of 6.5V to 36V to deliver 4.5V regular outputs with better than 1% set-point accuracy at load currents up to 42A per output. Applying dynamic phase shedding, the converter shows good performance at light load. The converter can achieve as high as 81% efficiency at 15mA per output. With peak current control mode, the converter only has $\pm 8.3\%$ output voltage vibration when output current jumps from 21A to 86A in 1 μ s.

The LM5137F-Q1 is stackable, two LM5137F-Q1 in the same package are daisy chained together into a four-phase interleaved voltage regulator, with the first controller as the primary controller and the second as the secondary controller. In the configuration, the COMP1 and COMP2 of the two controllers are connected together, all outputs are connected together to maintain the switching frequency. Four-phase interleaving effectively reduces ripple current compared to single-phase controllers, thus reducing ripple voltage of output capacitors.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage	/	6.5	13.5	36	Volt
Input current	/		14	26	Amper
OUTPUT CONDITIONS					
Output voltage	/		4.5		Volt
Output current	/	0		42	Amper
Output voltage ripple	Full range V_{in} , full range load			40	mV
Output power	/			200	Watt
SYSTEM CHARACTERISTICS					
Efficiency (η)	$V_{in} = 13.5V$, $V_{out} = 4.5V$, $I_{out} = 15mA$		81.1		%
	$V_{in} = 13.5V$, $V_{out} = 4.5V$, $I_{out} = 21A$		95.5		%
	$V_{in} = 13.5V$, $V_{out} = 4.5V$, $I_{out} = 40A$		94.1		%
Operating ambient	Open frame	-25	25	85	°C
Switching frequency			400		kHz
Load transient	21A-42A-56A-83A-21A, 1 μ s slew time ¹ 12 \times 47 μ F/1210 output caps	-5.5		+5.5	%
	21A-83A-56A-42A-21A, 1 μ s slew time ² 12 \times 47 μ F/1210 output caps	-8.3		+8.3	%
Board form factor	FR4 material, 6-layer, 2-oz copper	126 \times 87 \times 35			mm

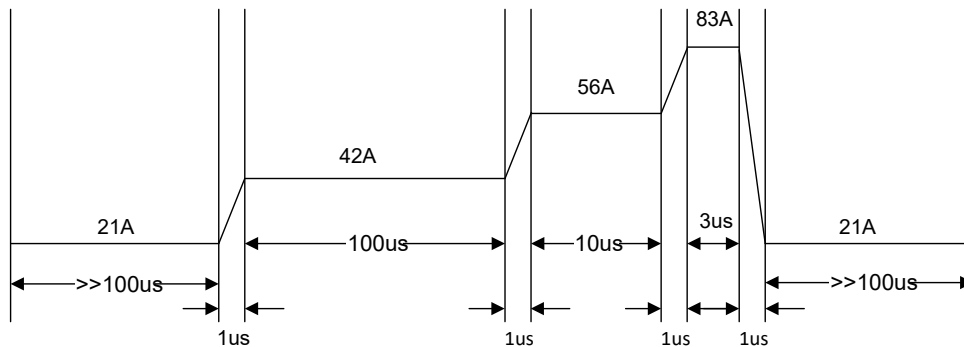


Figure 1-1. Load Transient 21A, 42A, 56A, 83A, 21A Waveforms

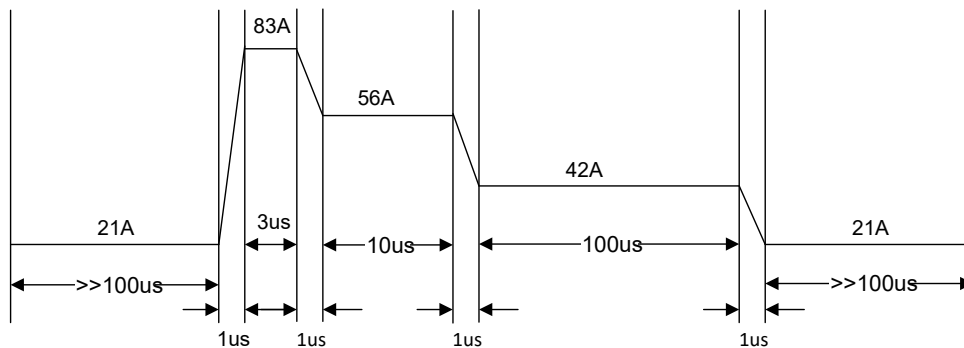


Figure 1-2. Load Transient 21A, 83A, 56A, 42A, 21A Waveforms

2 System Overview

This section shows the block diagram of the four phase interleaved buck converter.

2.1 Block Diagram

Figure 2-1 shows the high-level block diagram of this reference design. The main part of this design is the controller LM5137F-Q1.

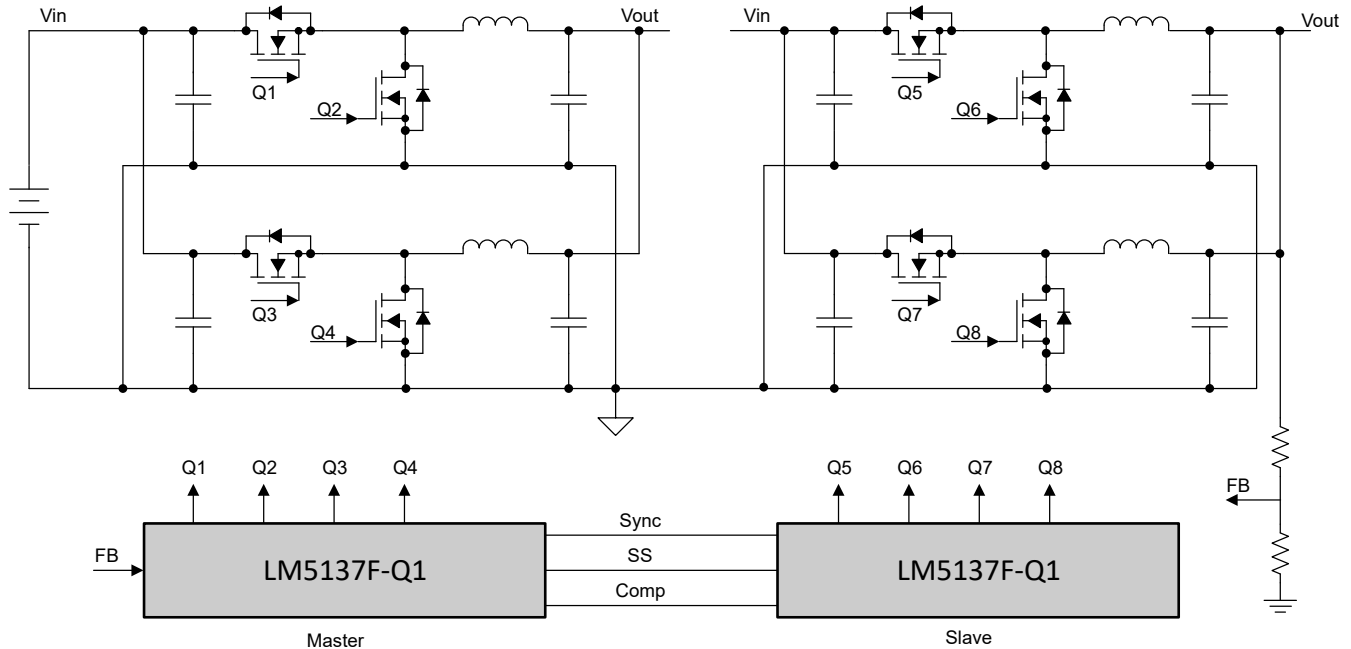


Figure 2-1. Block Diagram

2.2 Design Considerations

To design a four-phase interleaved buck converter, you can leverage LM5137F-Q1 data sheet to calculate the value of components. The only consideration left is how to test the load transient.

2.2.1 Load Transient Test Circuit

In this reference design, an auxiliary circuit was added to assist load transient test, as figure [Figure 2-2](#) shows. The main part of auxiliary consists of a MOSFET and a 10mΩ SHUNT. An arbitrary waveform generator (like AFG3252) can be used to output a drive signal to MOSFET by connecting to J1 head pin.

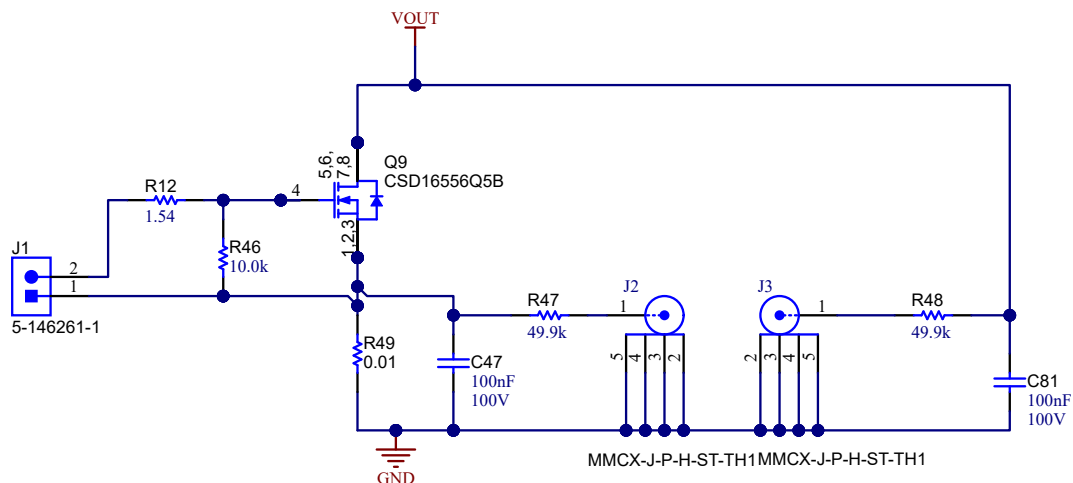


Figure 2-2. Auxiliary Circuit

Notice, this circuit can be in parallel with 21A eLoad connected to the output as default. First, determine what voltage level through the gate corresponds to the different load levels (42A, 56A, 83A) and then use this info in writing the piecewise function in the ArbExpress software, as [Figure 2-3](#) shows.

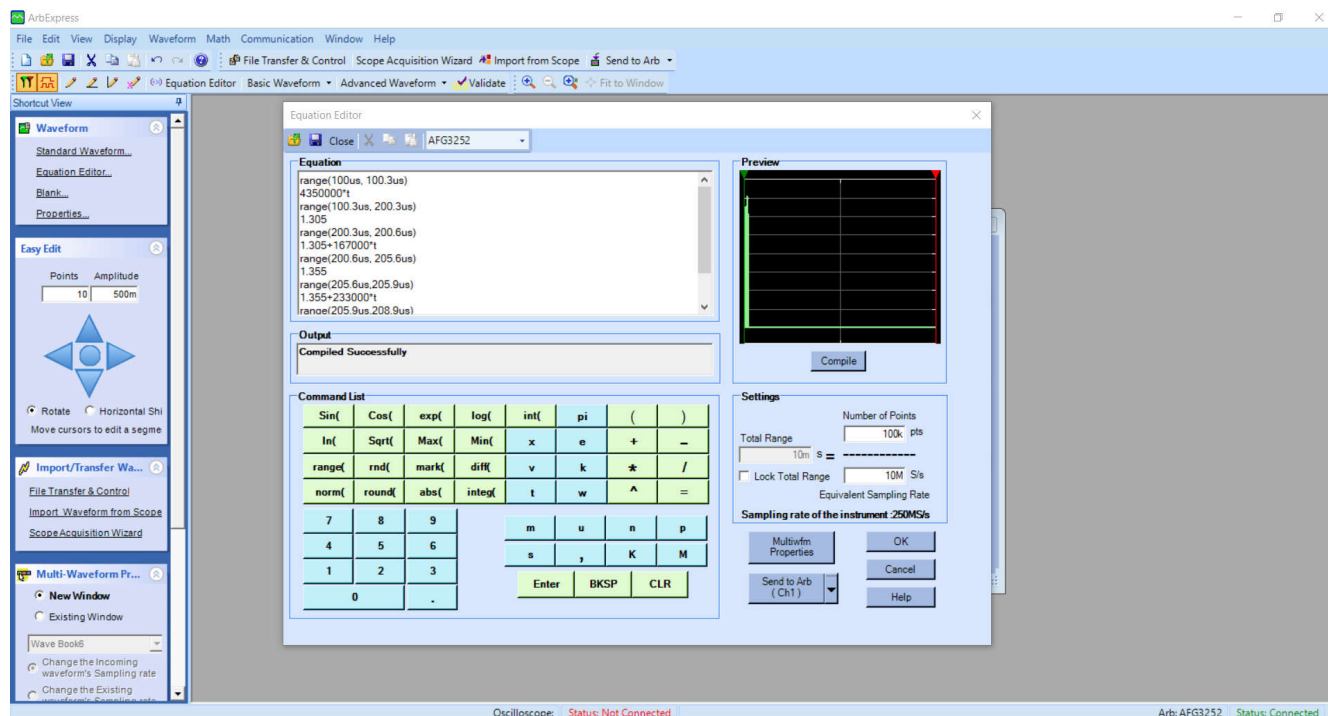


Figure 2-3. ArbExpress Equation Editor

After entering the piecewise into the equation editor in the software and set 100k points and 10M sampling rate, use the “Send to Arb” button when having laptop connected to the signal generator, to where the waveform looks like the ArbExpress internal simulation for the most part, as [Figure 2-4](#) shows:

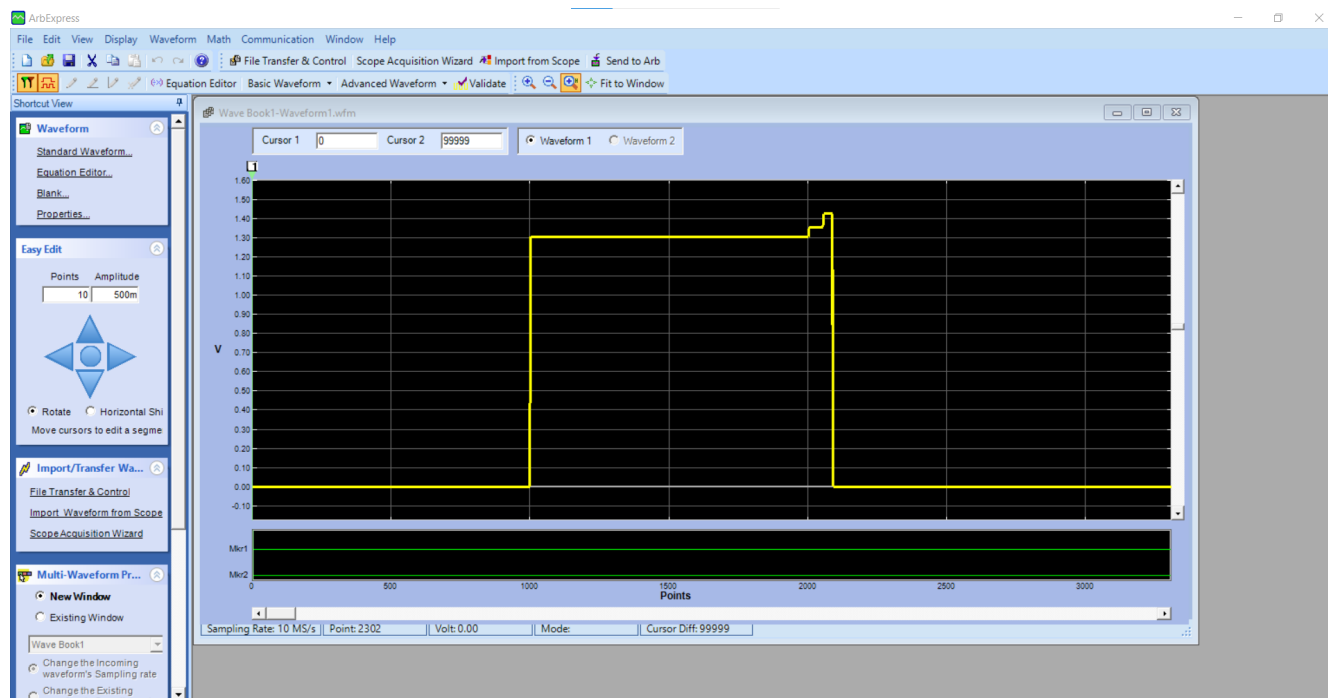


Figure 2-4. ArbExpress Internal Simulation Waveform

Using the Amphenol 523-095-850-206-024 on the Isense connector J2 or a differential probe across the sense resistor R49, one can test the current load. Using the Amphenol 523-095-850-206-024 on the Vsense connector J3, one can test the output voltage.

Through this method, one can get the load transient test results as [Section 3.3.6](#) shows.

2.3 Highlighted Products

2.3.1 LM5137F-Q1 Overview

The LM5137F-Q1 is an 80V dual-channel buck controller offered from a family with three options for functional safety: Capable, ASIL B, or ASIL D. The device uses an interleaved, stackable, peak current mode architecture for easy loop compensation, fast transient response, excellent load and line regulation, and accurate current sharing with paralleled phases for high output current. A high-side switch minimum on-time of 15ns facilitates large step-down ratios, enabling the direct conversion from 12V, 24V, or 48V automotive inputs to low-voltage rails for reduced system design cost and complexity. The LM5137F-Q1 continues operating during input voltage dips as low as 4V, at 100% duty cycle if needed.

Features:

- AEC-Q100 qualified for automotive applications
- Device temperature grade 1: -40°C to 125°C ambient operating temperature
- Functional Safety-Compliant targeted
- Developed for functional safety applications
- Three orderable part numbers for Capable, ASIL B, and ASIL D options
- Documentation available to aid ISO 26262 system design up to ASIL D are available upon production release
- Systematic capability up to ASIL D targeted
- Hardware integrity up to ASIL D targeted
- Versatile dual synchronous buck DC/DC controller
- 1% accurate, fixed 3.3V, 5V, 12V, or adjustable outputs from 0.8V to 60V
- Current monitor output for each channel
- Charge-pump gate drivers for 100% duty cycle
- No-load sleep current of 12.7µA (typical)
- Internal hiccup-mode overcurrent protection
- Two interleaved synchronous buck channels
- Dual channel or single-output multiphase
- Stackable up to four phases
- Designed for ultra-low EMI requirements
- Dual Random Spread Spectrum (DRSS)
- Switching frequency from 100kHz to 2.5MHz
- VQFN-36 package with wettable flanks

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The following hardware is required for this reference design:

- PMP41158 board

The following test equipment is needed to power and evaluate the DUT:

- DC Source: Chroma 62012P-100-50
- DC Load: Chroma 6312A+63103A
- Multimeter: Fluke 287C
- Oscilloscope: Tektronix DPO3054
- Electrical thermography: Fluke TiS55
- Vector Network Analyzer: OMICRON Bode100
- Digital power meter: WT210

3.2 Test Setup

- 1.2kW DC power supply: 13.5V, 25A
- 600W e load: 21A
- Power meter
- Oscilloscope with passive probes for voltage and current

3.3 Test Results

3.3.1 Efficiency Data

Efficiency data is shown in [Table 3-1](#). Test condition is room temperature, no air flow.

Table 3-1. Efficiency at 8V_{in}

V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
7.9565	0.010052	4.481	0.01547	86.67%
7.9179	0.01965	4.481	0.03043	87.64%
7.879	0.029348	4.481	0.04542	88.02%
7.8404	0.0391	4.481	0.06043	88.33%
7.7633	0.0588	4.481	0.0904	88.74%
7.6102	0.099	4.48	0.1503	89.37%
7.5003	0.13206	4.479	0.1997	90.30%
7.9864	0.1847	4.49	0.3001	91.35%
7.9834	0.3036	4.489	0.4997	92.55%
7.9775	0.4833	4.489	0.801	93.26%
7.9745	0.6	4.489	0.998	93.63%
7.9688	0.9	4.489	1.4981	93.77%
7.9618	1.1908	4.489	1.9913	94.28%
7.9475	1.7955	4.489	2.9963	94.26%
7.9335	2.3682	4.489	3.9853	95.22%
7.9192	2.9464	4.489	4.9894	95.99%
7.9039	3.5341	4.489	5.9925	96.30%
7.8893	4.117	4.489	6.9816	96.49%
7.8746	4.7122	4.489	7.9856	96.61%
7.8607	5.3092	4.489	8.9906	96.70%

Table 3-1. Efficiency at 8V_{in} (continued)

V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
7.8464	5.8986	4.489	9.9769	96.77%
7.8168	7.103	4.489	11.989	96.93%
7.7848	8.315	4.489	13.981	96.96%
7.755	9.541	4.489	15.978	96.94%
7.7244	10.79	4.489	17.983	96.86%
7.6942	12.049	4.489	19.981	96.75%
7.663	13.323	4.489	21.974	96.62%
7.6303	14.634	4.489	23.983	96.42%
7.5632	17.275	4.489	27.973	96.11%
7.8245	17.942	4.489	29.977	95.85%
7.8	20.482	4.489	33.96	95.42%
7.7872	21.78	4.489	35.973	95.21%
7.7743	23.079	4.489	37.962	94.98%
7.7615	24.395	4.489	39.955	94.73%

Table 3-2. Efficiency at 13.5V_{in}

V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
13.481	0.006335	4.481	0.01545	81.07%
13.466	0.012255	4.481	0.03042	82.60%
13.451	0.01819	4.481	0.04542	83.18%
13.436	0.024105	4.48	0.06042	83.58%
13.406	0.035857	4.48	0.0904	84.25%
13.347	0.05886	4.479	0.1501	85.58%
13.297	0.07837	4.486	0.1997	85.97%
13.427	0.112	4.482	0.3002	89.47%
13.48	0.182	4.481	0.4997	91.27%
13.478	0.29	4.481	0.801	91.83%
13.476	0.359	4.487	0.99	91.82%
13.471	0.542	4.489	1.4981	92.11%
13.467	0.7181	4.489	1.9931	92.52%
13.458	1.075	4.489	2.9953	92.94%
13.45	1.4251	4.489	3.9844	93.31%
13.442	1.7731	4.489	4.9903	93.99%
13.433	2.1507	4.489	5.9934	93.13%
13.425	2.4989	4.489	6.9816	93.42%
13.415	2.8796	4.489	7.9856	92.80%
13.406	3.2636	4.489	8.9916	92.26%
13.398	3.6189	4.489	9.9788	92.39%
13.379	4.3526	4.489	11.989	92.42%
13.362	5.067	4.489	13.983	92.71%

Table 3-2. Efficiency at 13.5V_{in} (continued)

V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
13.346	5.7146	4.489	15.978	94.04%
13.331	6.384	4.489	17.987	94.88%
13.315	7.054	4.489	19.981	95.50%
13.297	7.77	4.489	21.974	95.47%
13.278	8.497	4.489	23.983	95.42%
13.243	9.952	4.489	27.973	95.28%
13.226	10.695	4.489	29.981	95.15%
13.189	12.185	4.489	33.965	94.87%
13.17	12.947	4.489	35.973	94.70%
13.151	13.709	4.489	37.966	94.53%
13.131	14.509	4.489	39.955	94.14%

Table 3-3. Efficiency at 18V_{in}

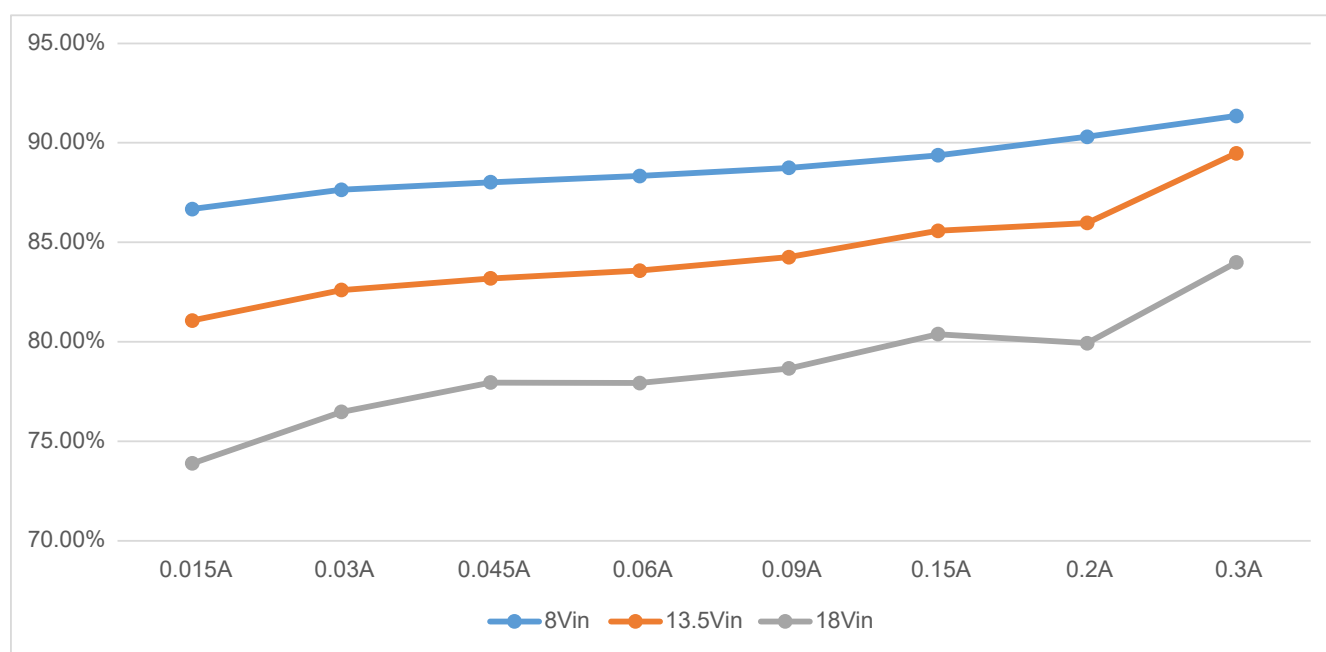
V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
17.996	0.0052	4.481	0.01543	73.89%
17.993	0.0099	4.481	0.0304	76.47%
17.99	0.0145	4.481	0.04538	77.95%
17.988	0.0193	4.48	0.06039	77.93%
17.982	0.0286	4.48	0.0903	78.66%
17.972	0.0466	4.479	0.1503	80.38%
17.962	0.0624	4.486	0.1997	79.93%
17.946	0.0893	4.485	0.3001	83.99%
17.914	0.1434	4.485	0.4996	87.23%
17.982	0.2224	4.491	0.7922	88.96%
17.98	0.275	4.491	0.9891	89.84%
17.977	0.4131	4.491	1.4981	90.60%
17.974	0.54769	4.491	1.9913	90.84%
17.968	0.8164	4.491	2.9963	91.73%
17.961	1.0901	4.491	3.9834	91.37%
17.955	1.3567	4.489	4.9903	91.96%
17.948	1.6283	4.489	5.9944	92.08%
17.941	1.8904	4.488	6.9823	92.40%
17.934	2.1932	4.488	7.9866	91.13%
17.927	2.472	4.488	8.9925	91.07%
17.921	2.7419	4.488	9.9816	91.17%
17.907	3.289	4.488	11.99	91.37%
17.893	3.8283	4.488	13.983	91.61%
17.882	4.331	4.488	15.978	92.59%
17.869	4.832	4.488	17.985	93.48%
17.854	5.31	4.488	19.98	94.58%

Table 3-3. Efficiency at 18V_{in} (continued)

V _{IIN}	I _{IN}	V _{OUT}	I _{OUT}	Efficiency
17.841	5.8332	4.487	21.974	94.74%
17.828	6.3804	4.487	23.984	94.61%
17.801	7.461	4.487	27.973	94.50%
17.788	8.012	4.487	29.981	94.39%
17.762	9.113	4.487	33.963	94.15%
17.748	9.676	4.487	35.973	93.99%
17.734	10.238	4.487	37.966	93.83%
17.72	10.805	4.487	39.955	93.64%

3.3.2 Efficiency Graphs

Efficiency is shown in [Figure 3-1](#) and [Figure 3-2](#). Test condition is room temperature, no air flow.


Figure 3-1. Efficiency at Load Less Than 300mA

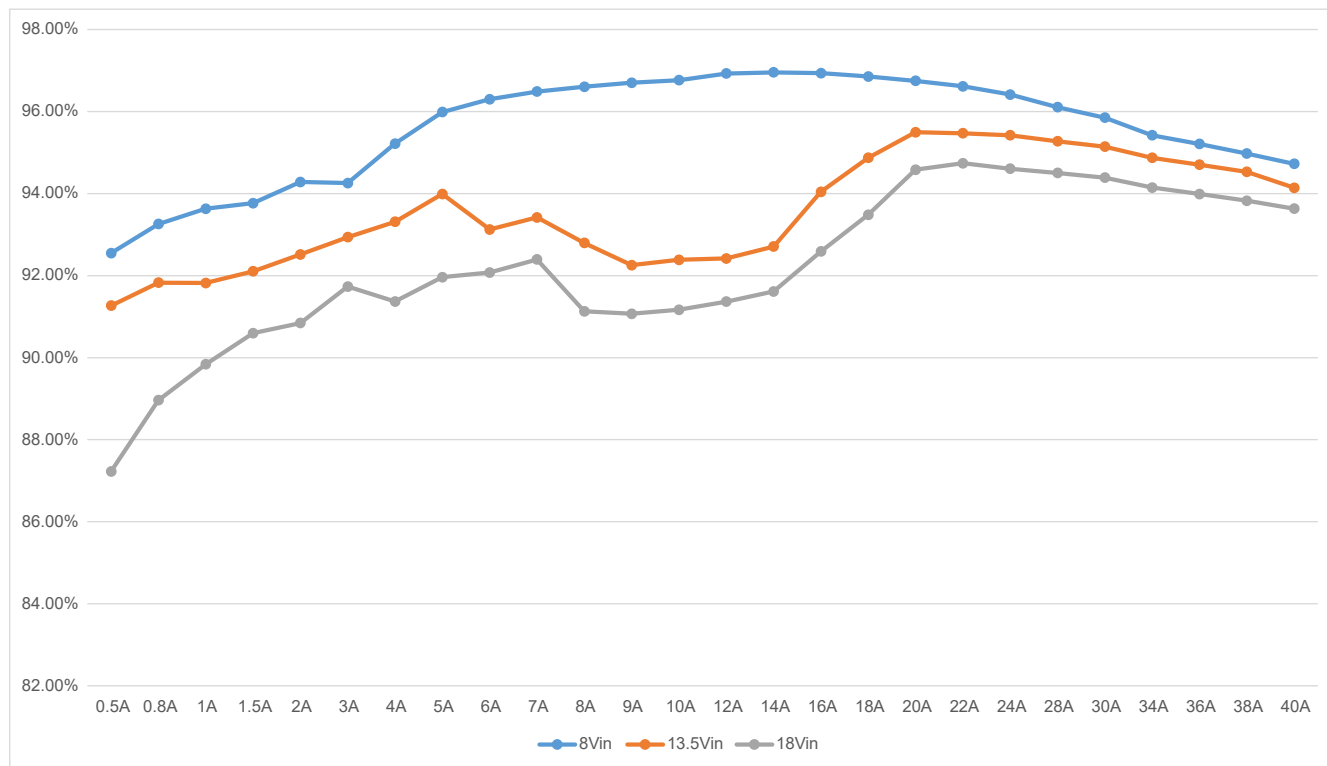


Figure 3-2. Efficiency at Load Between 300mA and 40A

3.3.3 Output Voltage Ripple

Output voltage ripple is shown in Figure 3-3 through Figure 3-11. Test condition is room temperature, no air flow.

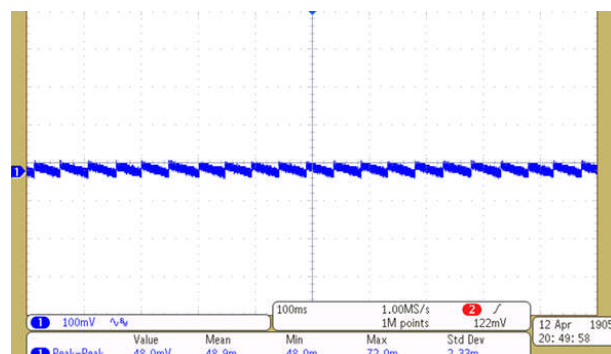


Figure 3-3. Output Voltage Ripple at 8V_{in}, 4.5V_{out}, 0A

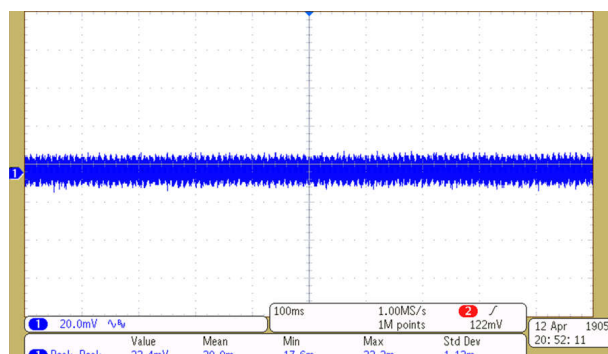


Figure 3-4. Output Voltage Ripple at 8V_{in}, 4.5V_{out}, 21A

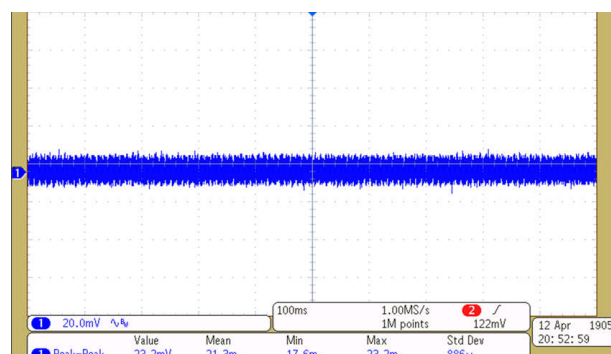


Figure 3-5. Output Voltage Ripple at 8V_{in}, 4.5V_{out}, 42A

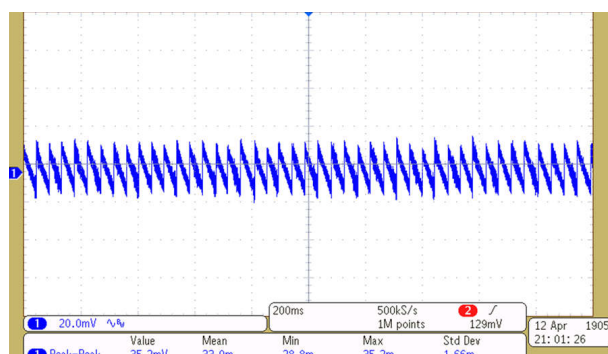


Figure 3-6. Output Voltage Ripple at 13.5V_{in}, 4.5V_{out}, 0A

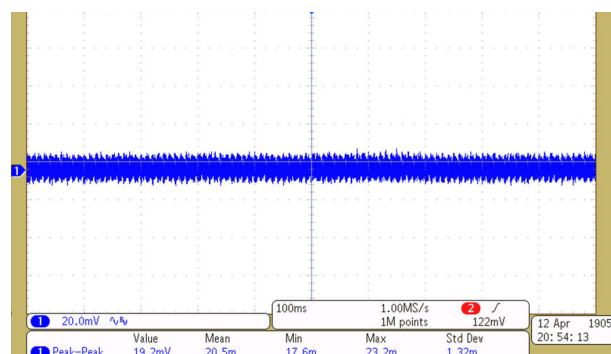


Figure 3-7. Output Voltage Ripple at 13.5V_{in}, 4.5V_{out}, 21A

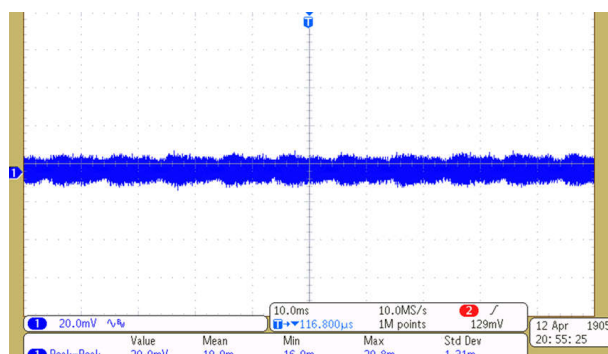


Figure 3-8. Output Voltage Ripple at 13.5V_{in}, 4.5V_{out}, 42A

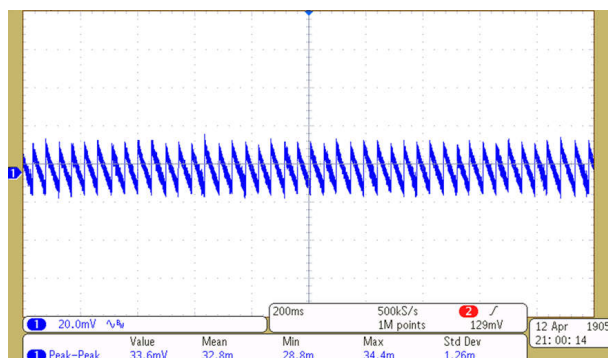


Figure 3-9. Output Voltage Ripple at 18V_{in}, 4.5V_{out}, 0A

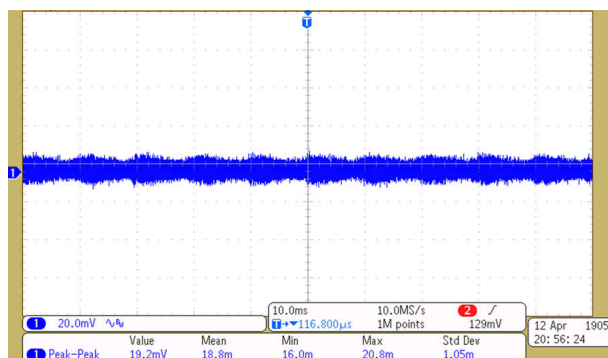


Figure 3-10. Output Voltage Ripple at 18V_{in}, 4.5V_{out}, 21A

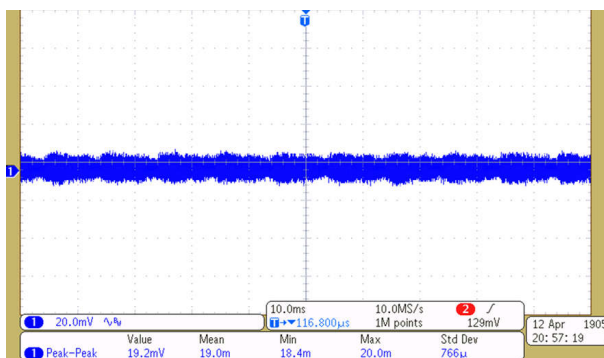


Figure 3-11. Output Voltage Ripple at 18V_{in}, 4.5V_{out}, 42A

3.3.4 Thermal Images

Thermal image is shown in [Figure 3-12](#) and [Figure 3-13](#). Test condition is room temperature, no air flow.

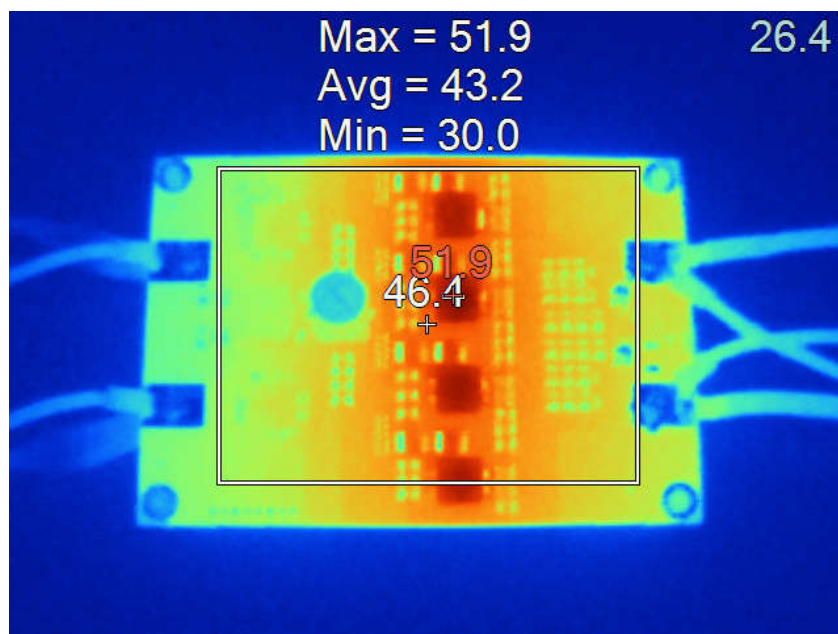


Figure 3-12. Thermal Image at 13.5V_{in}, 4.5V_{out}, 21A load

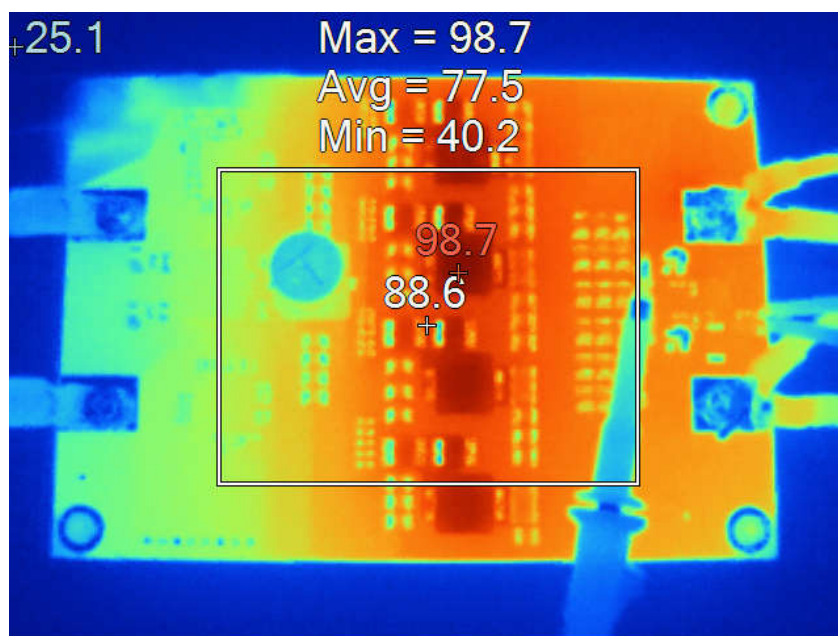


Figure 3-13. Thermal Image at 13.5V_{in}, 4.5V_{out}, 42A load

3.3.5 Bode Plots

Bode plot is shown in Figure 3-14 through Figure 3-16. Test condition is room temperature, no air flow.

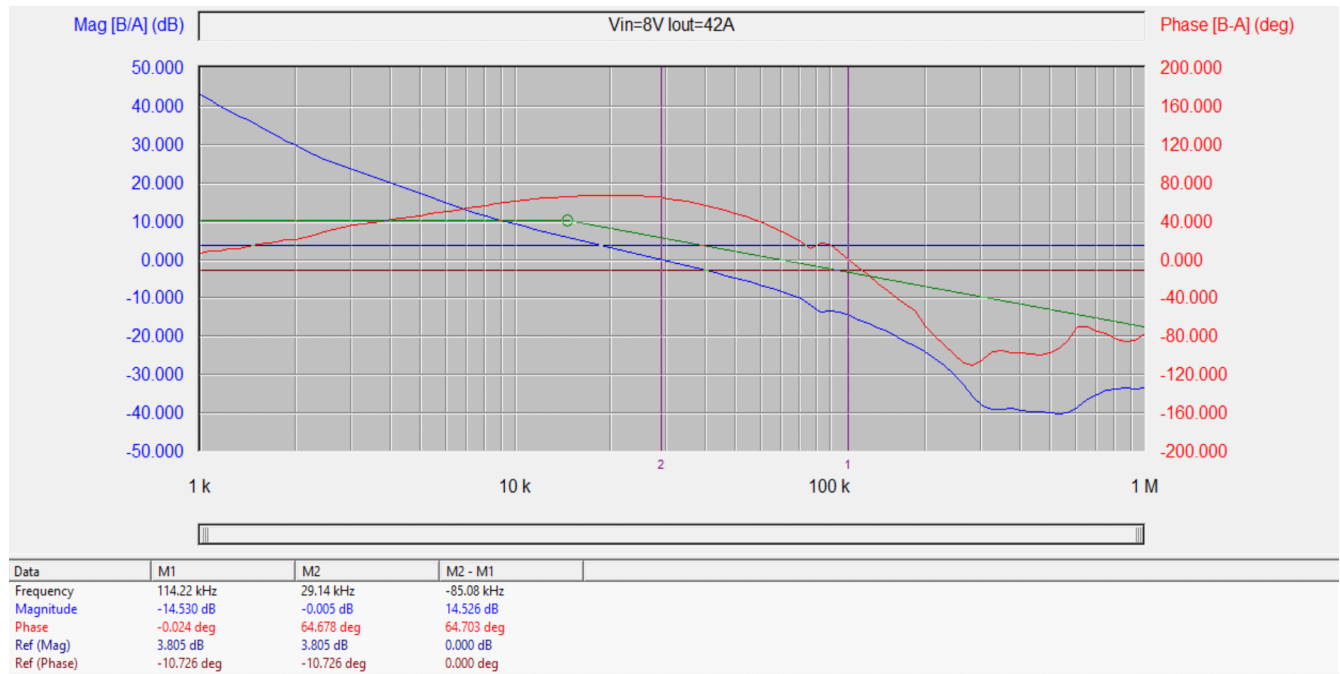


Figure 3-14. Bode Plot at 8V_{in}, 4.5V_{out}, 42A Load

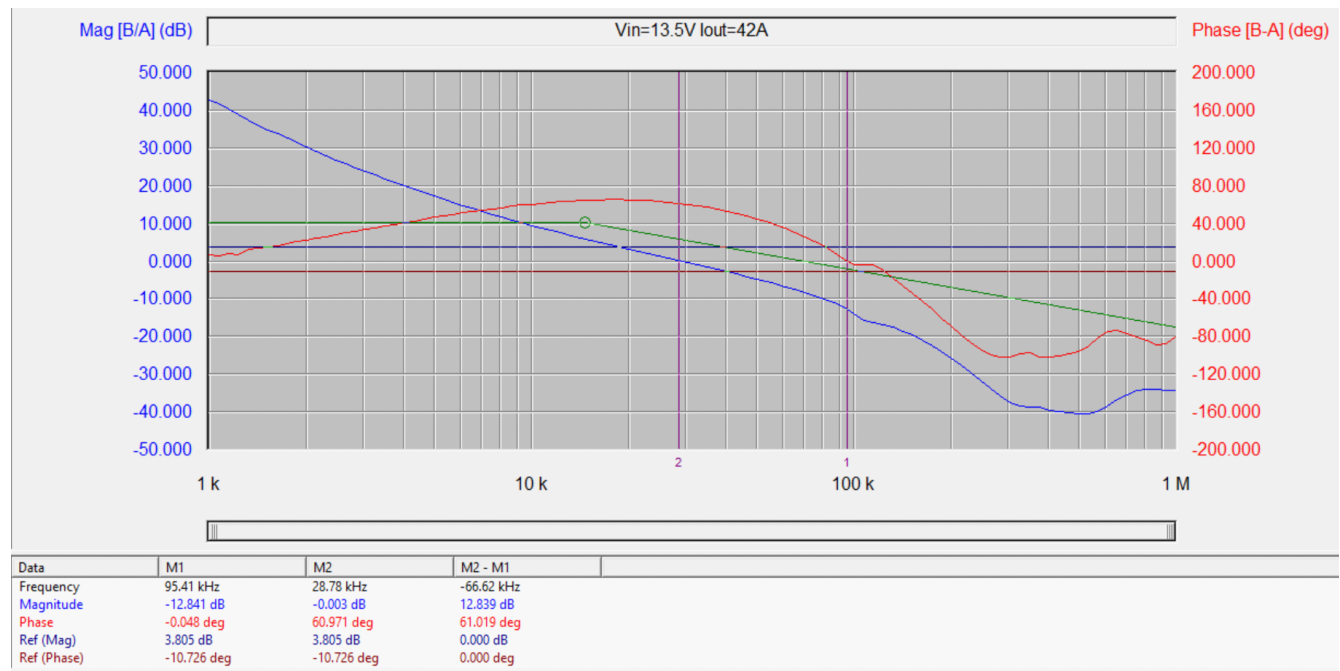


Figure 3-15. Bode Plot at 13.5V_{in}, 4.5V_{out}, 42A Load

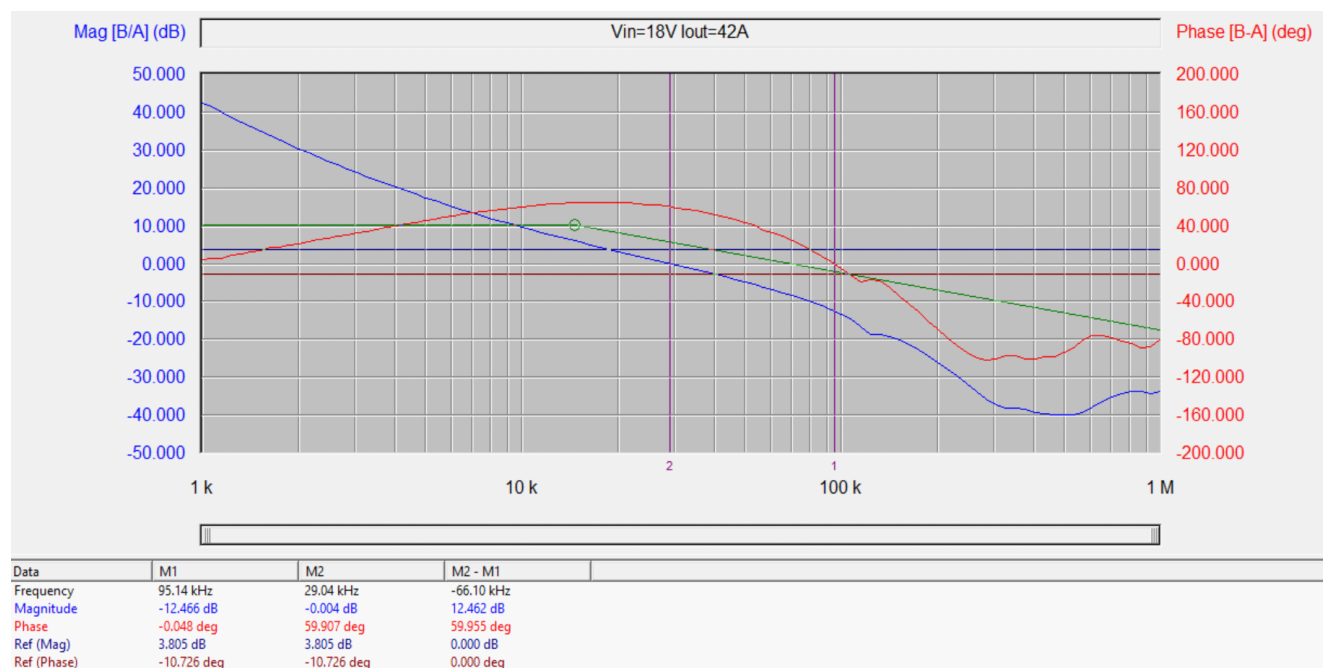


Figure 3-16. Bode Plot at 18V_{in}, 4.5V_{out}, 42A Load

3.3.6 Load Transients

Load transient response is shown in Figure 3-17 and Figure 3-18. Test condition is room temperature, no air flow. Output capacitors are 3pcs ceramic caps for each phase, making a total of $12 \times 47\mu\text{F}/1210$ caps.

Load transient 1 is 21A-42A-56A-83A-21A, $1\mu\text{s}$ slew time. V_{out} is within $\pm 5.3\%$. Load transient 1 is 21A-83A-56A-42A-21A, $1\mu\text{s}$ slew time. V_{out} is within $\pm 8.5\%$.

CH1: output voltage

CH2: voltage signal of SHUNT R49

M: math curve based on $\text{CH2}/0.01+21$

In which:

0.01 is SHUNT R49's resistance 0.01Ω .

21 is 21A electric load.

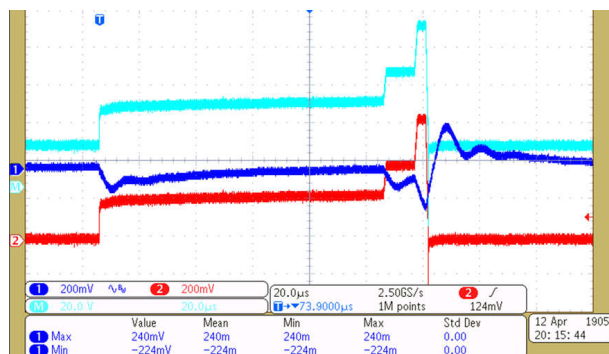


Figure 3-17. Load Transient 1

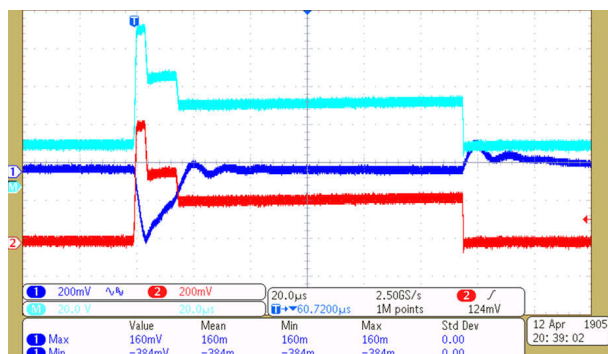


Figure 3-18. Load Transient 2

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files [here](#).

4.1.2 BOM

To download the bill of materials (BOM), see the design files [here](#).

4.1.3 Altium Project

To download the Altium Project, see the design files [here](#).

4.1.4 Gerber Files

To download the Gerber files, see the design files [here](#).

4.1.5 Assembly Drawings

To download the Assembly Drawings, see the design files [here](#).

4.2 Documentation Support

For related documentation, see the following:

- Texas Instruments, [LM5137-Q1 Automotive, 4V to 80V, 100% Duty Cycle Capable, Dual-Channel Synchronous Buck Controller](#) data sheet.
- Texas Instruments, [LM25137-Q1 Evaluation Module](#) EVM user's guide.
- Texas Instruments, [Achieving functional safety compliance in automotive offbattery buck preregulator designs](#) technical article.
- Texas Instruments, [Powering next-generation ADAS processors with TI Functional Safety-Compliant buck regulators](#) technical article.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

4.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

5 About the Author

Daniel Gao works as a system engineer for the Texas Instruments Power Supply Design Services team, where he focuses on developing OBC and DC/DC converters. He received the M.S. degree from Central South University in 2010.

Yuxin Xie is working as field application engineer focusing on analog knowledge and products at Texas Instruments and currently responsible for this reference design. Before joining TI she received her master's degree in integrated circuits at the East China Normal University.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated