Test Report: PMP41134

3.6kW Bidirectional SR-DAB Converter Reference Design for Energy Storage System

Description

The series resonant dual-active-bridge (SR-DAB) DCDC converter offers advantages like soft-switching, lower circulating current and high efficiency. The design is beneficial where power density, cost, galvanic isolation, wide gain range, and high efficiency are needed for portable power stations and energy storage applications. This design illustrates control of the power topology using a C2000™ MCU in closed current-loop mode, which supports the bidirectional operation to support battery charging and discharging applications.

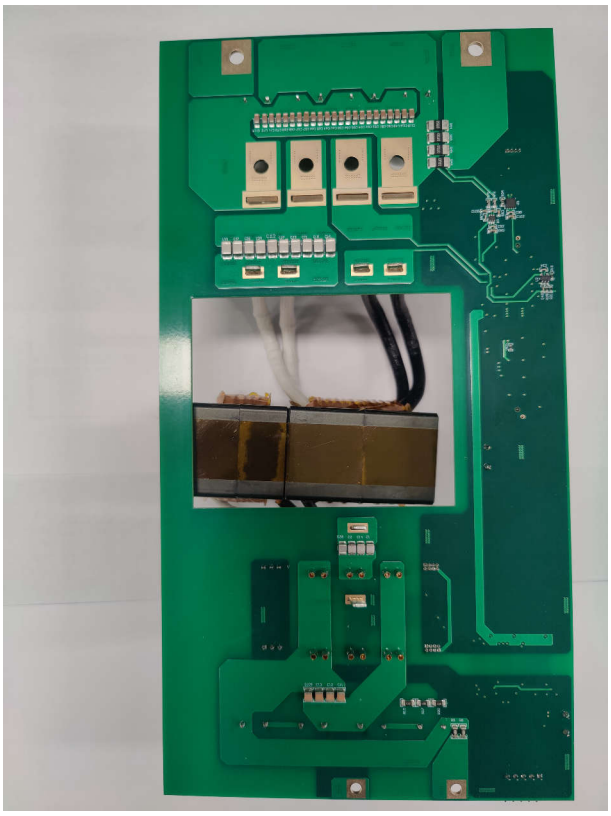
Features

- Vprim: 360–550VDC; Vsec: 40–60VDC
- Maximum power: 3.6kW
- Achieve 98.5% peak efficiency
- Soft switching with Zero Voltage Switching (ZVS) on the primary and secondary side which enables higher efficiency
- TMS320F28P55x controller for implementation of digital control

Applications

- Energy storage systems
- Portable power station
- Power conversion system (PCS)

Top Overview



Bottom Overview

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	360VDC to 550VDC (400VDC typical)
Output Voltage Range	40VDC to 60VDC (48VDC typical)
Output Current	75A maximum
Output Power	3.6kW maximum

1.2 Required Equipment

- DC Voltage Source
- Electronic load
- Multimeters
- Oscilloscope
- Power meter

1.3 Dimensions

The dimensions of the board are 250mm ×130mm × 55mm.

1.4 Test Setup

Figure 1-1 shows the board overview for hardware settings.

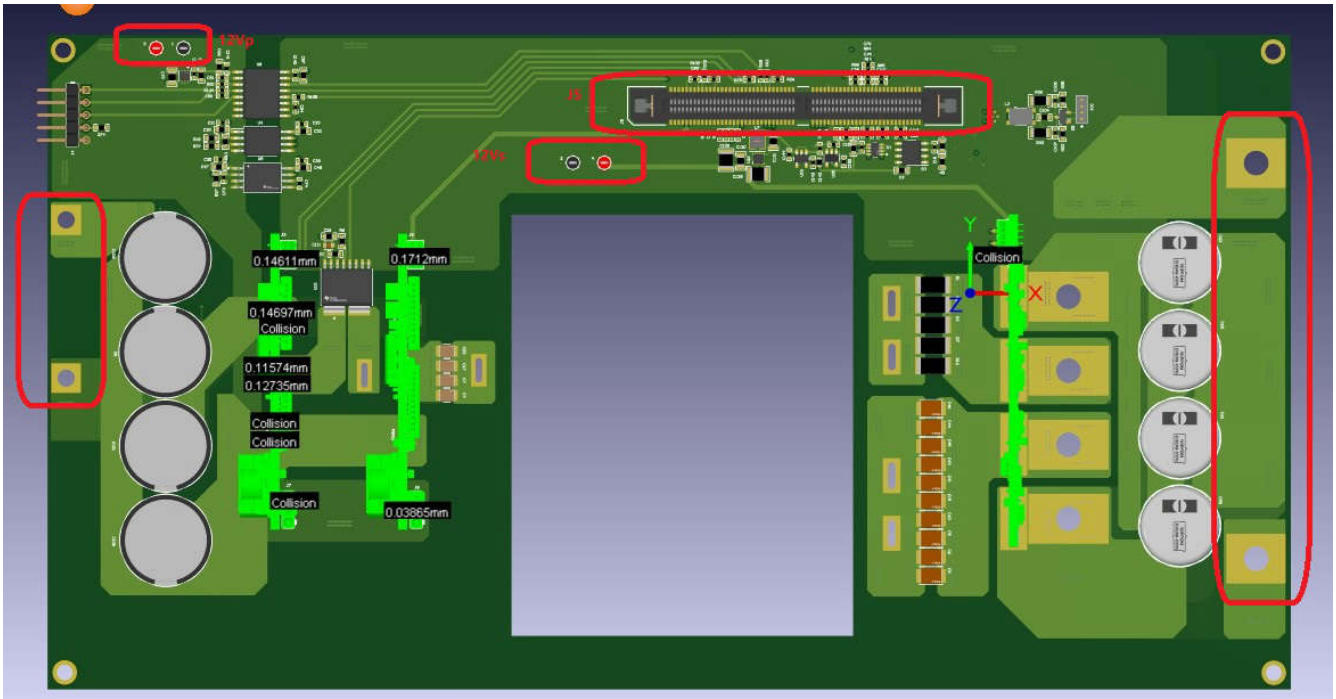


Figure 1-1. Board Overview

- Make sure no power source is connected to the board.
- Insert the 28P55 controlCARD in the J5 slot.
- Connect a power source for the primary and secondary auxiliary power (+12V, 1A) at the test points.
- To connect JTAG, use a USB cable from the controlCARD and connect the cable to a host computer.
- Connect the DC power supply to the input ports and the electrical load to the output ports, the electrical load sets to CV mode with limited current based on the output power.

1.5 Software Setup

1. To get started, click Cyclone_Project_V01.c item in Project Explorer.
2. In the srcdab_settings.h file, change the LAB number to select different LAB to run different function as shown in Figure 1-2.
3. Right click on the project name and click Rebuild Project. Then, click Run → Debug to launch a debugging session.
4. The project then loads on the device and the CCS debug view becomes active. The code halts at the start of the main routine.
5. Add the variables in the watch-expressions window. Click on the *Continuous Refresh* button on the watch window to enable continuous update of values from the controller. The watch window appears as shown in Figure 1-3.
6. *SRCDAB_Direction* defines the power flow, *1* represents the charging mode and *0* represents the discharging mode, set the *SRCDAB_Direction* in CCS watch window before power up.
7. Lab1 is open loop check, set phase shift angle *Phase1_Alpha*, *Phase2_Beta*, *Phase2_Fai* and frequency *SRCDAB_pwmPeriodRef_pu* based on power level and input and output range, then set *SRCDAB_start* to *1*, the PWM sends out
8. Lab2 is close current loop check, the output current can be controlled by setting *SRCDAB_iSecRef_pu*.

Getting Started | Debug | srcdab_settings.h | Cyclone_Project_V00.c

```
151// 8 -> Closed loop voltage with resistive load
152//
153
154// SRCDAB LAB - New Labs
155// Power Flow Prim -> Sec
156// 1 -> Open loop check for PWM and ADC drivers with protection,
157// 2 -> Closed current loop check with resistive load
158
159// Power Flow Sec -> Prim
160// 3 -> Open loop check for PWM and ADC drivers with protection,
161// 4 -> Closed current loop check with resistive load
162//
163
164#define SRCDAB_LAB 1
165
166#if SRCDAB_LAB == 1
167//#define SRCDAB_CONTROL_RUNNING_ON 1
168#define SRCDAB_POWER_FLOW SRCDAB_POWER_FLOW_PRIM_SEC
169#define SRCDAB_INCR_BUILD SRCDAB_OPEN_LOOP_BUILD
170#define SRCDAB_TEST_SETUP SRCDAB_TEST_SETUP_RES_LOAD
171#define SRCDAB_PROTECTION SRCDAB_PROTECTION_DISABLED
172#define SRCDAB_SFRA_TYPE  1
173#define SRCDAB_SFRA_AMPLITUDE (float32_t)SRCDAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
174#endif
```

Figure 1-2. Test Lab Selection File

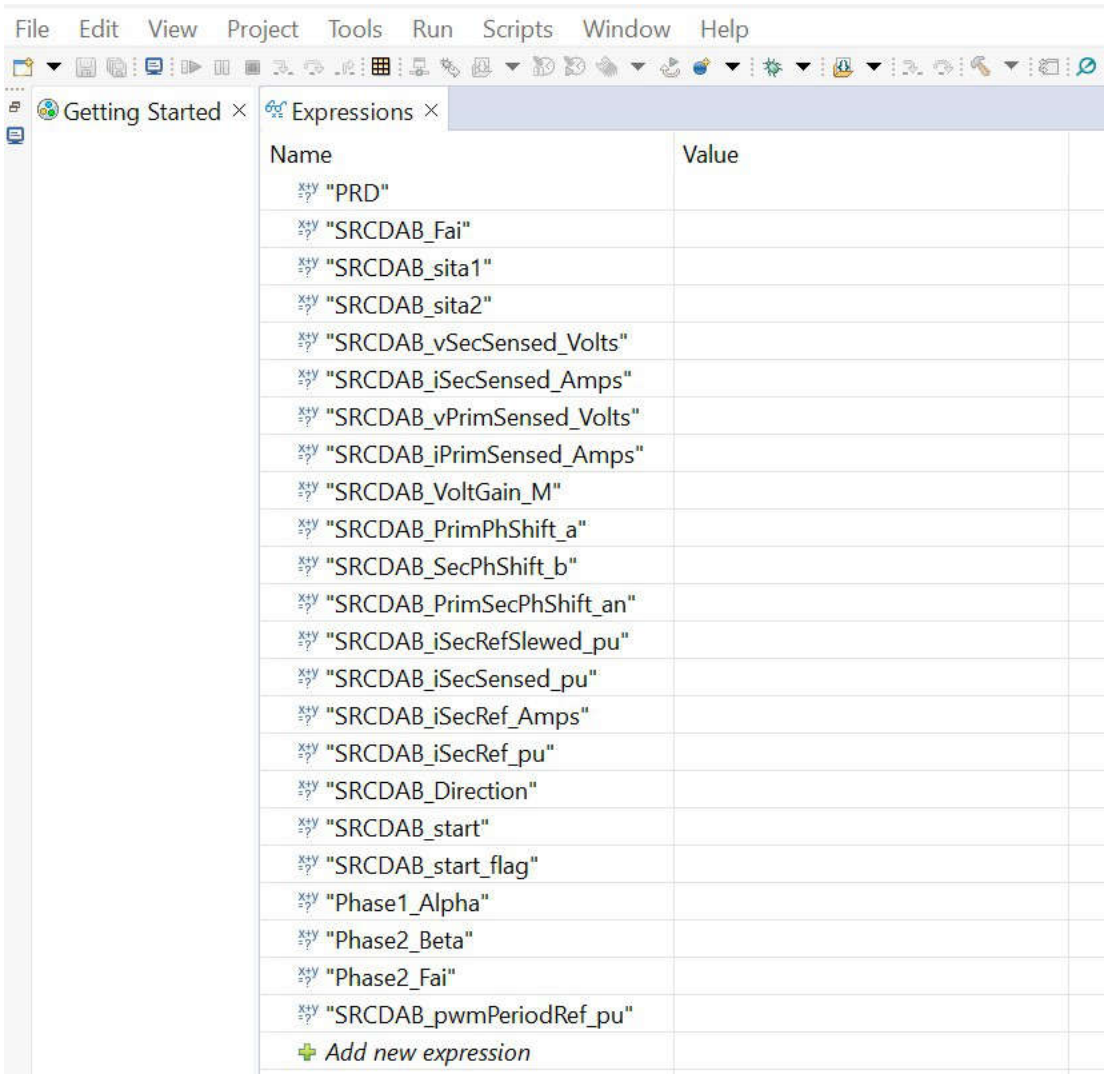


Figure 1-3. Expression Watch Window

Note

Supply the primary and secondary 12V auxiliary power after downloading the firmware into device and running the code.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1 and Figure 2-2. The data was created in charging mode under different load conditions.

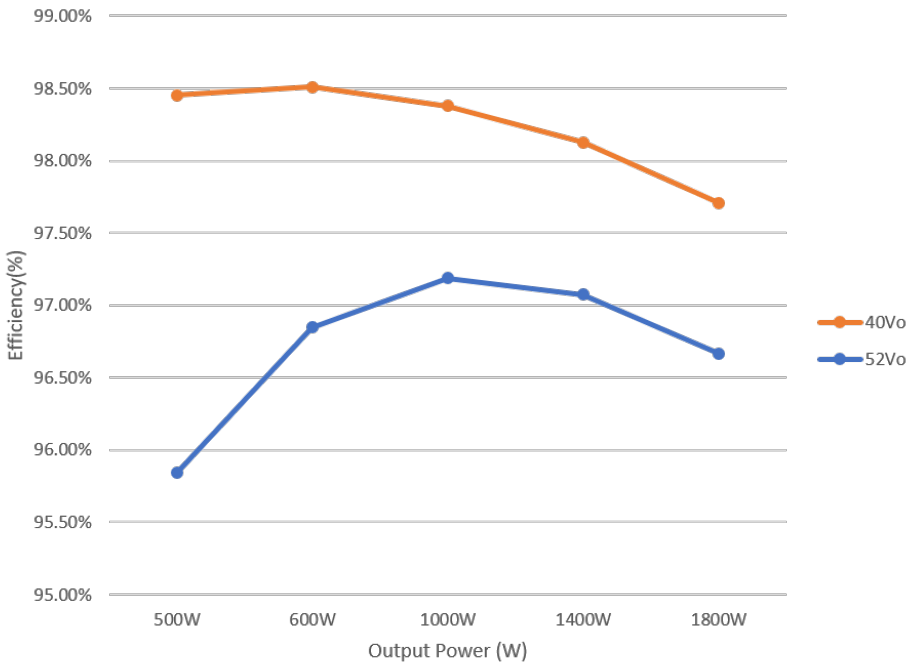


Figure 2-1. Efficiency Graph in Charging Mode

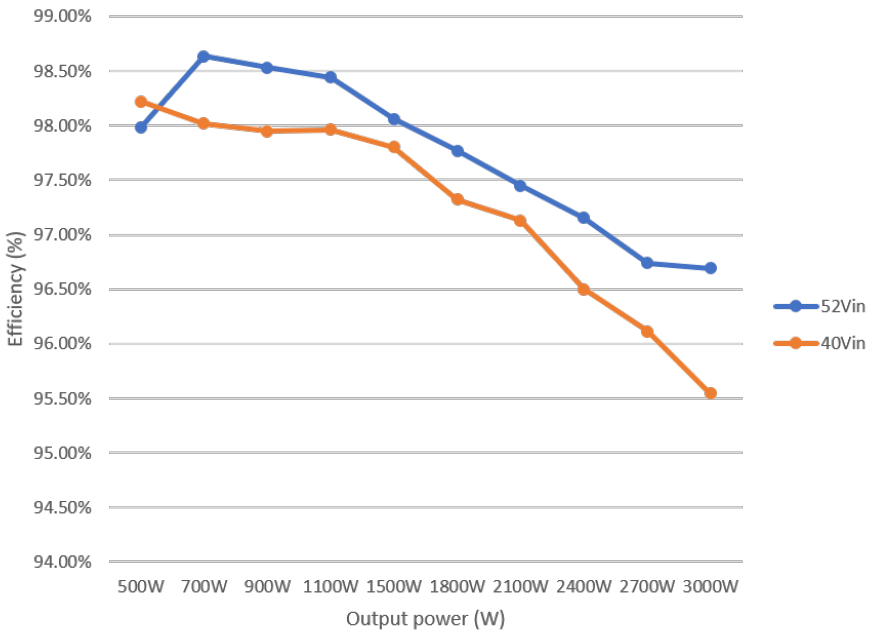


Figure 2-2. Efficiency Graph in Discharging Mode

2.2 Efficiency Data

Efficiency data in discharging mode is shown in Table 2-1.

Table 2-1. Efficiency Data in Discharging Mode With 52Vin

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
51.74	9.2	476.008	400	1.166	466.4	97.98
51.63	14.06	725.918	400	1.79	716	98.63
51.45	22.39	1151.97	400	2.835	1134	98.44
51.47	29.18	1501.89	400	3.682	1472.8	98.06
51.25	43.89	2249.36	400	5.48	2192	97.45
51.01	54.61	2785.66	400	6.737	2694.8	96.74
50.92	61.03	3107.65	400	7.512	3004.8	96.69

Table 2-2. Efficiency Data in Discharging Mode With 40Vin

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
39.66	13.78	546.515	400	1.342	536.8	98.22
39.55	18.16	718.228	400	1.76	704	98.02
39.35	28.65	1127.38	400	2.761	1104.4	97.96
39.23	36.51	1432.29	400	3.502	1400.8	97.8
38.98	55	2143.9	400	5.206	2082.4	97.13
38.83	71.23	2765.86	400	6.646	2658.4	96.11
38.05	80	3044	400	7.271	2908.4	95.55

Efficiency data in charging mode is shown in Table 2-3.

Table 2-3. Efficiency Data in Charging Mode With 40Vo

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
399.58	1.4248	569.322	40.148	13.961	560.506	98.45
399.56	1.6772	670.142	40.179	16.43	660.141	98.51
399.52	2.5236	1008.23	40.276	24.627	991.877	98.38
399.45	3.4858	1392.4	40.392	33.826	1366.3	98.13
399.35	4.5722	1825.91	40.514	44.035	1784.03	97.71

Table 2-4. Efficiency Data in Charging Mode With 52Vo

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)
399.79	1.417	566.502	52.095	10.422	542.934	95.84
399.64	1.7835	712.758	52.077	13.255	690.281	96.85
399.67	2.5302	1011.25	52.149	18.846	982.8	97.19
399.63	3.5205	1406.9	52.281	26.123	1365.74	97.07
399.56	4.523	1807.21	52.288	33.41	1746.94	96.67

During charging mode, the voltage stress on low voltage side is close to the FET drain to source rated voltage when load is over half load. Thus the efficiency is only tested below half load.

3 Waveforms

3.1 Switching

Figure 3-1 through Figure 3-3 show the switching behavior waveforms.

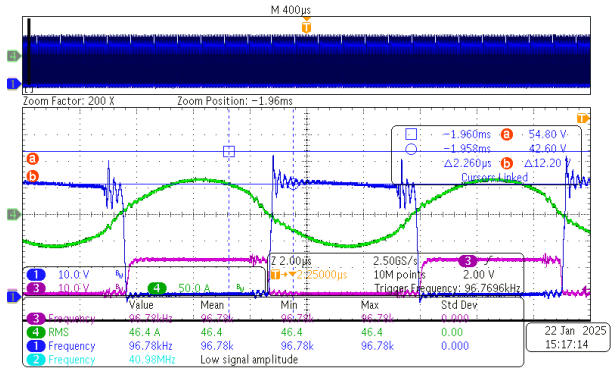


Figure 3-1. Charging Mode, 400V_{IN}, 40V_{OUT}, 1800W

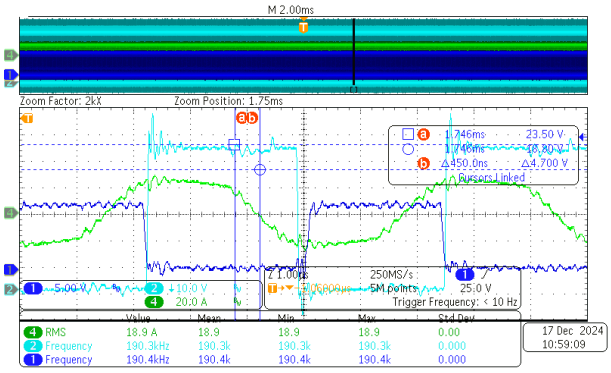


Figure 3-2. Charging Mode, 400V_{IN}, 52V_{OUT}, 700W

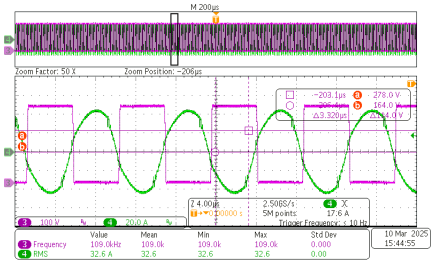


Figure 3-3. Discharging Mode, 52V_{IN}, 400V_{OUT}, 1600W

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