Test Report: PMP41139

3.5kW, 800V to 14V DC-DC Converter Reference Design

Description

This reference design describes a 3.5kW, 800V to 14V DC-DC converter with 650V Gallium nitride (GaN) high-electron mobility transistors (HEMT). Using stacked half-bridge (SHB) topology makes the converter work at 800V with 650V GaN HEMT. Using LMG3522R030 as primary switches makes the converter work at a high switching frequency. In this design, the converter uses a smaller transformer size. To ease the thermal performance of active clamping metal-oxide semiconductor field effect transistors (MOSFETs), the converter uses two channel active clamping circuits.

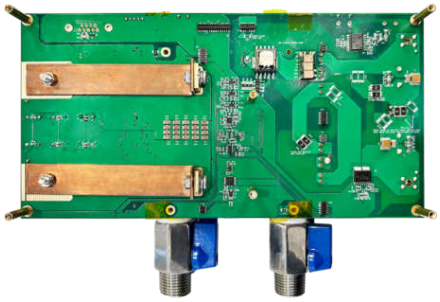
Features

- 650V GaN based stacked half-bridge (SHB) using LMG3522 in 800V battery system
- 200kHz switching frequency, magnetic size is 35% less than 100kHz
- 95.48% at 200kHz, 800V V_{in}, 13.5V V_{out}, about 1kW
- Dual active clamping circuits for high-frequency scenario and low synchronous rectifier (SR) MOSFET voltage stress
- Light load efficiency optimization promotes maximum 5% efficiency

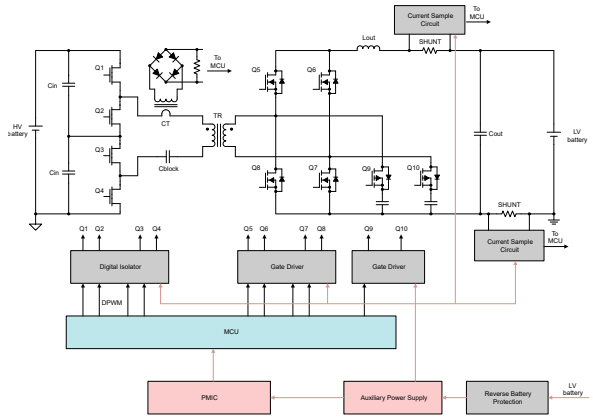
Applications

- Hybrid, electric, and powertrain systems
- DC/DC converter system

Top of Board



Bottom of Board



Block Diagram

1 Test Prerequisites

This chapter describes the functional parameters of high-voltage to low-voltage DC/DC converters and the required test equipments.

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	MIN	TYP	MAX	UNITS
V_{in}	400	800	900	V
I_{in}			10	A
V_{out}	9	14	16	V
I_{out}	0		250	A
P_{out}			3500	W
Switching Frequency		200		kHz

1.2 Required Equipment

- DC Source: Chroma 62150H-1000
- DC Source: GW Instek GPS-3303C
- DC Load: Chroma 63208E-600-560
- Multimeter: Fluke 287C
- Oscilloscope: Tektronix DPO3054
- Electrical thermography: Fluke TiS55
- Vector Network Analyzer: OMICRON Bode100

1.3 Considerations

Commonly, for high-voltage to low-voltage DC/DC applications, the input and output voltage both are in a wide range. Figure 1-1 shows the relationship with input voltage and output voltage. The maximum output voltage is 14V while input voltage drops to 200V. When the output voltage is between 14V and 16V, the converter can output full power with the current derated. When the output voltage is between 9V and 14V, the converter can output maximum current with power derated. The details are shown in Figure 1-2.

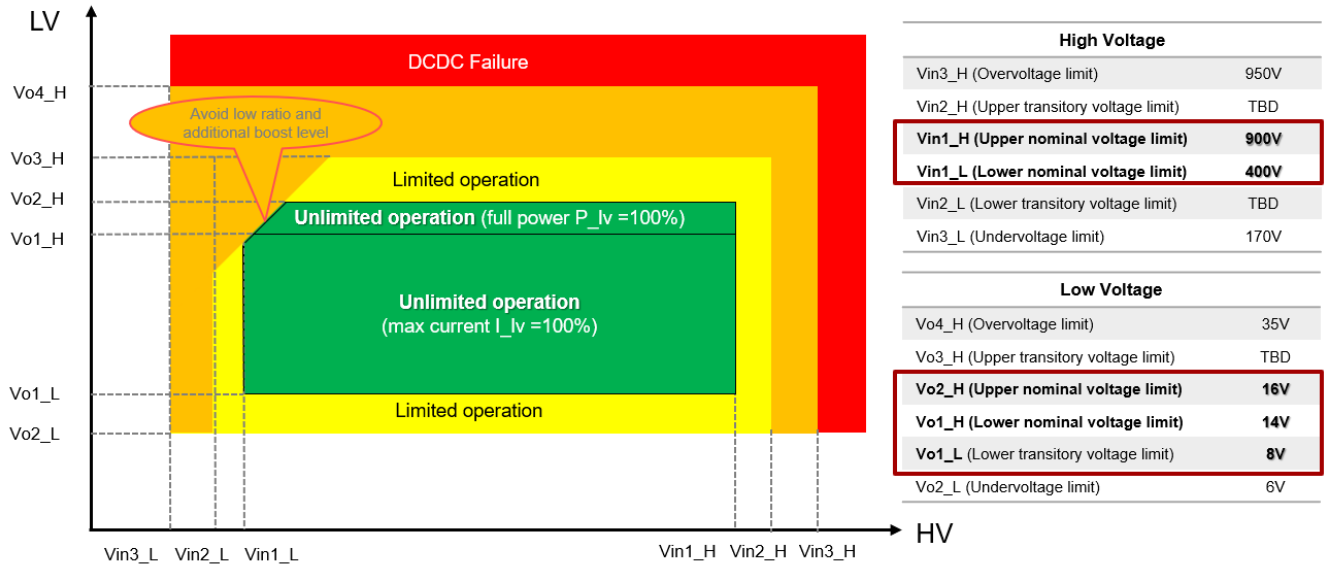
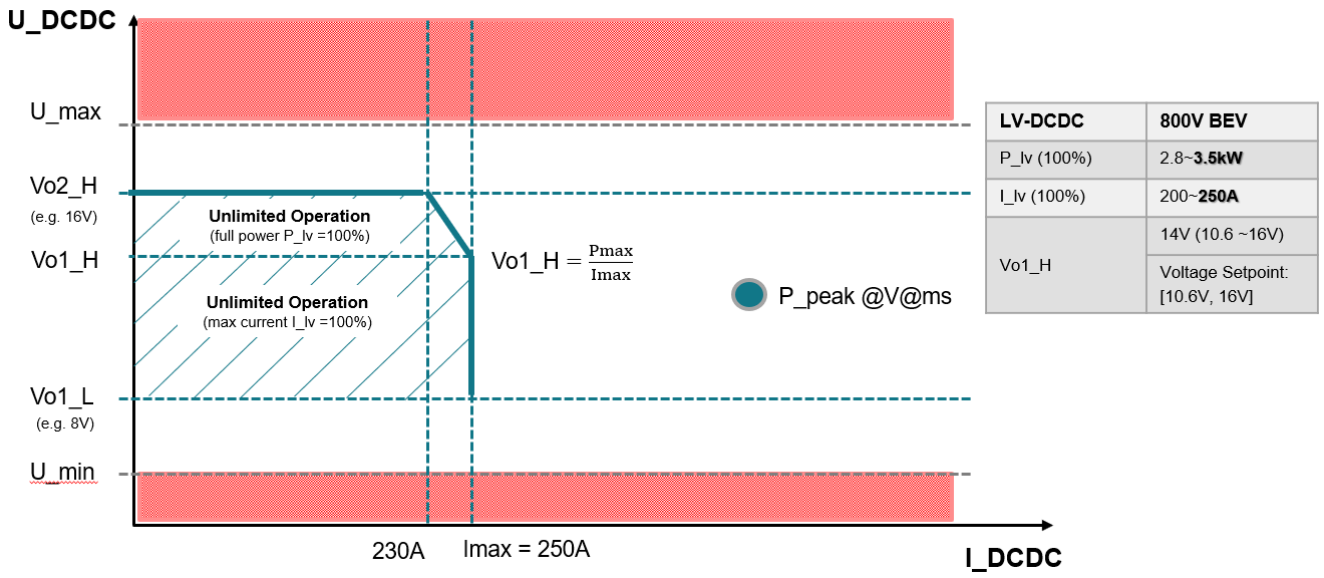


Figure 1-1. Input Voltage and Output Voltage



LV-DCDC	800V BEV
P_lv (100%)	2.8~**3.5kW**
I_lv (100%)	200~**250A**
Vo1_H	14V (10.6 ~16V)
	Voltage Setpoint: [10.6V, 16V]

Figure 1-2. Maximum Output Power and Maximum Output Current

1.4 Dimensions

The board dimensions are 252.5mm (length) × 130mm (width) × 68mm (height).

Figure 1-3. Dimensions

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1.

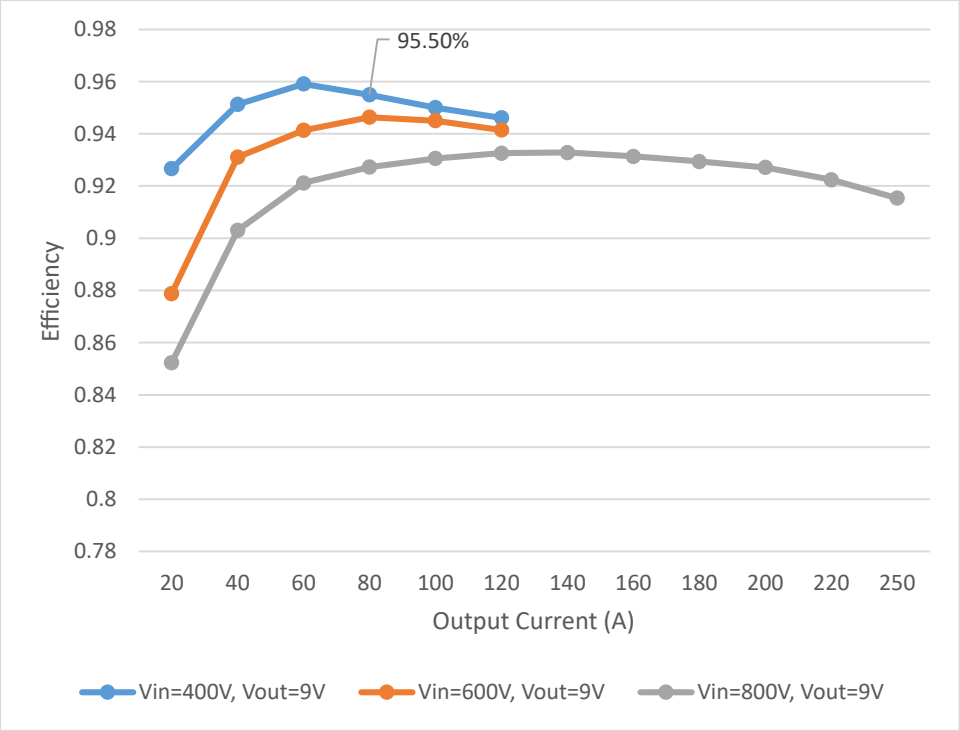


Figure 2-1. Efficiency Graph at $9V_{out}$

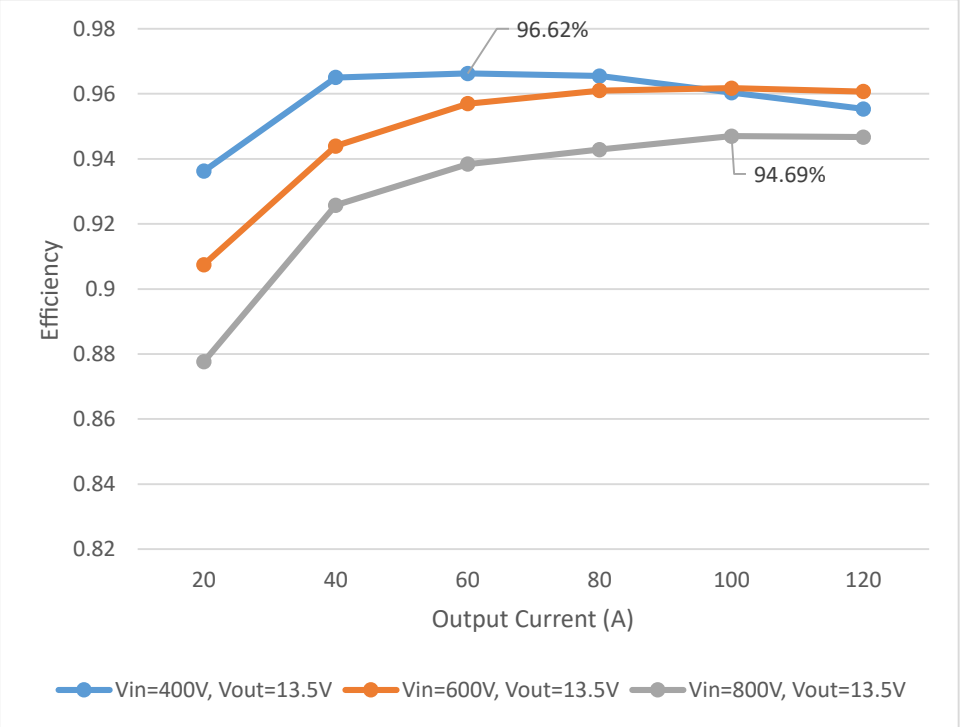


Figure 2-2. Efficiency Graph at $13.5V_{out}$

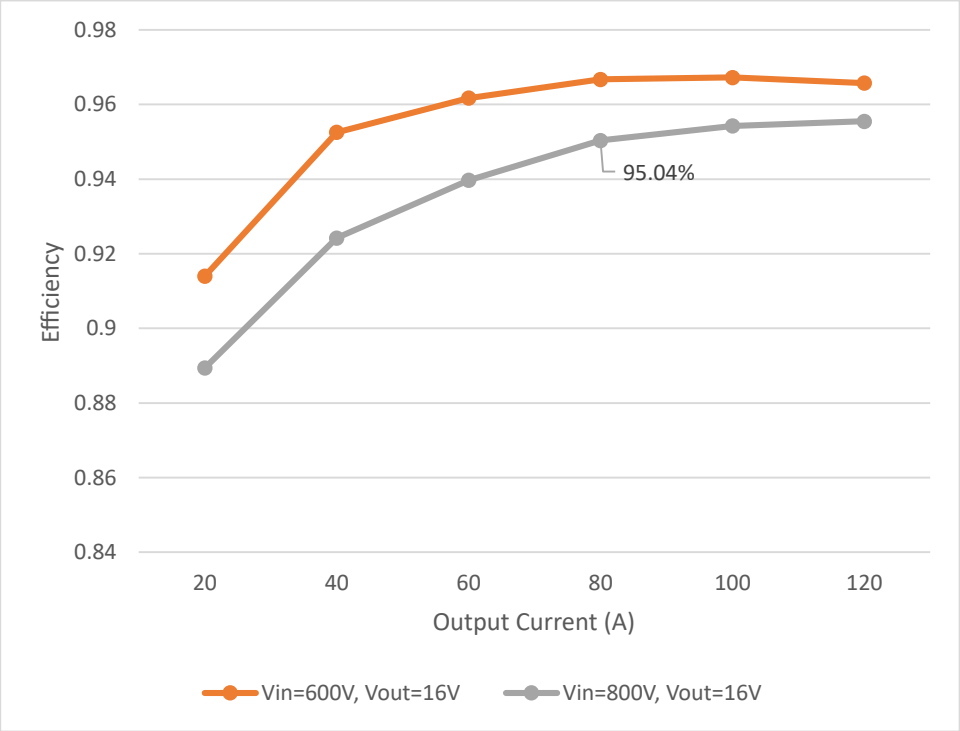


Figure 2-3. Efficiency Graph at $16V_{out}$

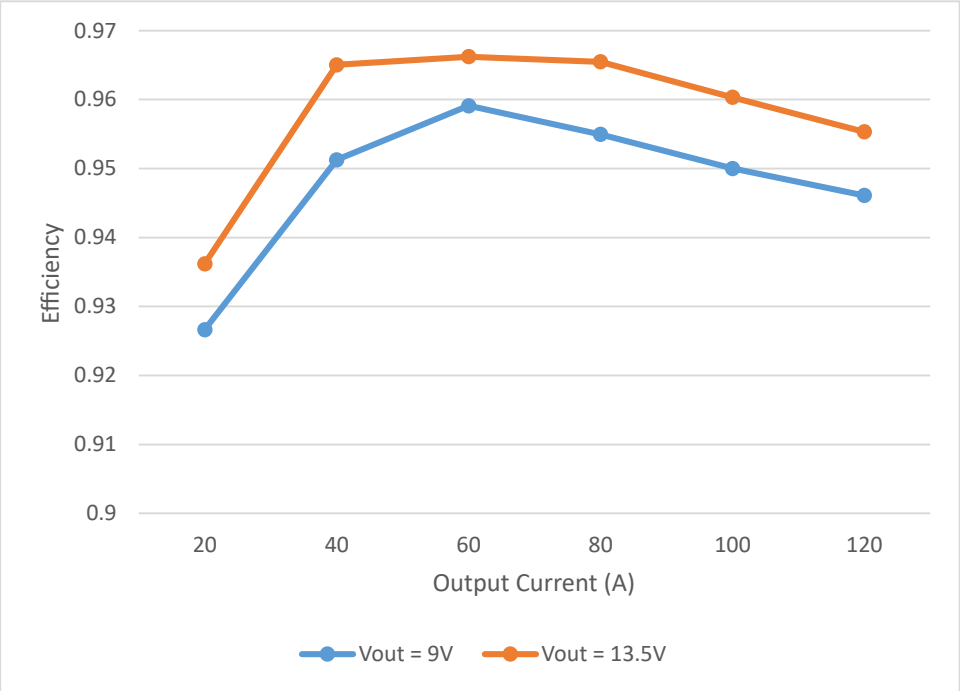


Figure 2-4. Efficiency Graph at $400V_{in}$

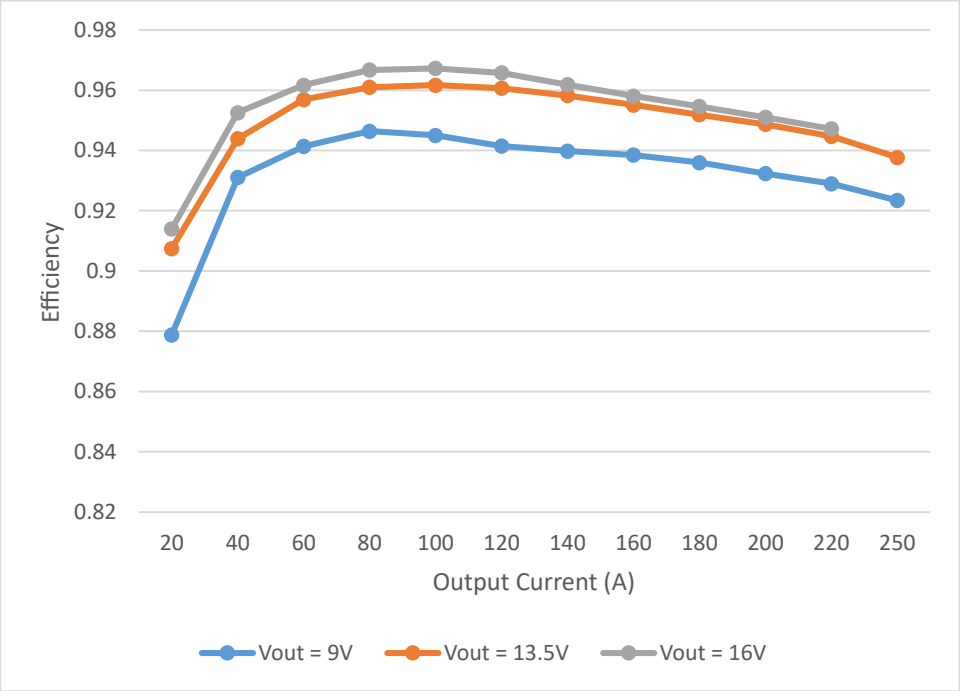


Figure 2-5. Efficiency Graph at 600V_{in}

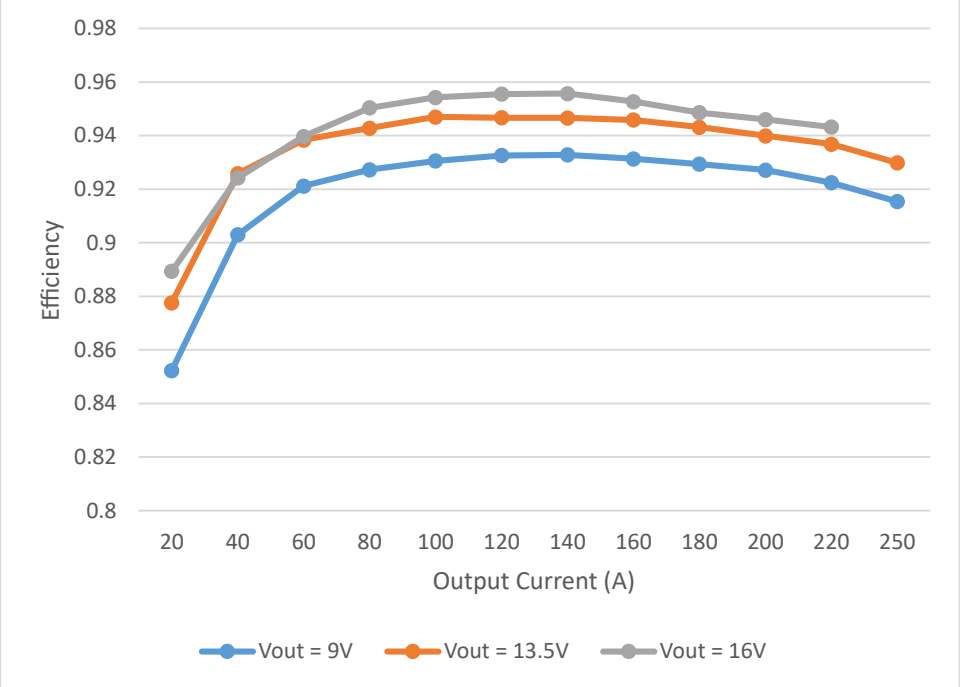


Figure 2-6. Efficiency Graph at 800V_{in}

2.2 Efficiency Data

Efficiency data is shown in Table 2-1.

Table 2-1. Efficiency at $400V_{in}$, $9V_{out}$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss}(W)	Efficiency
400	0.484	193.6	8.97	20	179.4	14.2	92.67%
400	0.944	377.6	8.98	40	359.2	18.4	95.13%
400	1.406	562.4	8.99	60	539.4	23	95.91%
400	1.887	754.8	9.01	80	720.8	34	95.50%
400	2.371	948.4	9.01	100	901	47.4	95.00%
400	2.857	1142.8	9.01	120	1081.2	61.6	94.61%

Table 2-2. Efficiency at $400V_{in}$, $13.5V_{out}$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
400	0.721	288.4	13.5	20	270	18.4	93.62%
400	1.401	560.4	13.52	40	540.8	19.6	96.50%
400	2.102	840.8	13.54	60	812.4	28.4	96.62%
400	2.809	1123.6	13.56	80	1084.8	38.8	96.55%
400	3.53	1412	13.56	100	1356	56	96.03%
400	4.186	1674.4	13.33	120	1599.6	74.8	95.53%

Table 2-3. Efficiency at $600V_{in}$, $9V_{out}$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
600	0.341	204.6	8.99	20	179.8	24.8	87.88%
600	0.643	385.8	8.98	40	359.2	26.6	93.11%
600	0.955	573	8.99	60	539.4	33.6	94.14%
600	1.268	760.8	9	80	720	40.8	94.64%
600	1.589	953.4	9.01	100	901	52.4	94.50%
600	1.914	1148.4	9.01	120	1081.2	67.2	94.15%
600	2.237	1342.2	9.01	140	1261.4	80.8	93.98%
600	2.563	1537.8	9.02	160	1443.2	94.6	93.85%
600	2.891	1734.6	9.02	180	1623.6	111	93.60%
600	3.232	1939.2	9.04	200	1808	131.2	93.23%
600	3.572	2143.2	9.05	220	1991	152.2	92.90%
600	4.088	2452.8	9.06	250	2265	187.8	92.34%

Table 2-4. Efficiency at $600V_{in}$, $13.5V_{out}$

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
600	0.497	298.2	13.53	20	270.6	27.6	90.74%
600	0.957	574.2	13.55	40	542	32.2	94.39%
600	1.416	849.6	13.55	60	813	36.6	95.69%
600	1.88	1128	13.55	80	1084	44	96.10%
600	2.35	1410	13.56	100	1356	54	96.17%
600	2.823	1693.8	13.56	120	1627.2	66.6	96.07%

Table 2-4. Efficiency at 600V_{in}, 13.5V_{out} (continued)

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
600	3.302	1981.2	13.56	140	1898.4	82.8	95.82%
600	3.786	2271.6	13.56	160	2169.6	102	95.51%
600	4.277	2566.2	13.57	180	2442.6	123.6	95.18%
600	4.775	2865	13.59	200	2718	147	94.87%
600	5.267	3160.2	13.57	220	2985.4	174.8	94.47%
600	6.03	3618	13.57	250	3392.5	225.5	93.77%

Table 2-5. Efficiency at 600V_{in}, 16V_{out}

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
600	0.585	351	16.04	20	320.8	30.2	91.40%
600	1.124	674.4	16.06	40	642.4	32	95.26%
600	1.671	1002.6	16.07	60	964.2	38.4	96.17%
600	2.215	1329	16.06	80	1284.8	44.2	96.67%
600	2.769	1661.4	16.07	100	1607	54.4	96.73%
600	3.33	1998	16.08	120	1929.6	68.4	96.58%
600	3.896	2337.6	16.06	140	2248.4	89.2	96.18%
600	4.473	2683.8	16.07	160	2571.2	112.6	95.80%
600	5.047	3028.2	16.06	180	2890.8	137.4	95.46%
600	5.629	3377.4	16.06	200	3212	165.4	95.10%
600	6.213	3727.8	16.05	220	3531	196.8	94.72%

Table 2-6. Efficiency at 800V_{in}, 9V_{out}

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
800	0.264	211.2	9	20	180	31.2	85.23%
800	0.5	400	9.03	40	361.2	38.8	90.30%
800	0.736	588.8	9.04	60	542.4	46.4	92.12%
800	0.976	780.8	9.05	80	724	56.8	92.73%
800	1.217	973.6	9.06	100	906	67.6	93.06%
800	1.454	1163.2	9.04	120	1084.8	78.4	93.26%
800	1.694	1355.2	9.03	140	1264.2	91	93.29%
800	1.937	1549.6	9.02	160	1443.2	106.4	93.13%
800	2.191	1752.8	9.05	180	1629	123.8	92.94%
800	2.443	1954.4	9.06	200	1812	142.4	92.71%
800	2.701	2160.8	9.06	220	1993.2	167.6	92.24%
800	3.093	2474.4	9.06	250	2265	209.4	91.54%

Table 2-7. Efficiency at 800V_{in}, 13.5V_{out}

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
800	0.386	308.8	13.55	20	271	37.8	87.76%
800	0.734	587.2	13.59	40	543.6	43.6	92.57%
800	1.087	869.6	13.6	60	816	53.6	93.84%
800	1.434	1147.2	13.52	80	1081.6	65.6	94.28%

Table 2-7. Efficiency at 800V_{in}, 13.5V_{out} (continued)

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
800	1.786	1428.8	13.53	100	1353	75.8	94.69%
800	2.147	1717.6	13.55	120	1626	91.6	94.67%
800	2.505	2004	13.55	140	1897	107	94.66%
800	2.863	2290.4	13.54	160	2166.4	124	94.59%
800	3.242	2593.6	13.59	180	2446.2	147.4	94.32%
800	3.62	2896	13.61	200	2722	174	93.99%
800	4.004	3203.2	13.64	220	3000.8	202.4	93.68%
800	4.584	3667.2	13.64	250	3410	257.2	92.99%

Table 2-8. Efficiency at 800V_{in}, 16V_{out}

V_{in}(V)	I_{in}(A)	P_{in}(W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	P_{loss} (W)	Efficiency
800	0.452	361.6	16.08	20	321.6	40	88.94%
800	0.871	696.8	16.1	40	644	52.8	92.42%
800	1.285	1028	16.1	60	966	62	93.97%
800	1.692	1353.6	16.08	80	1286.4	67.2	95.04%
800	2.109	1687.2	16.1	100	1610	77.2	95.42%
800	2.529	2023.2	16.11	120	1933.2	90	95.55%
800	2.95	2360	16.11	140	2255.4	104.6	95.57%
800	3.382	2705.6	16.11	160	2577.6	128	95.27%
800	3.826	3060.8	16.13	180	2903.4	157.4	94.86%
800	4.26	3408	16.12	200	3224	184	94.60%
800	4.697	3757.6	16.11	220	3544.2	213.4	94.32%

2.3 Thermal Images

Figure 2-7 shows the test setup of PMP41139 converter. Thermal images at 120A and 250A output current are shown in Figure 2-8 and Figure 2-9. Not too much thermal data can be gained from the top view due to SR card and GaN cards being vertical to main board and screwed to water-cooling heat sink.

Test condition: 800Vin, 13.5Vout, room temperature, 20°C degree liquid coolant.

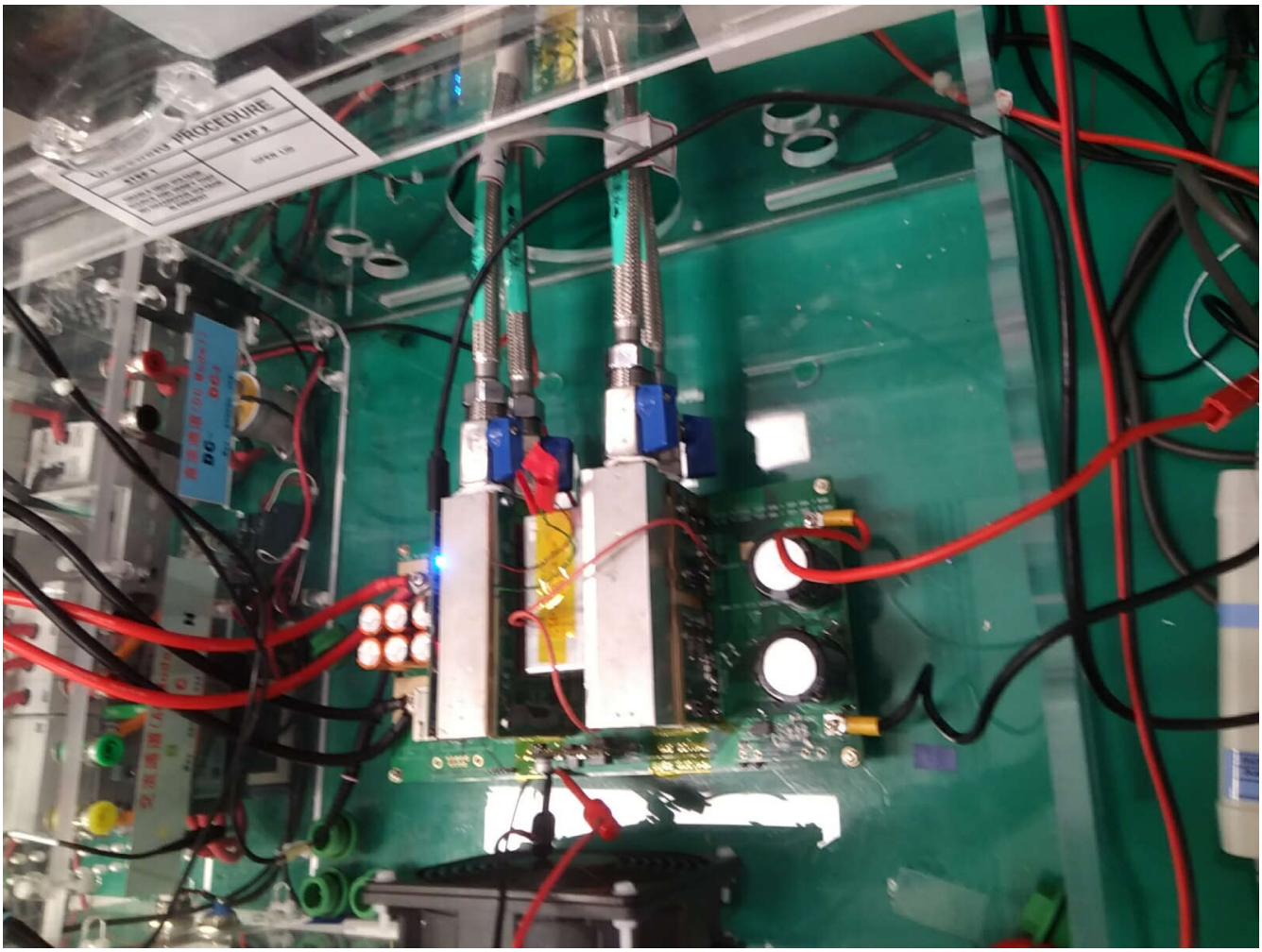


Figure 2-7. Thermal Setup

Figure 2-8. Thermal Image at 120A

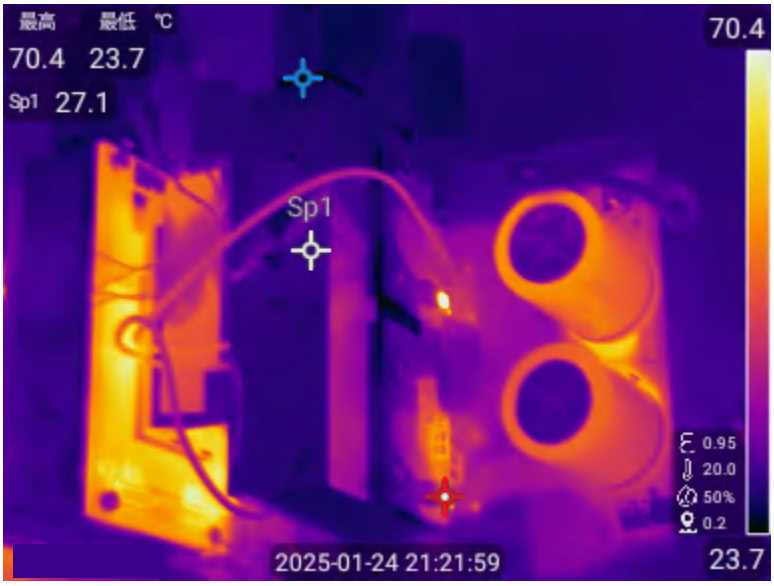


Figure 2-9. Thermal Image at 250A

The magnetics of HV to LV DC/DC converter contain a transformer and a choke. The leakage of Transformer is used as resonant inductor in PSFB-SHB topology. PMP41139 and PMP41078 use the same magnetics, so please refer to PMP41078 reference design to check the thermal performance of transformer and choke.

2.4 Bode Plots

Bode plot are shown in Figure 2-10 through Figure 2-12. The test condition is 800V_{in}, 13.5V_{out}, 120A I_{out}, room temperature. As shown in Figure 2-12, the gain margin is -17.98dB. The phase margin is 70.33 degrees with 2.16kHz bandwidth.

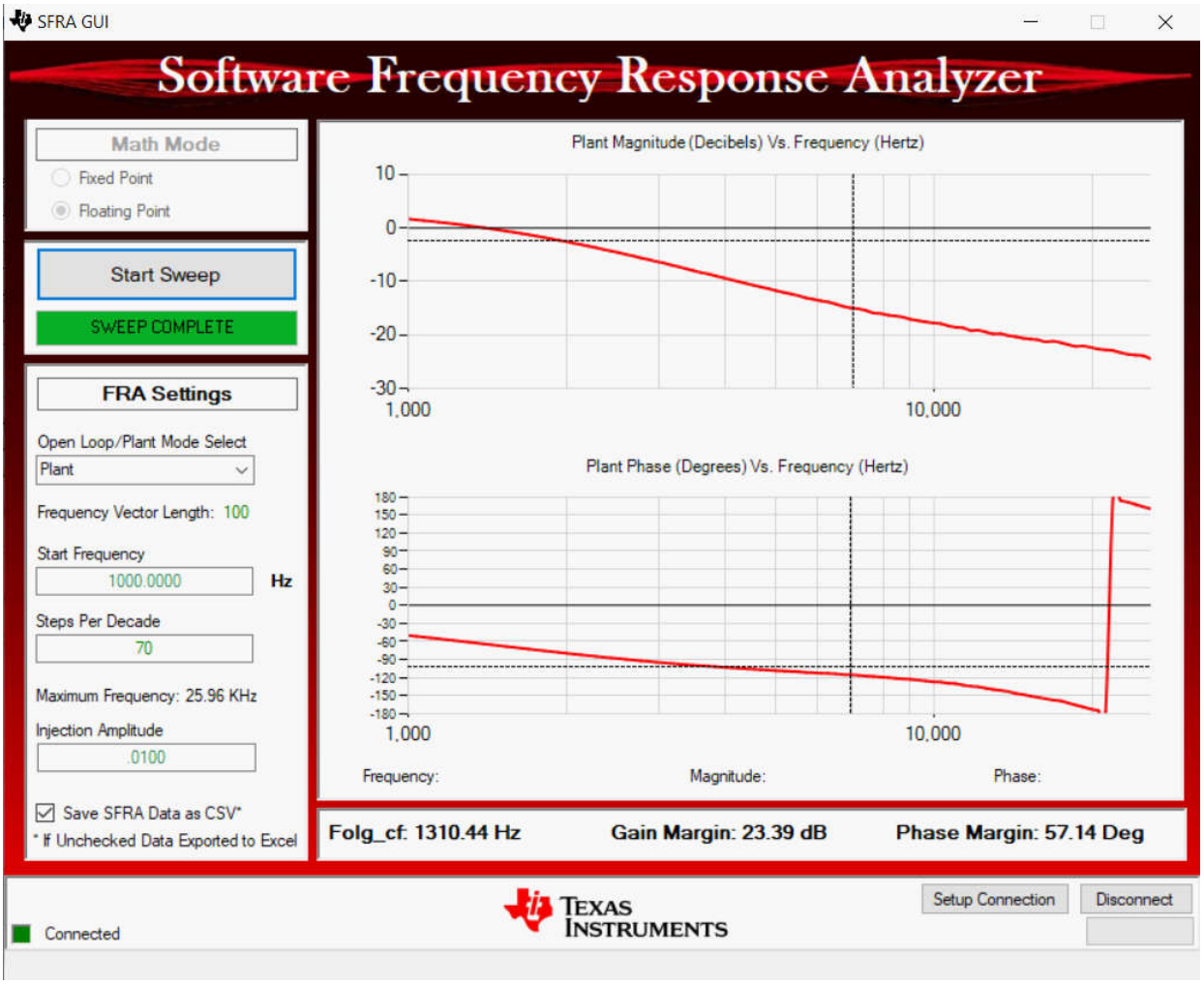


Figure 2-10. Power Stage Bode Plot

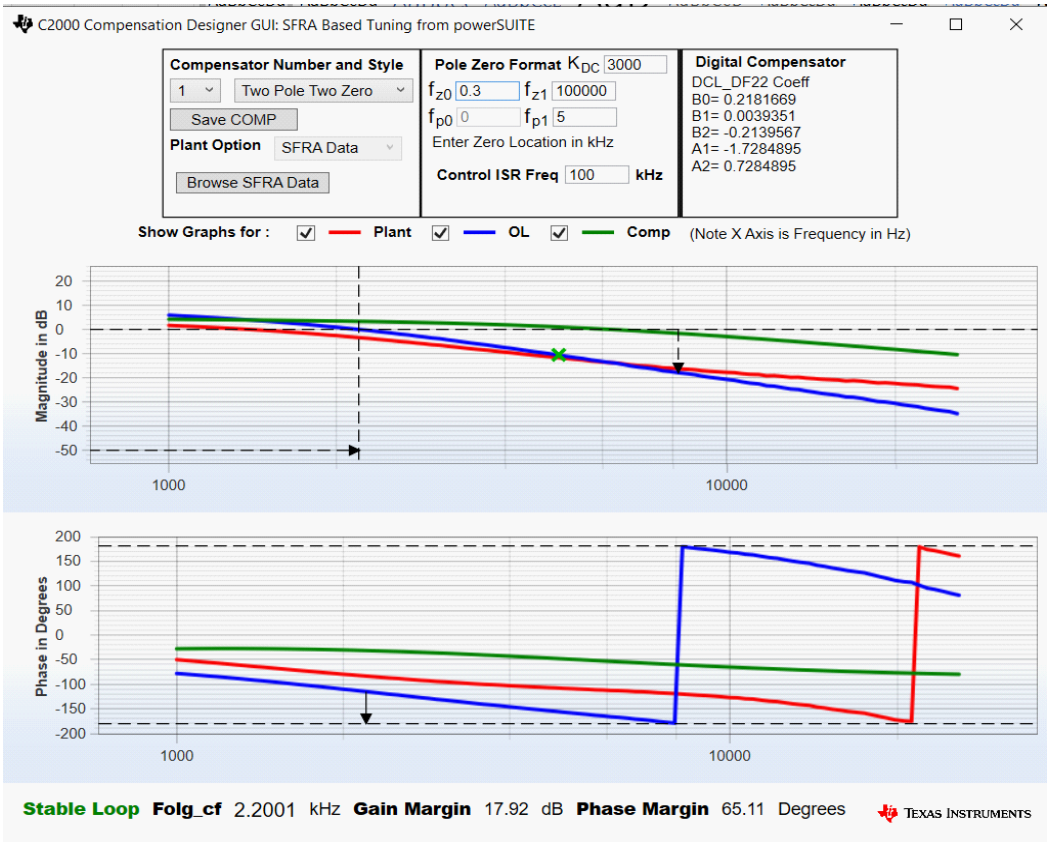


Figure 2-11. Compensator Bode Plot

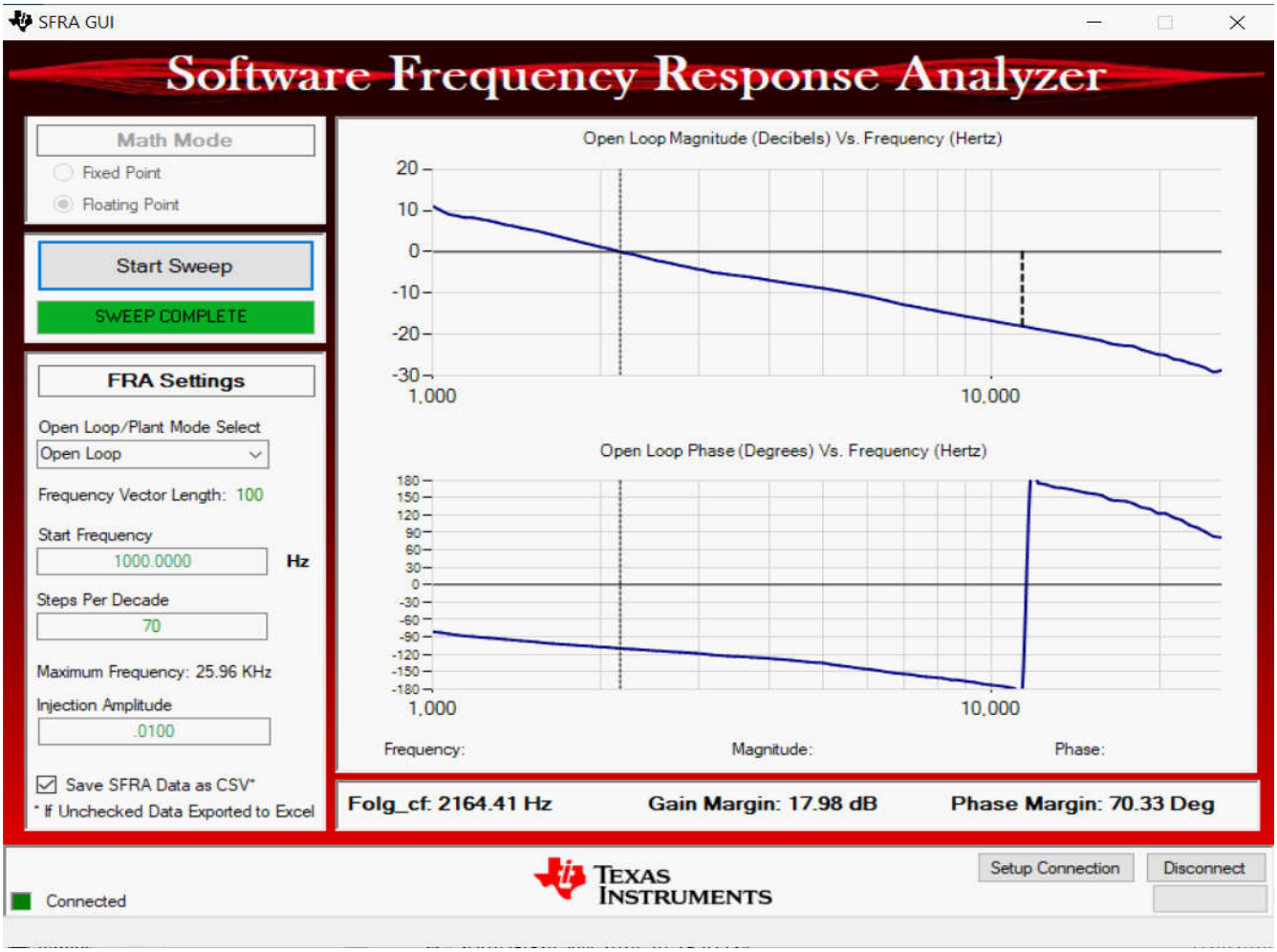


Figure 2-12. Converter Bode Plot

2.5 Light Load Efficiency Optimization

Considering the converter is working in synchronous rectification status, the light load efficiency is very low. There are two options we can adopt to optimize the efficiency. One option is decreasing the switching frequency or adopting burst mode and another option is adjustable dead time. Of course, we also can combine the two options into one.

Table 2-9 lists the difference between Frequency Reduction Mode and Hysteretic Burst Mode.

Table 2-9. Control Scheme

	Frequency reduction mode	Hysteretic burst mode
Principle	Continuously switches, reduce effective duty cycle while maintaining a minimum on-time	When Vcomp becomes <Vburst_threshold, the FETs stops switching
Transient response	Reduced control loop bandwidth	Fast
CPU utilization	Large, need to compute required F**SW**	Small, enable/disable switching based on comparator
Output ripple	Small	Larger compared to FR mode

Figure 2-13 to Figure 2-15 show the waveforms with or without optimization. CH1 is Vgs of secondary FET, CH2 is Vds of secondary FET, CH3 is voltage of transformer primary winding, CH4 is current of transformer primary winding.

With no optimization, the efficiency is only 80.05% when V_{in} is 600V, V_{out} is 9V with 20A output current. With hysteretic burst mode, the efficiency rises to 82.46%. With frequency reduction mode, the efficiency is 87.88%, making the best performance.

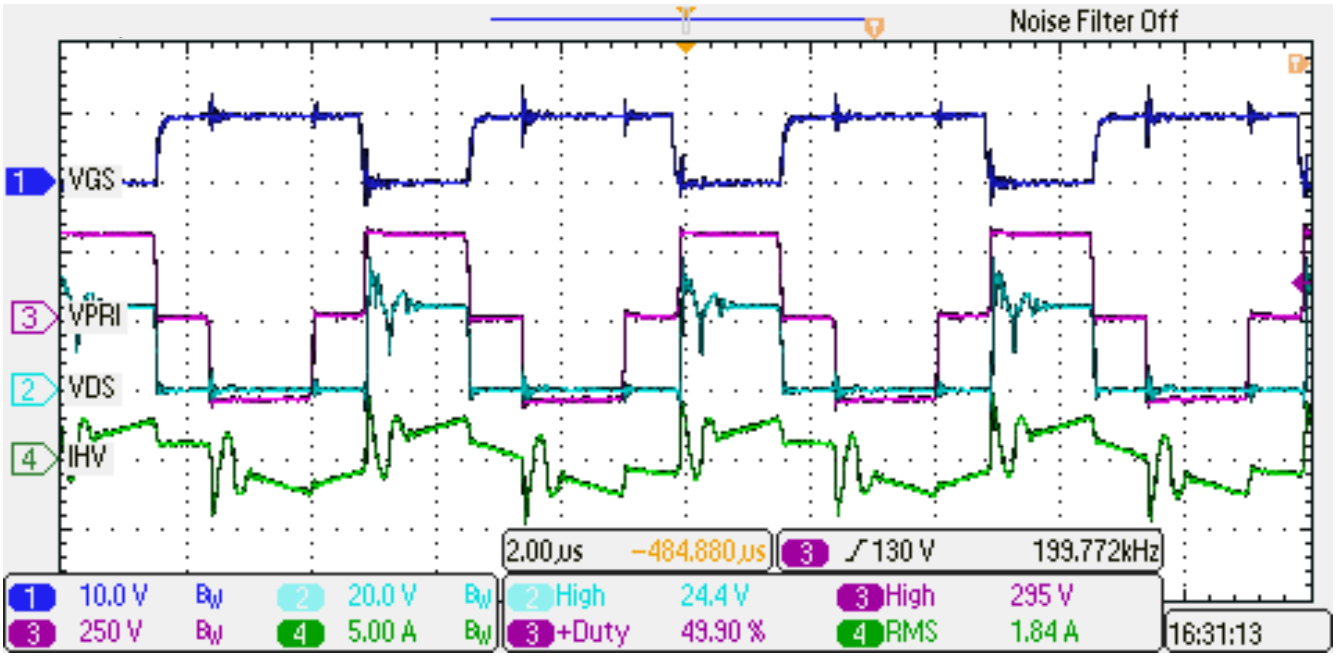


Figure 2-13. Waveforms Without Optimization

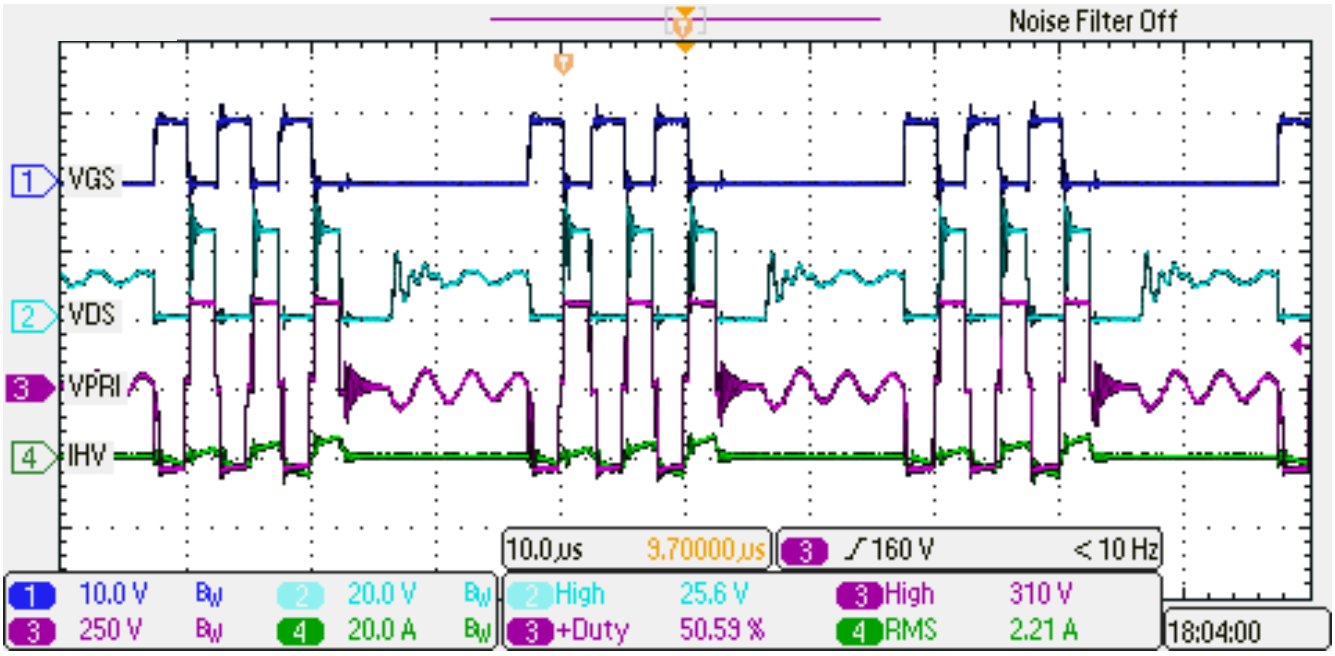


Figure 2-14. Waveforms with Burst Mode

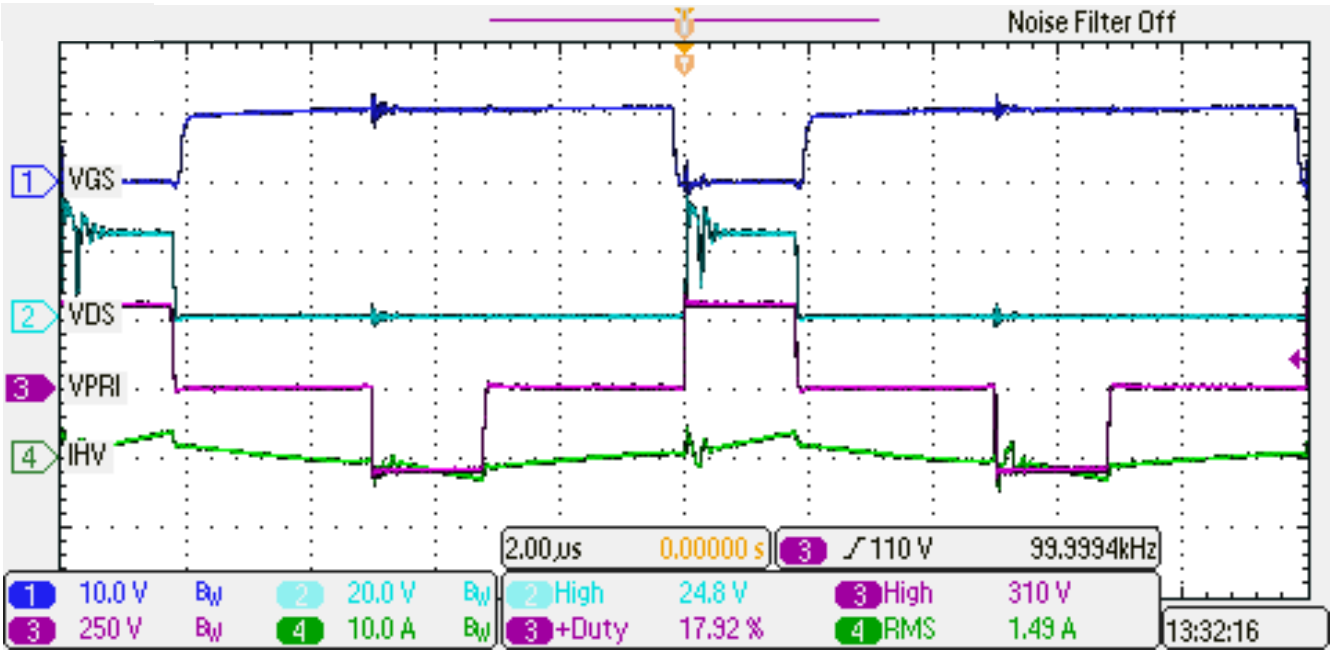


Figure 2-15. Waveforms with Frequency Reduction Mode

Similar as PSFB topology, *lag* bridge of SHB topology is challenging to achieve ZVS. To optimize efficiency, dead time must be optimized to achieve valley switching. As shown in Figure 2-16 to Figure 2-18, when output current is low, like 20A, this takes a longer time on Coss charging, so valley switching is usually with longer deadtime. When output current is high, like 120A, this takes a shorter time on Coss charging, so valley switching is usually with shorter deadtime.

Notice: When output current is low, ZVS can be achieved. Deadtime must not be too long, otherwise Coss oscillates with Ls.

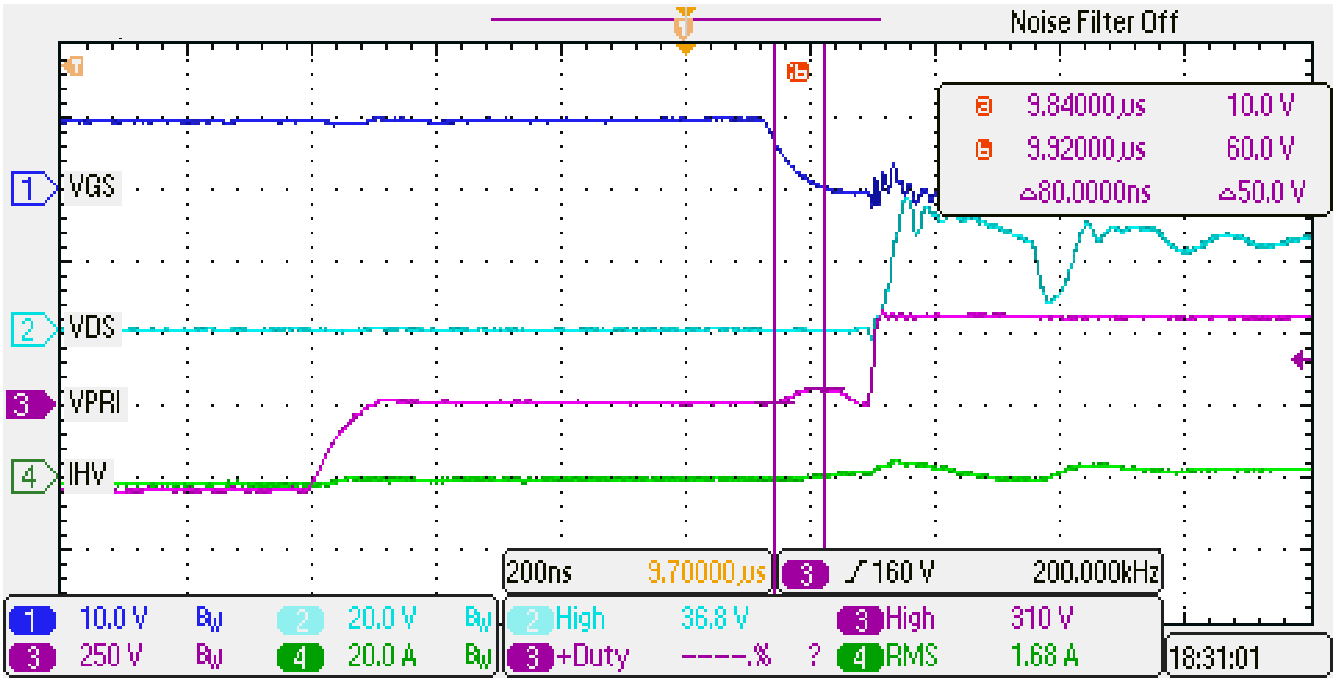


Figure 2-16. I_{out} 20A：Dead Time Must be 80ns

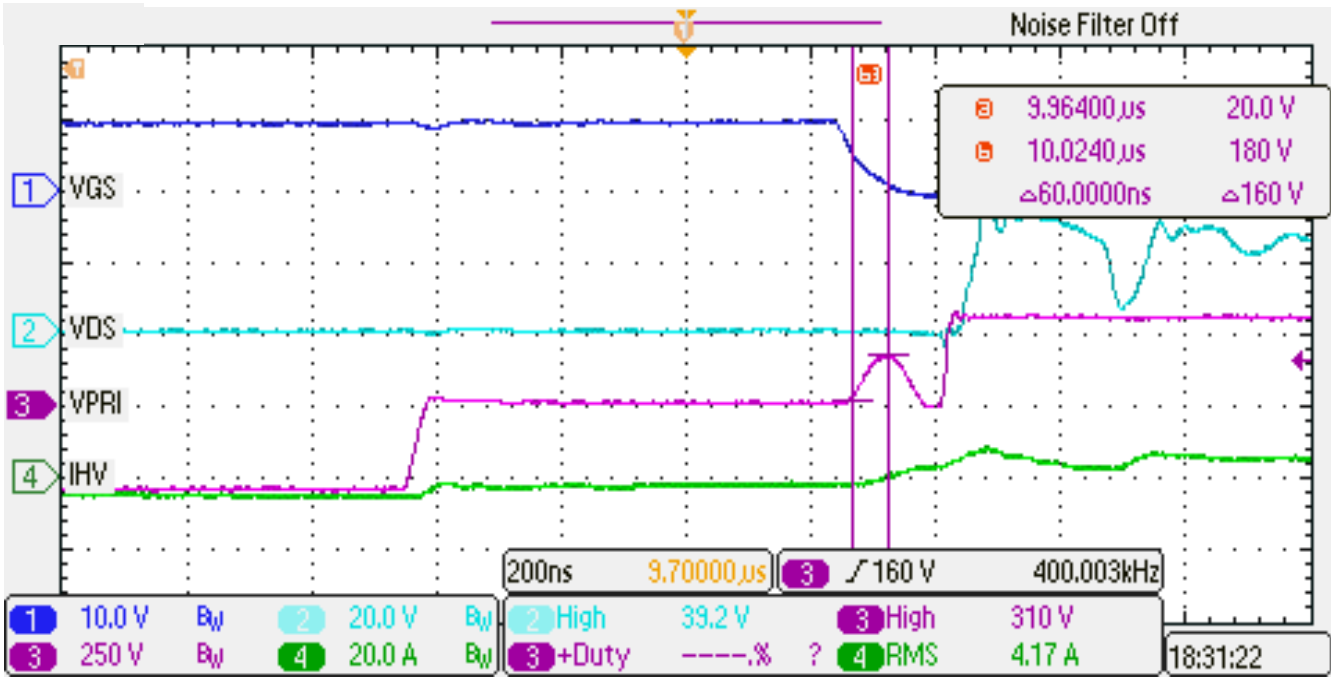


Figure 2-17. I_{out} 60A：Dead Time Must be 60ns

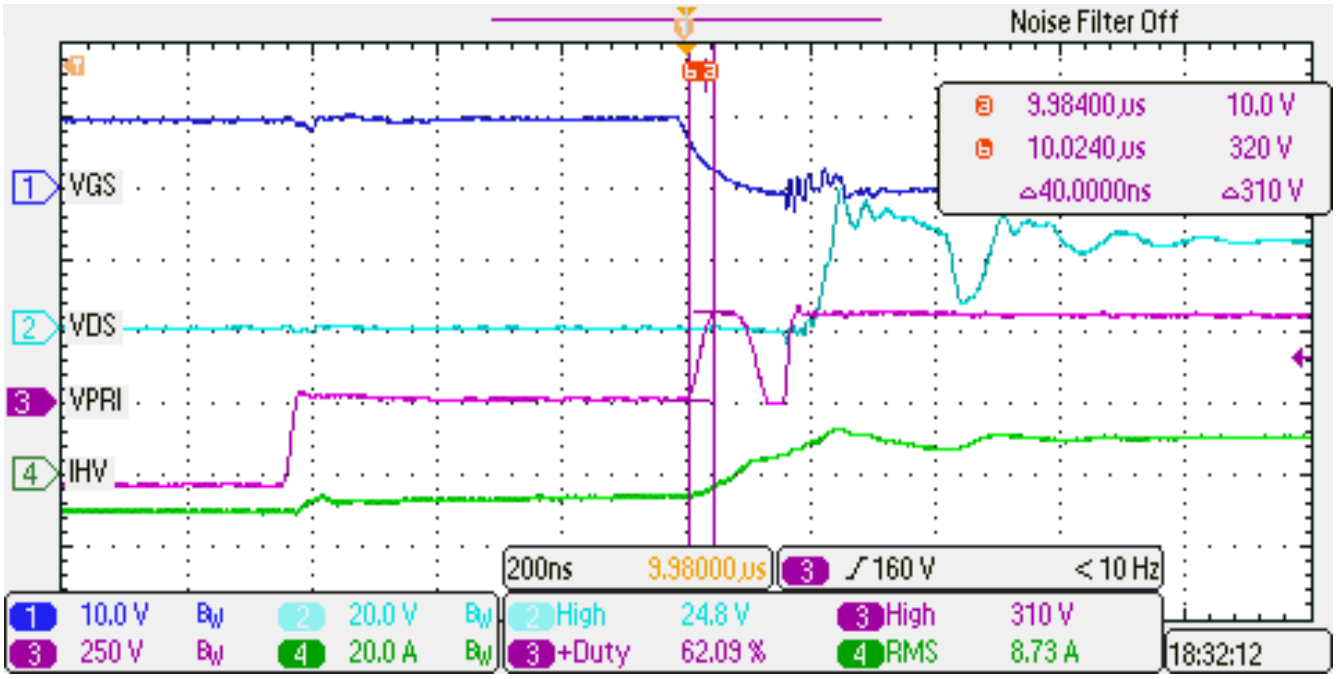


Figure 2-18. I_{out} 120A：Dead Time Must be 40ns

2.6 Midpoint Voltage Balance Control of Input Capacitors

The high voltage battery in an electric vehicle is trending to 800V. To leverage the high frequency performance benefits of 650V GaN, the PSFB topology is rearchitected to the SHB. Conventional PSFB control results in ZVS, however this creates a voltage imbalance on the split input capacitors. This voltage imbalance results from the circulation current during the *1-D* phase always being drawn in the same direction (into or out) of the capacitor midpoint.

Many ways can achieve midpoint voltage balance of input capacitors. Remember the basic principle for the sequence is:

- I_{MID} average is 0A
- $I_{D,RMS}$ is the same for each FET
- ZVS is achieved for each FET

Table 2-10 shows the difference with and without midpoint voltage balance control. When input 400V, the differential voltage between top and bottom capacitor is as high as 28V, not to mention 800V application. Applying voltage balance control is necessary.

Table 2-10. Effect of Voltage Balance Control

Control Scheme	VCAP_TOP	VCAP_BOT	VCAP_DIFF
Without voltage balance control	218V	190V	28V
With voltage balance control	204V	202V	2V

Figure 2-19 to Figure 2-21 show the midpoint voltage at various input voltages. One can conclude that midpoint average voltage is very close to half of input voltage and the maximum deviation is no more than 5V.

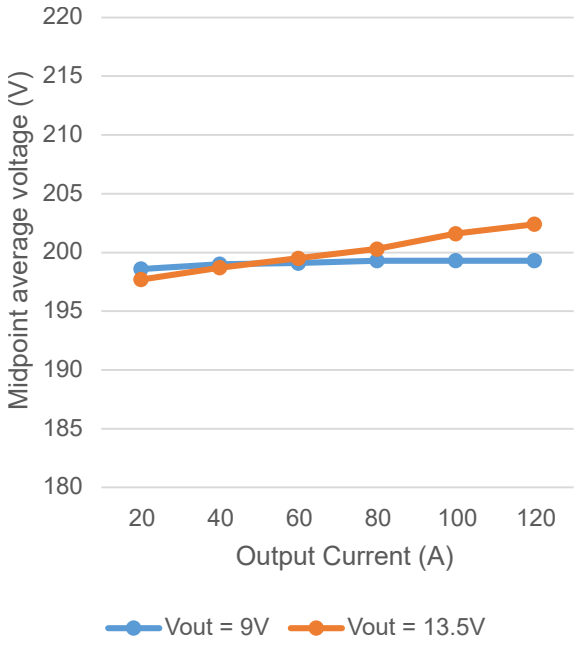


Figure 2-19. Midpoint voltage at 400V_{in}

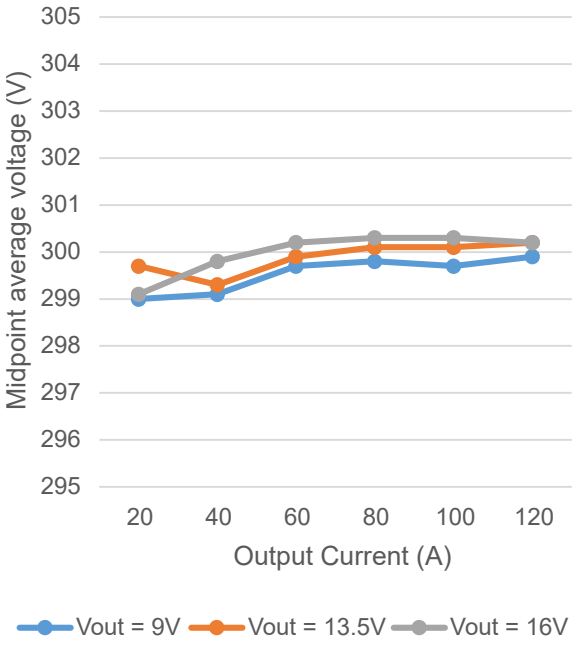


Figure 2-20. Midpoint voltage at 600V_{in}

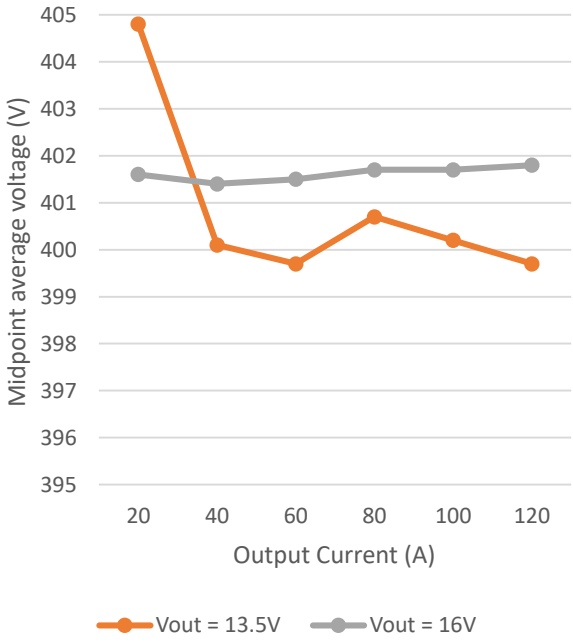


Figure 2-21. Midpoint voltage at 800V_{in}

3 Waveforms

3.1 Switching

Switching behavior of Secondary MOSFET is shown in Figure 3-1 through Figure 3-24. The test condition is room temperature.

CH1: Vgs of Secondary MOSFET

CH2: Vds of Secondary MOSFET

CH3: Differential voltage of transformer primary winding

CH4: Current waveform of transformer primary winding

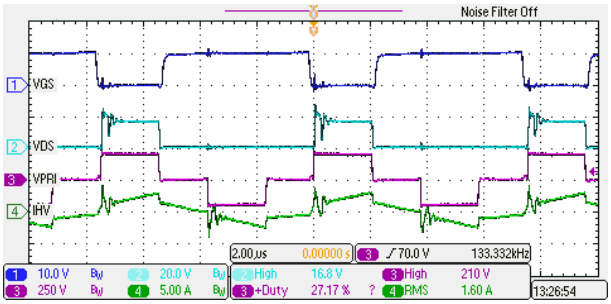


Figure 3-1. Switching at 400V_{in}, 9V_{out}, 20A Load

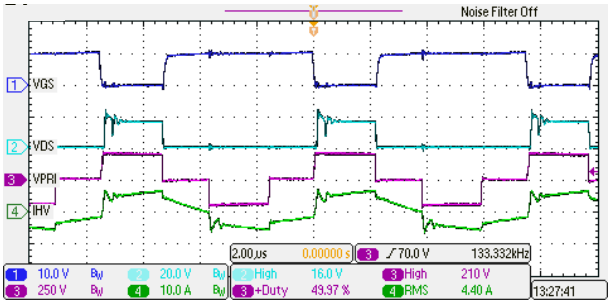


Figure 3-2. Switching at 400V_{in}, 9V_{out}, 60A Load

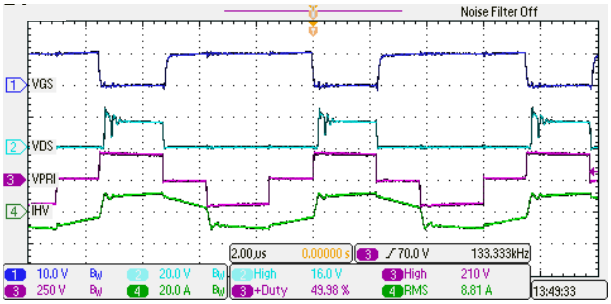


Figure 3-3. Switching at 400V_{in}, 9V_{out}, 120A Load

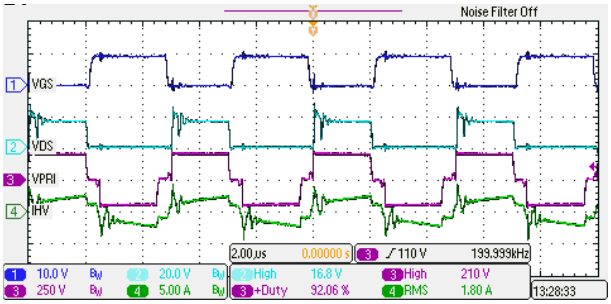


Figure 3-4. Switching at 400V_{in}, 13.5V_{out}, 20A Load

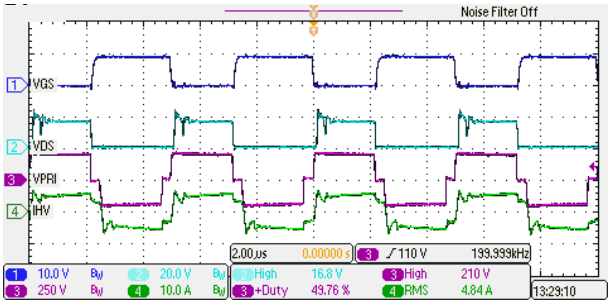


Figure 3-5. Switching at 400V_{in}, 13.5V_{out}, 60A Load

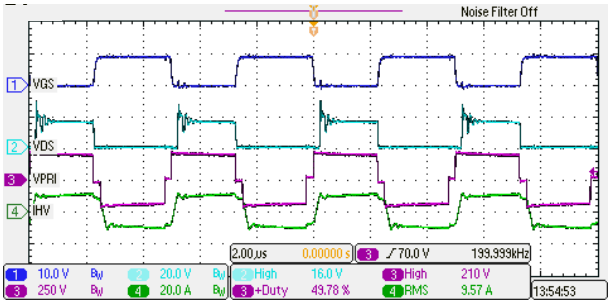


Figure 3-6. Switching at 400V_{in}, 13.5V_{out}, 120A Load

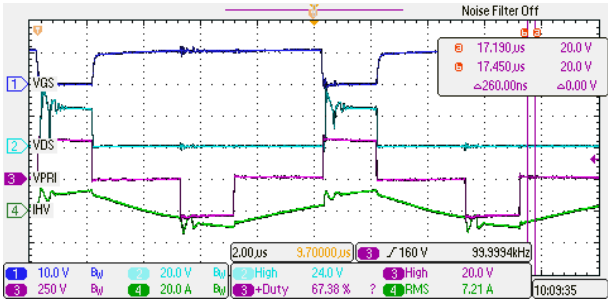


Figure 3-7. Switching at 600V_{in}, 9V_{out}, 20A Load

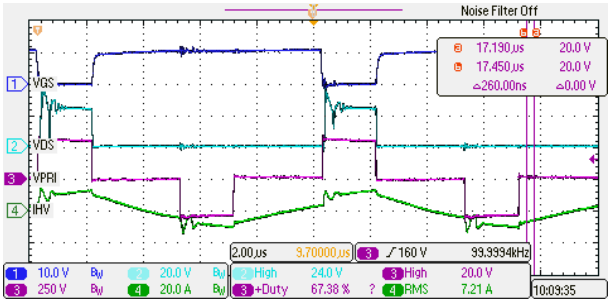


Figure 3-8. Switching at 600V_{in}, 9V_{out}, 120A Load

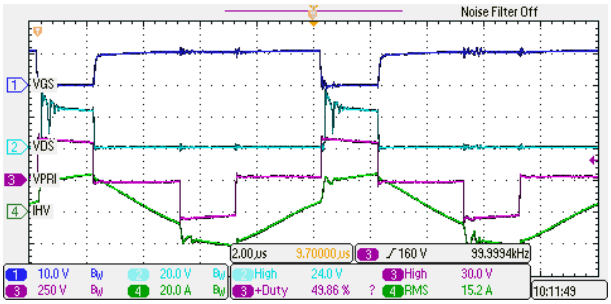


Figure 3-9. Switching at 600V_{in}, 9V_{out}, 250A Load

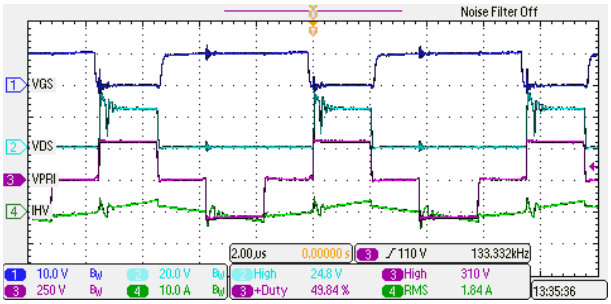


Figure 3-10. Switching at 600V_{in}, 13.5V_{out}, 20A Load

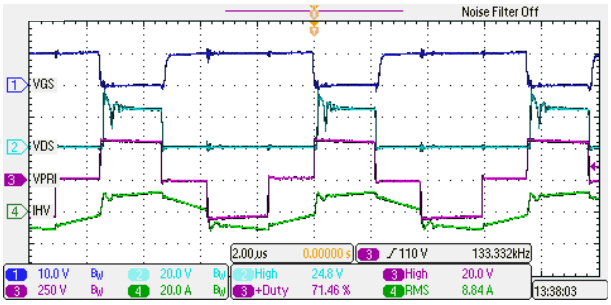


Figure 3-11. Switching at 600V_{in}, 13.5V_{out}, 120A Load

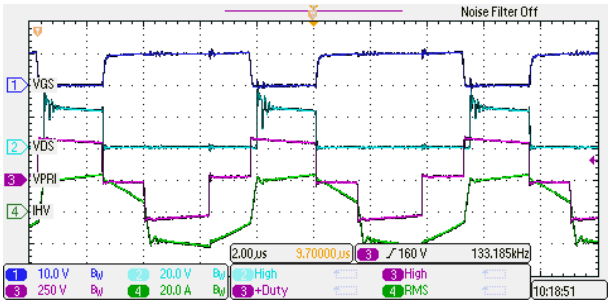


Figure 3-12. Switching at 600V_{in}, 13.5V_{out}, 250A Load

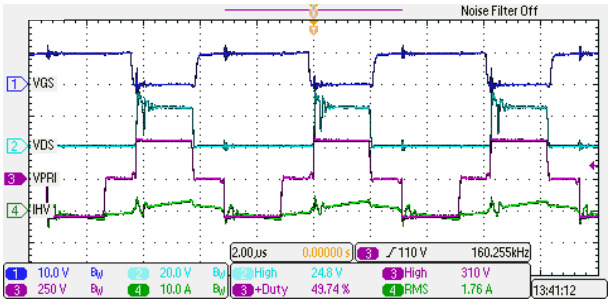


Figure 3-13. Switching at 600V_{in}, 16V_{out}, 20A Load

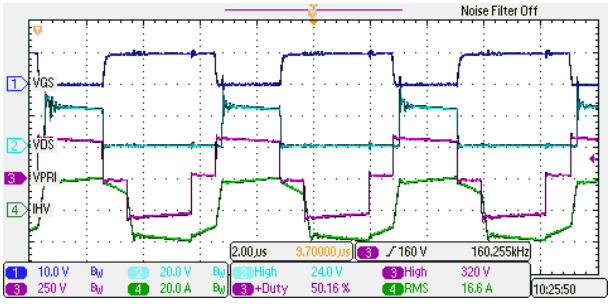


Figure 3-14. Switching at 600V_{in}, 16V_{out}, 120A Load

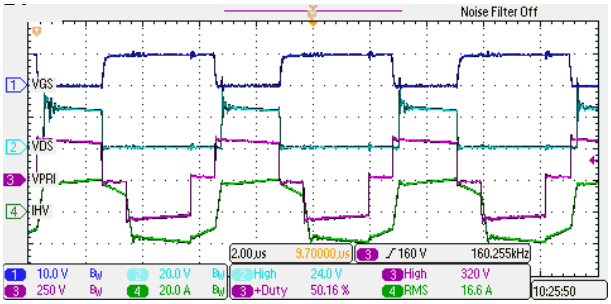


Figure 3-15. Switching at 600V_{in}, 16V_{out}, 250A Load

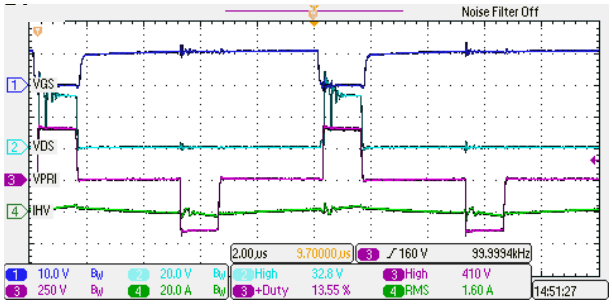


Figure 3-16. Switching at 800V_{in}, 9V_{out}, 20A Load

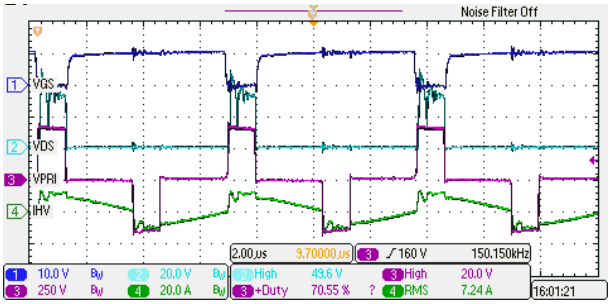


Figure 3-17. Switching at 800V_{in}, 9V_{out}, 120A Load

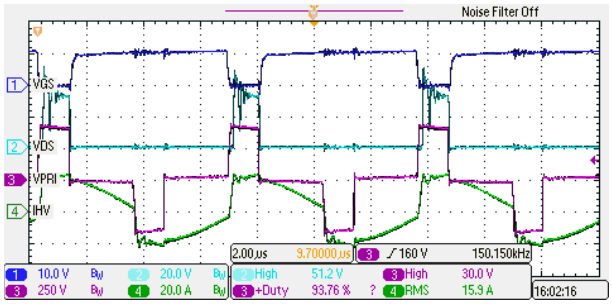


Figure 3-18. Switching at 800V_{in}, 9V_{out}, 250A Load

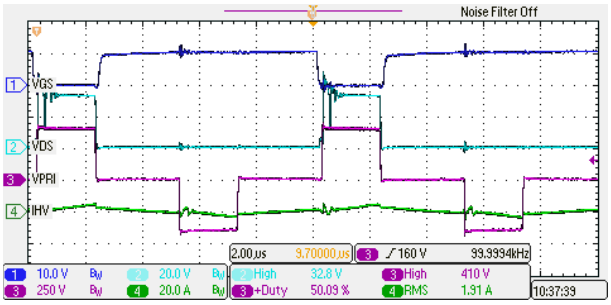


Figure 3-19. Switching at 800V_{in}, 13.5V_{out}, 20A Load

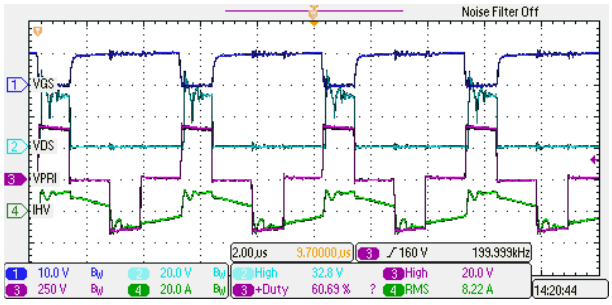


Figure 3-20. Switching at 800V_{in}, 13.5V_{out}, 120A Load

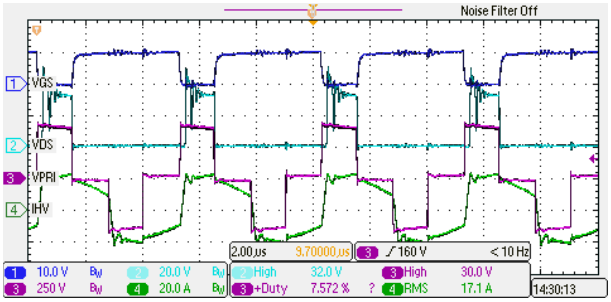


Figure 3-21. Switching at 800V_{in}, 13.5V_{out}, 250A Load

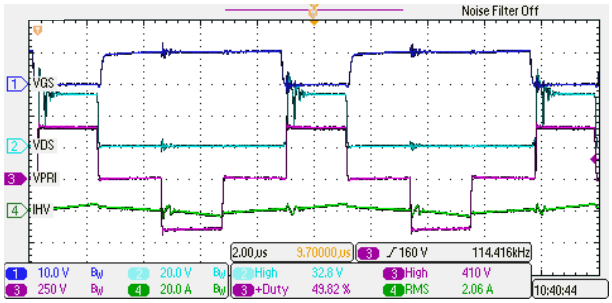


Figure 3-22. Switching at 800V_{in}, 16V_{out}, 20A Load

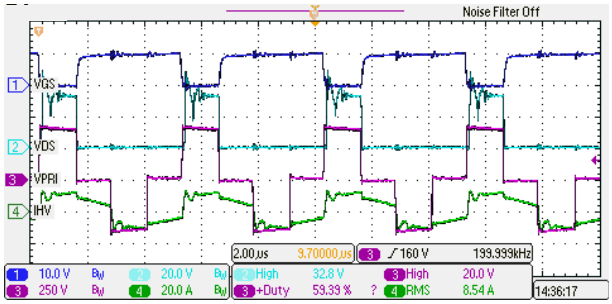


Figure 3-23. Switching at 800V_{in}, 16V_{out}, 120A Load

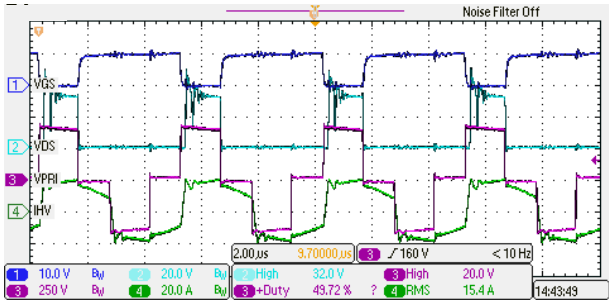


Figure 3-24. Switching at 800V_{in}, 16V_{out}, 250A Load

3.2 Output Voltage Ripple

Output voltage ripple is shown in Figure 3-25 through Figure 3-30. The test condition is room temperature.

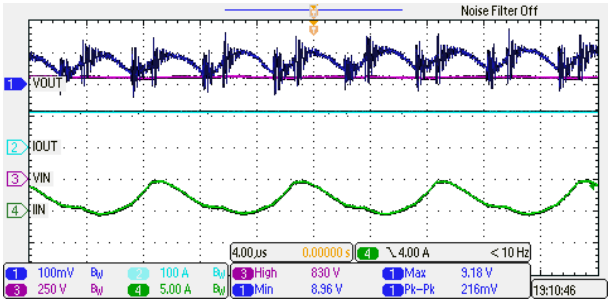


Figure 3-25. Output Voltage Ripple at 400V_{in}, 9V_{out}, 20A Load

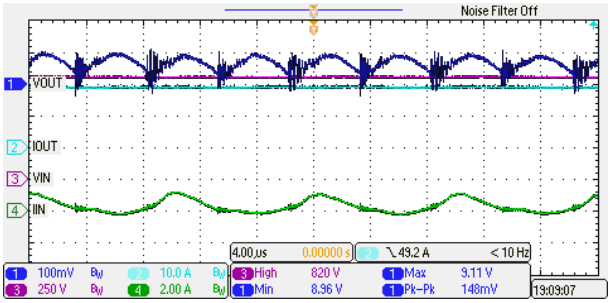


Figure 3-26. Output Voltage Ripple at 400V_{in}, 9V_{out}, 120A Load

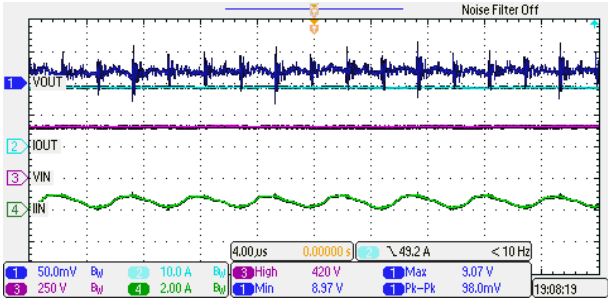


Figure 3-27. Output Voltage Ripple at 600V_{in}, 9V_{out}, 20A Load

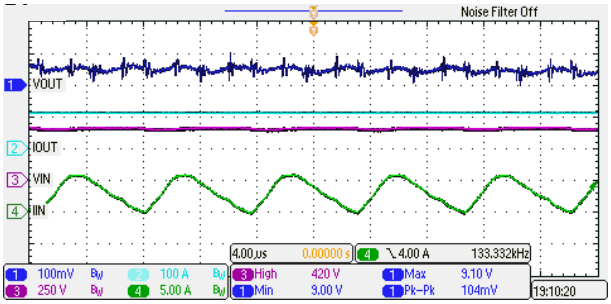


Figure 3-28. Output Voltage Ripple at 600V_{in}, 9V_{out}, 120A Load

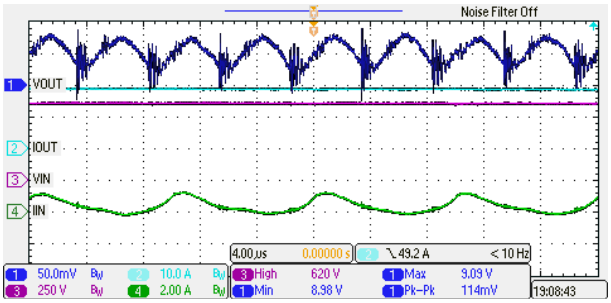


Figure 3-29. Output Voltage Ripple at 800V_{in}, 9V_{out}, 20A Load

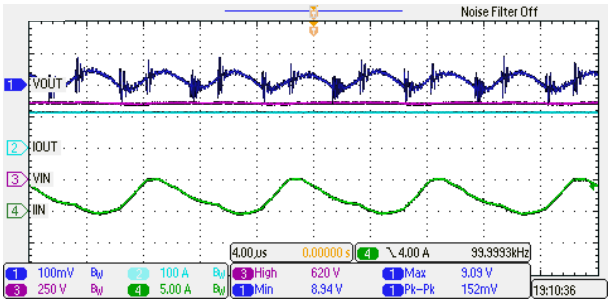


Figure 3-30. Output Voltage Ripple at 800V_{in}, 9V_{out}, 120A Load

3.3 Turn ON and OFF

Turn ON and OFF behavior is shown in Figure 3-31 through Figure 3-34. The test condition is 800V_{in}, 13.5V_{out}, room temperature.

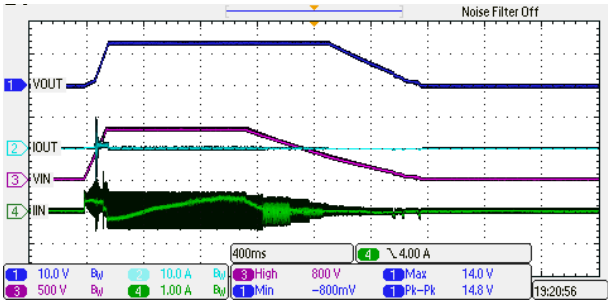


Figure 3-31. Turn On and Off at 0A

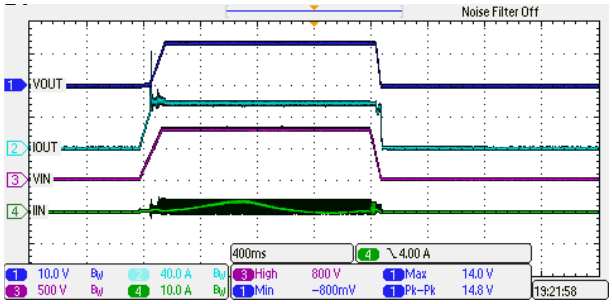


Figure 3-32. Turn On and Off at 60A

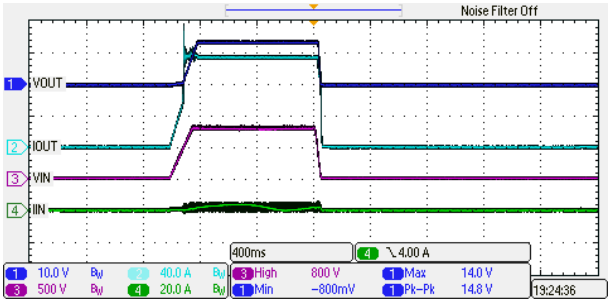


Figure 3-33. Turn On and Off at 120A

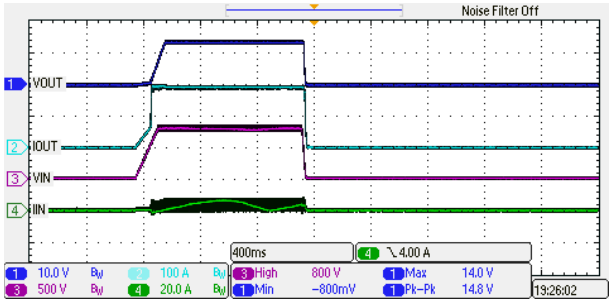


Figure 3-34. Turn On and Off at 200A

3.4 Load Transients

Load transient response is shown in Figure 3-35 through Figure 3-38. The test condition is 600V_{in}, 13.5V_{out}, 20A to 120A, room temperature.

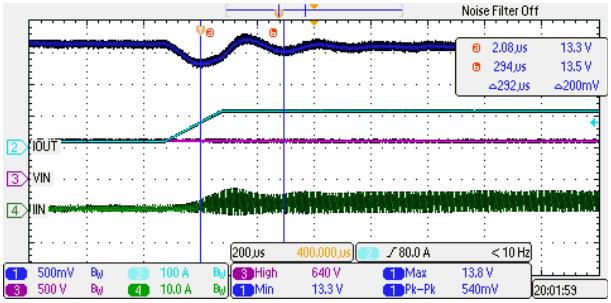


Figure 3-35. Load Transient On at 0.5A/µs

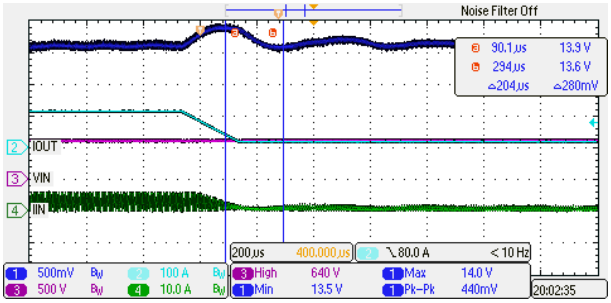


Figure 3-36. Load Transient Off at 0.5A/µs

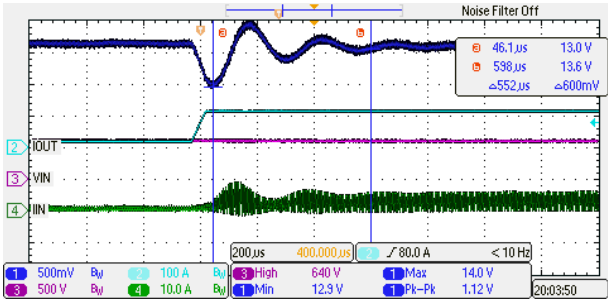


Figure 3-37. Load Transient On at 2A/µs

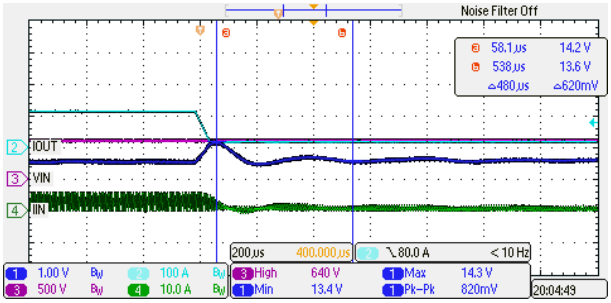


Figure 3-38. Load Transient Off at 2A/µs

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