Test Report: PMP23468

48V Input, 875W Peak Power, Multiphase Buck Converter Reference Design for Audio Systems

Description

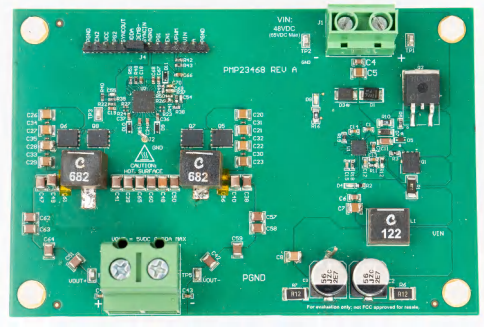
This reference design provides protection and power for automotive audio systems. Operation with a 48VDC input was tested across the full output voltage range: 6VDC to 35VDC. The design exhibits a peak efficiency of 97% at nominal load, and no significant output voltage undershoot and overshoot for loaded transitions between 6VDC and 35VDC. This test report includes operational data spanning the output voltage range and load, including bode plots, switching waveforms, load transient responses, start-up and shutdown waveforms, and thermal images.

Features

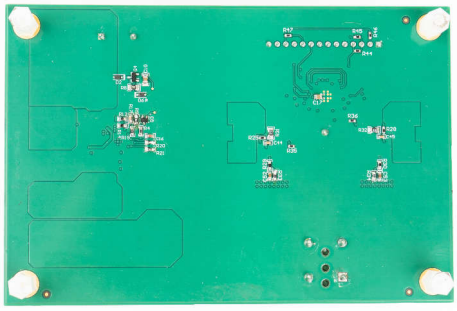
- Able to provide 245W continuous power, and 875W peak power
- Variable output voltage during operation across a 6V to 35V range
- Design done with a simple two-phase converter, controlled by a single controller, LM5143A-Q1
- Back-to-back diodes controlled by LM74930-Q1 with overvoltage and reverse voltage protection
- No significant output voltage overshoot or undershoot for 6V to 35V V_{OUT} transition
- Peak efficiency of 97% at nominal load

Applications

- Premium audio
- Software-defined vehicle



Top Photo



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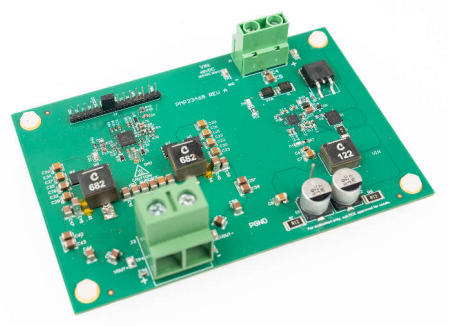

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1 Test Prerequisites

This section provides the testing guide used in the detailed testing of the power supply.

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	36VDC to 54VDC Use J1 onboard (Phoenix Contact 1714971, 9.52mm, 2 x 1, TH)
V_{OUT}	6VDC to 35VDC (adjustable)
I_{OUT}	9A, maximum continuous; 25A, maximum peak Use J3 onboard (Eaton EM292902-UL, 10.16mm, 2x1, Tin, R/A, TH)
F_{SW}	400kHz, nominal
Various Signals	Connect a conductor (jumper) from the J4 pin 7 (DEMB) to pin 6 (VDDA) for two-phase operation Connect the positive of a function generator to J4 pin 11 (VPWM), and the negative to J4 pin 14 for output voltage control

1.2 Required Equipment

- Power supply able to support 48V, 12A, and 600W, such as HP 6030A
- Electronic load able to support 35V, 14A, and 500W, such as Kikusui PLZ603WH
- Function generator to apply a variable duty cycle PWM signal, such as Tektronix AFG3102
- Oscilloscope such as Tektronix MDO34 with TPP0500B 10 × voltage probes and 30A TCP0030A current probes
- Digital multimeters such as Fluke 87iii or 87V
- For bode plots, Vector Network Analyzer such as Bode 100 from OMICRON Lab
- Thermal camera such as FLIR E75
- Keysight 34970 data acquisition, switch unit along with calibrated 10A current shunts for efficiency measurements
- A fan for cooling of the board if sustained high-current testing is desired

1.3 Considerations

When testing at 12A load and above for a sustained period of time, or when testing at 20A to 25A of transient load, use a fan to maintain safety.

1.4 Dimensions

The dimensions of the board are 5.20 inches by 3.45 inches.

2 Testing and Results

2.1 Efficiency Graphs

The efficiency and associated power losses of the system are shown in Figure 2-1 and Figure 2-2 respectively. These measurements were taken with an input voltage of 48V across the output voltage range and up to the expected nominal load (7A).

According to Figure 2-1, when operating at the nominal load of 7A, the efficiency can range from 90%, when the output voltage is 6V, to 97%, when the output voltage is 35V. The peak efficiency measured is 97.2% with an output voltage of 35V and a load of 9A.

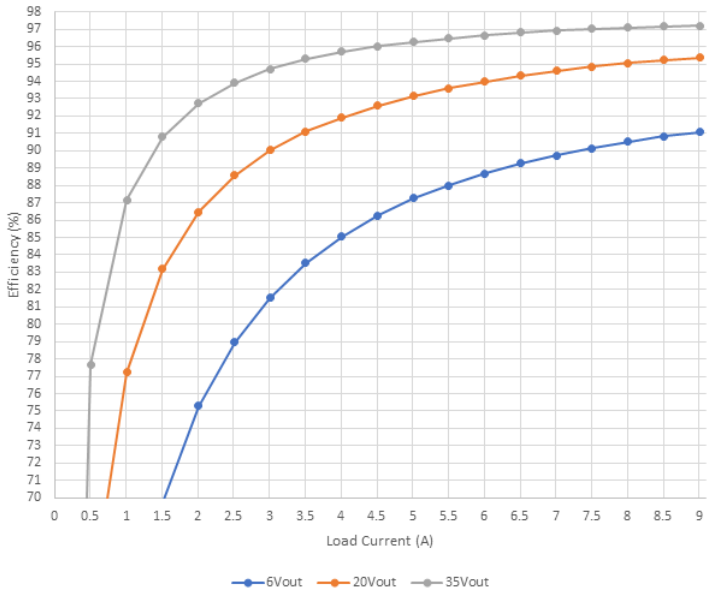

Figure 2-1. Efficiency at 6, 20, and 35V_{OUT} from 0A to 9A

According to Figure 2-2, when operating at the nominal load of 7A, the expected power losses range from 5W, when the output voltage is 6V; to 8W, when the output voltage is 20V. This can be compared to the no load losses that range from 4.25W, when the output voltage is 6V; to 5.75W, when the output voltage is 20V.

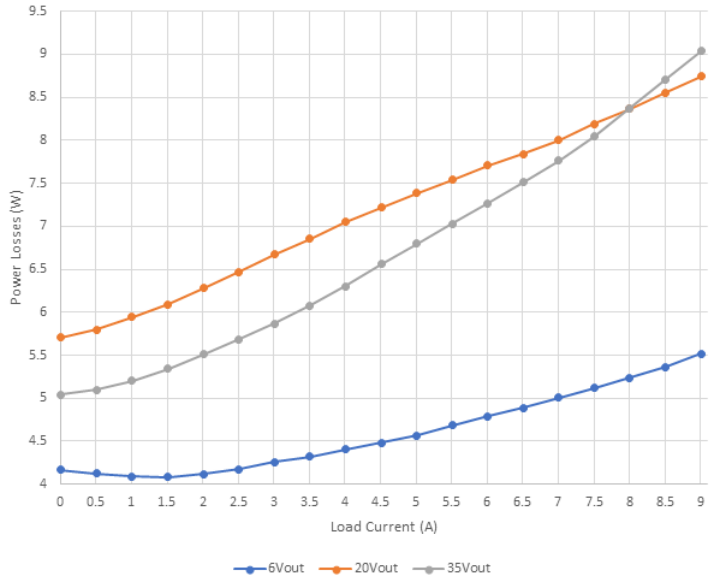

Figure 2-2. Power Losses at 6, 20, and 35V_{OUT} from 0A to 9A

2.2 Efficiency Data

This section details the efficiency data at output voltages of 6V, 20V, and 35V, from 0A to 9A of load.

Table 2-1. Efficiency Data for 6V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
48.717	0.086	6.248	0.002	4.180	0.011	4.169	0.270
48.714	0.150	6.246	0.507	7.291	3.166	4.125	43.420
48.712	0.213	6.247	1.008	10.384	6.295	4.089	60.620
48.710	0.277	6.247	1.508	13.505	9.422	4.083	69.770
48.707	0.342	6.245	2.010	16.668	12.550	4.118	75.290
48.705	0.407	6.246	2.509	19.845	15.672	4.173	78.970
48.703	0.473	6.243	3.008	23.037	18.781	4.256	81.530
48.700	0.538	6.243	3.508	26.217	21.898	4.319	83.530
48.698	0.604	6.243	4.009	29.429	25.027	4.402	85.040
48.696	0.670	6.244	4.508	32.633	28.149	4.484	86.260
48.693	0.736	6.245	5.008	35.840	31.273	4.567	87.260
48.691	0.802	6.243	5.508	39.073	34.387	4.686	88.010
48.688	0.868	6.241	6.006	42.275	37.488	4.787	88.680
48.686	0.934	6.242	6.506	45.497	40.611	4.886	89.260
48.684	1.001	6.243	7.005	48.731	43.727	5.003	89.730
48.681	1.067	6.242	7.505	51.963	46.846	5.117	90.150
48.679	1.134	6.242	8.005	55.200	49.964	5.236	90.510
48.676	1.201	6.243	8.505	58.455	53.092	5.363	90.830
48.674	1.268	6.240	9.006	61.716	56.198	5.518	91.060

Table 2-2. Efficiency Data for 20V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
48.715	0.118	20.005	0.002	5.741	0.034	5.707	0.600%
48.708	0.327	20.006	0.507	15.950	10.151	5.799	63.640%
48.700	0.536	20.005	1.008	26.106	20.161	5.945	77.230%
48.693	0.744	20.006	1.507	36.251	30.157	6.094	83.190%
48.685	0.954	20.004	2.008	46.456	40.176	6.281	86.480%
48.678	1.164	20.007	2.508	56.644	50.177	6.467	88.580%
48.670	1.373	20.006	3.007	66.832	60.163	6.669	90.020%
48.663	1.582	20.004	3.507	77.004	70.153	6.851	91.100%
48.655	1.793	20.004	4.008	87.229	80.181	7.049	91.920%
48.647	2.002	20.005	4.508	97.406	90.186	7.220	92.590%
48.640	2.211	20.006	5.007	107.560	100.176	7.383	93.140%
48.633	2.421	20.005	5.508	117.724	110.184	7.540	93.600%
48.625	2.630	20.005	6.006	127.866	120.160	7.706	93.970%
48.617	2.839	20.005	6.507	138.001	130.160	7.841	94.320%
48.610	3.048	20.005	7.005	148.142	140.142	8.000	94.600%
48.602	3.258	20.004	7.506	158.331	150.139	8.192	94.830%

Table 2-2. Efficiency Data for 20V Output (continued)

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
48.595	3.467	20.003	8.004	168.461	160.097	8.363	95.040%
48.587	3.677	20.003	8.504	178.668	170.115	8.554	95.210%
48.580	3.888	20.001	9.006	188.875	180.132	8.743	95.370%

Table 2-3. Efficiency Data for 35V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
48.716	0.104	34.995	0.001	5.090	0.048	5.042	0.949
48.703	0.469	34.994	0.508	22.864	17.764	5.100	77.696
48.690	0.832	34.994	1.009	40.499	35.295	5.205	87.148
48.677	1.194	34.992	1.508	58.101	52.756	5.345	90.801
48.664	1.558	34.995	2.009	75.811	70.300	5.512	92.730
48.651	1.921	34.993	2.508	93.450	87.768	5.682	93.920
48.637	2.285	34.995	3.008	111.129	105.265	5.864	94.723
48.624	2.649	34.995	3.506	128.789	122.709	6.080	95.279
48.611	3.015	34.993	4.008	146.563	140.261	6.302	95.700
48.598	3.381	34.992	4.508	164.291	157.732	6.559	96.008
48.585	3.746	34.994	5.007	182.006	175.208	6.798	96.265
48.572	4.113	34.992	5.508	199.755	192.727	7.028	96.482
48.559	4.478	34.992	6.007	217.452	210.187	7.265	96.659
48.545	4.845	34.994	6.506	235.178	227.665	7.514	96.805
48.532	5.210	34.993	7.004	252.864	245.099	7.764	96.929
48.519	5.578	34.993	7.505	270.659	262.613	8.046	97.027
48.506	5.947	34.995	8.004	288.452	280.082	8.370	97.098
48.492	6.316	34.993	8.504	306.298	297.591	8.708	97.157
48.479	6.687	34.993	9.005	324.162	315.128	9.034	97.213

2.3 Thermal Images

The thermal images in Figure 2-3, Figure 2-4, Figure 2-5, and Figure 2-6 were taken with an input voltage of 48V, an output voltage of 35V, and a load of 8.57A to achieve a total output power of 300W.

Both of the power stage inductors, L2 and L3, as seen in Figure 2-4 and Figure 2-5, experienced a rise of 57°C and 54°C respectively above the ambient room temperature of 23°C. Similarly, the power stage controller (U2), as seen in Figure 2-6, experienced a 50°C rise above that 23°C ambient temperature.

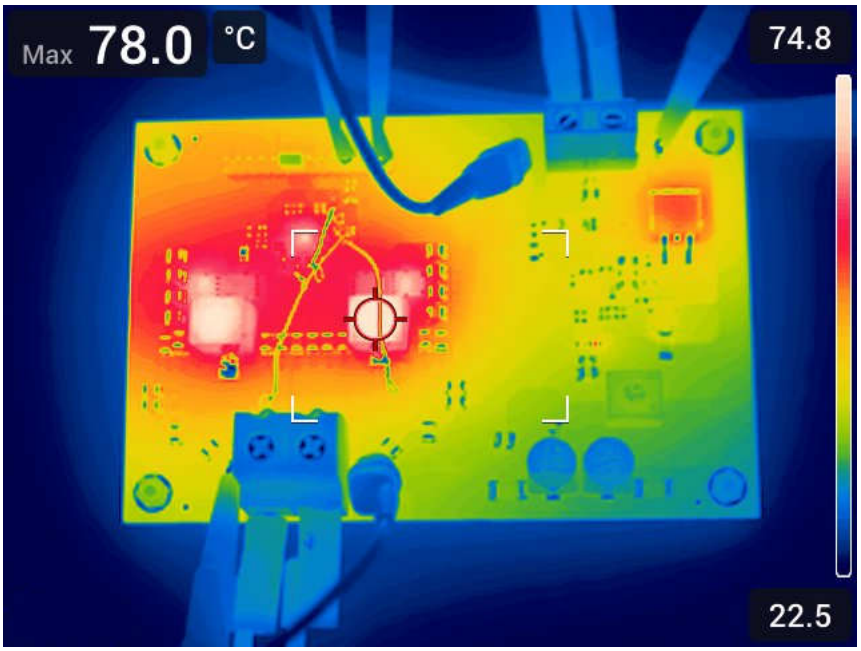

Figure 2-3. Board Overview

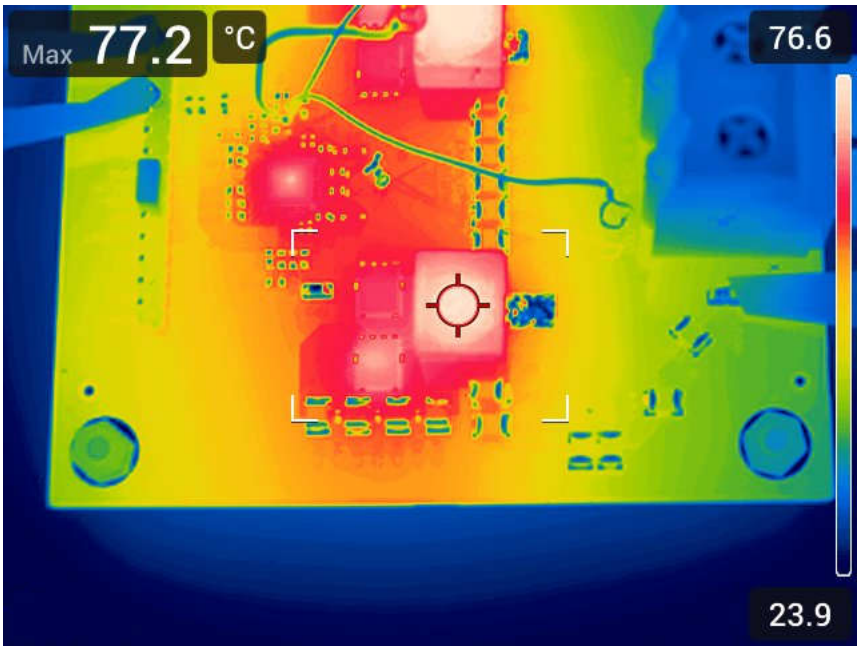

Figure 2-4. L3 Temperature

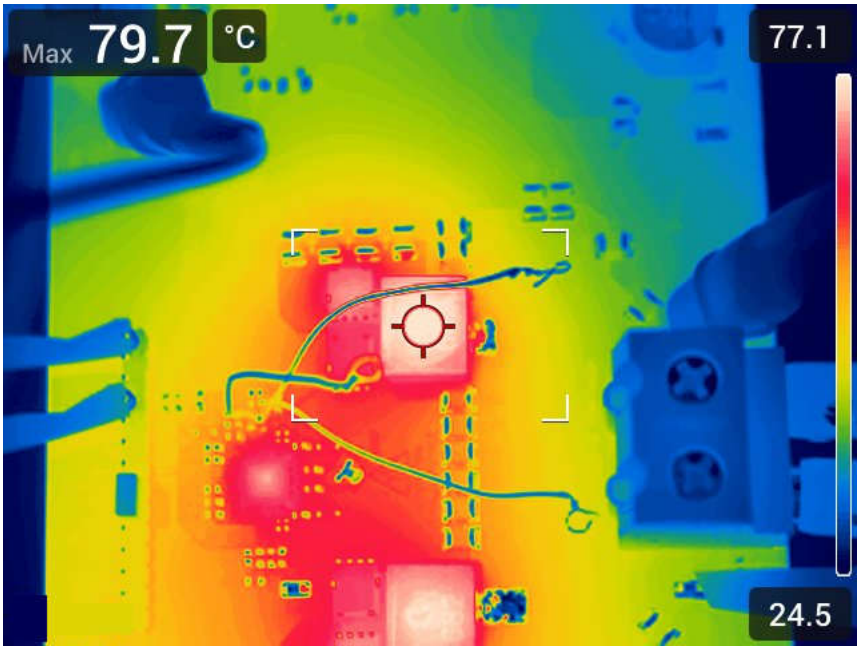

Figure 2-5. L2 Temperature

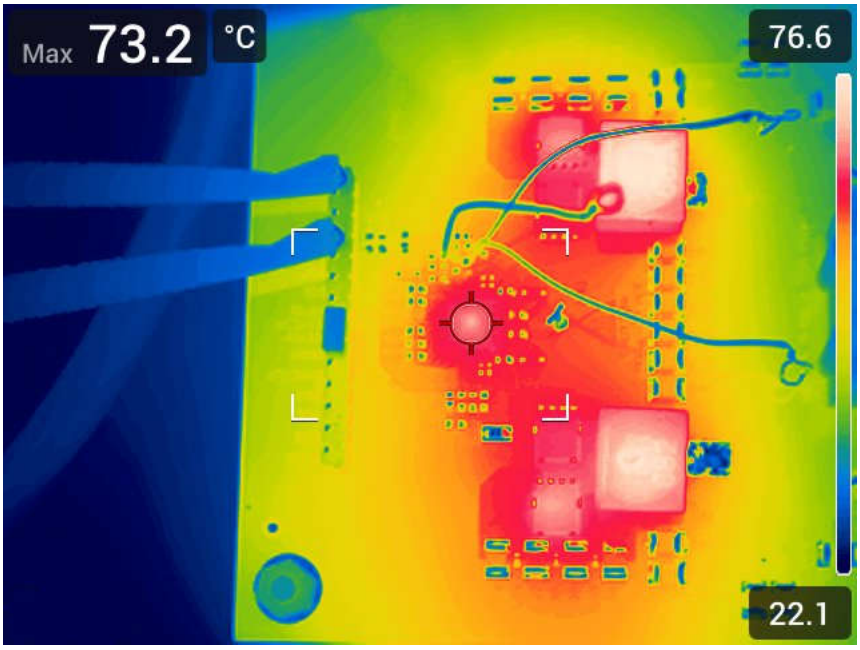

Figure 2-6. U2 Temperature

2.4 Bode Plots

Each bode plot is shown at 48V input, with different output voltage and loading conditions.

Figure 2-7 show a bode plot where the output voltage is set to 20V and is connected to a 2.5Ω load for 8A of output current. Figure 2-8 shows a bode plot where the output voltage is set to 35V and is connected to a 5Ω load for 7A of output current.

Crossover frequency increases as output voltage increases from 19.240kHz at $20V_{OUT}$, to 30.325kHz at $35V_{OUT}$, but the phase margin is always at least 55 degrees, and gain margin is always above 10dB.

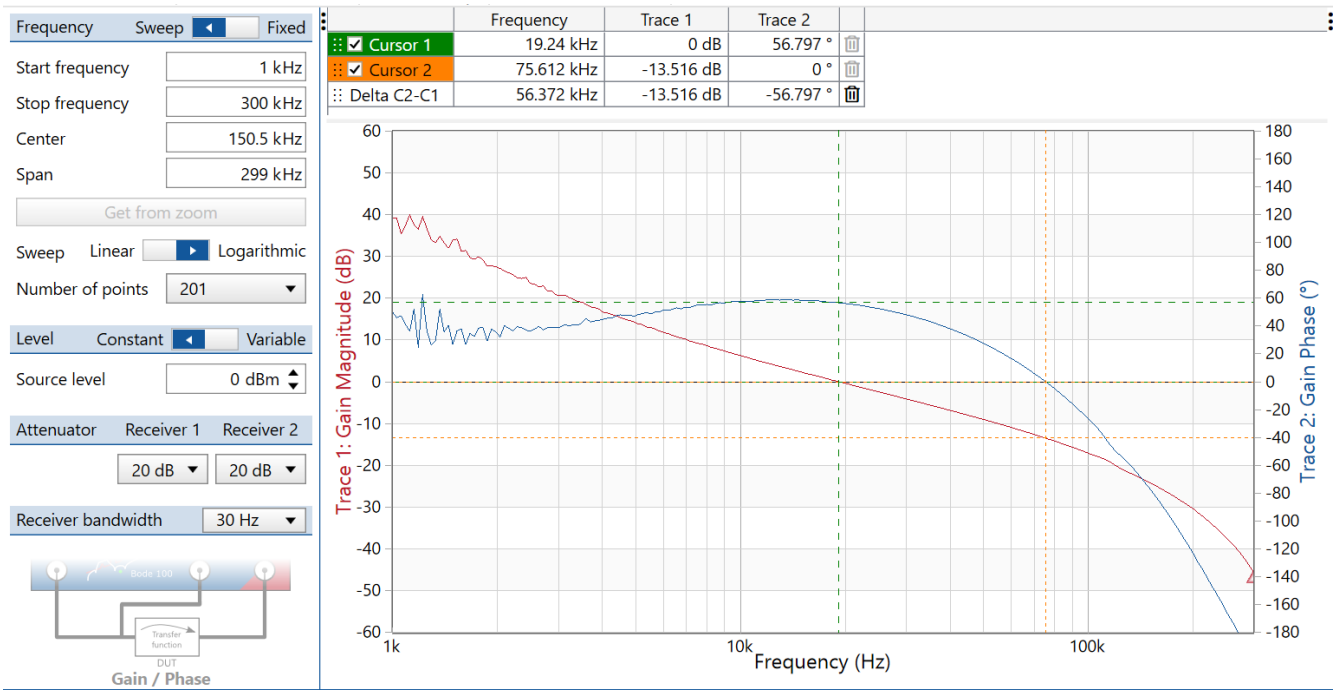

Figure 2-7. $20V_{OUT}$, 2.5Ω Load Bode Plot

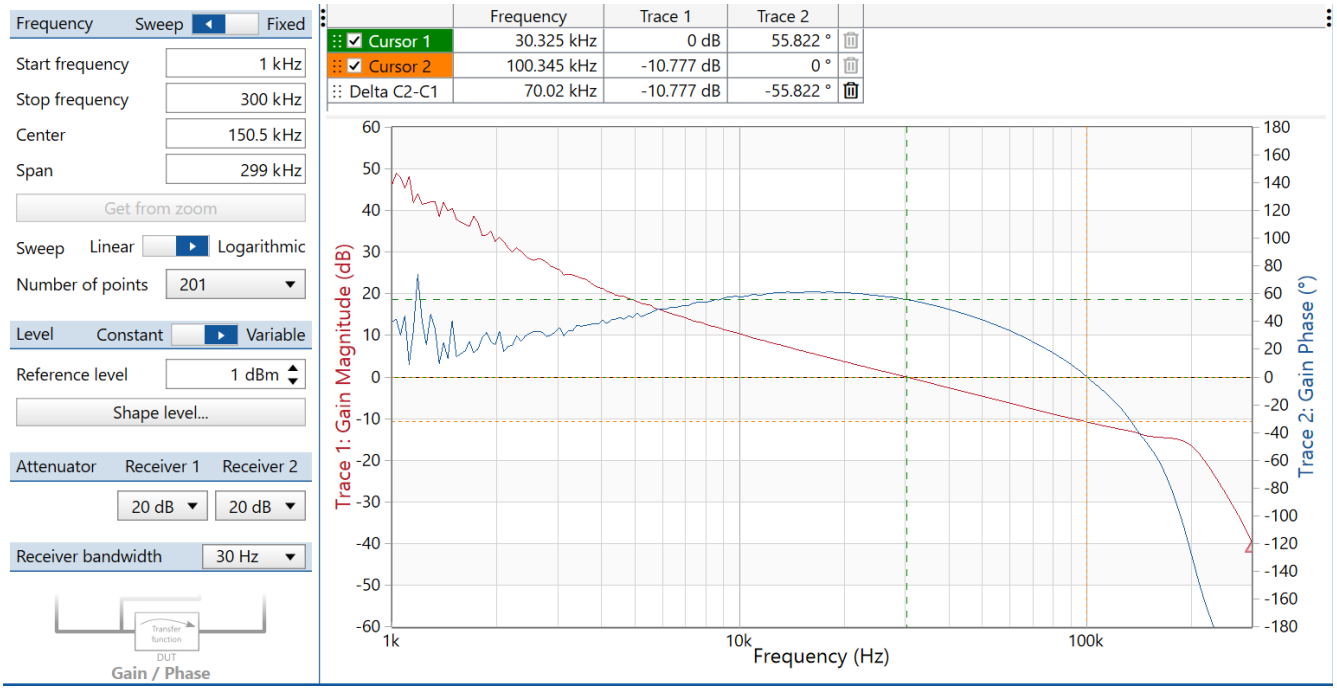

Figure 2-8. $35V_{OUT}$, 2.5Ω Load Bode Plot

2.5 PWM Duty Cycle Versus Output Voltage

Table 2-4 lists out the duty cycle of the PWM signal for various output voltages. A limitation on the accuracy of this measurement, is the quality of the PWM signal emitted from the function generator. Therefore, these measurements can vary depending on the PWM applied.

Table 2-4. PWM Duty Cycles

D_{PWM} (%)	V_{OUT} (V)
0	35.108
0.05	33.649
0.1	32.189
0.15	30.730
0.2	29.270
0.25	27.811
0.3	26.351
0.35	24.892
0.4	23.432
0.45	21.973
0.5	20.513
0.55	19.054
0.6	17.594
0.65	16.135
0.7	14.675
0.75	13.216
0.8	11.756
0.85	10.297
0.9	8.837
0.95	7.378
1	5.918

3 Waveforms

3.1 Switching

Figure 3-1 and Figure 3-2 show the switching waveforms across different output voltages, but all use an input voltage of 48V, and a resistive load of 2.5Ω. These signals were measured at the source pins of the high-side power stage FETs (Q5 and Q6) but only one waveform is shown, as operation is similar across the FETs. Additionally, a tip and barrel probe was used for this measurement, with the tip at the source pins of the FET and the barrel at the GND of the nearby input capacitors.

Figure 3-1 was taken with an output voltage of 6V and has an overshoot of 3.2V above the 48V input voltage, while Figure 3-2 with an output voltage of 20V has an overshoot of 2.8V above of the 48V input voltage. This is well within the 60V drain-to-source voltage rating of the FET.

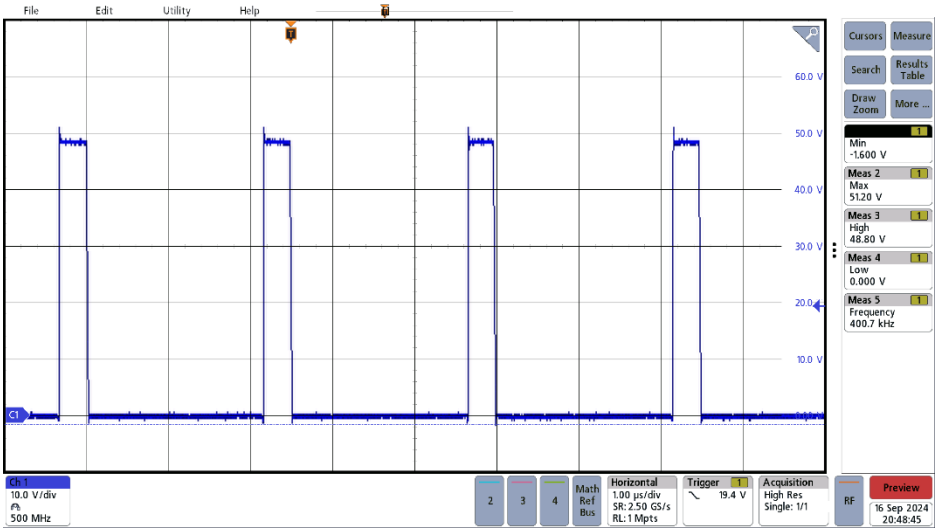

Figure 3-1. $6V_{OUT}$ Switching Waveform

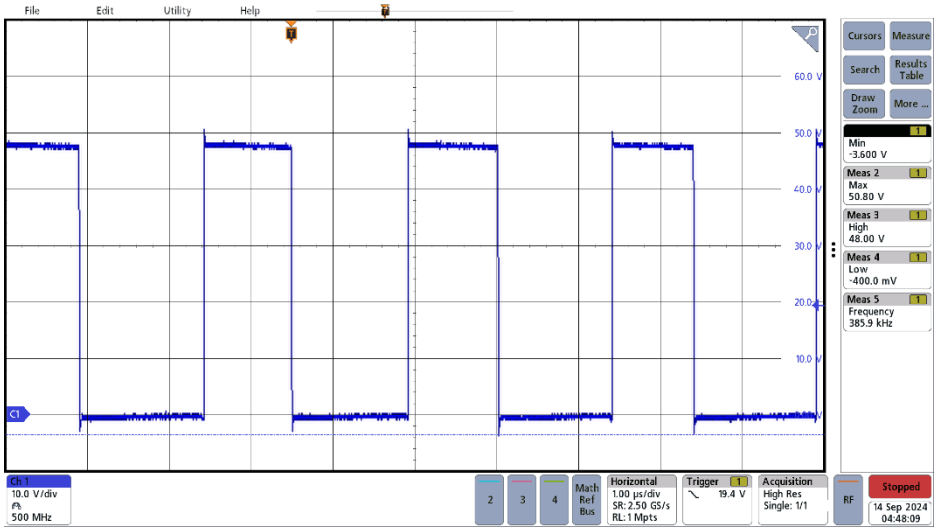

Figure 3-2. $20V_{OUT}$ Switching Waveform

3.2 Output Voltage Transitions

Figure 3-3 and Figure 3-4 show how the output voltage transitions from 6V to 35V and from 35V to 6V respectively with an input voltage of 48V, and with a 2.5Ω load. No significant overshoot was observed.

The PWM signal is included in the measurements on channel 1 to show what is triggering this voltage change. Although the PWM signal looks as though the signal transitions from a constant 3.3V to a constant 0V, this is a product of the 1ms timescale that is used to show the output voltage transition. In reality, the *constant 3.3* portion just has a very high duty cycle, while the *constant 0* has a very low duty cycle.

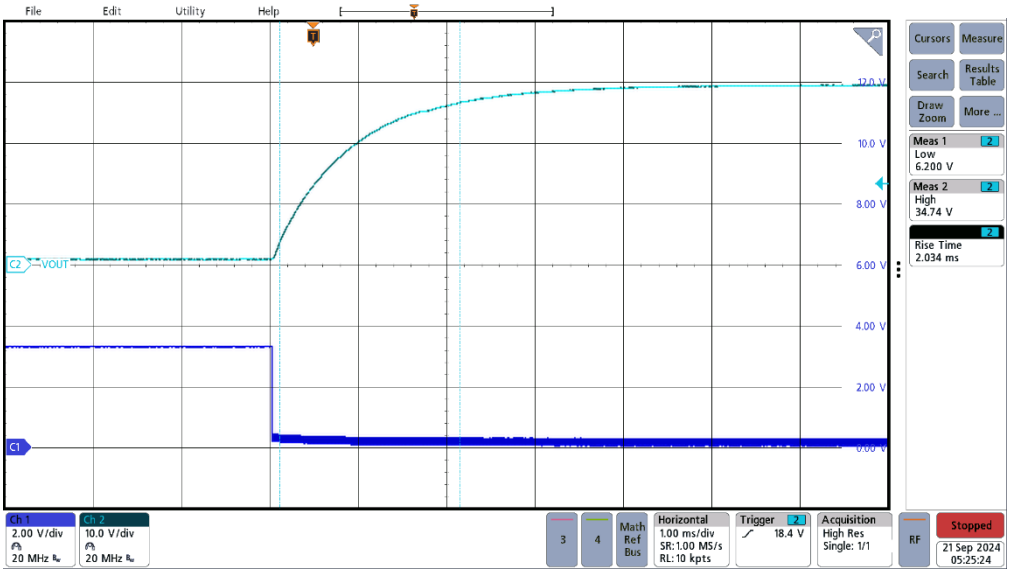

Figure 3-3. 6V to 35V_{OUT} Transition With 2.5Ω Load

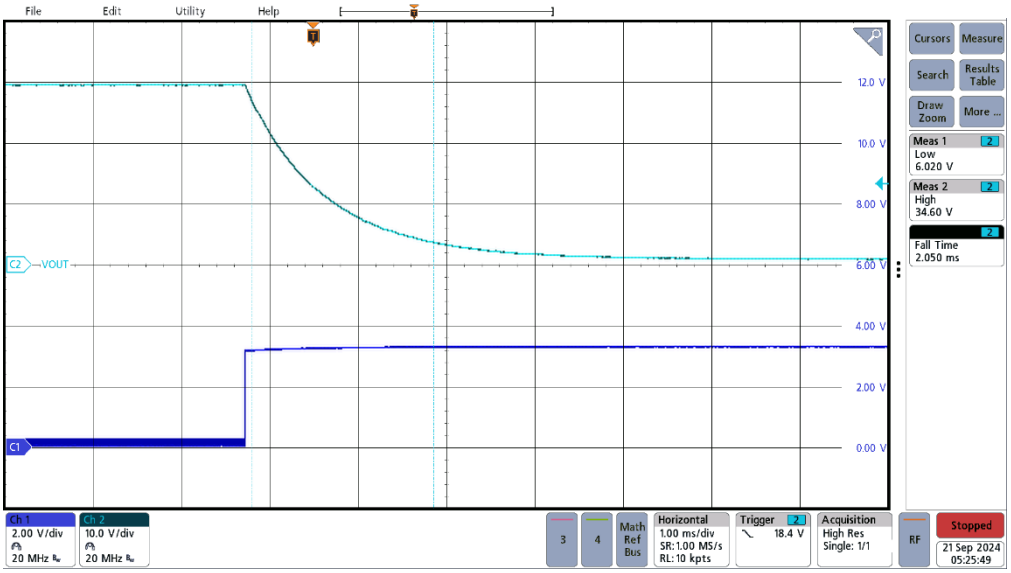

Figure 3-4. 35V to 6V_{OUT} Transition with 2.5Ω Load

3.3 Load Transients

Figure 3-5 and Figure 3-6 show how the system responds to a load step from 0Ω to 2.5Ω where the input voltage is 48V, the output voltage is 20V and 35V respectively.

Figure 3-5, with a 20V output voltage, experiences an 8A increase in current as a load is applied, and this results in an undershoot of 150mV or 0.75%. Figure 3-6, with a 35V output voltage, experiences a 14A increase in current as a load is applied, and this results in an undershoot of 250mV or 0.7%.

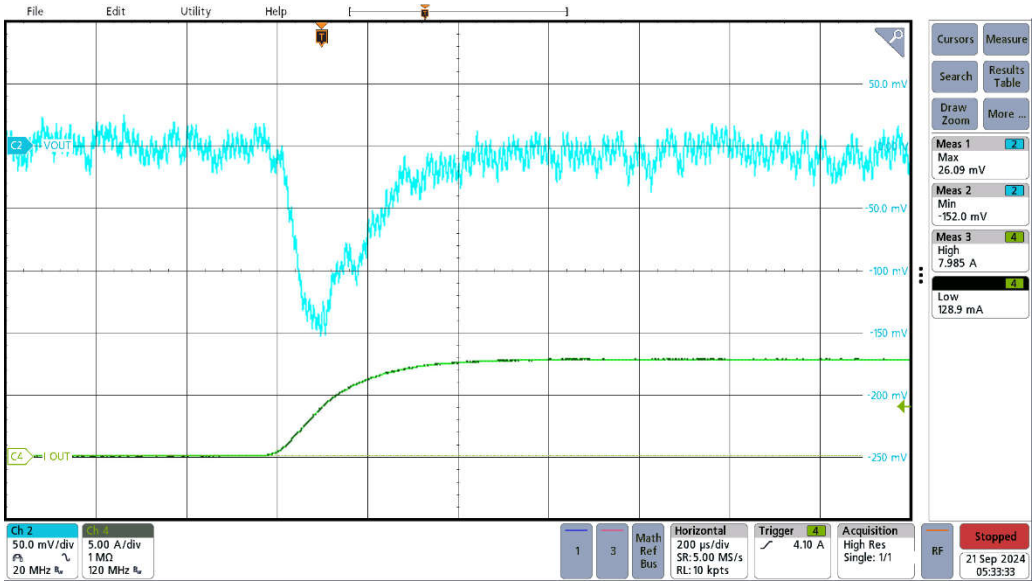

Figure 3-5. 20V$_{OUT}$, 2.5Ω Load Step

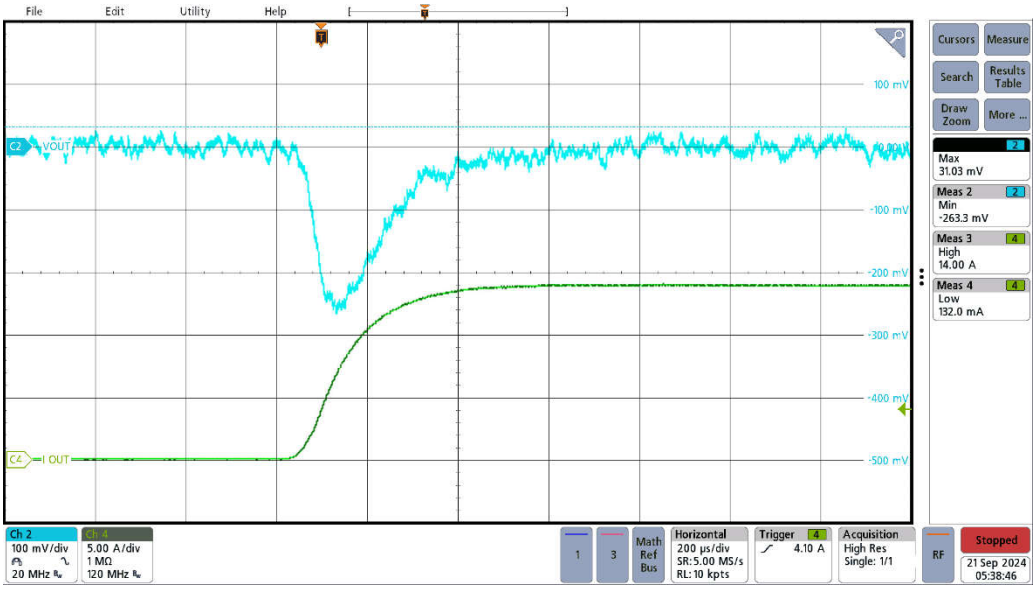

Figure 3-6. 35V$_{OUT}$, 2.5Ω Load Step

Figure 3-7 and Figure 3-8 show how the system responds to a load dump from 2.5Ω to 0Ω where the input voltage is 48V, and the output voltage is 20V and 35V respectively.

Figure 3-7, with a 20V output voltage, experiences an 8A decrease in current as the load is disconnected, and this results in an overshoot of 330mV or 1.65%. Figure 3-8, with a 35V output voltage, experiences a 14A decrease in current as the load is disconnected, and this results in an overshoot of 550mV or 1.57%.

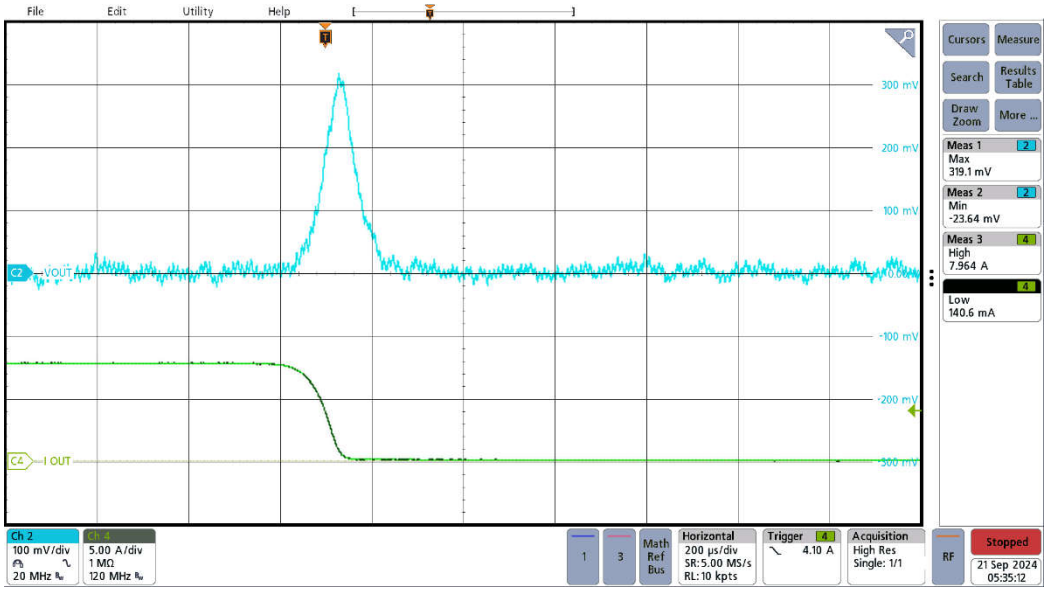

Figure 3-7. 20V_{OUT}, 2.5Ω Load Dump

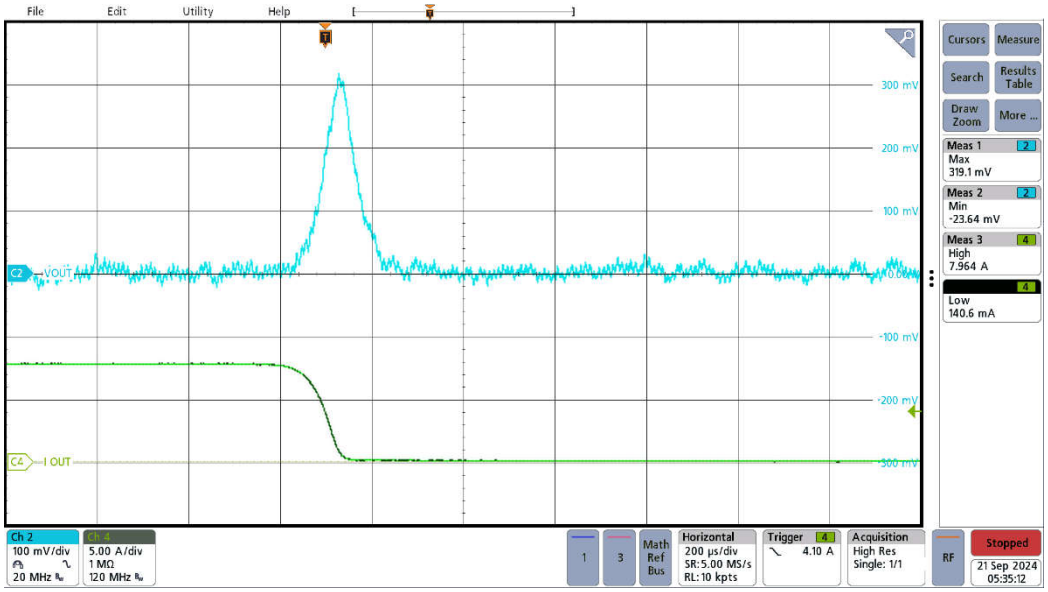

Figure 3-8. 35V_{OUT}, 2.5Ω Load Dump

3.4 High Current Load Transients

Figure 3-9 shows how the system responds to a load transient that starts at a nominal 7.5A, and in-line with audio applications, jumps up to 25A for a brief period. Operation is completed with 48V at the input, and 35V at the output, such that the system jumps from a nominal 262W of power to 875W of power.

On the load step from 7.5A to 25A, an undershoot of 1.47V, or 4.20%, is present; while on the load dump from 25A to 7.5A, an overshoot of 1.3V, or 3.71%, is present.

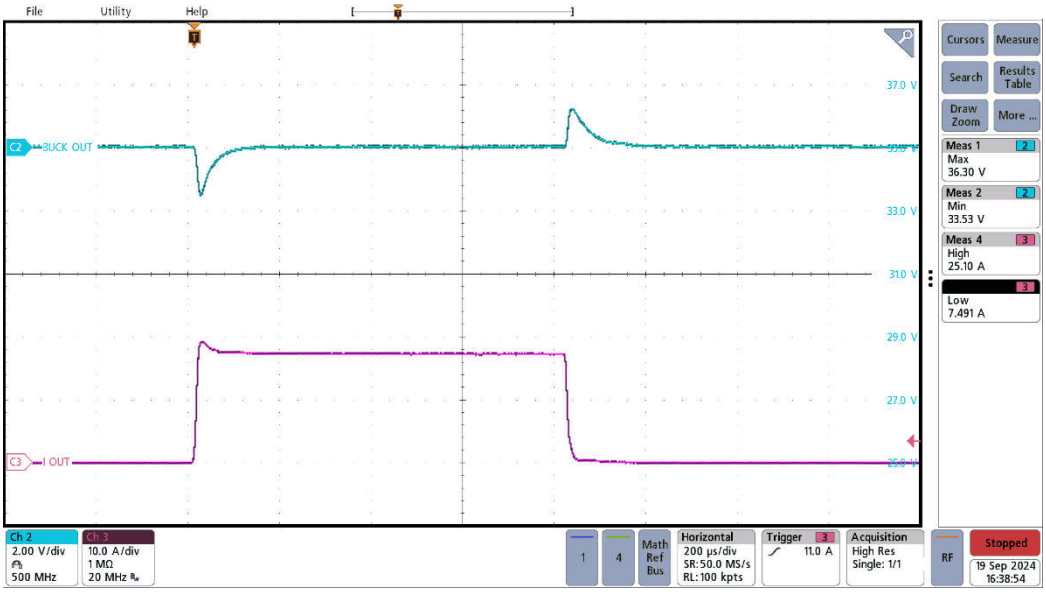

Figure 3-9. 7.5A to 25A Load Transient at 35V_{OUT}

3.5 Start-up and Shutdown Sequences

Figure 3-10 and Figure 3-11 show the start-up waveforms with an input voltage of 48V, a load of 2.5Ω, and at an output voltage of 6V and 20V respectively.

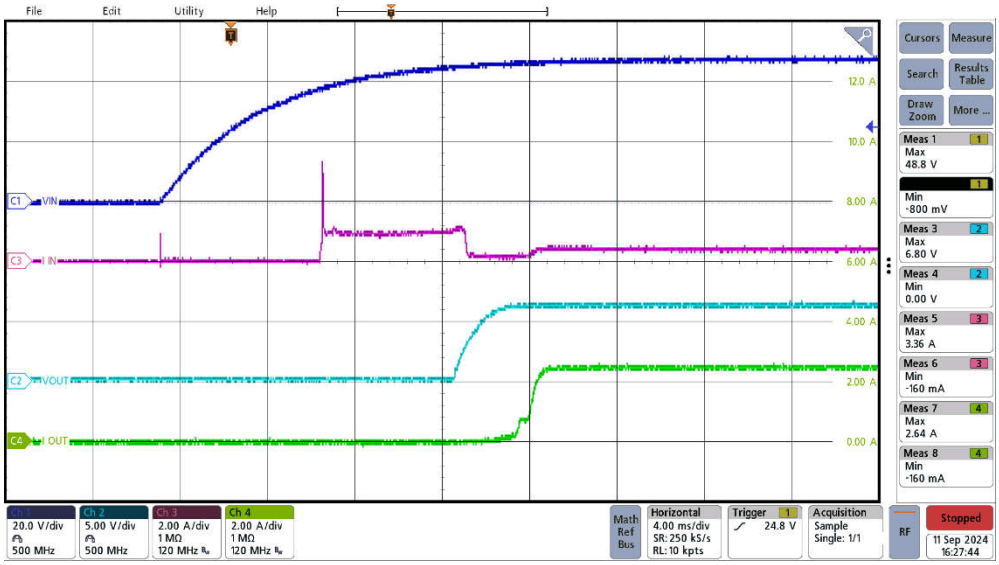

Figure 3-10. 6V_{OUT} Start-Up

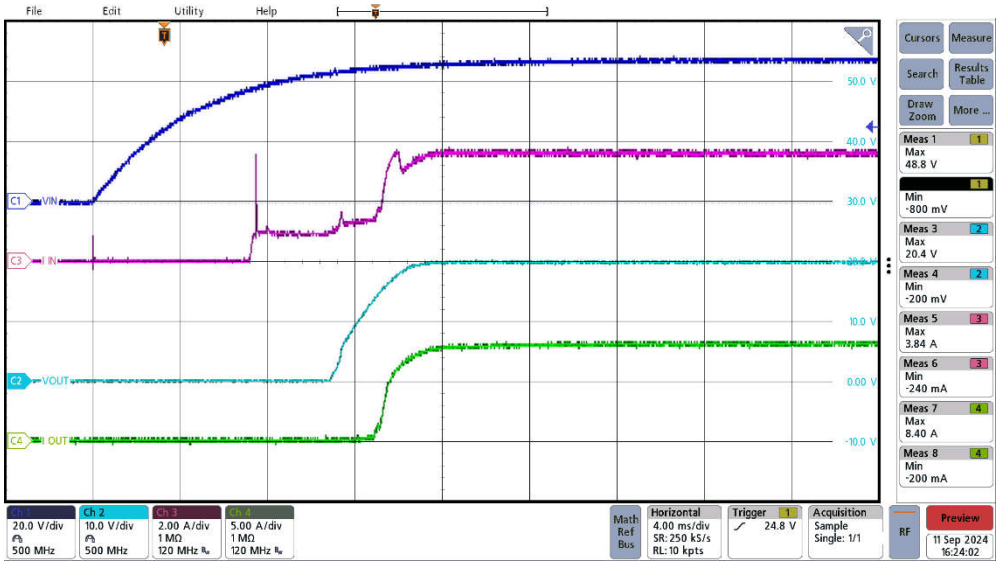

Figure 3-11. 20V_{OUT} Start-Up

Figure 3-12 shows shutdown waveforms with an input voltage of 48V, a load of 2.5Ω, at an output voltage of 6V.

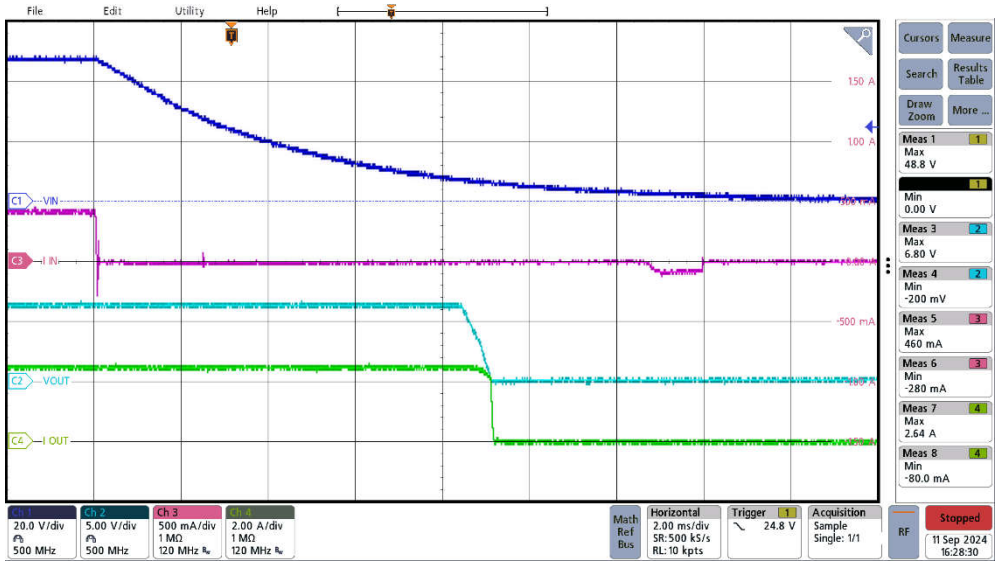

Figure 3-12. 6V_{OUT} Shutdown

3.6 Overvoltage Protection

Figure 3-13 and Figure 3-14 show one of the protection features of the front-end of this design, overvoltage protection. The LM74930-Q1 is set to an overvoltage clamp configuration, where LM74930-Q1 retries passing through the input voltage until the capacitor on the TMR pin is charged up, then falls to 0V.

Figure 3-13 shows operation at 55V of input voltage, while Figure 3-14 shows operation at 57V of input voltage. At the higher input voltage, the hysteresis frequency is more apparent.

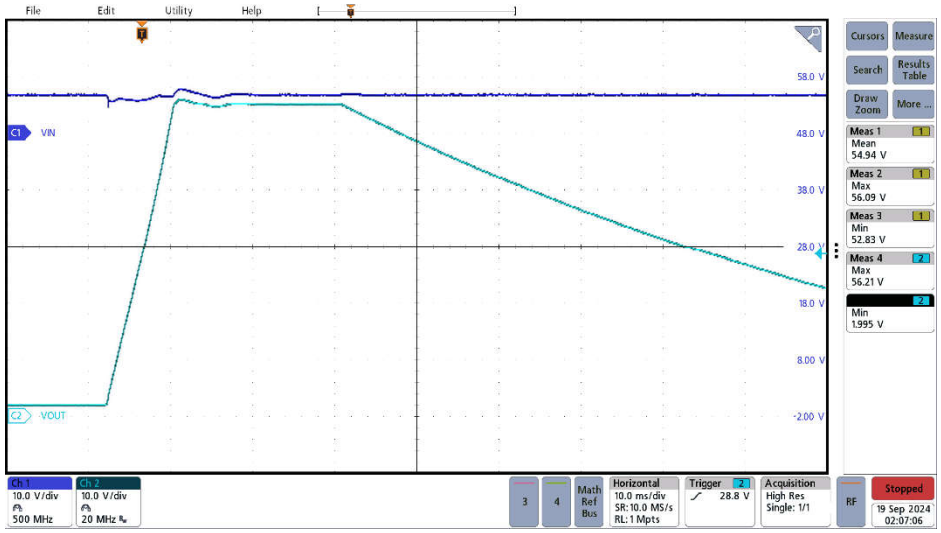

Figure 3-13. Overvoltage Protection at $55V_{IN}$

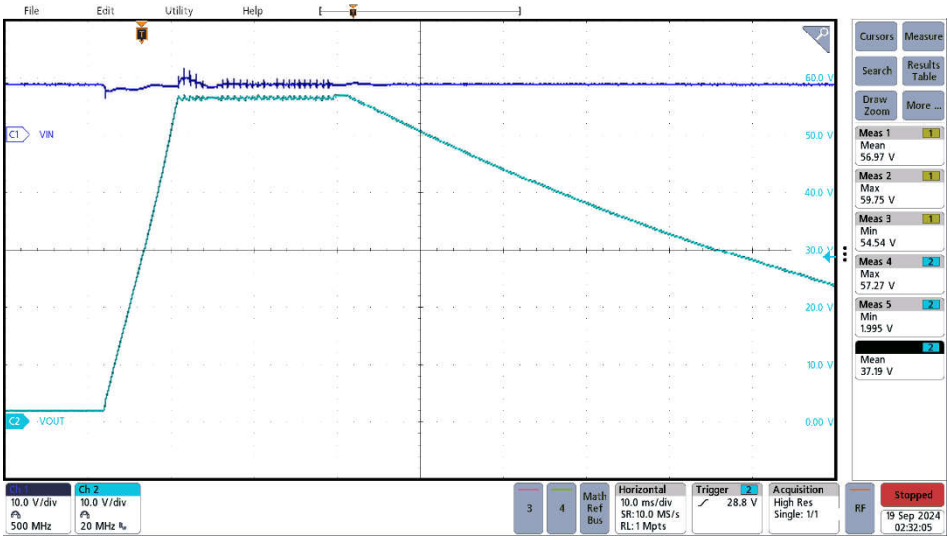

Figure 3-14. Overvoltage Protection at $57V_{IN}$

Figure 3-15 shows the frequency at which the system retries start-up after the input voltage has been completely blocked. This measurement shows operation at 57V, but is similar across input voltage.

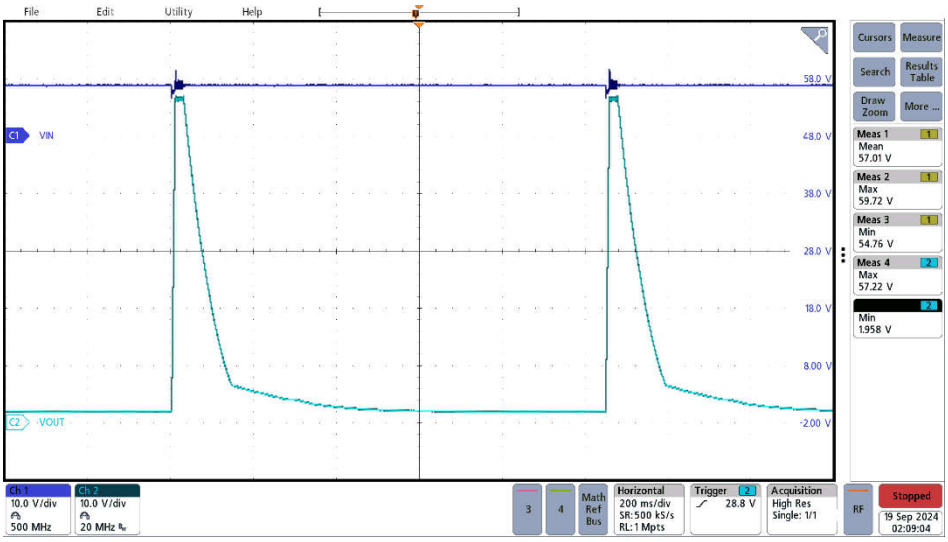

Figure 3-15. Overvoltage Protection at 57V_{IN} – Zoomed Out

3.7 Reverse Voltage Protection

Figure 3-16 shows the reverse voltage protection provided by the design up to -48V of input voltage results in no voltage at V_{OUT}.

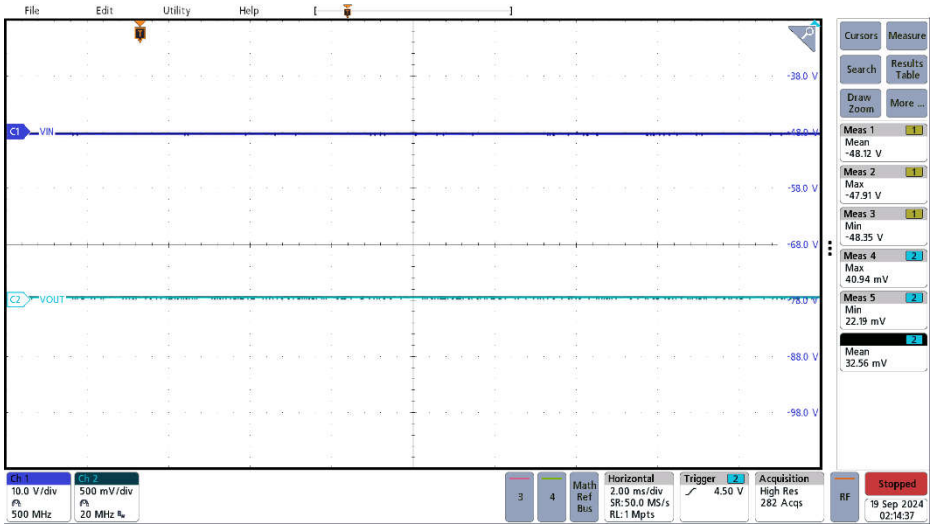

Figure 3-16. Reverse Voltage Protection at -48V_{IN}

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