Test Report: PMP23340C2K

48 V–12 V GaN-Enabled 1.1 kW 1/8th Brick Power Module Reference Design Using C2000™

Description

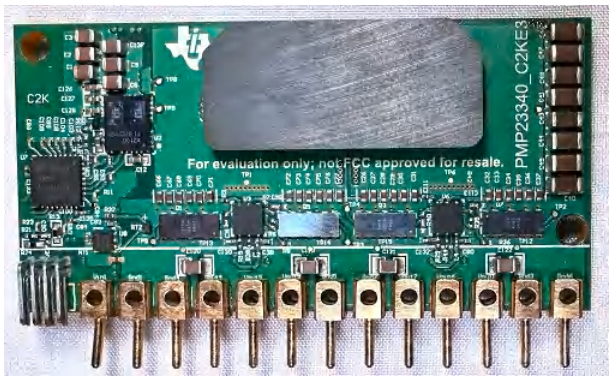
This reference design is a 1.1-kW, high-density, 48-V to 12-V open-loop bus converter. The design achieves 97.7% efficiency and is implemented with TI's high-performance gallium nitride (GaN) switches. An integrated printed wiring board (PWB) transformer is utilized to minimize size and maximize efficiency. The control is implemented with a F2800157QRHBRQ1 high-performance microcontroller in a 32-pin QFN package.

Features

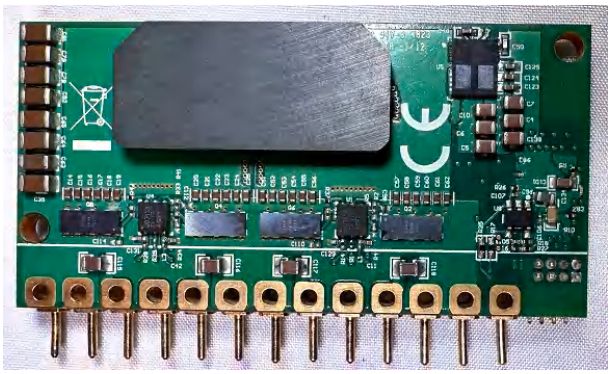
- Efficiency 97.7%
- 1-MHz switching frequency
- Power density 1300 W/in^3 (without connector)
- Total thickness without heat sink 10 mm

Applications

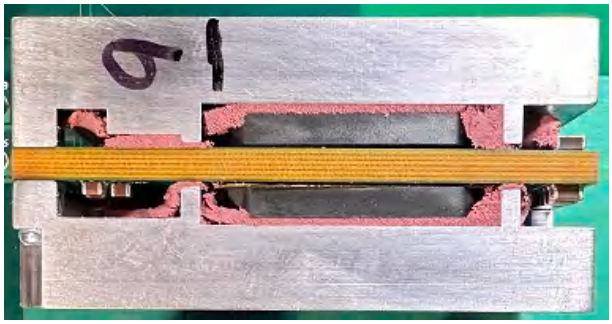
- High performance computing
- Merchant DC/DC
- Brick power modules



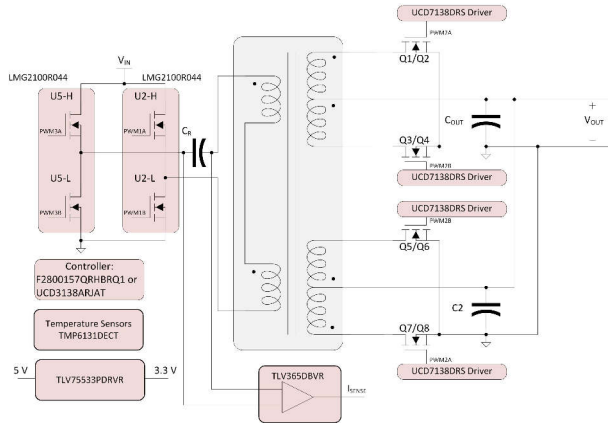
Top Side Photo



Bottom Side Photo



Side View Photo of Final Assembly



Simplified Schematic

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	40 V–60 V
V_{OUT}	10 V–15 V
Maximum Power	1.1 kW
Switching Frequency	1 MHz

1.2 Dimensions

The board dimensions are 22.9 mm × 58.4 mm. An additional 6.5 mm is reserved for a card edge connector. The total thickness of the design without the heat sink is 10.16 mm.

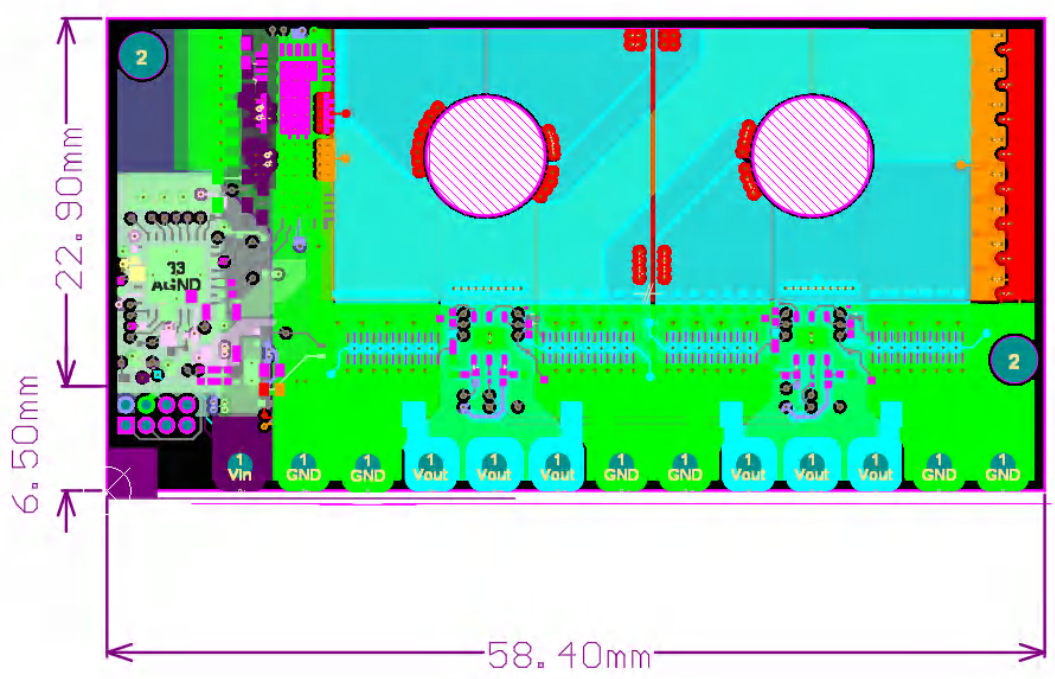


Figure 1-1. Board Dimensions

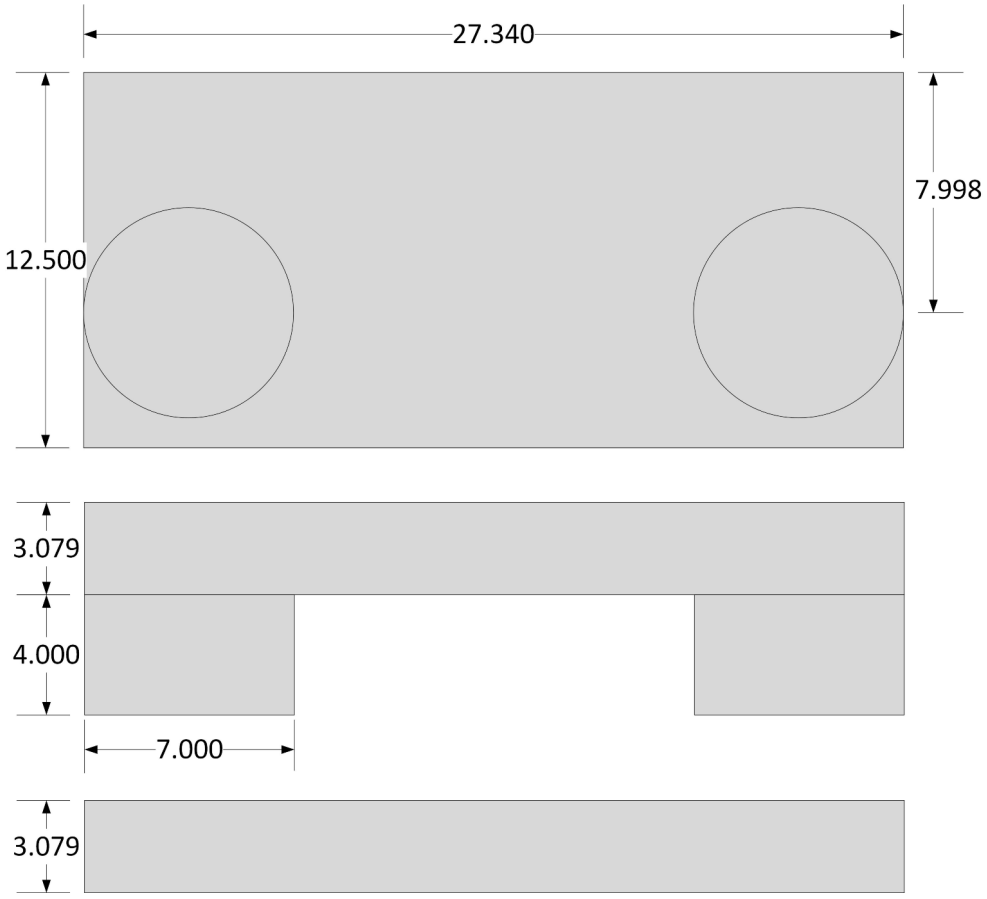


Figure 1-2. Transformer Core

The transformer core is composed of Proterial ML91S material. The part numbers for the two pieces are: ML91S U-27.34-7.08-12.5 and ML91S I-27.34-3.08-12.5.

1.3 Test Setup

The board in the test jig with the heat sink mounted is shown in the following figure.

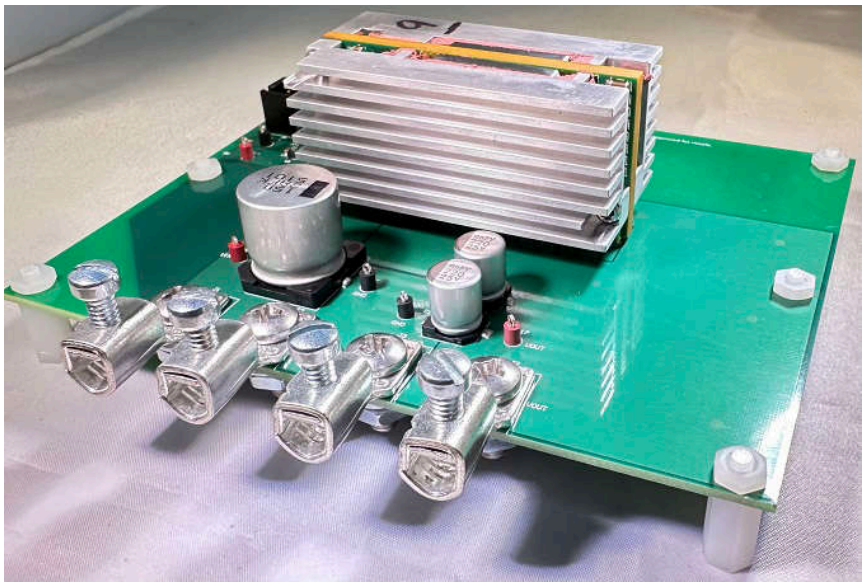


Figure 1-3. Test Setup

The fan used in the tests was PFB0412EN-E from Delta. This fan runs on 12 V with an input current draw of 2.6 A and a maximum air flow of 38 CFM.

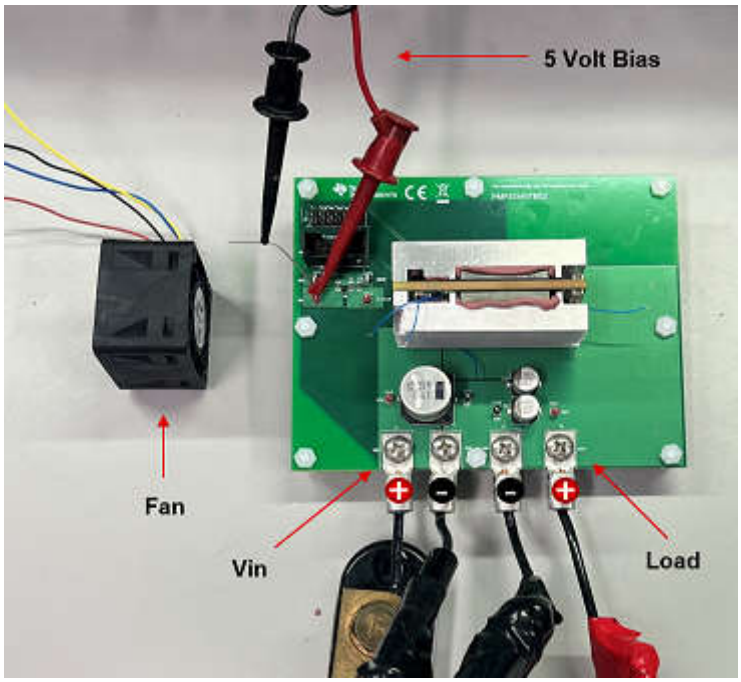


Figure 1-4. Test Connections

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in the following figure across the input operating voltage range. The peak efficiency is just under 98% while the full load 12-V efficiency is above 95.5%. Efficiency was measured on the test fixture. Actual module efficiency is higher due to additional loss present in the test fixture.

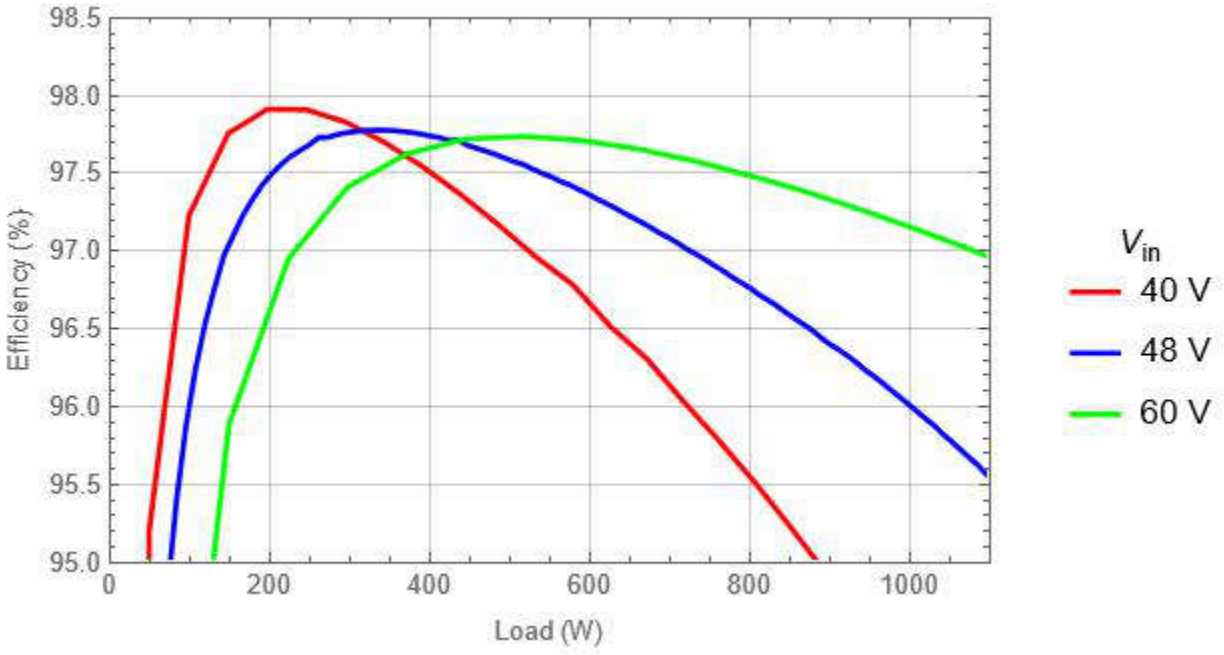


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

Table 2-1 shows the efficiency data for 48-V input.

Table 2-1. 48-V Input Efficiency Data

V_{BIAS} (V)	V_{IN} (V)	V_{OUT} (V)	I_{BIAS} (A)	I_{IN} (A)	I_{OUT} (A)	P_{BIAS} (W)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency no Bias	Efficiency with Bias
4.8	48.0	12.0	0.3	0.8	3.0	1.6	39.9	36.0	3.9	90.3%	86.8%
4.8	48.0	12.0	0.3	1.8	7.0	1.6	87.9	83.8	4.1	95.4%	93.6%
4.8	47.9	12.0	0.3	2.8	11.0	1.6	135.9	131.5	4.4	96.8%	95.6%
4.8	47.9	11.9	0.3	3.8	15.0	1.6	183.8	178.9	4.9	97.3%	96.5%
4.8	47.9	11.9	0.3	4.8	19.0	1.6	231.7	226.2	5.5	97.6%	96.9%
4.8	47.9	11.9	0.3	5.8	23.0	1.6	279.7	273.3	6.3	97.7%	97.2%
4.8	47.9	11.9	0.3	6.8	27.0	1.6	327.5	320.2	7.3	97.8%	97.3%
4.8	47.9	11.8	0.3	7.8	31.0	1.6	375.2	366.9	8.4	97.8%	97.3%
4.8	47.8	11.8	0.3	8.8	35.0	1.6	423.0	413.4	9.6	97.7%	97.4%
4.8	47.8	11.8	0.3	9.8	39.0	1.6	470.8	459.8	11.0	97.7%	97.3%
4.8	47.8	11.8	0.3	10.8	43.0	1.6	518.4	505.8	12.6	97.6%	97.3%
4.8	47.8	11.7	0.3	11.8	47.0	1.6	566.1	551.8	14.3	97.5%	97.2%
4.8	47.8	11.7	0.3	12.9	51.0	1.6	613.8	597.7	16.2	97.4%	97.1%
4.8	47.7	11.7	0.3	13.9	55.0	1.6	661.3	643.1	18.2	97.2%	97.0%

Table 2-1. 48-V Input Efficiency Data (continued)

V_{BIAS} (V)	V_{IN} (V)	V_{OUT} (V)	I_{BIAS} (A)	I_{IN} (A)	I_{OUT} (A)	P_{BIAS} (W)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency no Bias	Efficiency with Bias
4.8	47.7	11.7	0.3	14.9	59.0	1.6	709.0	688.5	20.5	97.1%	96.9%
4.8	47.7	11.7	0.3	15.9	63.0	1.6	756.6	733.8	22.9	97.0%	96.8%
4.8	47.7	11.6	0.3	16.9	67.0	1.6	804.1	778.6	25.5	96.8%	96.6%
4.8	47.7	11.6	0.3	17.9	71.0	1.6	851.5	823.2	28.2	96.7%	96.5%
4.8	47.6	11.6	0.3	18.9	75.0	1.6	898.8	867.6	31.2	96.5%	96.4%
4.8	47.6	11.5	0.3	19.9	79.0	1.6	946.6	912.1	34.4	96.4%	96.2%
4.8	47.6	11.5	0.3	20.9	83.0	1.6	993.9	956.1	37.8	96.2%	96.0%
4.8	47.6	11.5	0.3	21.9	87.0	1.6	1041.3	999.7	41.5	96.0%	95.9%
4.8	47.6	11.5	0.3	22.9	91.0	1.6	1088.5	1043.0	45.5	95.8%	95.7%
4.8	47.6	11.4	0.3	23.9	95.0	1.6	1136.2	1086.4	49.8	95.6%	95.5%
4.8	47.6	11.4	0.3	24.4	97.0	1.6	1159.8	1107.8	52.0	95.5%	95.4%

Table 2-2 shows the efficiency data for 40-V input.

Table 2-2. 40-V Input Efficiency Data

V_{BIAS} (V)	V_{IN} (V)	V_{OUT} (V)	I_{BIAS} (A)	I_{IN} (A)	I_{OUT} (A)	P_{BIAS} (W)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency no Bias	Efficiency with Bias
4.8	40.0	10.0	0.3	0.1	0.0	1.6	2.3	0.0	2.4	0.0%	0.0%
4.8	39.9	10.0	0.3	1.3	5.0	1.6	52.3	49.8	2.5	95.2%	92.4%
4.8	39.9	10.0	0.3	2.6	10.0	1.6	102.2	99.4	2.8	97.2%	95.7%
4.8	39.9	9.9	0.3	3.8	15.0	1.6	152.1	148.7	3.4	97.8%	96.7%
4.8	39.9	9.9	0.3	5.1	20.0	1.6	202.0	197.8	4.2	97.9%	97.1%
4.8	39.9	9.9	0.3	6.3	25.0	1.6	251.8	246.5	5.3	97.9%	97.3%
4.8	39.8	9.8	0.3	7.6	30.0	1.6	301.5	295.0	6.5	97.8%	97.3%
4.8	39.8	9.8	0.3	8.8	35.0	1.6	351.2	343.1	8.1	97.7%	97.3%
4.8	39.8	9.8	0.3	10.1	40.0	1.6	400.8	391.0	9.8	97.5%	97.2%
4.8	39.8	9.7	0.3	11.3	45.0	1.6	450.4	438.5	11.9	97.4%	97.0%
4.8	39.7	9.7	0.3	12.6	50.0	1.6	499.8	485.7	14.1	97.2%	96.9%
4.8	39.7	9.7	0.3	13.8	55.0	1.6	549.5	532.8	16.7	97.0%	96.7%
4.8	39.7	9.7	0.3	15.1	60.0	1.6	599.2	579.9	19.3	96.8%	96.5%
4.8	39.7	9.6	0.3	16.3	65.0	1.6	648.5	625.9	22.6	96.5%	96.3%
4.8	39.7	9.6	0.3	17.6	70.0	1.6	697.7	671.9	25.8	96.3%	96.1%
4.8	39.6	9.6	0.3	18.8	75.0	1.6	746.9	717.2	29.6	96.0%	95.8%
4.8	39.6	9.5	0.3	20.1	80.0	1.6	796.1	762.5	33.6	95.8%	95.6%
4.8	39.6	9.5	0.3	21.3	85.0	1.6	845.4	807.4	38.0	95.5%	95.3%
4.8	39.6	9.5	0.3	22.6	90.0	1.6	894.2	851.5	42.7	95.2%	95.1%
4.8	39.6	9.4	0.3	23.9	95.0	1.6	943.3	895.5	47.8	94.9%	94.8%

Table 2-3 shows the efficiency data for 60-V input.

Table 2-3. 60-V Input Efficiency Data

V_{BIAS} (V)	V_{IN} (V)	V_{OUT} (V)	I_{BIAS} (A)	I_{IN} (A)	I_{OUT} (A)	P_{BIAS} (W)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency no Bias	Efficiency With Bias
4.8	59.9	15.0	0.3	0.1	0.0	1.6	6.0	0.1	5.9	1.5%	1.2%
4.8	59.9	15.0	0.3	1.4	5.0	1.6	80.9	74.9	6.0	92.5%	90.8%
4.8	59.9	14.9	0.3	2.6	10.0	1.6	155.8	149.4	6.4	95.9%	94.9%
4.8	59.9	14.9	0.3	3.9	15.0	1.6	230.7	223.7	7.0	96.9%	96.3%
4.8	59.9	14.9	0.3	5.1	20.0	1.6	305.6	297.7	7.9	97.4%	96.9%
4.8	59.8	14.9	0.3	6.4	25.0	1.6	380.4	371.4	9.0	97.6%	97.2%
4.8	59.8	14.8	0.3	7.6	30.0	1.6	455.1	444.7	10.4	97.7%	97.4%
4.8	59.8	14.8	0.3	8.9	35.0	1.6	529.7	517.7	12.0	97.7%	97.4%
4.8	59.8	14.8	0.3	10.1	40.0	1.6	604.6	590.7	13.8	97.7%	97.5%
4.8	59.8	14.7	0.3	11.4	45.0	1.6	679.2	663.3	15.9	97.7%	97.4%
4.8	59.7	14.7	0.3	12.6	50.0	1.6	753.7	735.4	18.3	97.6%	97.4%
4.8	59.7	14.7	0.3	13.9	55.0	1.6	828.3	807.3	20.9	97.5%	97.3%
4.8	59.7	14.7	0.3	15.1	60.0	1.6	903.0	879.2	23.8	97.4%	97.2%
4.8	59.7	14.6	0.3	16.4	65.0	1.6	977.1	950.2	26.9	97.2%	97.1%
4.8	59.7	14.6	0.3	17.6	70.0	1.6	1051.5	1021.2	30.3	97.1%	97.0%
4.8	59.6	14.6	0.3	18.9	75.0	1.6	1125.8	1091.8	34.0	97.0%	96.8%
4.8	59.6	14.5	0.3	20.1	80.0	1.6	1200.1	1162.1	38.0	96.8%	96.7%
4.8	59.6	14.5	0.3	21.4	85.0	1.6	1274.3	1231.9	42.3	96.7%	96.6%
4.8	59.5	14.5	0.3	22.6	90.0	1.6	1348.2	1301.2	47.0	96.5%	96.4%

2.3 Thermal Data

Figure 2-2 shows the thermal image. The heat sink has been removed and the applied load is 500 W.

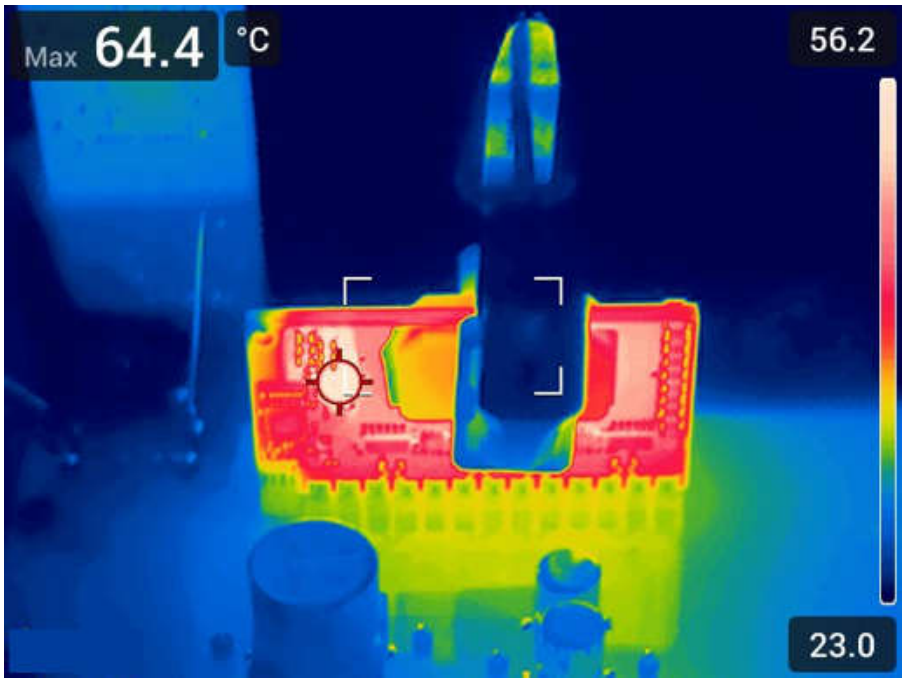


Figure 2-2. Thermal Image

FET temperatures were also measured with thermocouples. The heat sink and the thermal interface material (TIM) were applied for these measurements. The TIM used is LiPOLY T-work9000 with 1-mm thickness.

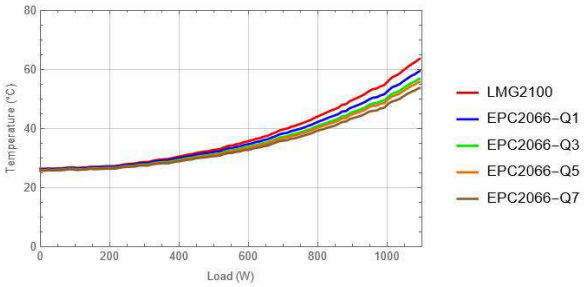


Figure 2-3. Thermocouple Data - Top Side Components

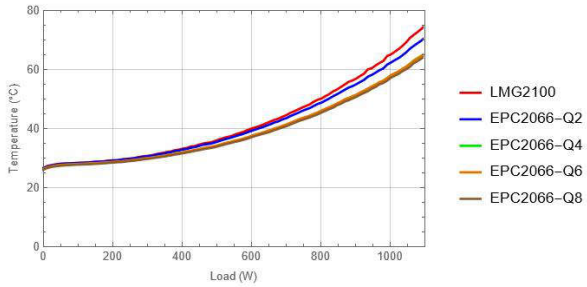


Figure 2-4. Thermocouple Data - Bottom Side Components

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figure. Channel 1 and 2 are the primary side switching nodes. Channel 3 is the synchronous rectifier switching node. Test conditions for the waveform shown are 48-V input and no load.

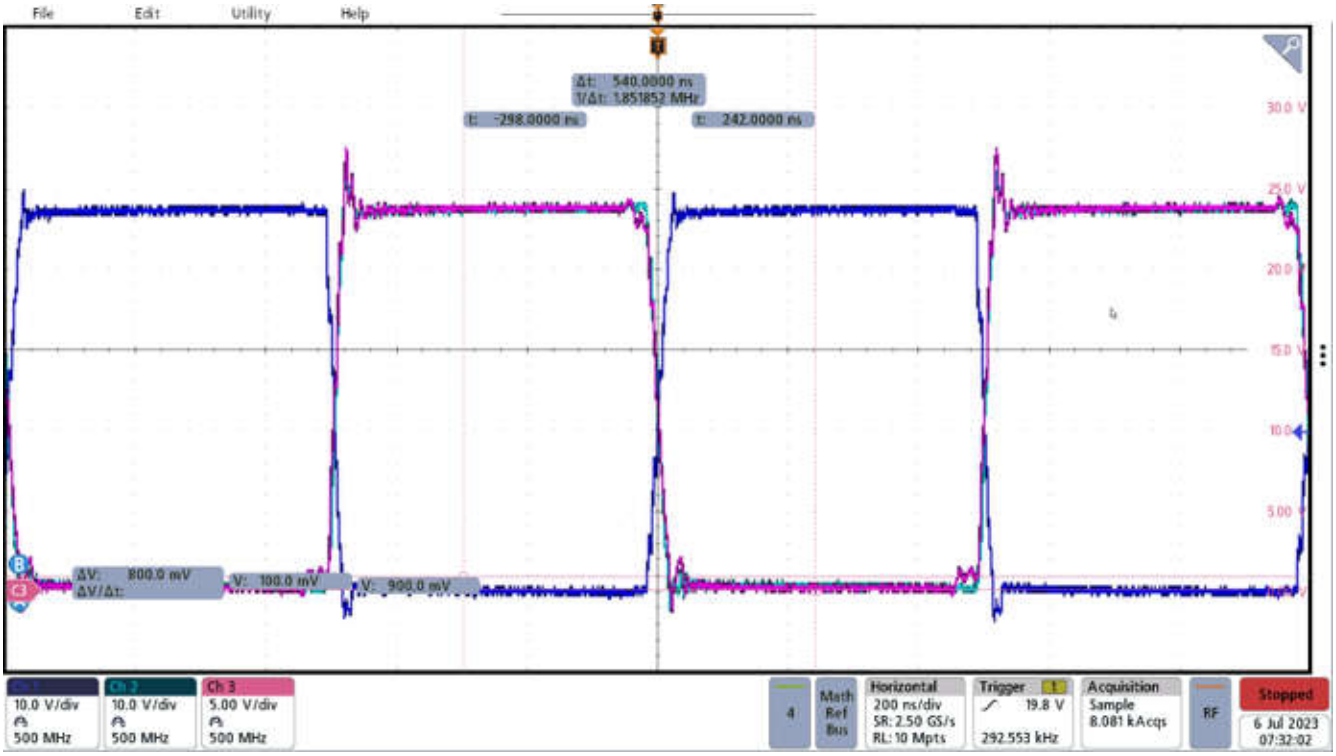


Figure 3-1. Switching Nodes

3.2 Start-Up Sequence

Start-up behavior is shown in the following figure for no load. Channel 2 is the input voltage and Channel 1 is the output voltage.

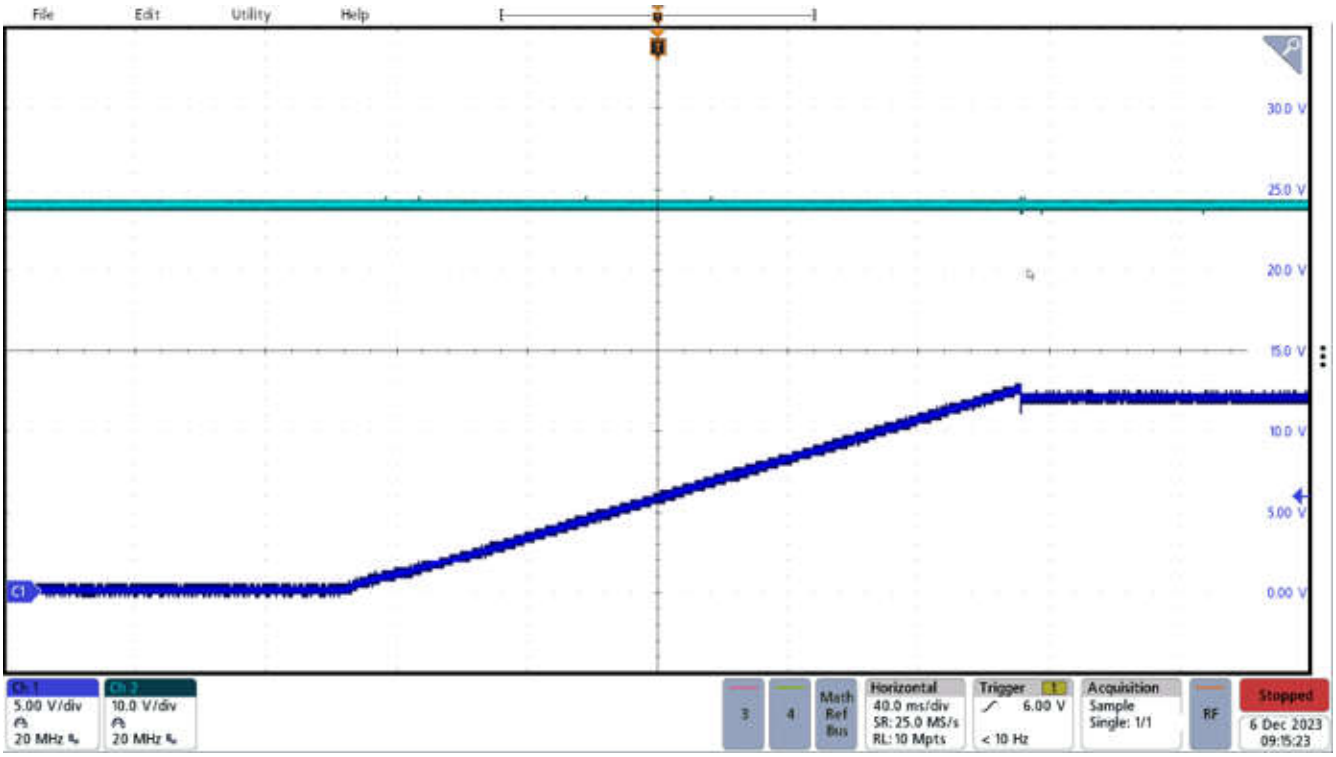


Figure 3-2. Start-Up

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