Test Report: PMP41079

2-Phase Interleaved Boost Converter Stage Reference Design for Class-H Audio Amplifier Application

Description

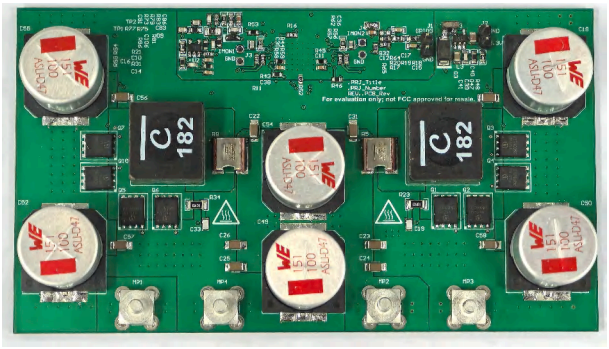
This reference design demonstrates a 450-W, 2-phase interleaved boost converter reference design for the Class-H audio amplifier application. To provide supply to the external audio amplifier, the controller is able to follow the Class-H control signal from the amplifier and generate an output voltage which tracks the speaker amplitude. Therefore, minimized overall power consumption and losses can be achieved.

Features

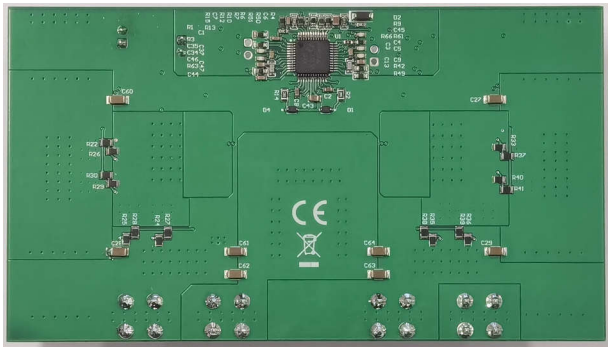
- Well-balanced internal current sharing between the two phases of the boost converter; power as well as thermal stress can be shared evenly with the small board size
- 450-W converter in 12 cm × 6.5 cm dimensions; high power and high power-density design
- Class-H control capable; boost output voltage is able to follow the speaker output amplitude to minimize power consumption as well as losses

Applications

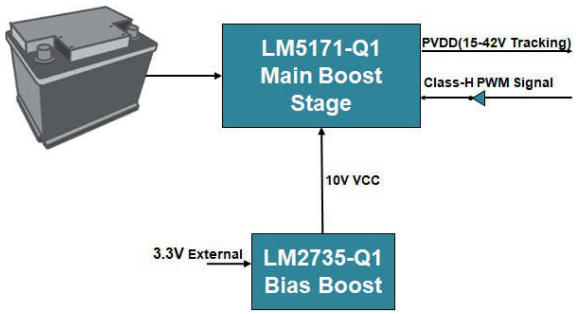
- Automotive external amplifier



Top of Board



Bottom of Board



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{in} (Main Boost Stage)	9 VDC to 16 VDC Continuous
V_{out} (Main Boost Stage)	15 VDC to 42 VDC
I_{out} (Main Boost Stage)	12 A maximum, rated at 10 A
F_{sw} (Main Boost Stage)	350 kHz per phase
V_{in} (Bias Boost Regulator)	3.3 VDC
V_{out} (Bias Boost Regulator)	10 VDC
I_{out} (Bias Boost Regulator)	0.7 A maximum, rated at 0.5 A
F_{sw} (Bias Boost Regulator)	1.6 MHz

1.2 Required Equipment

- Power supply: Chroma 62006P-100-50
- Electronic load: Chroma 63204
- Digital multimeter: Fluke 287C
- Oscilloscope: Tektronix DPO3054
- Frequency response analyzer: AP Instruments Model 310
- Thermal camera: Fluke TiS55

1.3 Considerations

The 2-phase off-battery boost converter is frequently referred to as *Main Boost Stage*.

The 3.3-V to 10-V bias boost converter is also referred to as a *Bias Boost Regulator*.

The maximum continuous runtime load current for the *Main Boost Stage* depends on the allowable temperature rise on the components and the ambient temperature. Mounting the board on a heat sink or using airflow (or both) results in a lower temperature rise on the components, allowing for higher prolonged or continuous runtime load current.

Make sure that properly-sized wire leads are used to connect the inputs and outputs, especially the low-voltage *Main Boost Stage* input, where the current can be around 50 A at full load. Consider using AWG#8 wire or wire with an even smaller gauge number.

Consider further optimization on the SW node plane area and high-frequency decoupling coop area to enhance EMI performance of the Main Boost Stage when building customized boards based on this reference design.

However, due to the thermal loss of MOSFETs (mainly low-side FETs) in this high-power reference design, reserve the plane area of the SW node to the degree where the heat dissipation is abundant. The heat dissipation of the power inductor can be enhanced by enlarging the non-switching node plane area of the inductor, along with the placement of thermal vias.

1.4 Dimensions

The board dimensions are 4.7 in × 2.6 in (12 cm × 6.7 cm).

2 Testing and Results

The measurements done in this part are under fan cooling condition (fan part number: PSD1208PMB1-A, power rating: 9.4 W).

2.1 Efficiency Graphs

The efficiency graph is shown in the following figure.

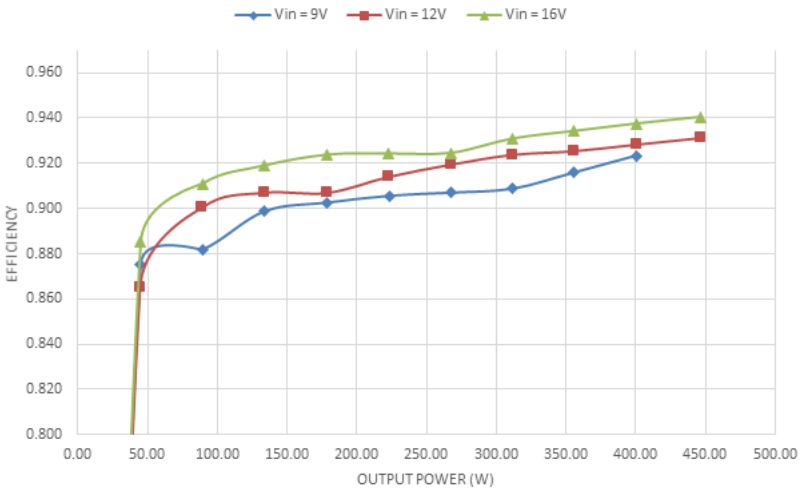


Figure 2-1. Efficiency vs Output Power of Main Boost Stage

2.2 Efficiency Data

Efficiency data is shown in the following tables.

Table 2-1. Efficiency and Total Power Loss at V_{IN} = 9 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency	P_{loss} (W)
9.00	0.48	44.45	0.00	4.29	0.00	0.000	4.29
9.00	5.70	44.45	1.01	51.28	44.89	0.875	6.39
9.00	11.26	44.45	2.01	101.31	89.34	0.882	11.97
9.00	16.54	44.45	3.01	148.86	133.79	0.899	15.07
9.00	22.05	44.45	4.03	198.45	179.13	0.903	19.32
9.00	27.43	44.45	5.03	246.87	223.58	0.906	23.29
9.00	32.78	44.45	6.02	295.02	267.59	0.907	27.43
9.00	38.15	44.45	7.02	343.35	312.04	0.909	31.31
9.00	43.19	44.45	8.01	388.71	356.04	0.916	32.67
9.00	48.19	44.45	9.01	433.71	400.49	0.923	33.22

Table 2-2. Efficiency and Total Power Loss at V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency	P_{loss} (W)
12.00	0.36	44.45	0.00	4.31	0.00	0.000	4.31
12.03	4.27	44.45	1.00	51.37	44.45	0.865	6.92
12.07	8.18	44.45	2.00	98.73	88.90	0.900	9.83
12.05	12.20	44.45	3.00	147.01	133.35	0.907	13.66
12.02	16.39	44.45	4.02	197.01	178.69	0.907	18.32
12.06	20.24	44.45	5.02	244.09	223.14	0.914	20.96
12.04	24.17	44.45	6.02	291.01	267.59	0.920	23.42
12.02	28.10	44.45	7.02	337.76	312.04	0.924	25.72
12.00	32.06	44.45	8.01	384.72	356.04	0.925	28.68
11.97	36.04	44.45	9.01	431.40	400.49	0.928	30.90
11.96	40.07	44.45	10.04	479.24	446.28	0.931	32.96

Table 2-3. Efficiency and Total Power Loss at V_{IN} = 16 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency	P_{loss} (W)
16.00	0.32	44.45	0.00	5.04	0.00	0.000	5.04
16.00	3.17	44.45	1.01	50.72	44.89	0.885	5.83
16.00	6.13	44.45	2.01	98.08	89.34	0.911	8.74
16.00	9.07	44.45	3.00	145.12	133.35	0.919	11.77
16.00	12.12	44.45	4.03	193.92	179.13	0.924	14.79
16.00	15.09	44.45	5.02	241.44	223.14	0.924	18.30
16.00	18.09	44.45	6.02	289.44	267.59	0.925	21.85
16.00	20.95	44.45	7.02	335.20	312.04	0.931	23.16
16.00	23.82	44.45	8.01	381.12	356.04	0.934	25.08
16.00	26.70	44.45	9.01	427.20	400.49	0.937	26.71
16.00	29.66	44.45	10.04	474.56	446.28	0.940	28.28

2.3 Thermal Images

Thermal image (at full load, I_{load} = 10 A, V_{IN} = 12 V, V_{OUT} = 45 V, with fan cooling) is shown in the following figure.

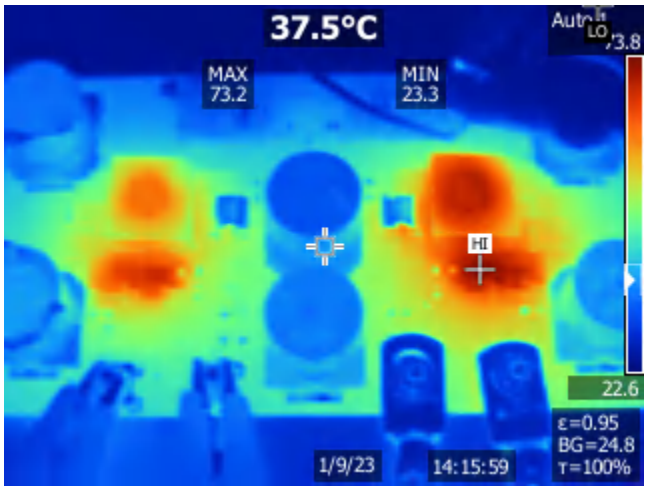
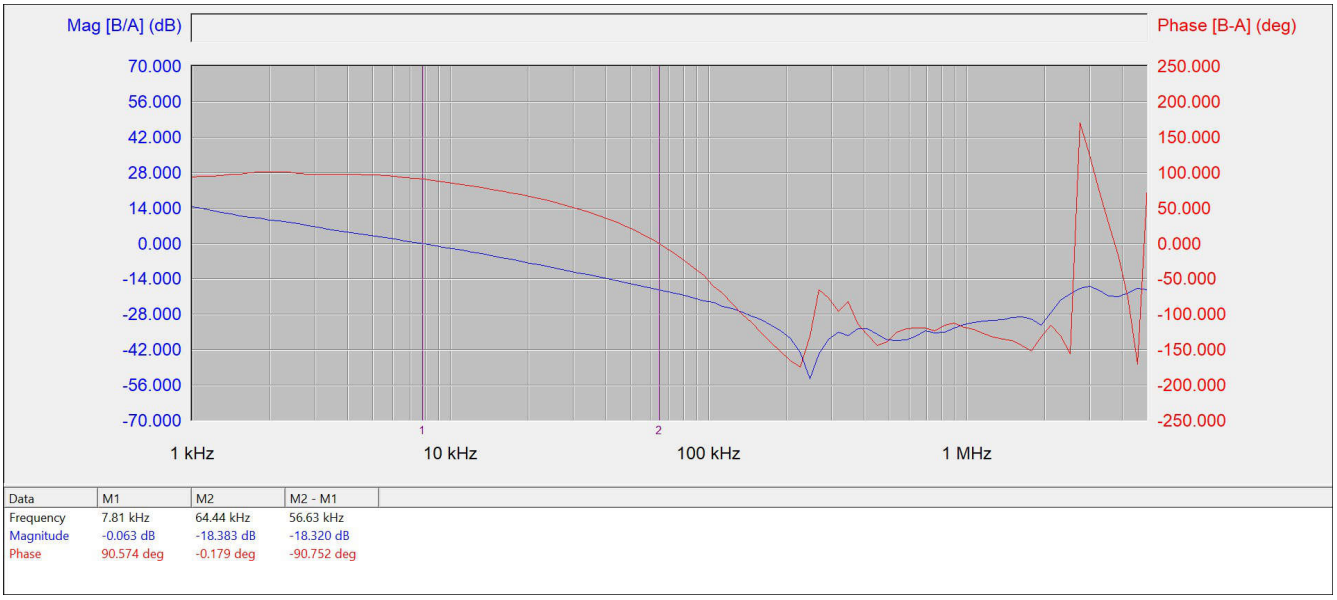


Figure 2-2. Thermal Image (at Full Load, With Fan Cooling)

2.4 Bode Plots

The bode plot is shown in the following figure.



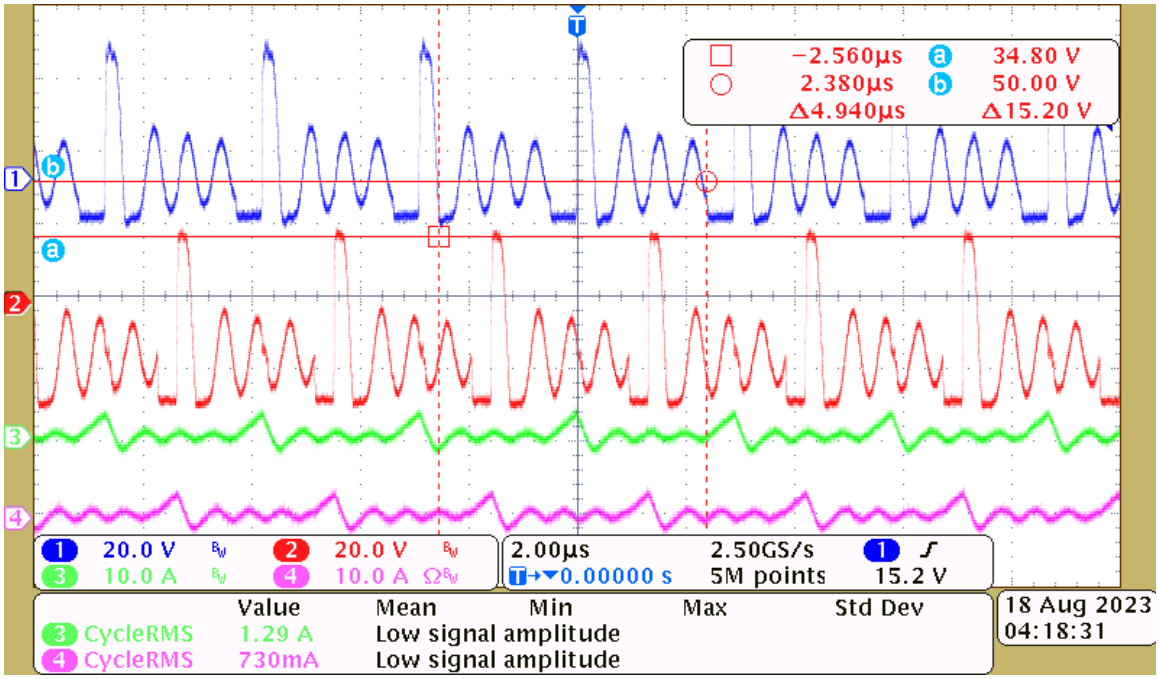
Gain Margin (GM) = 18.32 dB; Phase Margin (PM) = 90.75° ; Crossover Frequency (f_c) = 7.81 kHz

Figure 2-3. Bode Plot of the Main Boost Stage at Full Load, I_{load} = 10 A, V_{IN} = 12 V, V_{OUT} = 45 V

3 Waveforms

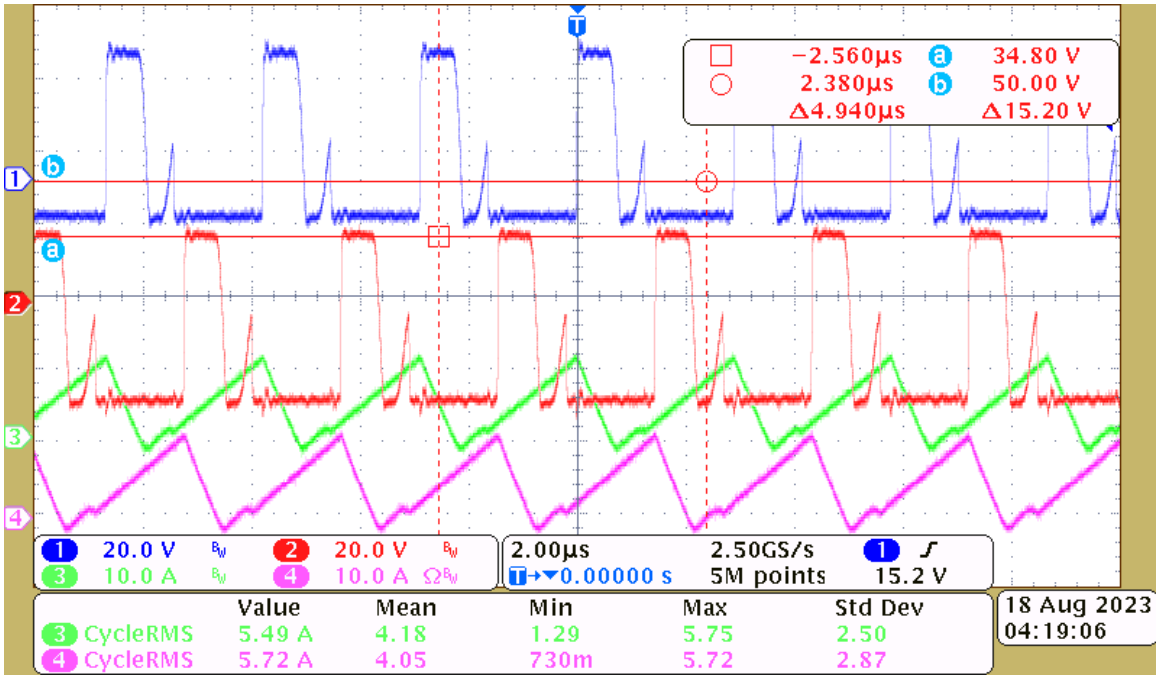
3.1 Switching

Switching behavior is shown in the following figures.



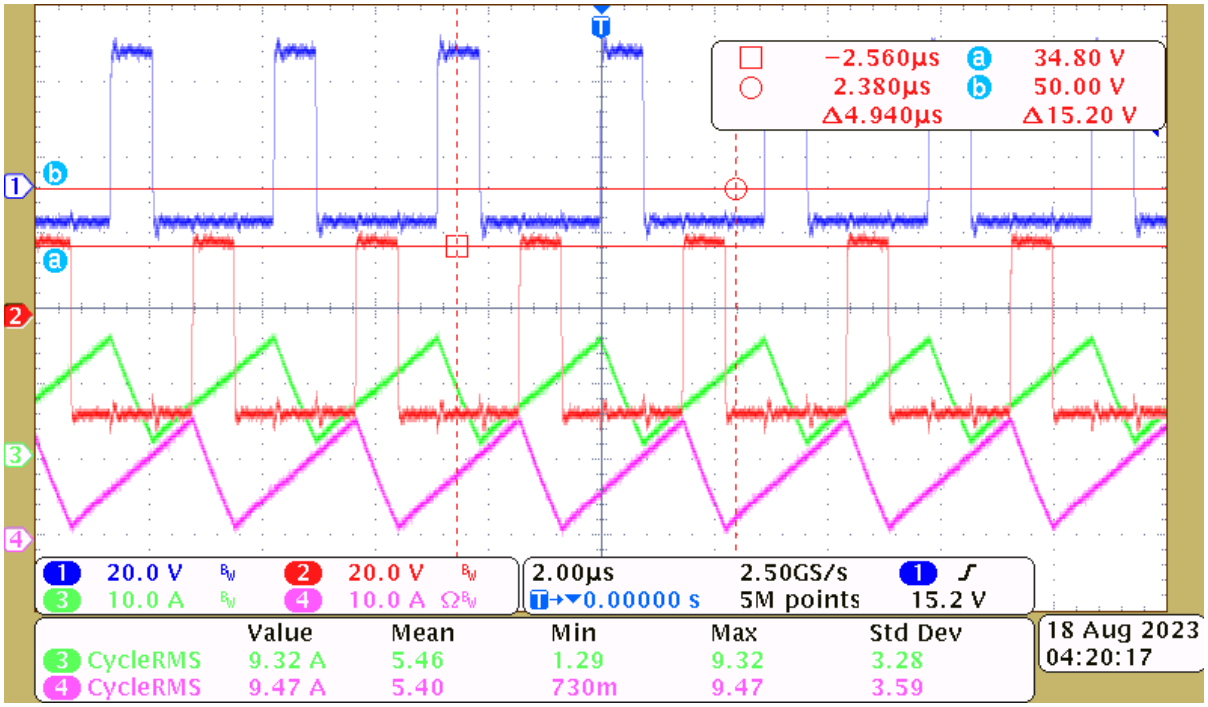
Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-1. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 0 A, V_{IN} = 12 V, V_{OUT} = 45 V



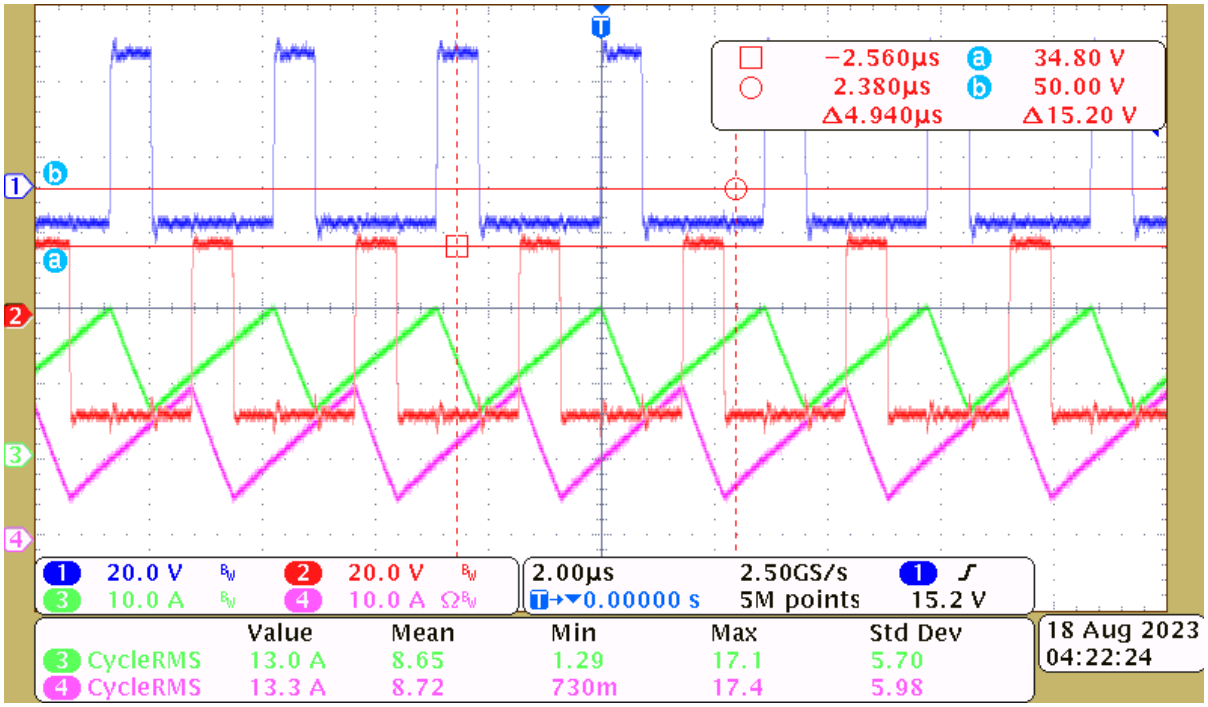
Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-2. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 2 A, V_{IN} = 12 V, V_{OUT} = 45 V



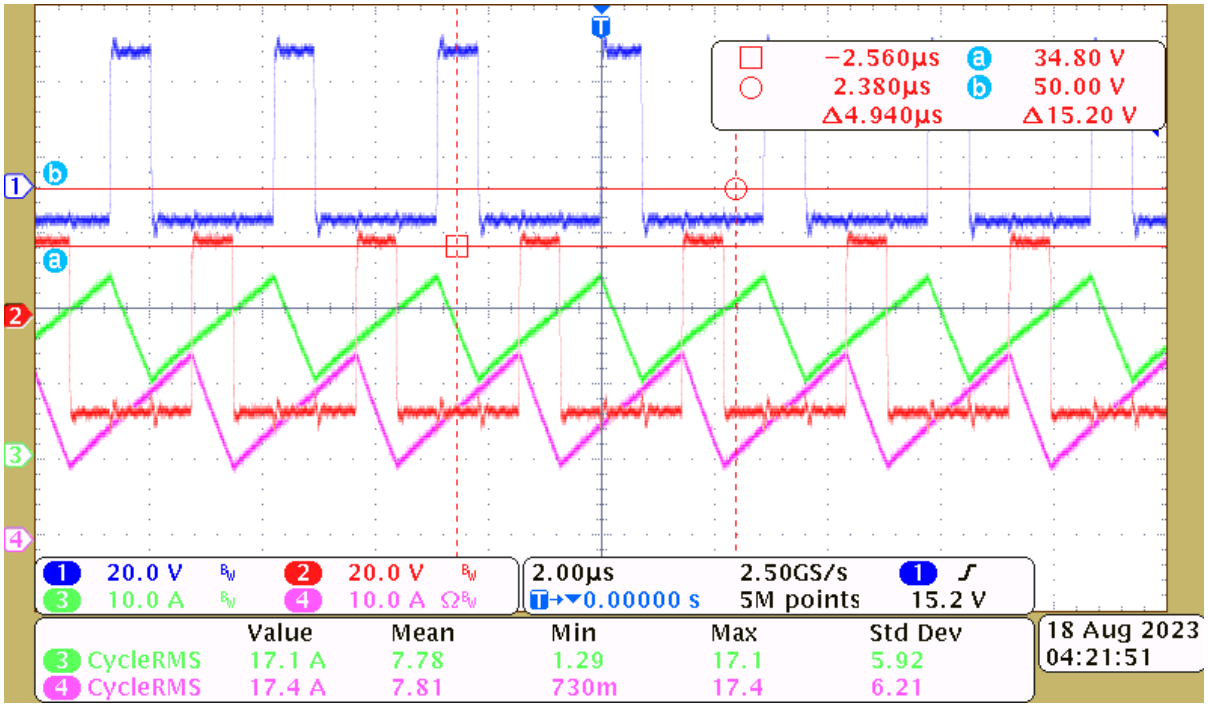
Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-3. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 4 A, V_{IN} = 12 V, V_{OUT} = 45 V



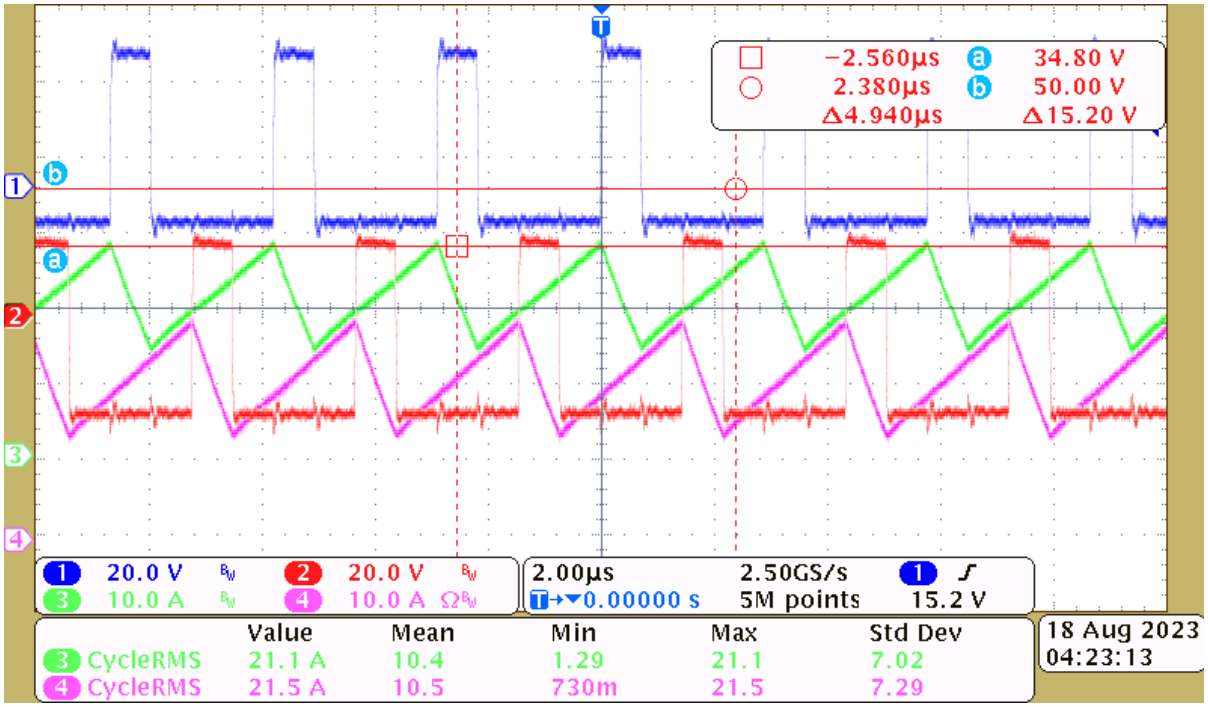
Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-4. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 6 A, V_{IN} = 12 V, V_{OUT} = 45 V



Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-5. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 8 A, V_{IN} = 12 V, V_{OUT} = 45 V



Phase 1 V_{SW} and I_L (CH1, CH3), Phase 2 V_{SW} and I_L (CH2, CH4)

Figure 3-6. Switch Node Voltages and Inductor Currents of Main Boost Stage, at I_{load} = 10 A, V_{IN} = 12 V, V_{OUT} = 45 V

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

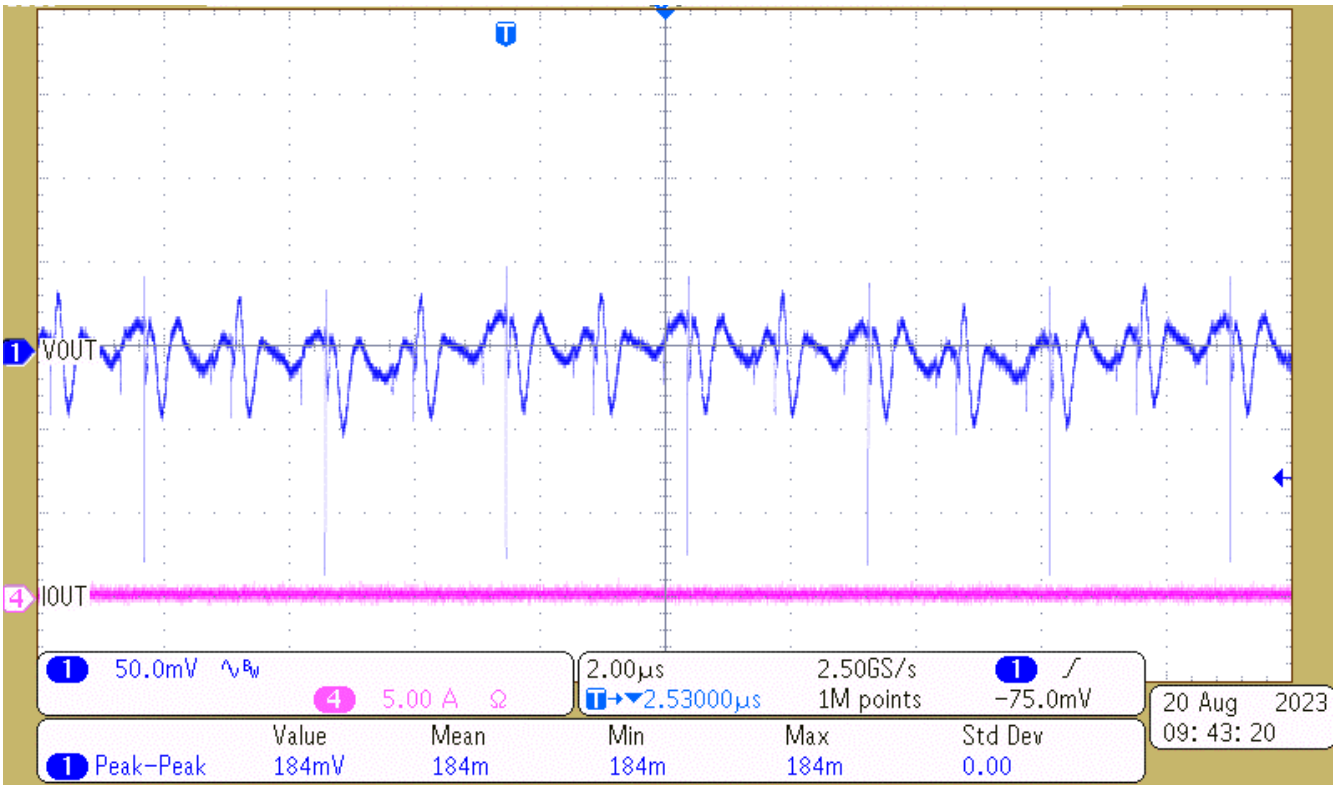


Figure 3-7. Output Voltage Ripple of Main Boost Stage at V_{IN} = 12 V, V_{OUT} = 45 V, I_{OUT} = 0 A

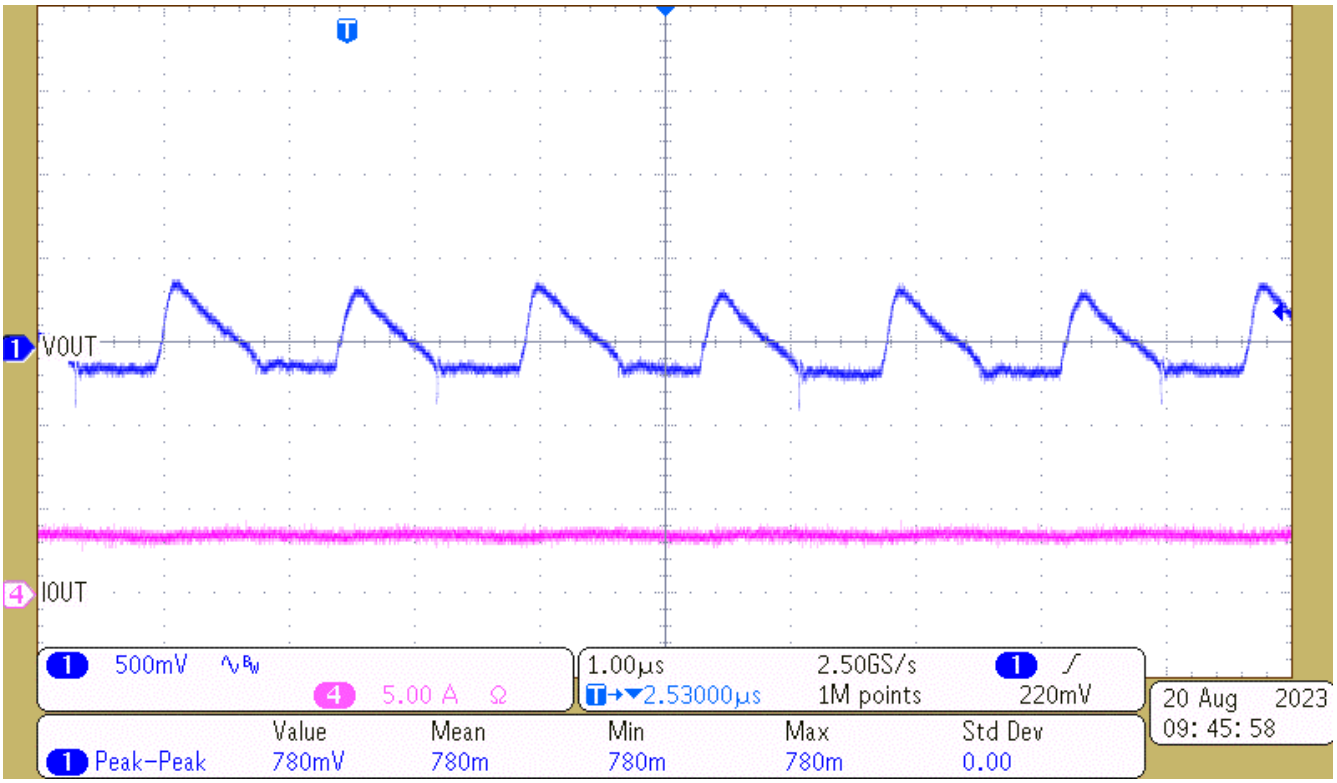


Figure 3-8. Output Voltage Ripple of Main Boost Stage at V_{IN} = 12 V, V_{OUT} = 45 V, I_{OUT} = 3.3 A

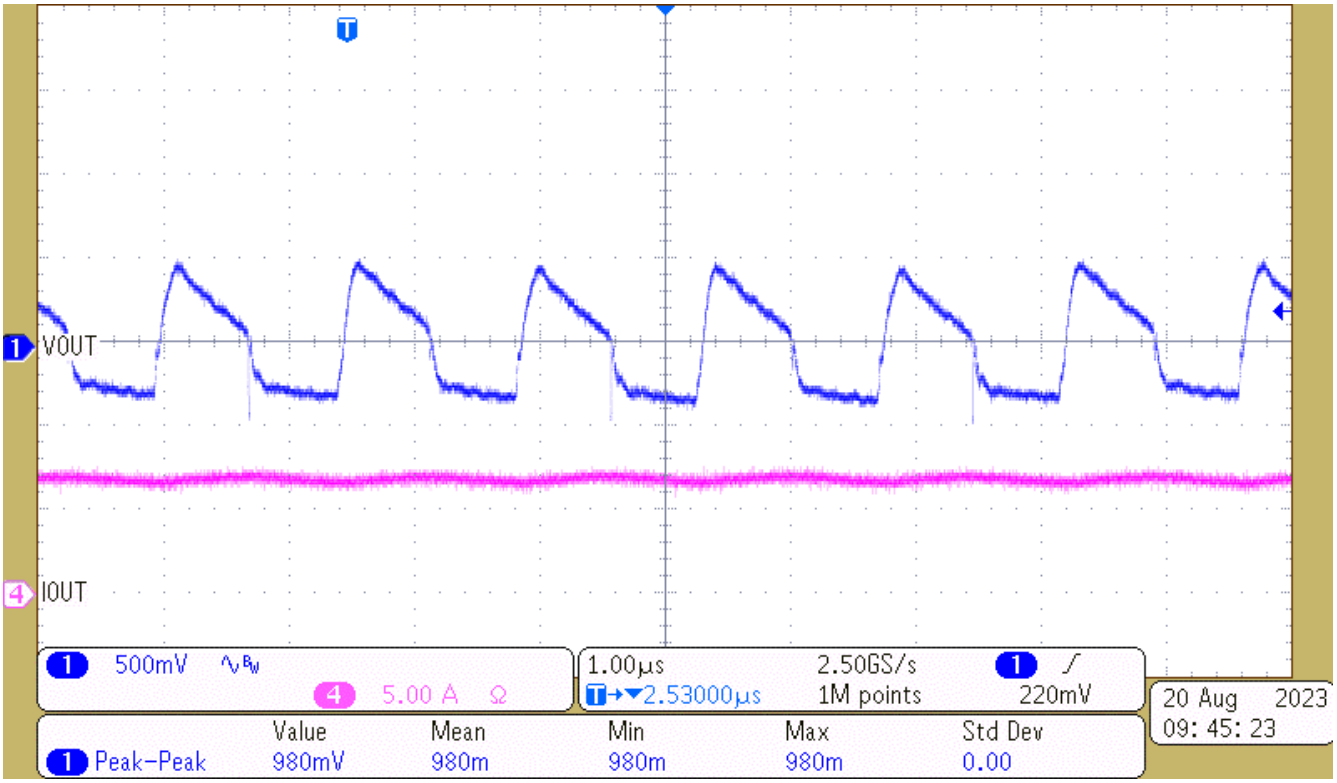


Figure 3-9. Output Voltage Ripple of Main Boost Stage at V_{IN} = 12 V, V_{OUT} = 45 V, I_{OUT} = 6.7 A

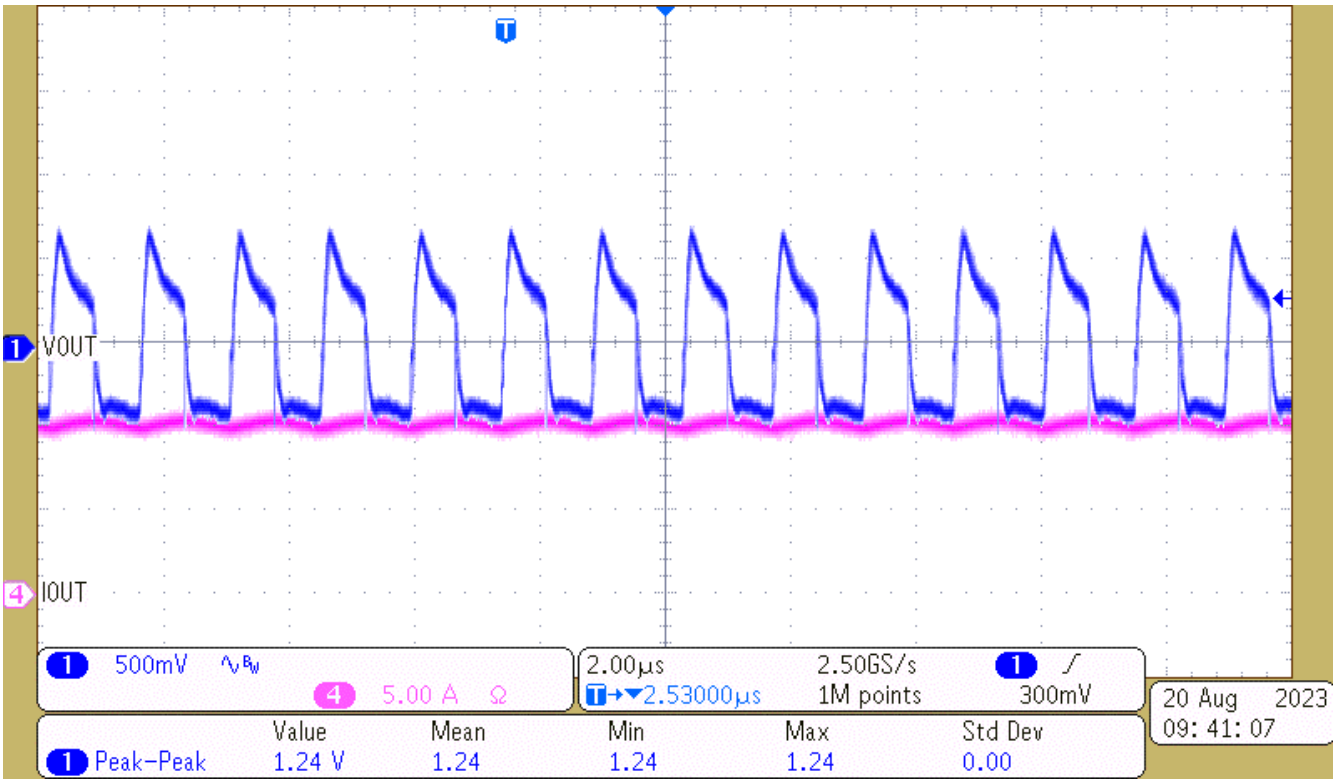


Figure 3-10. Output Voltage Ripple of Main Boost Stage at V_{IN} = 12 V, V_{OUT} = 45 V, I_{OUT} = 10 A

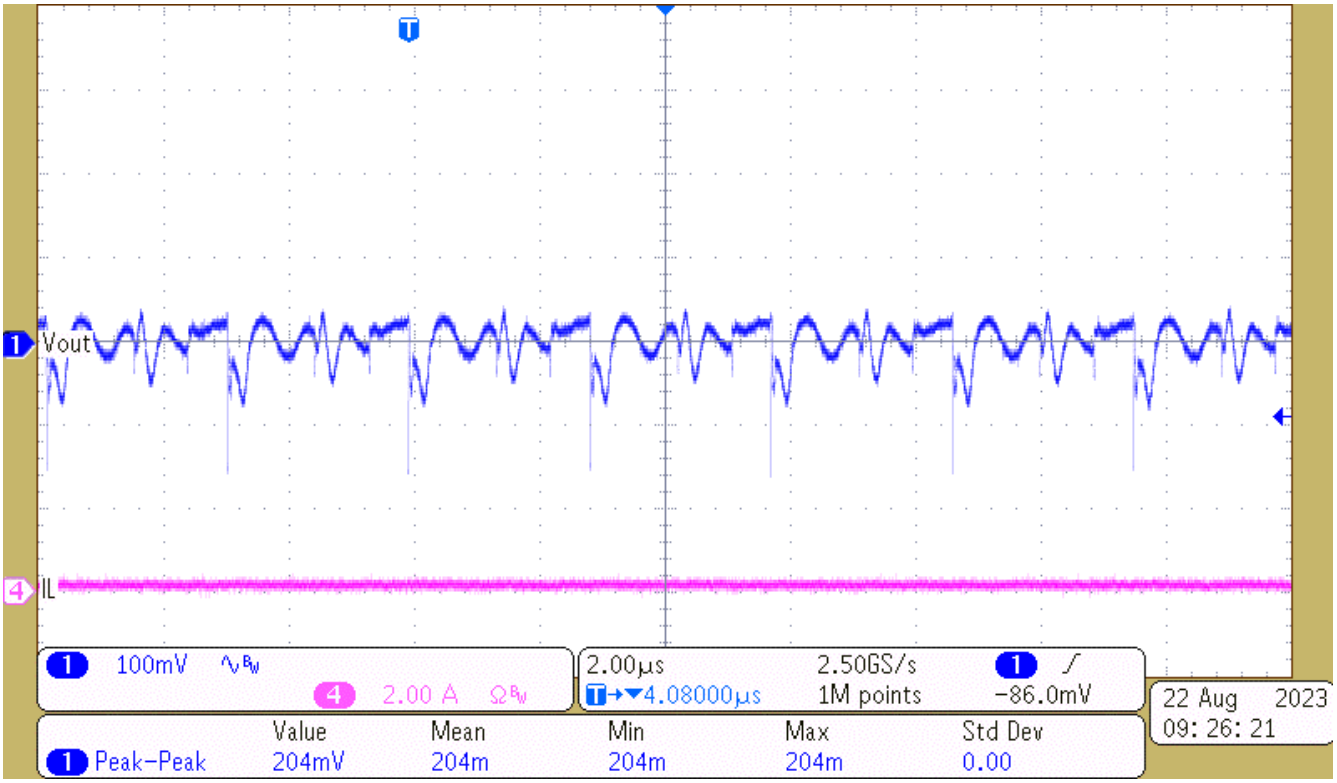


Figure 3-11. Output Voltage Ripple of Main Boost Stage at V_{IN} = 9 V, V_{OUT} = 45 V, I_{OUT} = 0 A

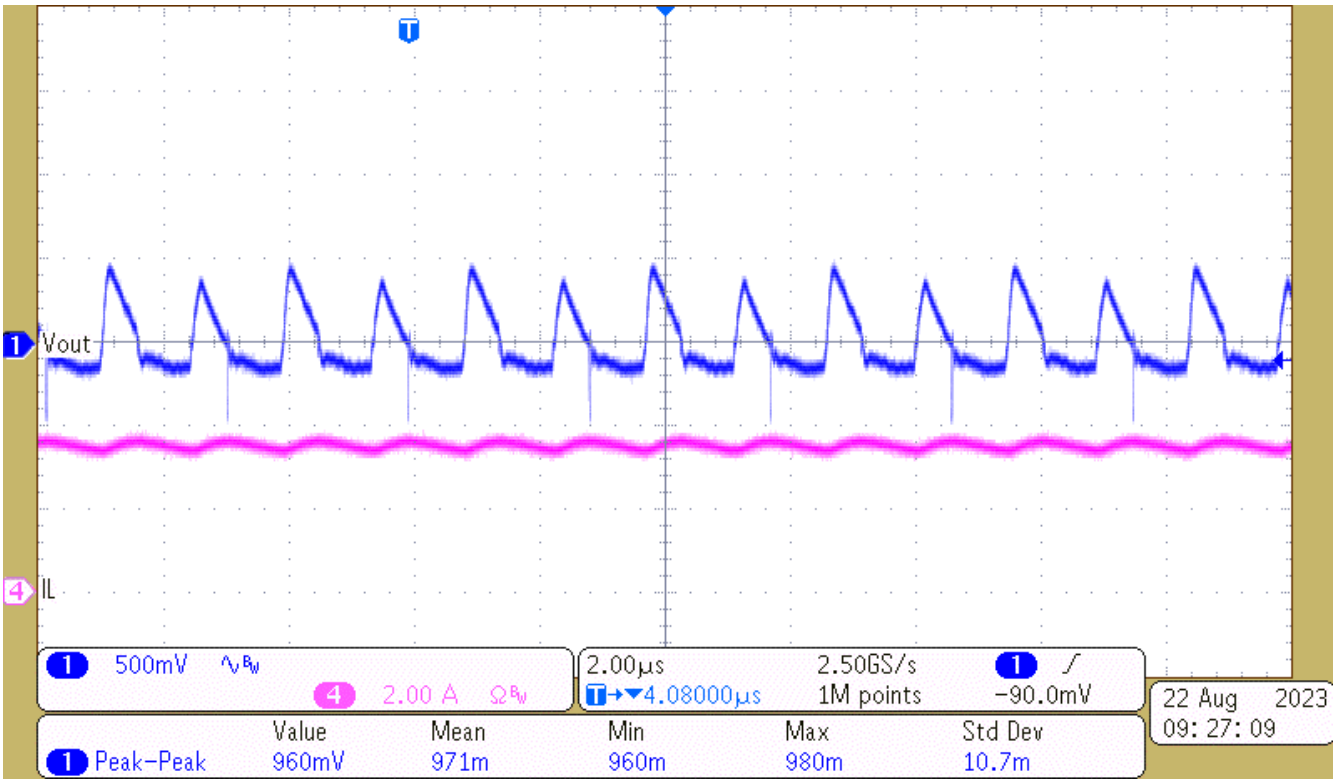


Figure 3-12. Output Voltage Ripple of Main Boost Stage at V_{IN} = 9 V, V_{OUT} = 45 V, I_{OUT} = 3.3 A

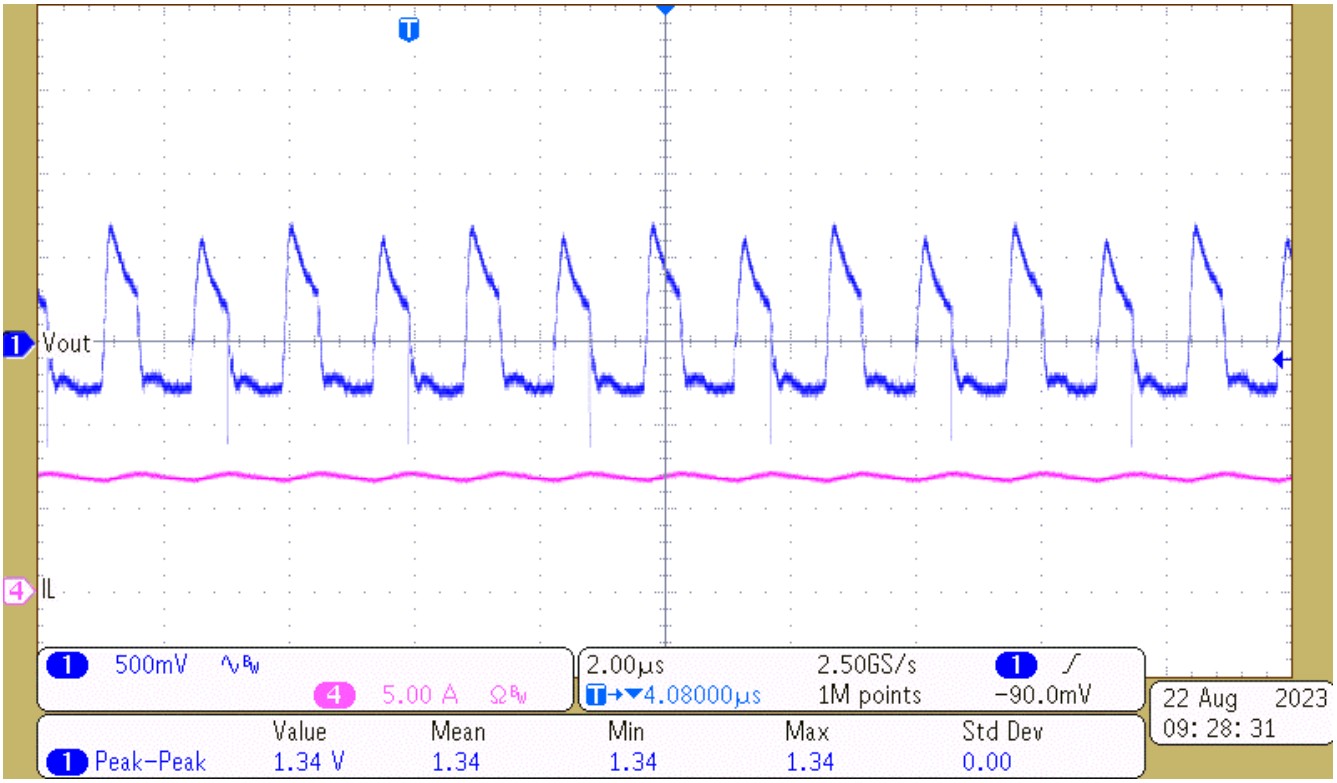


Figure 3-13. Output Voltage Ripple of Main Boost Stage at V_{IN} = 9 V, V_{OUT} = 45 V, I_{OUT} = 6.7 A

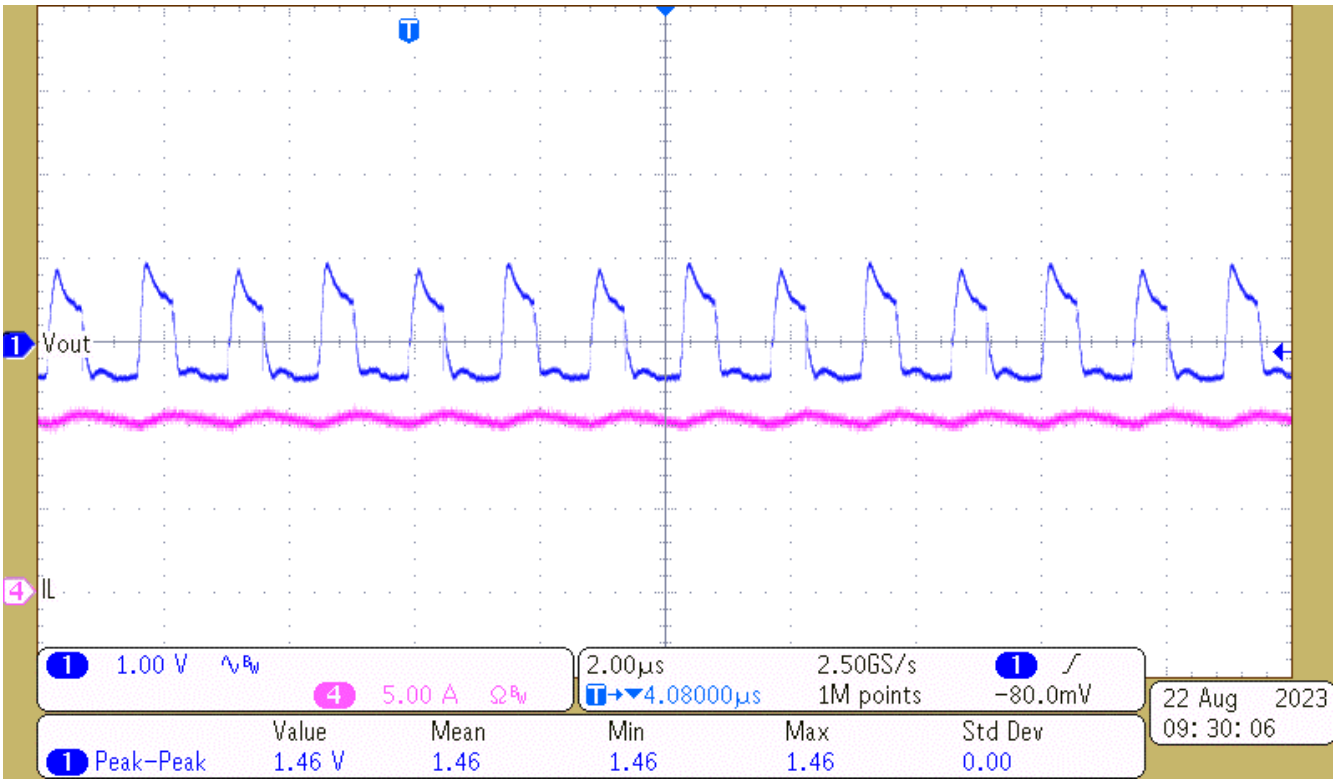


Figure 3-14. Output Voltage Ripple of Main Boost Stage at V_{IN} = 9 V, V_{OUT} = 45 V, I_{OUT} = 10 A

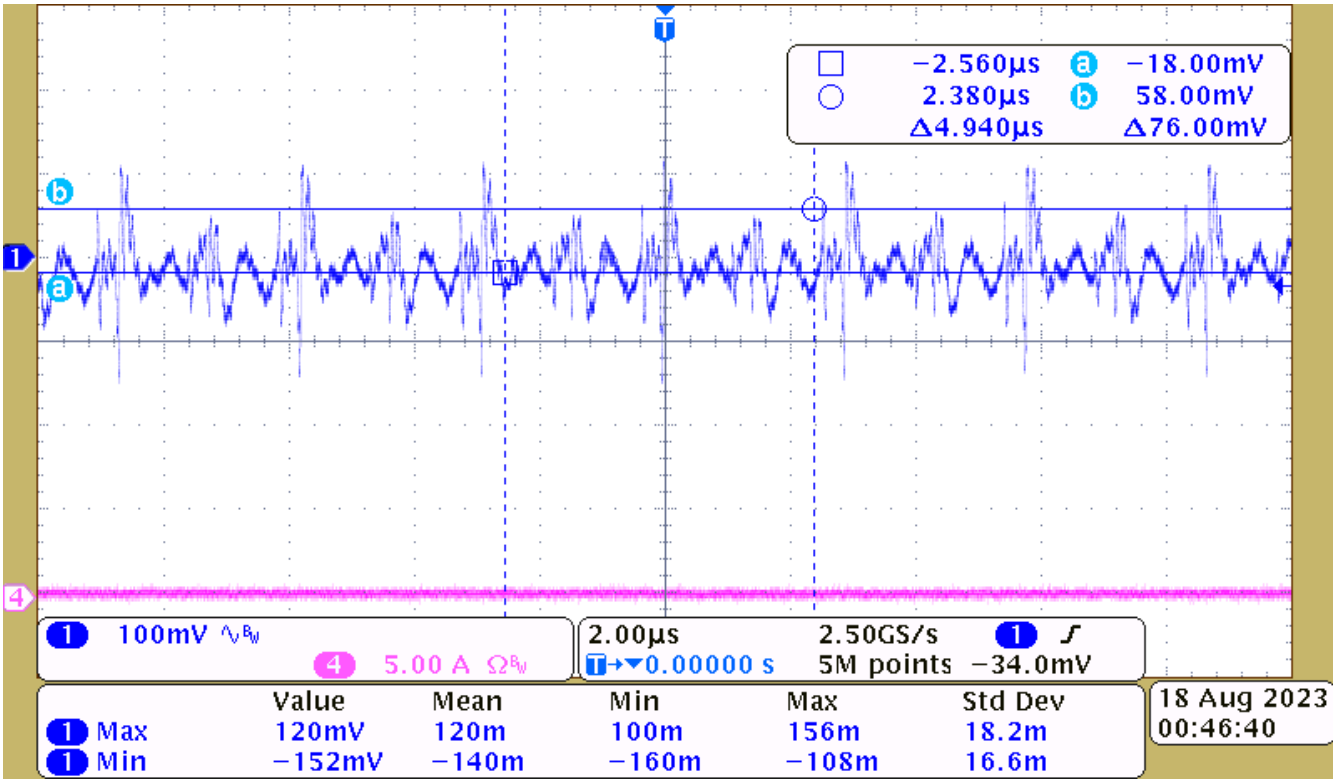


Figure 3-15. Output Voltage Ripple of Main Boost Stage at V_{IN} = 16 V, V_{OUT} = 45 V, I_{OUT} = 0 A

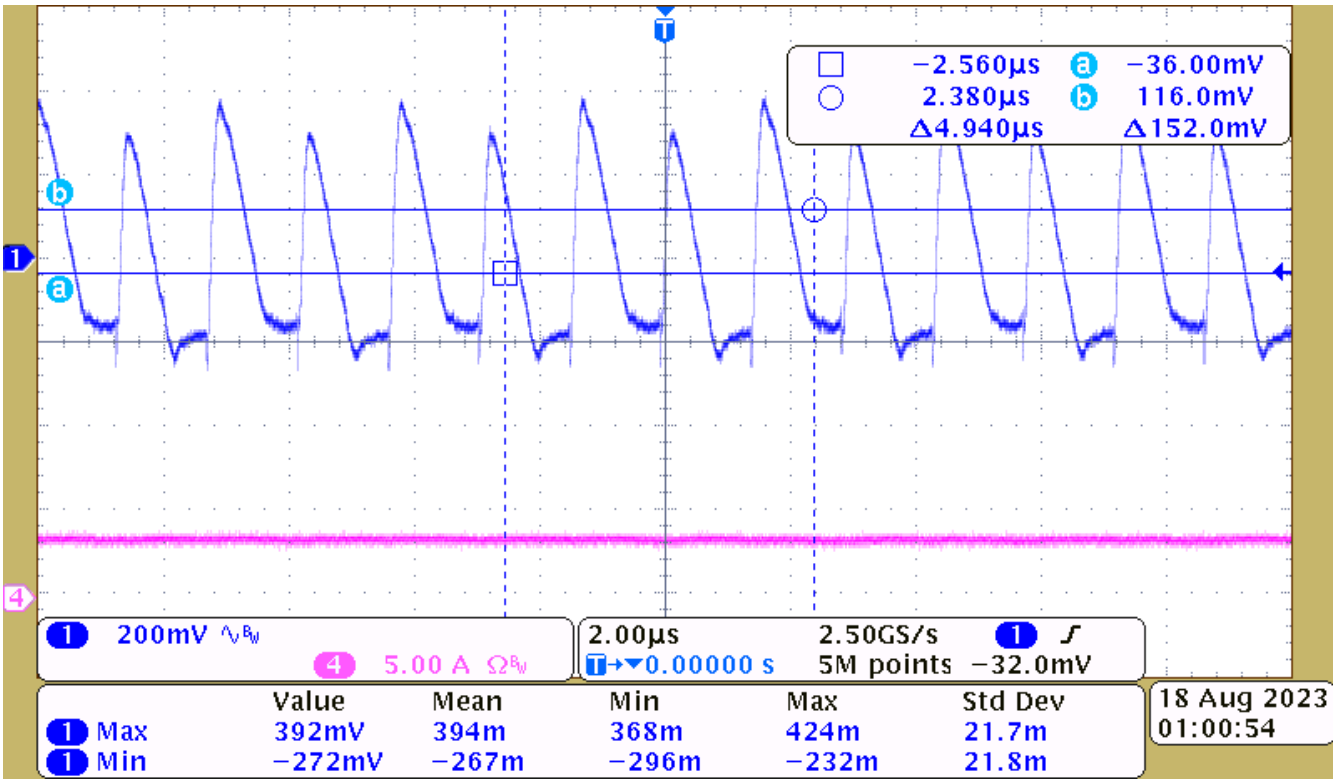


Figure 3-16. Output Voltage Ripple of Main Boost Stage at V_{IN} = 16 V, V_{OUT} = 45 V, I_{OUT} = 3.3 A

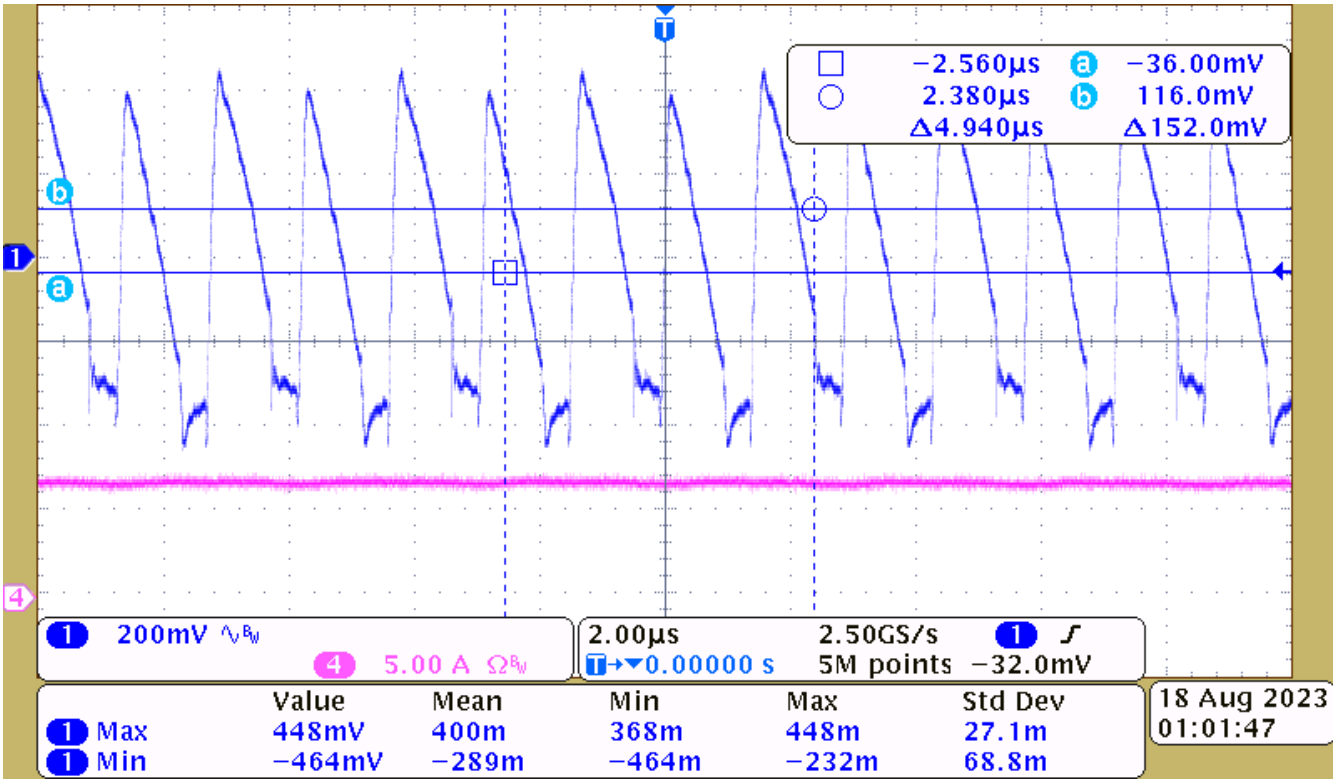


Figure 3-17. Output Voltage Ripple of Main Boost Stage at V_{IN} = 16 V, V_{OUT} = 45 V, I_{OUT} = 6.7 A

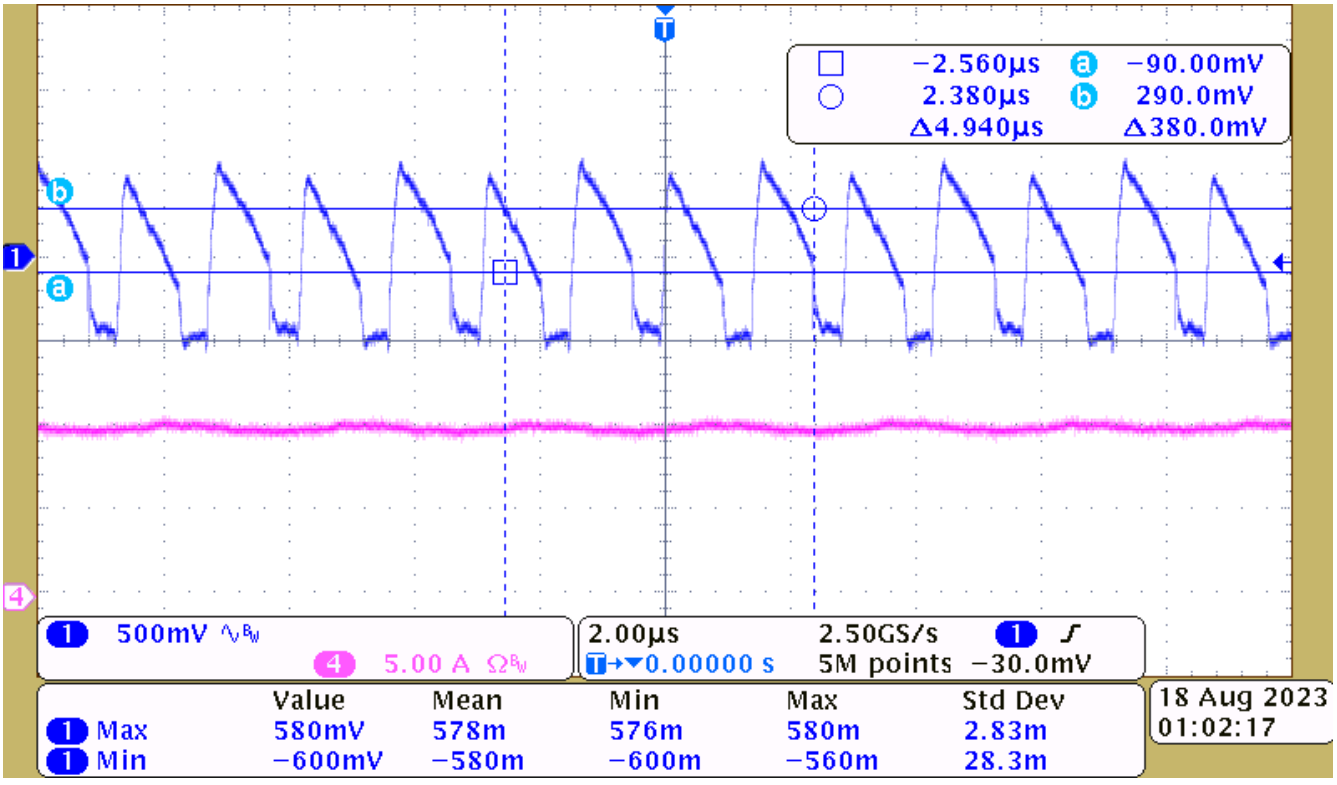


Figure 3-18. Output Voltage Ripple of Main Boost Stage at V_{IN} = 16 V, V_{OUT} = 45 V, I_{OUT} = 10 A

3.3 Load Transients

Load transient response of the Main Boost Stage at various input voltages undergoing a 25% to 75% (2.5 A to 7.5 A) and a 0% to 100% (0 A to 10 A) load step is shown in the following figures.

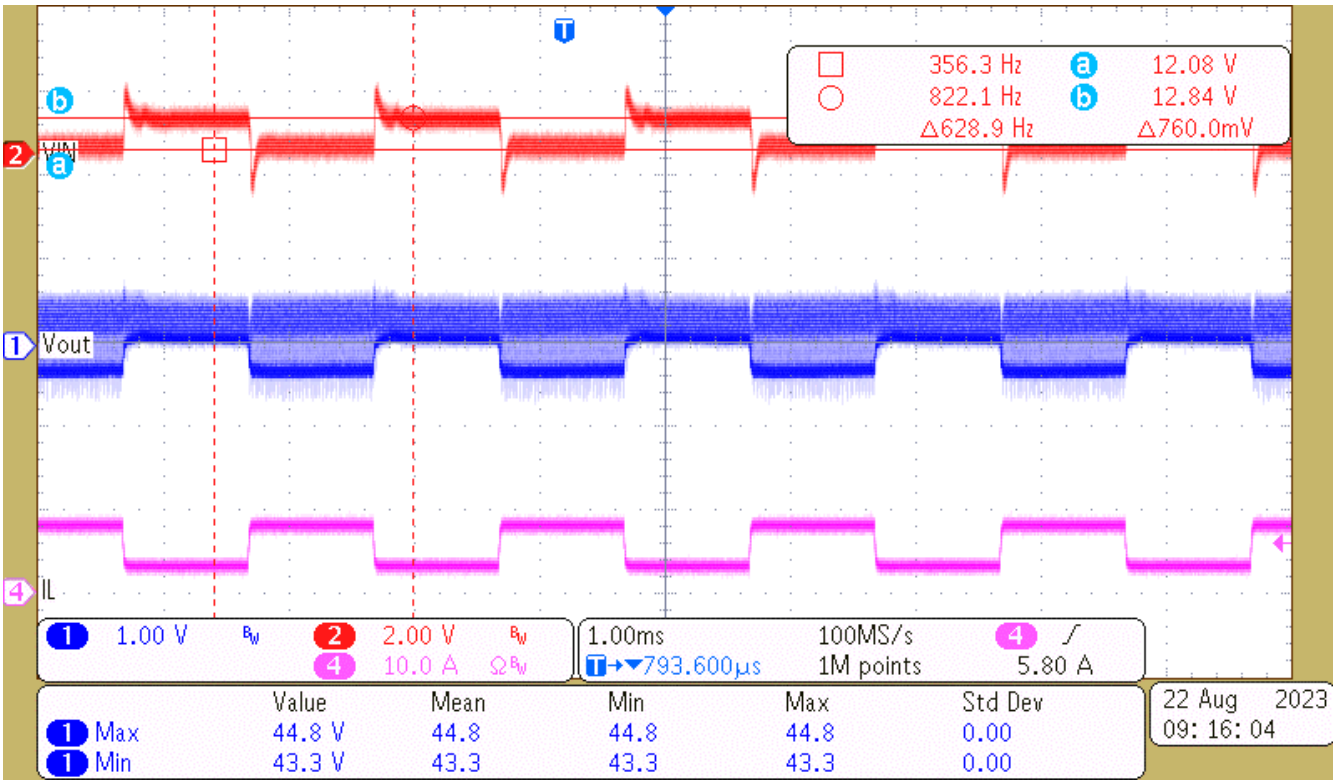


Figure 3-19. Main Boost Stage Load Transient Response, 12-V Input, 45-V Output, 2.5-A to 7.5-A Load Step

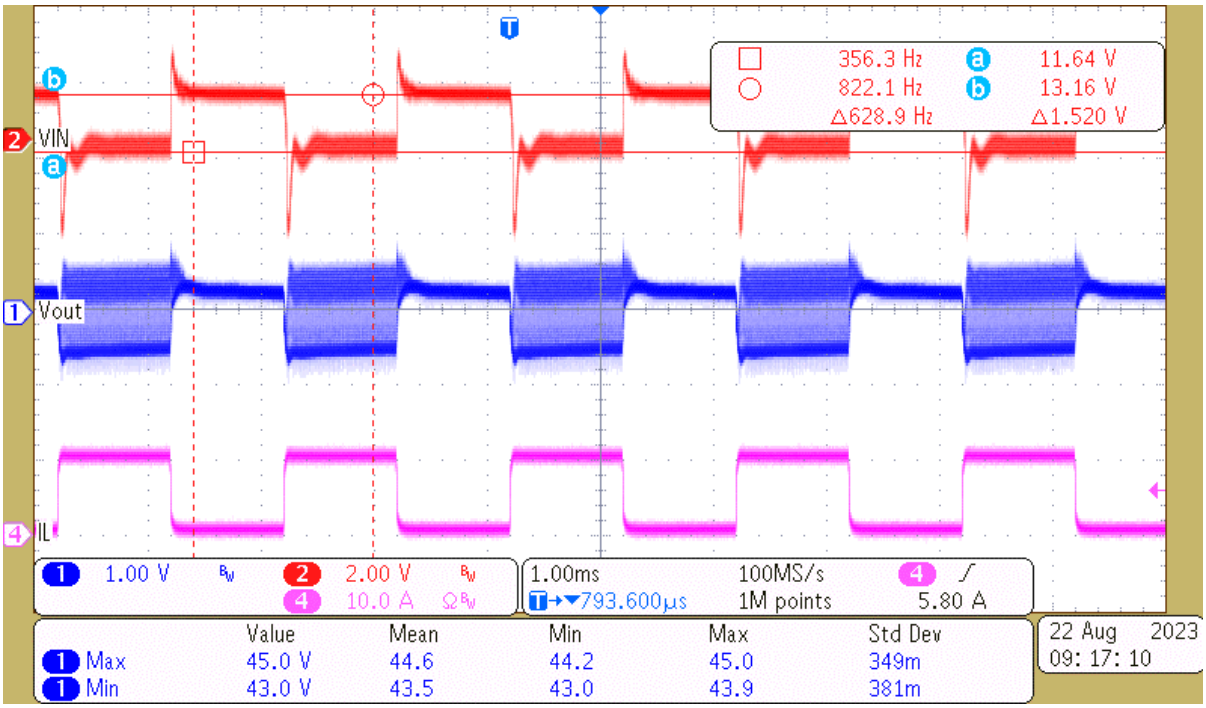


Figure 3-20. Main Boost Stage Load Transient Response, 12-V Input, 45-V Output, 0-A to 10-A Load Step

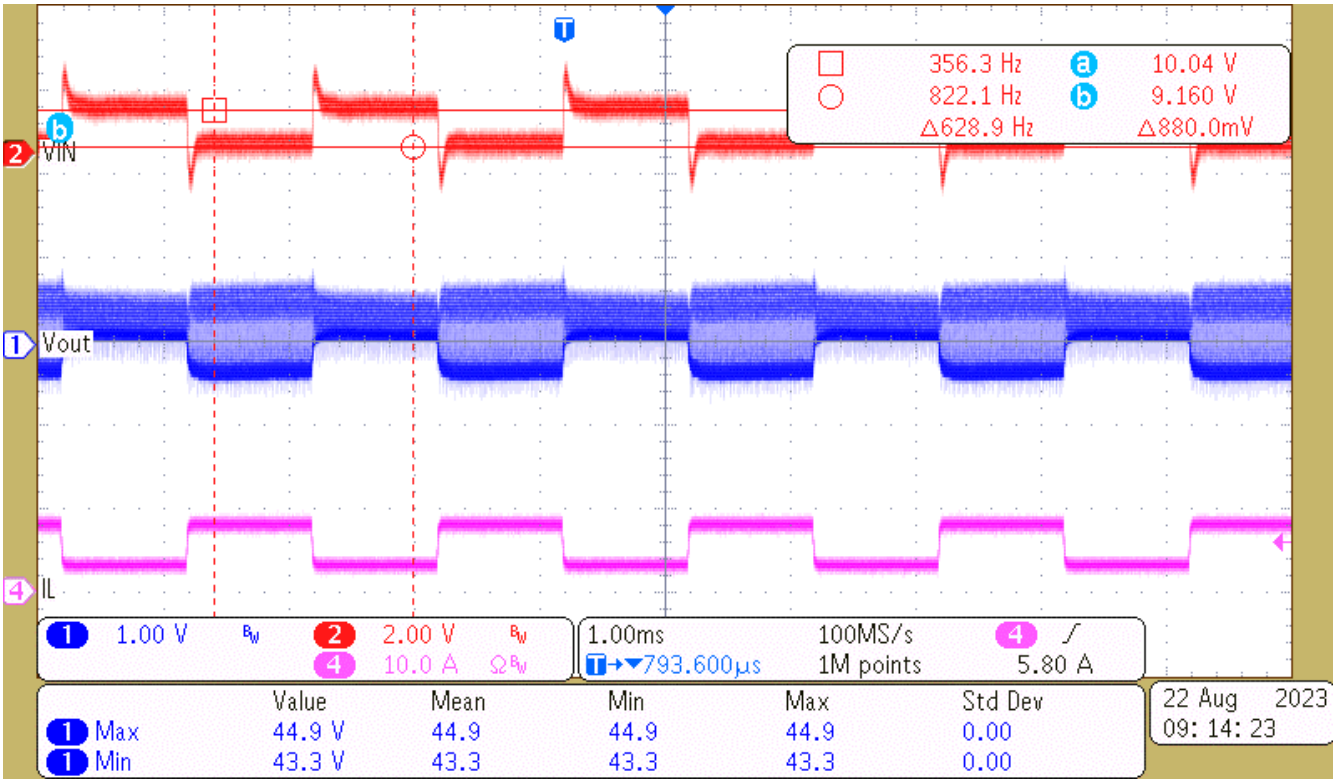


Figure 3-21. Main Boost Stage Load Transient Response, 9-V Input, 45-V Output, 2.5-A to 7.5-A Load Step

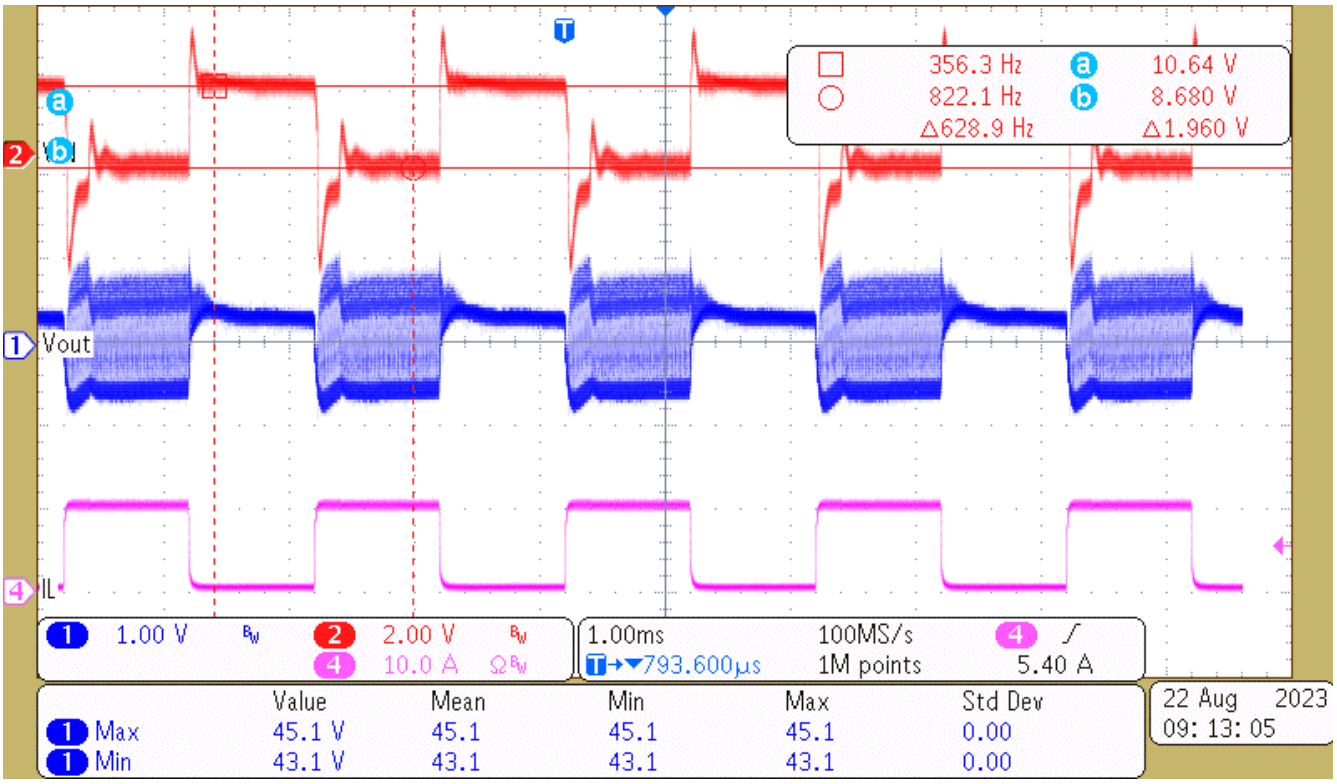


Figure 3-22. Main Boost Stage Load Transient Response, 9-V Input, 45-V Output, 0-A to 10-A Load Step

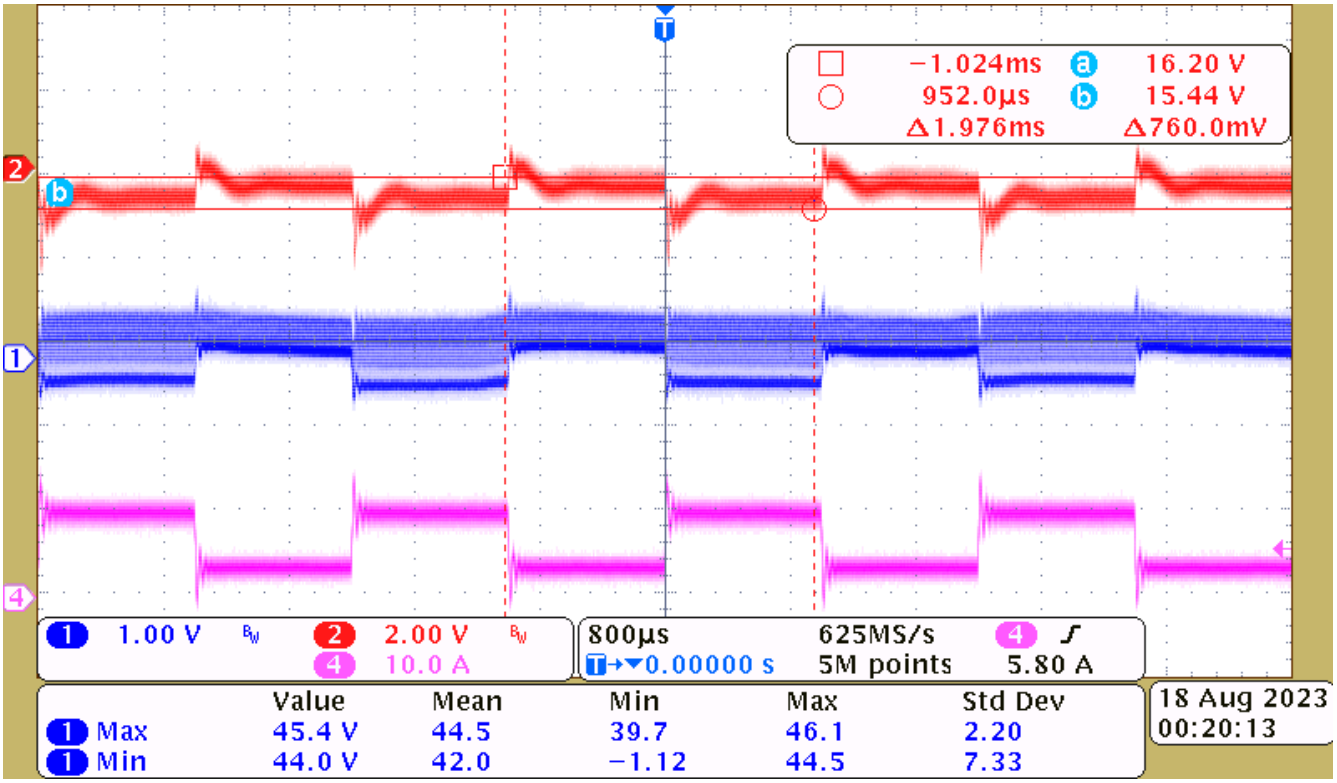


Figure 3-23. Main Boost Stage Load Transient Response, 16-V Input, 45-V Output, 2.5-A to 7.5-A Load Step

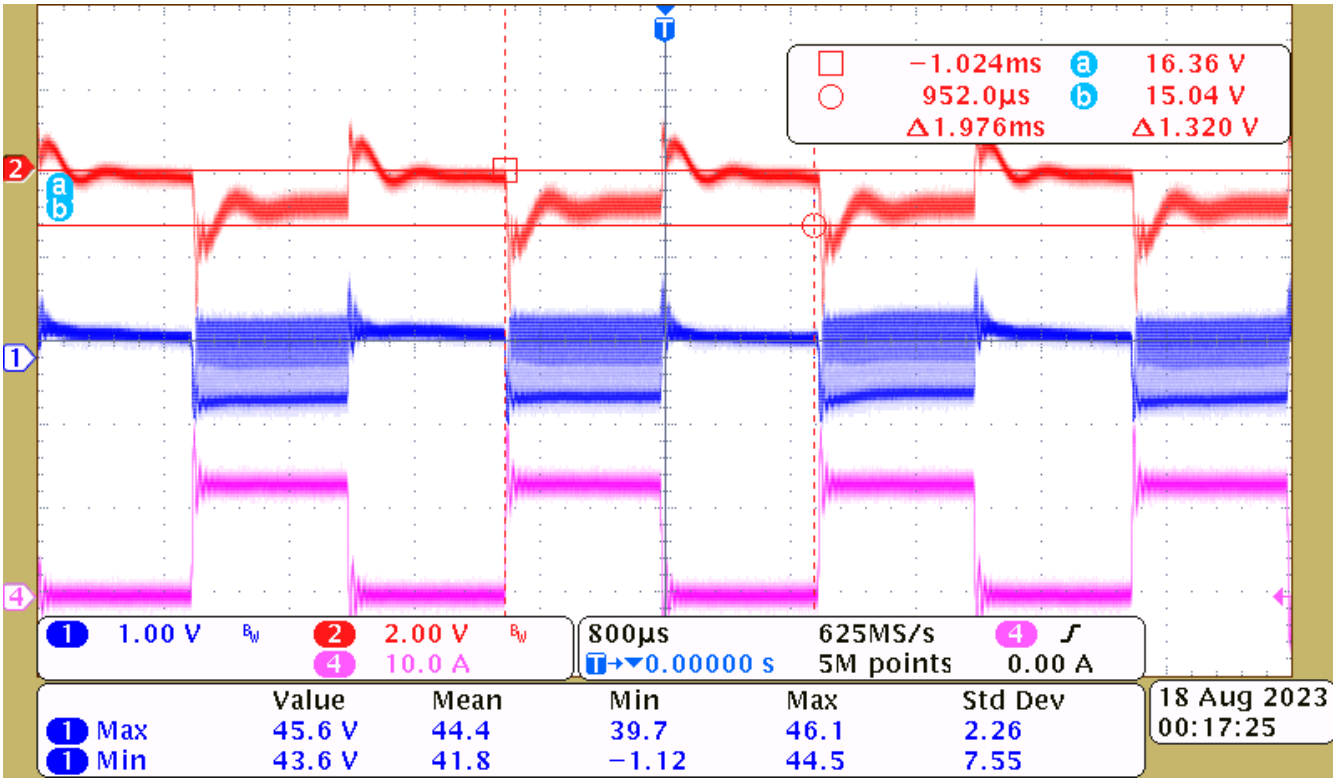


Figure 3-24. Main Boost Stage Load Transient Response, 16-V Input, 45-V Output, 0-A to 10-A Load Step

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