Test Report: PMP23242

Sitara™ MPU Discrete Automotive Power Reference Design

Description

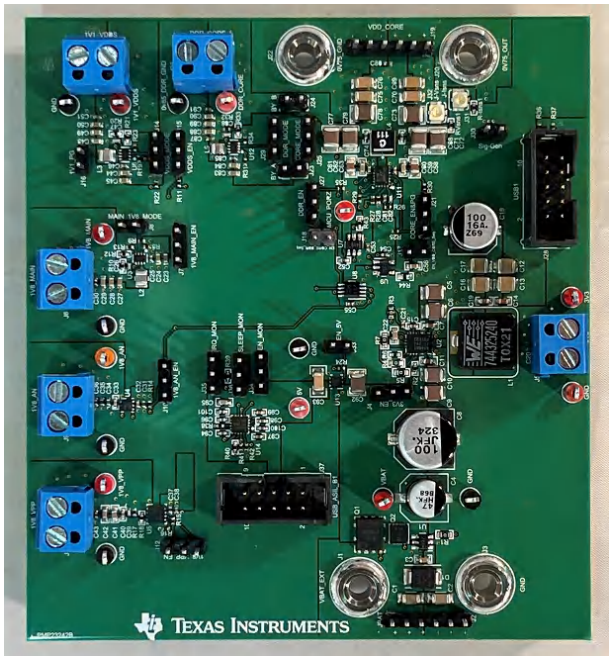
This reference design implements a power tree using low cost, automotive-qualified discrete voltage regulators, and details the specific power up or power down sequencing requirements for the AM62x-Q1 processor family.

Features

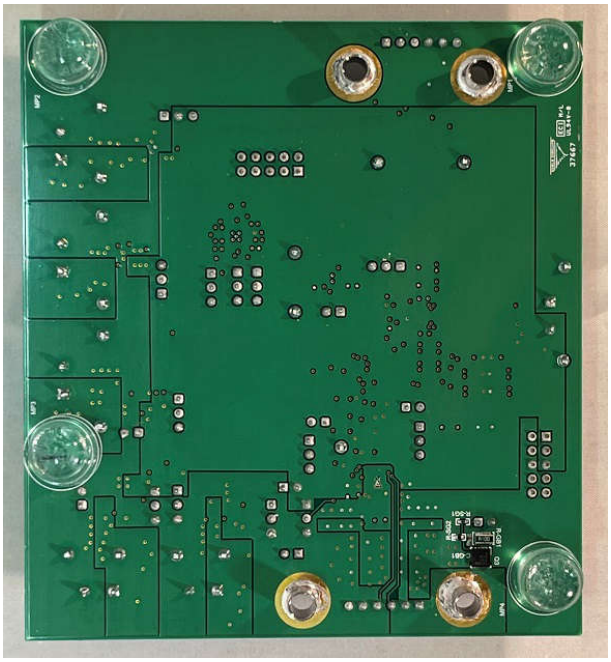
- Low-cost discrete automotive design
- Easily scalable to other AM62x-Q1 Sitara Microprocessor Units (MPUs)

Applications

- Mirror replacement, camera mirror system
- Front camera
- Driver monitoring
- Automotive cluster Display



Top of Board



Bottom of Board

1 Power Requirements

The AM62x-Q1 family of devices require four to eight power supply groups, depending on the system requirements. The power supply groups include the core supply (VDD_CORE), RAM supply (VDDR_CORE), DDR PHY IO supply (VDDS_DDR), 3.3-V digital supply (VDDSHVx), SD card interface supply (VDDSHV5), 1.8-V digital supply (VDDSHVy), 1.8-V analog supply (VDDA_1P8), and a 1.8-V eFuse programming supply (VPP).

Figure 1-1 shows a block diagram of the AM62x-Q1 power tree. The different voltage regulators for these rails were chosen based on cost, good efficiency, load transient performance, and power up or power down sequencing requirements. This reference design does not support any low-power modes for the AM62x-Q1.

The LM61480-Q1 buck converter is used to supply the 3.3 V, VDDSHVx, the 3.3-V VDDSHV5 rail, as well as act as the input supply for the rest of the voltage regulators. A couple of logic gates along with an RC delay are also required for proper sequencing of the VDD_CORE and VDDR_CORE rails. A logic gate and a programmable delay supervisor, TPS3808E-Q1 is also required for proper sequencing of MCU_PORz.

Figure 1-1 shows a detailed circuit schematic detailing the power design and sequencing.

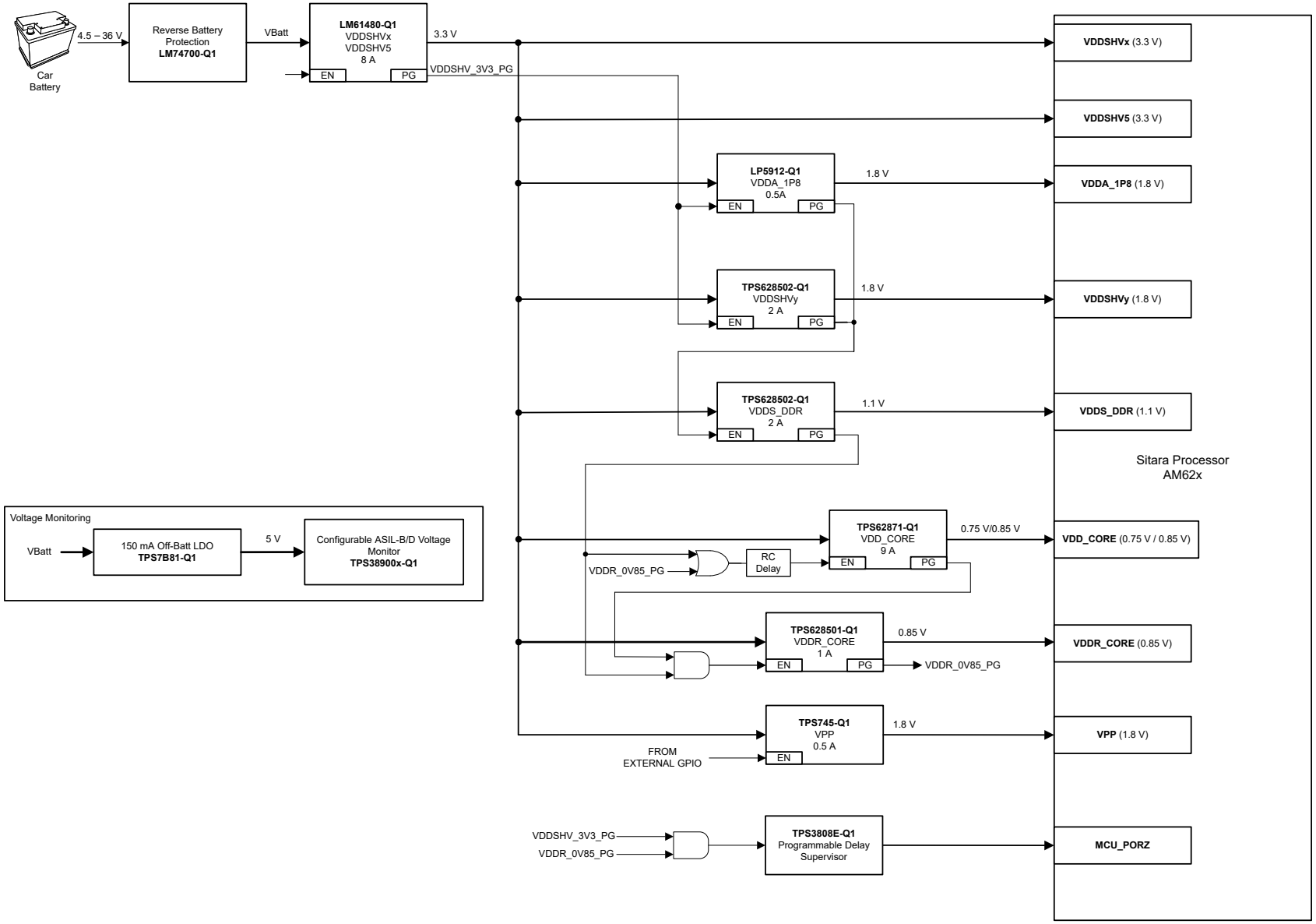


Figure 1-1. AM62x-Q1 Power Tree Block Diagram

Table 1-1 details the AM62x-Q1 power requirements.

Table 1-1. AMP62x-Q1 Power Requirements

Power Supply	V_{OUT} (V)	I_{OUT} (mA)	Output Voltage (V)	Power Supply	Nominal Rating	Grouping
LM61840-Q1	3.3	8000	3.3	VDDSHV_MCU, VDDSHV0, VDDSHV2, VDDSHV3, VDDSHV_CANUART, VDDA_3P3_USB, VMON_3P3_SOC	3.3 V ±5%	VDDSHVx
TPS628502-Q1	Adjustable	2000	1.8	VDDSHV1, VDDSHV4, VDDSHV5, VDDSHV6	1.8 V ±5%	VDDSHVy
LP5912-Q1	1.8	500	1.8	VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_PLL3, VDDA_PLL4, VDDA_PLL5, VDDA_1P8_CSIRX0, VDDA_1P8_USB, VMON_1P8_SOC, VDDA_TEMP0, VDDA_TEMP1, VDDA_TEMP2	1.8 V ±5%	VDDA_1P8
TPS628502-Q1	Adjustable	2000	1.1	VDDS_DDR, VDDS_DDR_C	1.1 V ±5%	VDDS_DDR
TPS628501-Q1	Adjustable	1000	0.85	VDDR_CORE	0.85 V ±5%	VDDR_CORE
TPS62871-Q1	Adjustable	9000	0.75	VDD_CORE, VDD_CANUART, VDDA_CORE_CSIRX0, VDDA_CORE_USB, VDDA_DDR_PLL0	0.75 V ±5%	VDD_CORE
TPS745-Q1	Adjustable	500	1.8	VPP	1.8 V ±5%	VPP

1.1 Power-On Sequence

The AM62x-Q1 requires the different power rails to be ramped up in a certain sequence to provide reliable and fault-free operation. Figure 1-2 shows the power-on sequence of the power rails. Shaded regions in Figure 1-2 indicate that a particular rail is allowed to ramp up at any time within this region. The 3V3, VDDSHVx and VDDSHV5 rails are the first rails to be powered on. Next, the 1.8-V analog and digital rails are ramped up. This is followed by the 1.1-V DDR rail. By ramping up the 0.75 V, VDD_CORE before the 0.85 V, VDDR_CORE, sequence makes sure that the VDDR_CORE voltage never exceeds the VDD_CORE voltage by 180 mV. If VDD_CORE is operating at 0.85 V, both VDD_CORE and VDDR_CORE can be supplied by the same rail and there is no ramp up requirement between them. The 1.8 V, VPP is the eFuse programming supply, which is left floating (HiZ) or grounded during power-up or power-down sequences and during normal device operation. This supply is only sourced while programming.

For a detailed description of the power-on sequencing, see the power-up sequencing section of the *AM62Ax Sitara™ Processors* data sheet.

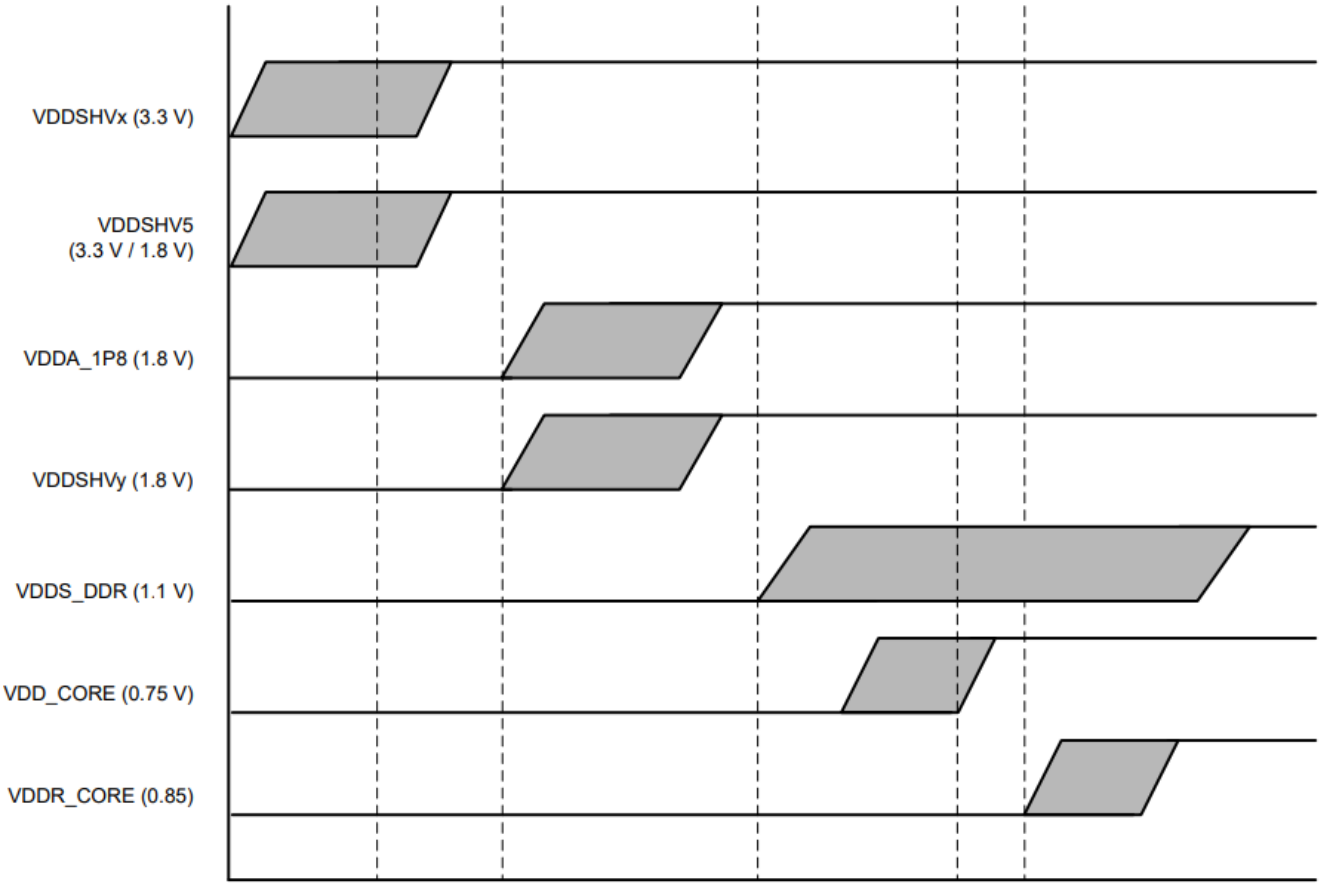


Figure 1-2. AM62x-Q1 Power-On Sequence

1.2 Power-Off Sequence

As described in the power-down sequencing section of the *AM62Ax Sitara™ Processors* data sheet, all power rails except VDD_CORE and VDDR_CORE can be ramped down independent of each other. If VDD_CORE is operating at 0.75 V, ramp down VDD_CORE after the 0.85 V VDDR_CORE. For the case where VDD_CORE and VDDR_CORE both run from a common 0.85-V supply, there is no ramp down requirement between them.

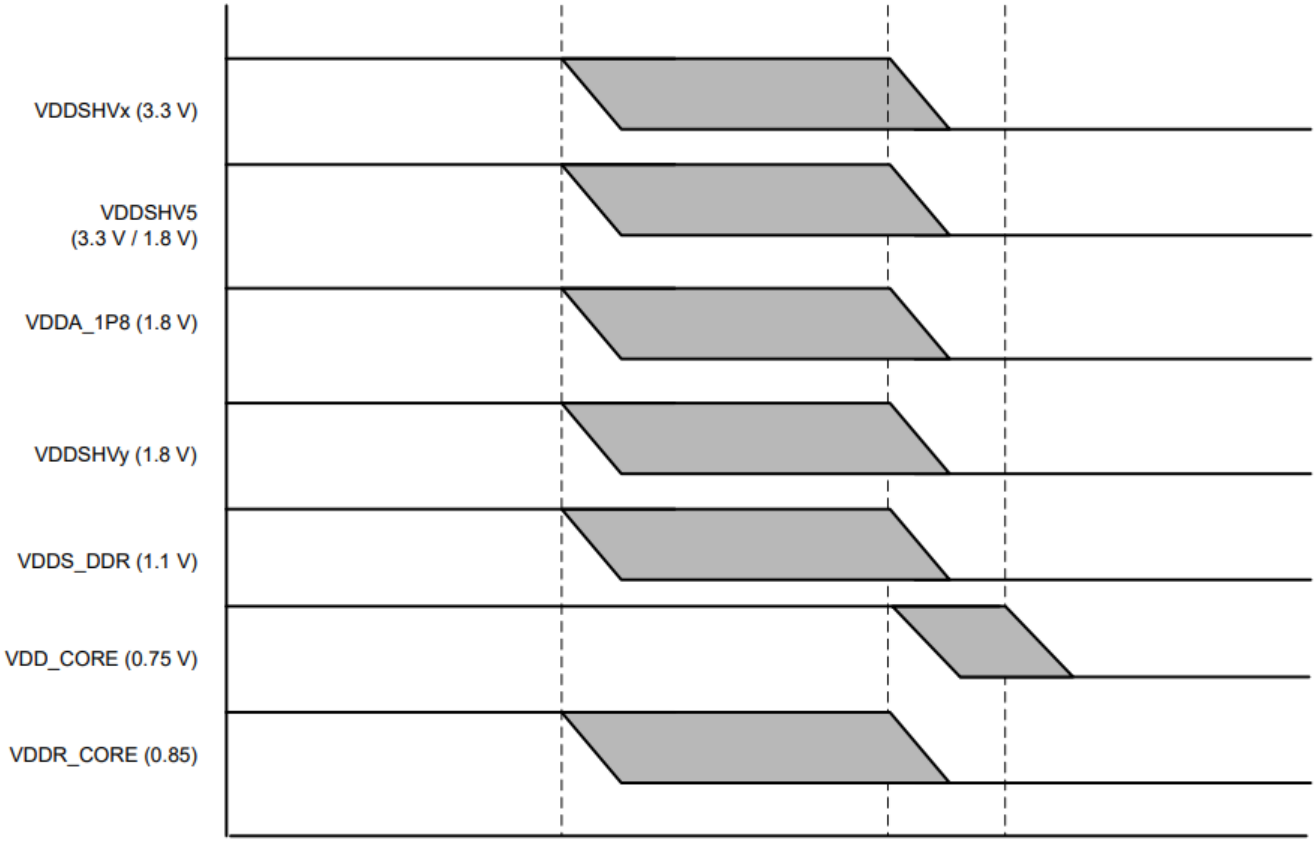


Figure 1-3. AM62x-Q1 Power-Off Sequence

1.3 Required Equipment

- Power supply (capable of 4.5 V to 36 V and 6 A)
- Electronic loads
- DMMs
- Oscilloscope
- USB2ANY interface adapter

1.4 Dimensions

The PCB is 110.67 mm × 100.28 mm.

2 Testing and Results

2.1 Efficiency Graphs

Figure 2-1 shows the efficiency of the LM61480-Q1 for an 8-V, 13.5-V, and 16-V input with the output being swept from 0 A to 8 A. The LM74700-Q1 reverse battery protection was powered on during this test and is factored into this measurement. This converter also supplies the power to the VDDSHVx rails of the AM62x-Q1 and acts as the input supply for the rest of the voltage regulators and logic devices.

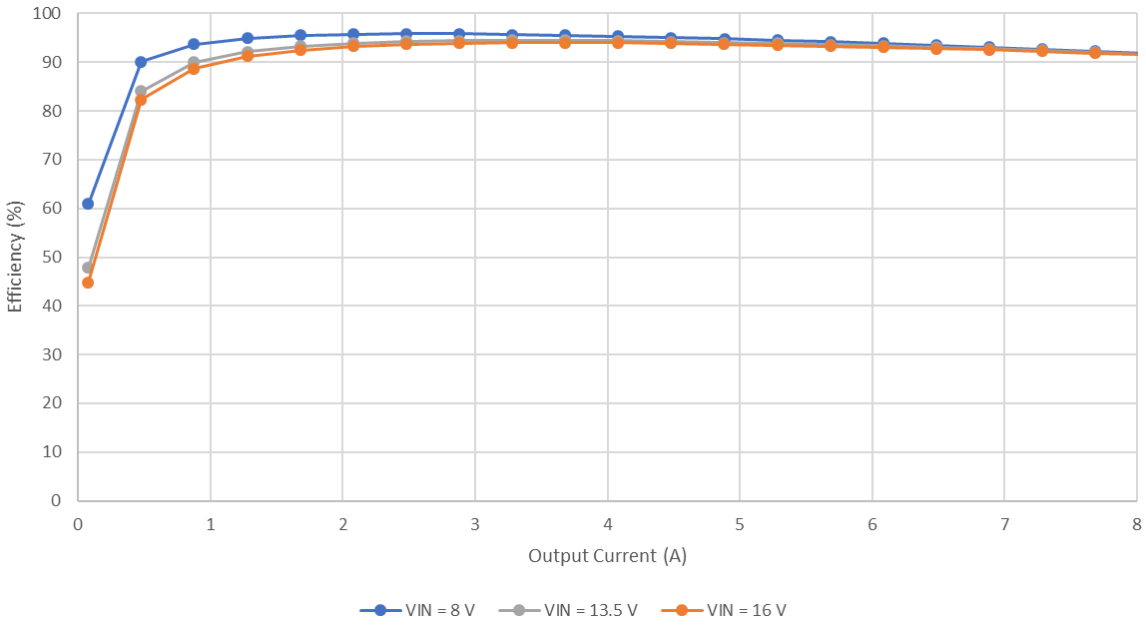


Figure 2-1. LM61480-Q1 Efficiency, 3.3-V Output

Figure 2-2 shows the TPS628502-Q1 efficiency for a 3.3-V input that is supplied directly from an external benchtop supply. The output was swept from 0 A to 2 A. This converter supplies the power to the VDDSHVy rails of the AM62x-Q1.

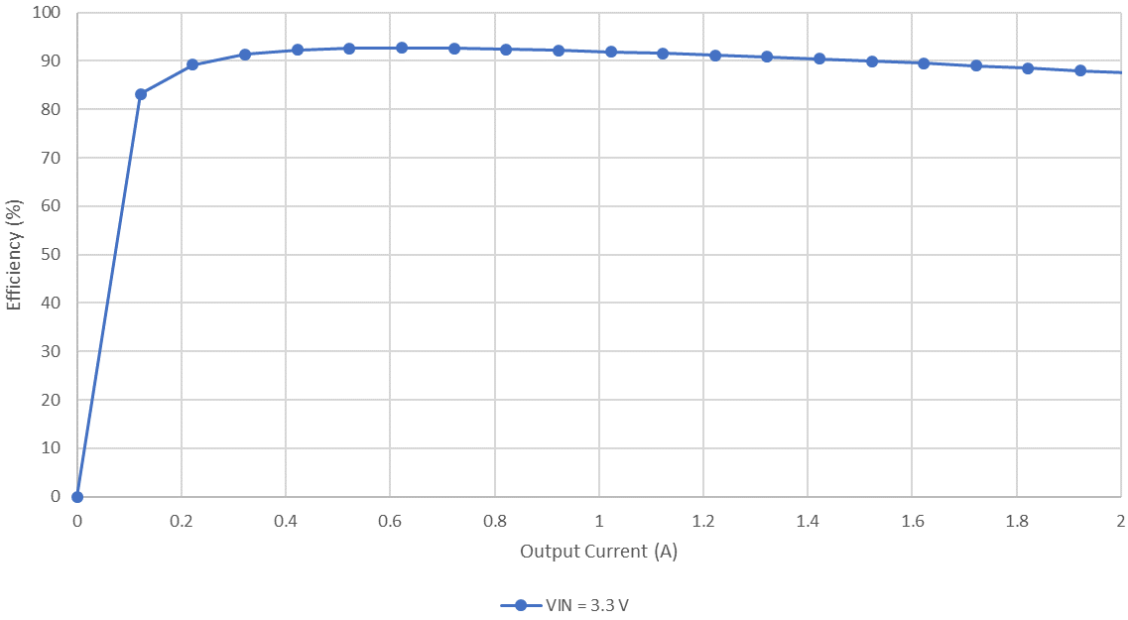


Figure 2-2. TPS628502-Q1 Efficiency, 1.8-V Output

Figure 2-3 shows the TPS628502-Q1 efficiency for a 3.3-V input that is supplied directly from an external benchtop supply. The output was swept from 0 A to 2 A. This converter supplies the power to the AM62x-Q1 VDDS_DDR rails.

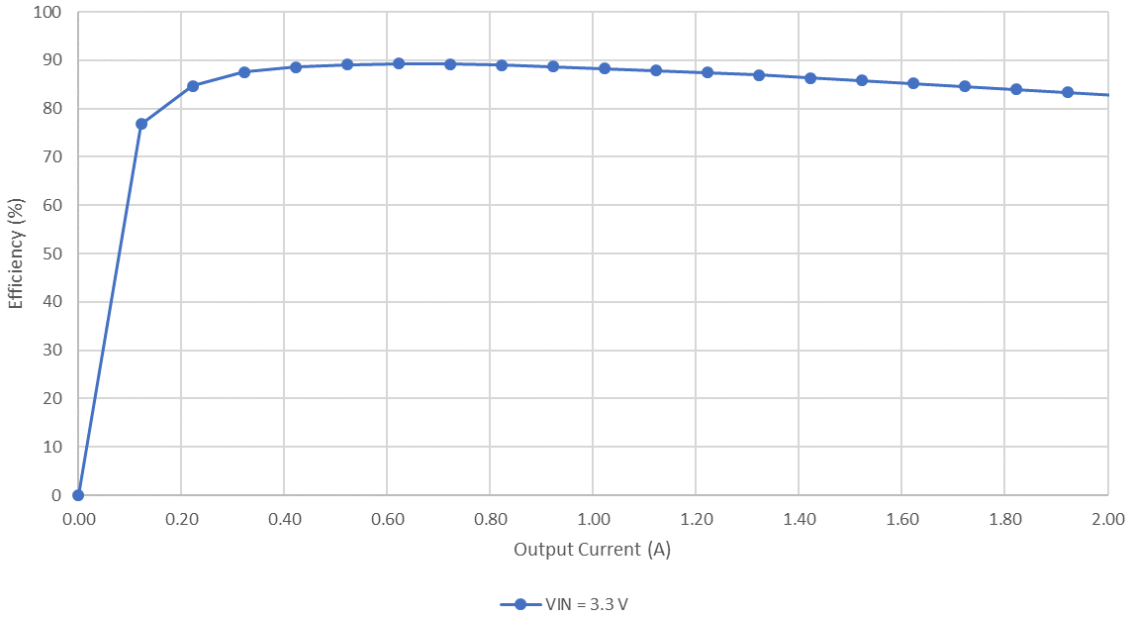


Figure 2-3. TPS628502-Q1 Efficiency, 1.1-V Output

Figure 2-4 shows the TPS628501-Q1 efficiency for a 3.3-V input that is supplied directly from an external benchtop supply. The output was swept from 0 A to 1 A. This converter supplies the power to the AM62x-Q1 VDDR_CORE rails.

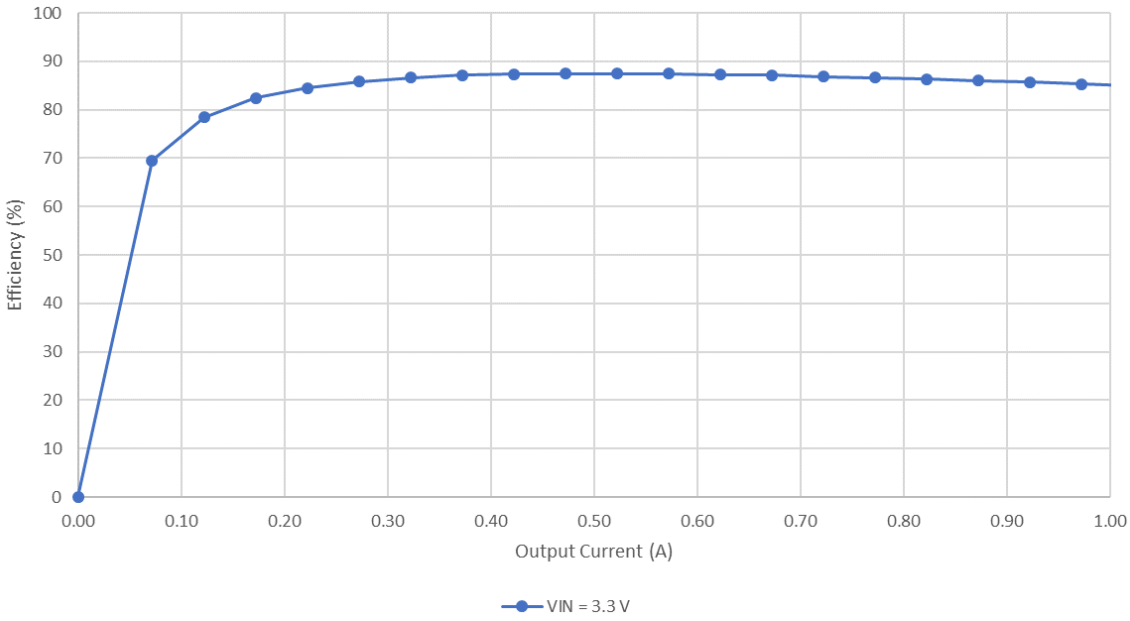


Figure 2-4. TPS628502-Q1 Efficiency, 0.85-V Output

The VDD_CORE can operate at 0.75 V or 0.85 V depending on the configuration of VDDR_CORE. Figure 2-5 and Figure 2-6 show the TPS62871-Q1 efficiency for a 3.3-V input that is supplied from an external benchtop supply with a 0.75-V and 0.85-V output, respectively. Each output was swept from 0 A to 9 A. This converter supplies the power to the AM62x-Q1 VDD_CORE rails.

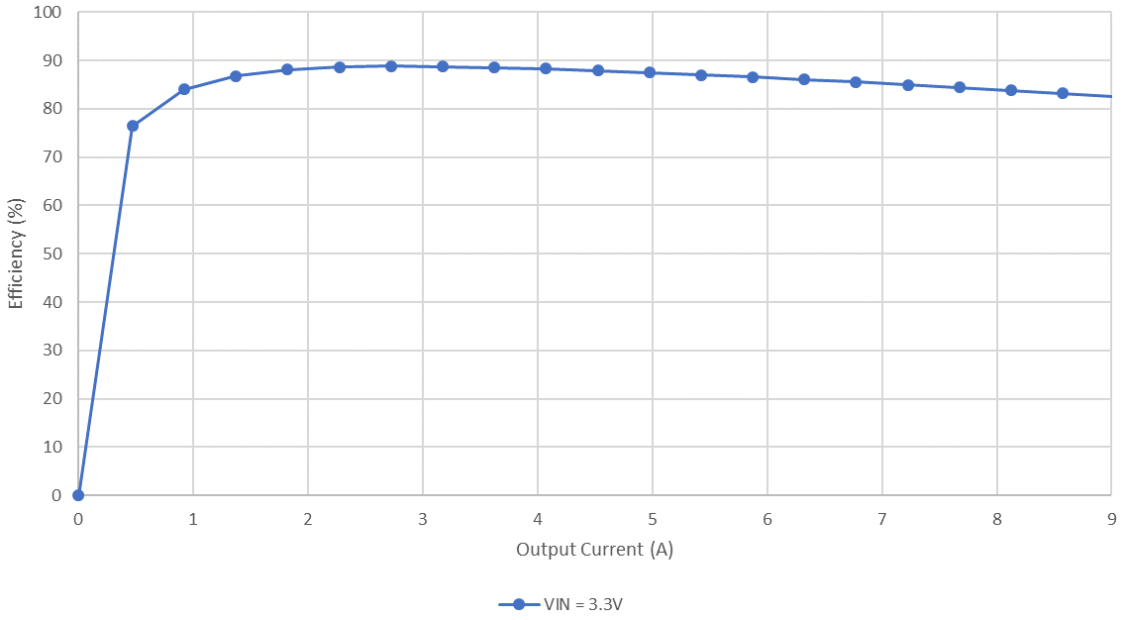


Figure 2-5. TPS62871-Q1 Efficiency, 0.75-V Output

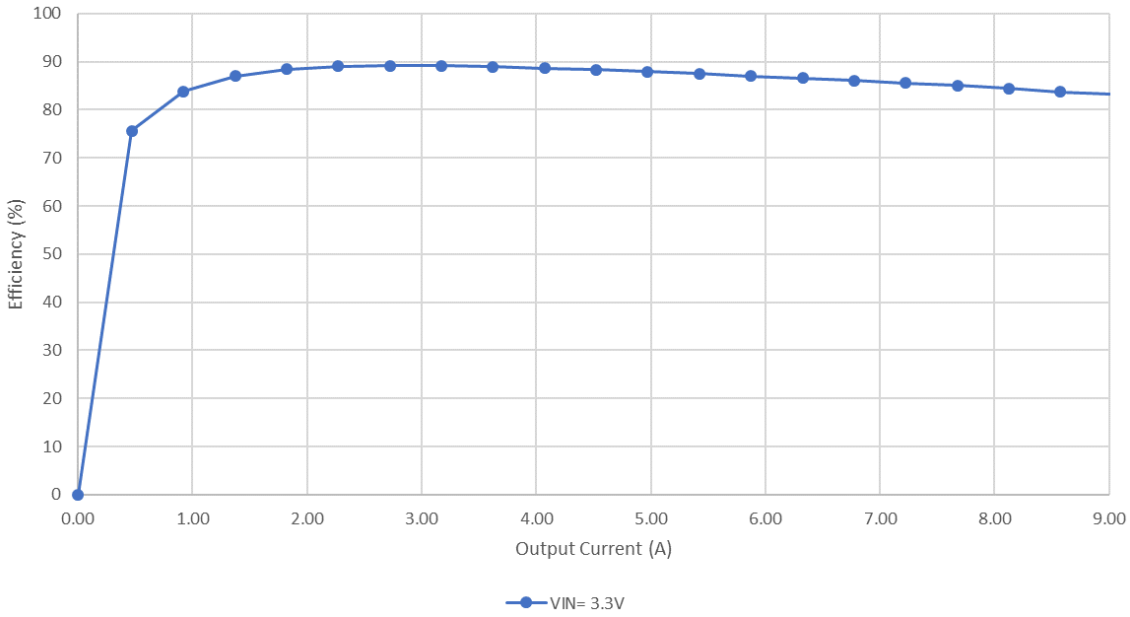


Figure 2-6. TPS62871-Q1 Efficiency, 0.85-V Output

2.2 Efficiency Data

Table 2-1 shows the LM61480-Q1 efficiency data at 8-V input and 3.3-V output.

Table 2-1. LM61480-Q1 Efficiency, 8-V Input, 3.3-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
8.073	0.051	3.301	0.08	0.42	0.25	60.87
8.051	0.218	3.300	0.48	1.75	1.58	90.07
8.027	0.385	3.300	0.88	3.09	2.90	93.70
8.005	0.555	3.300	1.28	4.44	4.22	94.98
7.981	0.727	3.300	1.68	5.80	5.54	95.54
7.958	0.900	3.300	2.08	7.16	6.86	95.78
7.937	1.075	3.300	2.48	8.54	8.18	95.86
7.957	1.247	3.299	2.88	9.92	9.50	95.80
7.940	1.425	3.299	3.28	11.31	10.82	95.68
7.926	1.604	3.299	3.68	12.71	12.14	95.52
7.909	1.787	3.299	4.08	14.13	13.47	95.31
7.893	1.970	3.299	4.48	15.55	14.79	95.06
7.875	2.157	3.298	4.88	16.99	16.11	94.80
7.857	2.347	3.298	5.28	18.44	17.42	94.51
7.851	2.535	3.298	5.68	19.90	18.74	94.19
7.837	2.727	3.297	6.08	21.37	20.06	93.86
7.814	2.926	3.297	6.48	22.86	21.38	93.51
7.825	3.115	3.296	6.88	24.37	22.70	93.12
7.802	3.320	3.296	7.28	25.90	24.01	92.71
7.801	3.518	3.295	7.69	27.45	25.33	92.28
7.812	3.714	3.295	8.09	29.01	26.64	91.83

Table 2-2 shows the LM61480-Q1 efficiency data at 13.5-V input and 3.3-V output.

Table 2-2. LM61480-Q1 Efficiency, 13.5-V Input, 3.3-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
13.654	0.039	3.301	0.08	0.53	0.25	47.80
13.646	0.137	3.300	0.48	1.87	1.57	84.09
13.638	0.236	3.300	0.88	3.22	2.90	90.01
13.629	0.336	3.300	1.28	4.58	4.22	92.18
13.622	0.436	3.300	1.68	5.94	5.54	93.28
13.615	0.537	3.300	2.08	7.30	6.86	93.92
13.502	0.643	3.300	2.48	8.68	8.18	94.27
13.464	0.747	3.299	2.88	10.06	9.50	94.44
13.499	0.848	3.299	3.28	11.45	10.82	94.52
13.530	0.950	3.299	3.68	12.85	12.14	94.47
13.502	1.057	3.299	4.08	14.27	13.46	94.37
13.488	1.163	3.299	4.48	15.69	14.78	94.24
13.467	1.271	3.298	4.88	17.12	16.10	94.05
13.458	1.379	3.298	5.28	18.56	17.42	93.86
13.428	1.491	3.298	5.68	20.01	18.74	93.63
13.418	1.602	3.297	6.08	21.49	20.06	93.34
13.418	1.712	3.297	6.48	22.97	21.38	93.08
13.409	1.824	3.297	6.88	24.46	22.70	92.77

Table 2-2. LM61480-Q1 Efficiency, 13.5-V Input, 3.3-V Output (continued)

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
13.402	1.938	3.296	7.28	25.98	24.01	92.43
13.392	2.054	3.296	7.69	27.51	25.33	92.06
13.381	2.172	3.295	8.09	29.06	26.64	91.68

Table 2-3 shows the LM61480-Q1 efficiency data at 16-V input and 3.3-V output.

Table 2-3. LM61480-Q1 Efficiency, 16-V Input, 3.3-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
16.183	0.035	3.301	0.08	0.57	0.26	44.84
16.156	0.119	3.300	0.48	1.92	1.58	82.34
16.156	0.202	3.300	0.88	3.27	2.90	88.72
16.142	0.286	3.300	1.28	4.62	4.22	91.21
16.118	0.372	3.300	1.68	5.99	5.54	92.50
16.099	0.457	3.300	2.08	7.36	6.86	93.25
16.065	0.544	3.300	2.48	8.73	8.18	93.68
16.073	0.629	3.299	2.88	10.12	9.50	93.91
16.040	0.717	3.299	3.28	11.51	10.82	94.04
16.005	0.807	3.299	3.68	12.91	12.14	94.04
16.029	0.894	3.299	4.08	14.33	13.46	93.98
16.022	0.983	3.298	4.48	15.75	14.78	93.88
16.008	1.073	3.298	4.88	17.18	16.10	93.73
16.076	1.158	3.298	5.28	18.62	17.42	93.54
16.071	1.249	3.298	5.68	20.08	18.74	93.33
16.062	1.342	3.297	6.08	21.55	20.06	93.09
16.049	1.435	3.297	6.48	23.03	21.38	92.82
16.032	1.530	3.296	6.88	24.52	22.69	92.53
16.009	1.626	3.296	7.28	26.04	24.01	92.22
15.995	1.723	3.296	7.68	27.57	25.33	91.87
16.040	1.815	3.295	8.09	29.12	26.64	91.50

Table 2-4 shows TPS62802-Q1 efficiency data at 3.3-V input, 1.8-V output.

Table 2-4. TPS62802-Q1 Efficiency 3.3-V Input, 1.8-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.335	0.079	1.809	0.122	0.26	0.22	83.18
3.329	0.135	1.809	0.222	0.45	0.40	89.22
3.326	0.192	1.808	0.322	0.64	0.58	91.38
3.321	0.249	1.808	0.422	0.83	0.76	92.28
3.317	0.307	1.807	0.522	1.02	0.94	92.59
3.311	0.366	1.807	0.622	1.21	1.12	92.67
3.305	0.426	1.806	0.722	1.41	1.30	92.64
3.299	0.487	1.806	0.822	1.61	1.48	92.43
3.294	0.548	1.805	0.922	1.81	1.66	92.20
3.289	0.610	1.805	1.022	2.01	1.85	91.91
3.273	0.676	1.805	1.122	2.21	2.03	91.57
3.268	0.740	1.804	1.222	2.42	2.21	91.20

Table 2-4. TPS62802-Q1 Efficiency 3.3-V Input, 1.8-V Output (continued)

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.261	0.805	1.804	1.323	2.63	2.39	90.82
3.247	0.874	1.803	1.423	2.84	2.57	90.39
3.241	0.942	1.803	1.523	3.05	2.75	89.94
3.234	1.011	1.802	1.623	3.27	2.92	89.48
3.226	1.081	1.802	1.723	3.49	3.10	89.00
3.219	1.153	1.802	1.823	3.71	3.28	88.49
3.211	1.226	1.801	1.923	3.94	3.46	87.97
3.205	1.300	1.801	2.023	4.17	3.64	87.43

Table 2-5 shows the TPS628502-Q1 efficiency data at 3.3-V input and 1.1-V output.

Table 2-5. TPS628502-Q1 Efficiency, 3.3-V Input, 1.1-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.339	0.052	1.099	0.122	0.17	0.13	76.84
3.336	0.086	1.099	0.222	0.29	0.24	84.71
3.333	0.121	1.098	0.322	0.40	0.35	87.49
3.330	0.157	1.098	0.422	0.52	0.46	88.59
3.326	0.193	1.097	0.522	0.64	0.57	89.12
3.323	0.230	1.097	0.622	0.76	0.68	89.26
3.320	0.267	1.097	0.722	0.89	0.79	89.20
3.316	0.305	1.096	0.822	1.01	0.90	88.97
3.315	0.344	1.096	0.922	1.14	1.01	88.68
3.312	0.383	1.095	1.022	1.27	1.12	88.30
3.309	0.423	1.095	1.122	1.40	1.23	87.87
3.308	0.463	1.094	1.222	1.53	1.34	87.39
3.305	0.504	1.094	1.323	1.66	1.45	86.89
3.301	0.546	1.094	1.423	1.80	1.56	86.34
3.298	0.588	1.093	1.523	1.94	1.66	85.79
3.295	0.632	1.093	1.623	2.08	1.77	85.21
3.291	0.676	1.092	1.723	2.22	1.88	84.61
3.288	0.720	1.092	1.823	2.37	1.99	84.00
3.285	0.766	1.092	1.923	2.52	2.10	83.36
3.282	0.813	1.091	2.023	2.67	2.21	82.71

Table 2-6 shows the TPS628501-Q1 efficiency data at 3.3-V input and 0.85-V output.

Table 2-6. TPS628501-Q1 Efficiency, 3.3-V Input, 0.85-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.341	0.026	0.847	0.072	0.087	0.061	69.47
3.340	0.039	0.847	0.122	0.131	0.103	78.43
3.339	0.053	0.847	0.172	0.177	0.146	82.43
3.338	0.067	0.847	0.222	0.223	0.188	84.46
3.337	0.080	0.846	0.272	0.268	0.230	85.80
3.335	0.094	0.846	0.322	0.315	0.273	86.63
3.334	0.108	0.846	0.372	0.361	0.315	87.09
3.333	0.123	0.846	0.422	0.409	0.357	87.35
3.332	0.137	0.846	0.472	0.457	0.399	87.47

Table 2-6. TPS628501-Q1 Efficiency, 3.3-V Input, 0.85-V Output (continued)

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.330	0.152	0.846	0.522	0.505	0.441	87.43
3.329	0.166	0.845	0.572	0.554	0.484	87.39
3.326	0.181	0.845	0.622	0.603	0.526	87.26
3.263	0.200	0.845	0.672	0.652	0.568	87.11
3.263	0.215	0.845	0.722	0.703	0.610	86.85
3.259	0.231	0.845	0.772	0.753	0.652	86.59
3.258	0.247	0.845	0.822	0.805	0.695	86.30
3.256	0.263	0.844	0.872	0.856	0.736	85.99
3.252	0.279	0.844	0.922	0.909	0.779	85.68
3.250	0.296	0.844	0.972	0.962	0.821	85.34
3.248	0.313	0.844	1.022	1.015	0.863	84.97

Table 2-7 shows the TPS62871-Q1 efficiency data at 3.3-V input and 0.75-V output.

Table 2-7. TPS62871-Q1 Efficiency, 3.3-V Input, 0.75-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.336	0.139	0.750	0.47	0.46	0.35	76.45
3.329	0.247	0.750	0.92	0.82	0.69	83.97
3.323	0.357	0.750	1.37	1.19	1.03	86.78
3.316	0.468	0.750	1.82	1.55	1.37	88.07
3.310	0.581	0.750	2.27	1.92	1.71	88.61
3.303	0.696	0.750	2.72	2.30	2.04	88.80
3.296	0.814	0.750	3.17	2.68	2.38	88.75
3.289	0.933	0.750	3.62	3.07	2.72	88.56
3.282	1.055	0.750	4.07	3.46	3.06	88.28
3.274	1.179	0.750	4.52	3.86	3.39	87.91
3.267	1.306	0.750	4.97	4.27	3.73	87.50
3.243	1.442	0.750	5.42	4.68	4.07	87.03
3.236	1.574	0.750	5.87	5.09	4.41	86.56
3.226	1.709	0.750	6.32	5.51	4.75	86.05
3.217	1.848	0.750	6.77	5.94	5.08	85.52
3.205	1.991	0.750	7.22	6.38	5.42	84.96
3.197	2.134	0.750	7.68	6.82	5.76	84.39
3.189	2.281	0.750	8.13	7.27	6.10	83.80
3.179	2.433	0.750	8.58	7.73	6.43	83.20
3.164	2.591	0.750	9.03	8.20	6.77	82.59

Table 2-8 shows the TPS62871-Q1 efficiency data at 3.3-V input and 0.85-V output.

Table 2-8. TPS62871-Q1 Efficiency, 3.3-V Input, 0.85-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.270	0.162	0.851	0.47	0.53	0.40	75.63
3.231	0.290	0.851	0.92	0.94	0.78	83.86
3.176	0.423	0.851	1.37	1.34	1.17	86.98
3.099	0.566	0.851	1.82	1.75	1.55	88.48
3.080	0.706	0.851	2.27	2.17	1.93	89.02
3.067	0.847	0.851	2.72	2.60	2.32	89.20
3.058	0.991	0.851	3.17	3.03	2.70	89.15

Table 2-8. TPS62871-Q1 Efficiency, 3.3-V Input, 0.85-V Output (continued)

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
3.047	1.138	0.851	3.62	3.47	3.08	88.97
3.041	1.286	0.851	4.07	3.91	3.47	88.69
3.024	1.442	0.851	4.52	4.36	3.85	88.35
3.032	1.588	0.851	4.97	4.81	4.23	87.97
3.003	1.757	0.851	5.42	5.28	4.62	87.52
2.991	1.921	0.851	5.87	5.74	5.00	87.05
2.982	2.085	0.851	6.32	6.22	5.38	86.57
2.970	2.257	0.851	6.77	6.70	5.77	86.05
2.970	2.421	0.851	7.22	7.19	6.15	85.54
3.000	2.560	0.851	7.67	7.68	6.53	85.06
2.966	2.761	0.851	8.13	8.19	6.92	84.45
2.977	2.930	0.851	8.58	8.72	7.30	83.70
2.959	3.116	0.851	9.03	9.22	7.68	83.29

2.3 Thermal Images

The thermal images in Figure 2-7 and Figure 2-8 show operation at 12-V input and maximum current for each output rail on the highest power AM62x processor with no airflow after the board had reached thermal equilibrium. Figure 2-7 is a thermal image when the VDD_CORE was 0.75 V with an output current of 5.7 A. Figure 2-8 shows a thermal image when VDD_CORE was 0.85 V with an output current of 6.9 A.

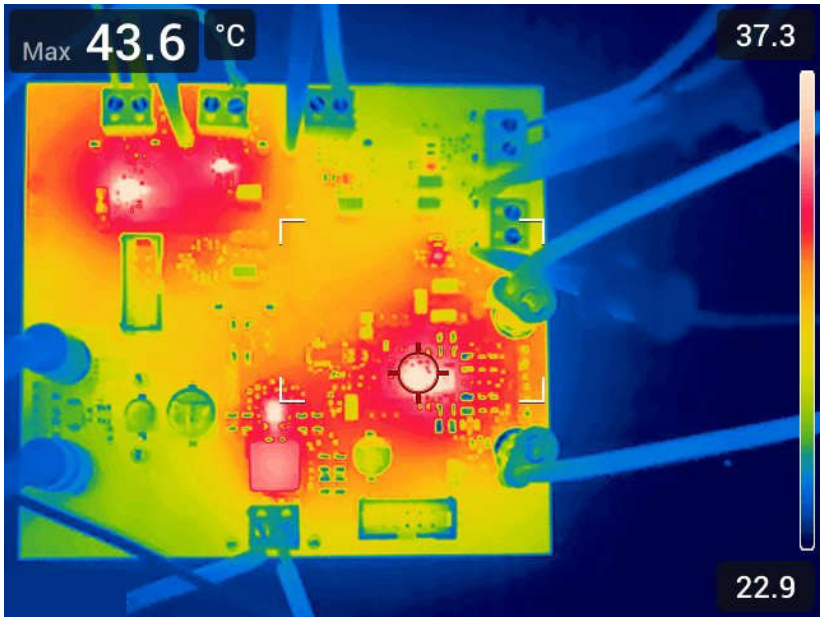


Figure 2-7. Thermal Image, 12-V Input, Full Load Output With 0.75-V VDD_CORE With 5.7-A Load

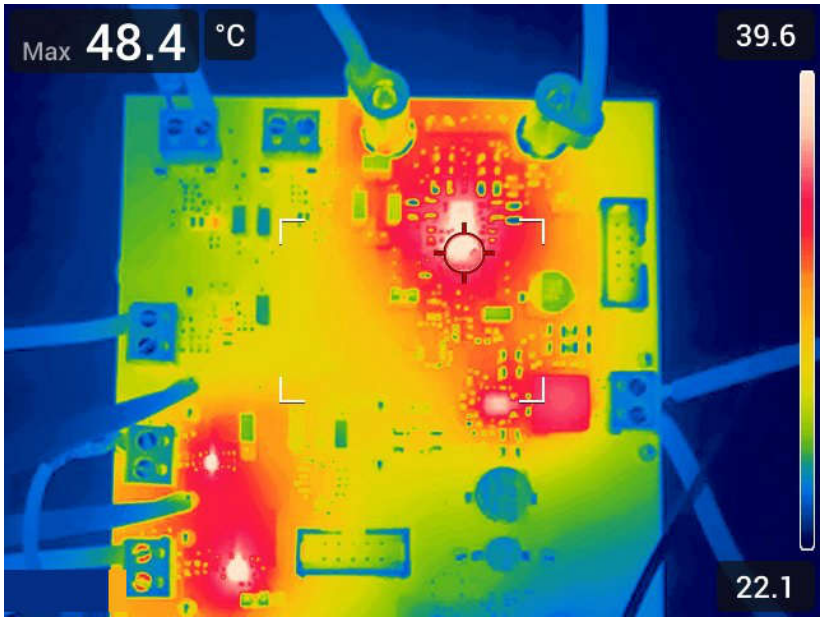


Figure 2-8. Thermal Image, 12-V Input, Full Load Output With 0.85-V VDD_CORE Output at 6.9 A

3 Waveforms

3.1 Start-Up Sequence

When VDD_CORE is supplied at 0.75 V instead of 0.85 V, power on or off sequencing between the VDD_CORE and VDDR_CORE rails become important. The sequencing requirement of ramping up the VDD_CORE rail before the VDDR_CORE rail during power on and ramping down after the VDDR_CORE rail during power off is achieved by using simple AND and OR gates along with an RC delay. The value of the RC delay depends on the value of the output discharge resistor or current sink of the converters supplying these rails. For the recommended TPS6287x-Q1 regulators, an RC delay of 7.05 ms made up with a 15 kΩ resistor and a 0.47-µF capacitor is sufficient.

Figure 3-1 shows the power on sequencing achieved between the VDD_CORE and VDDR_CORE as well as the other AM62x-Q1 power rails. In the waveform, 3V3 represents the VDDSHVx power supply grouping, 1V8_Main represents VDDSHVy, and 1V8_Analog represents VDDA_1P8. The PMP23242 board was connected to the SK-AM62A-LP evaluation board to confirm power-up sequence.

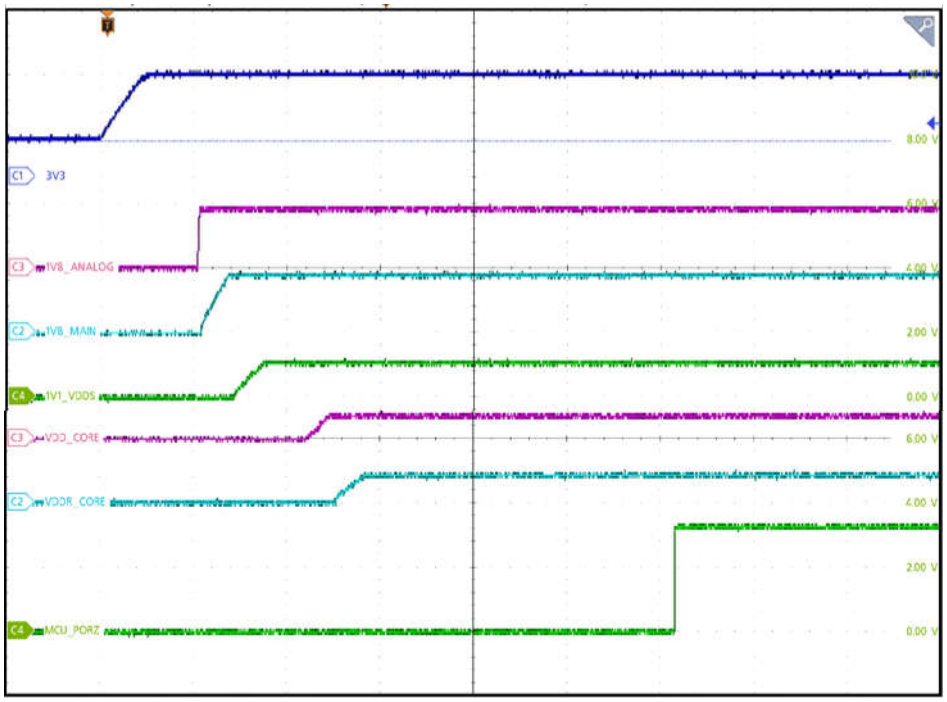


Figure 3-1. Start-Up Waveform

3.2 Shutdown Sequence

The waveform in Figure 3-2 shows the power-down sequence of the different power rails. In the waveform, 3V3 represents the VDDSHVx power supply grouping, 1V8_Main represents VDDSHVy, and 1V8_Analog represents VDDA_1P8. The PMP23242 board was blue wired to the SK-AM62A-LP evaluation board to confirm power-down sequence.

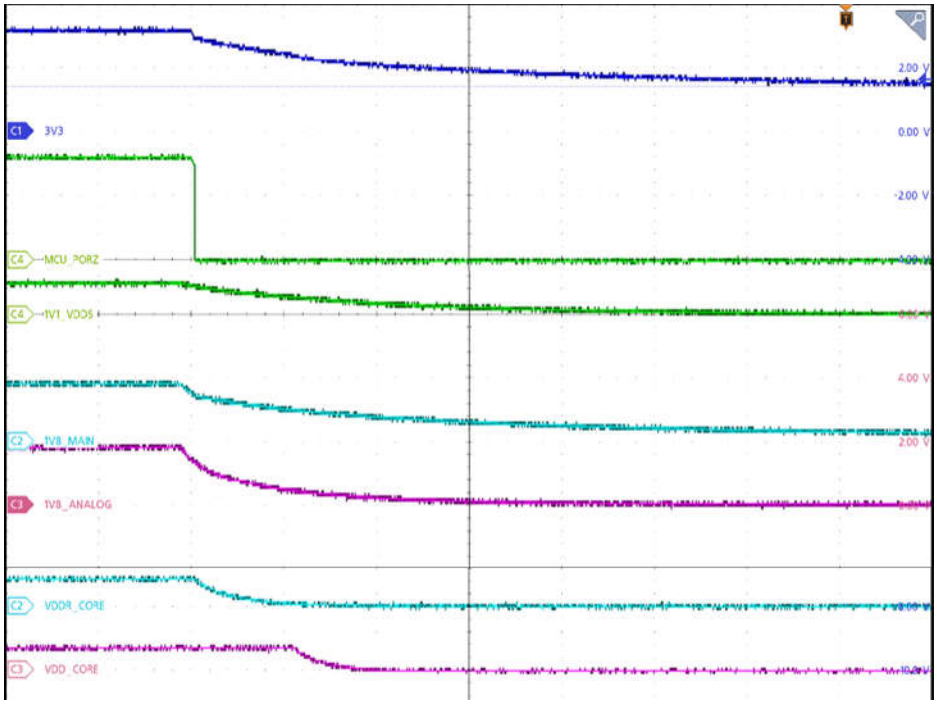


Figure 3-2. Shutdown 1

3.3 Output Voltage Ripple

The output voltage ripple for each power rail at loaded conditions is shown in Figure 3-3 to Figure 3-9.

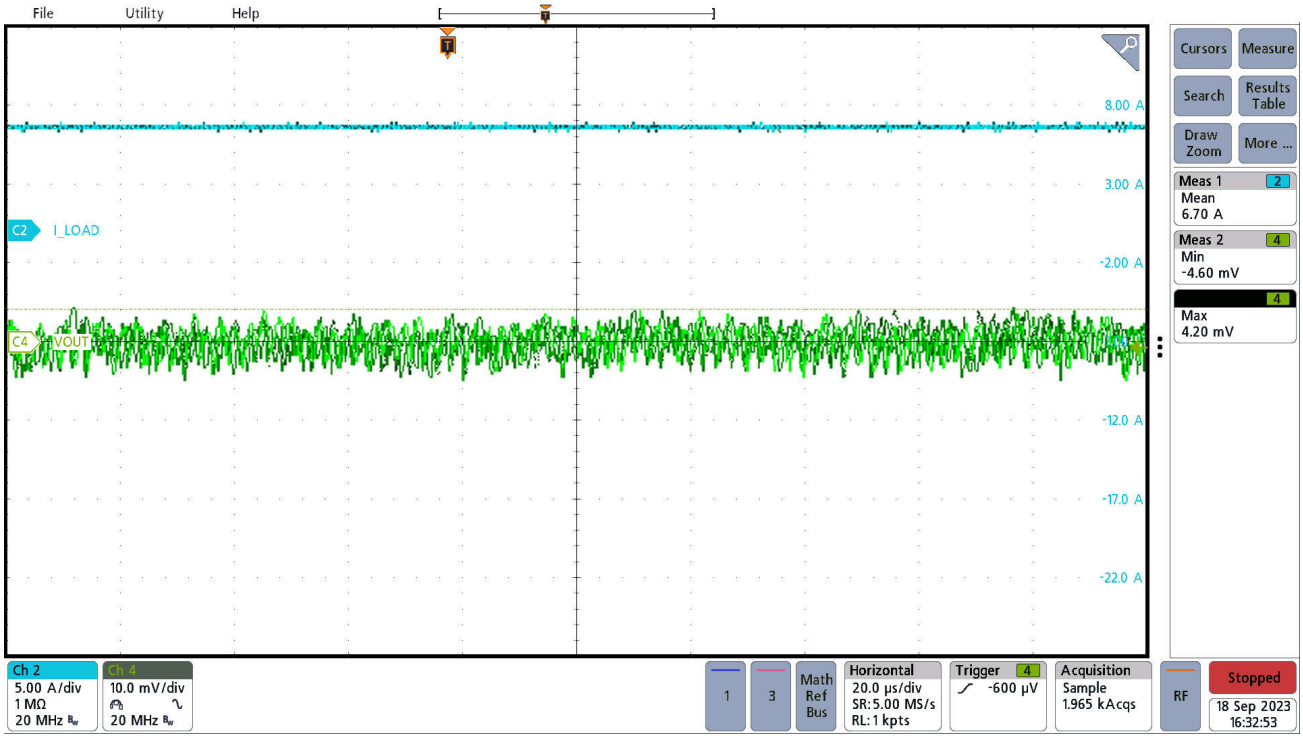


Figure 3-3. LM61480-Q1 Voltage Ripple, 3.3-V Output (VDDSHVx and VDDSHV5), 6.7-A Load

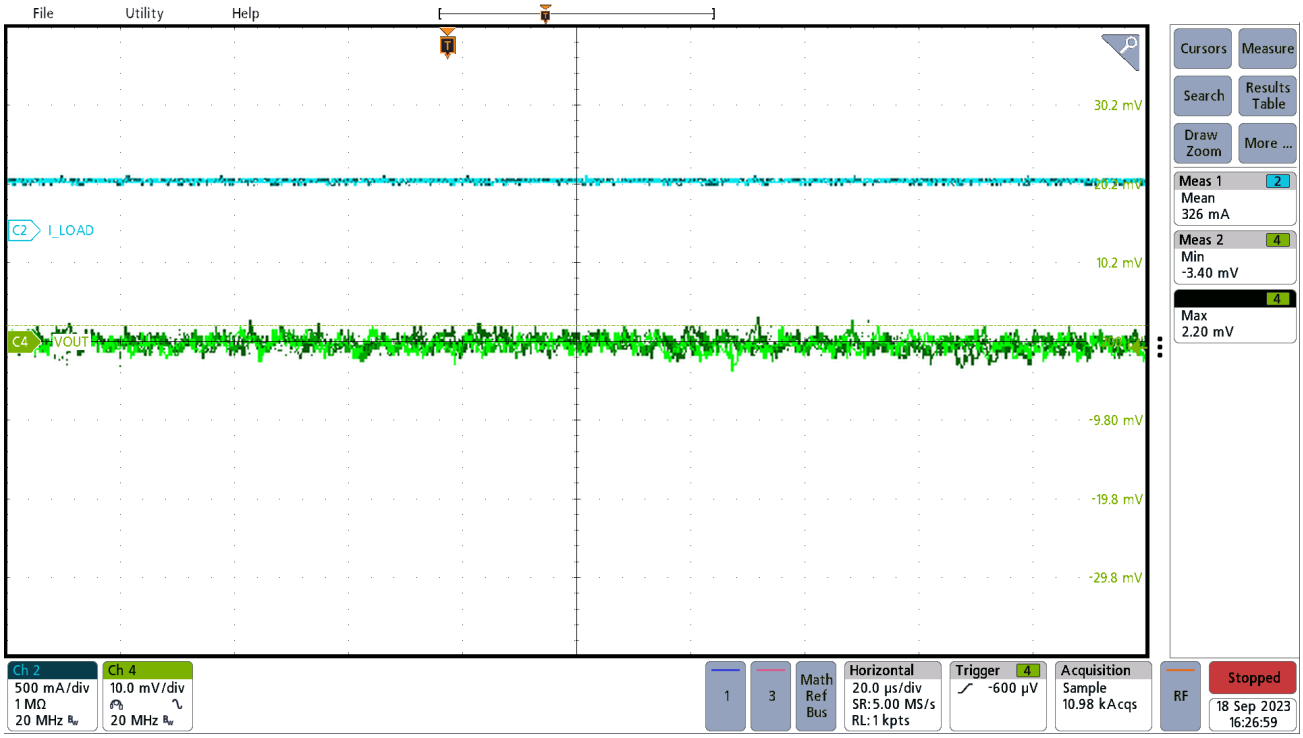


Figure 3-4. TPS628502-Q1 Voltage Ripple, 1.8-V Output (VDDSHVy), 325-mA Load

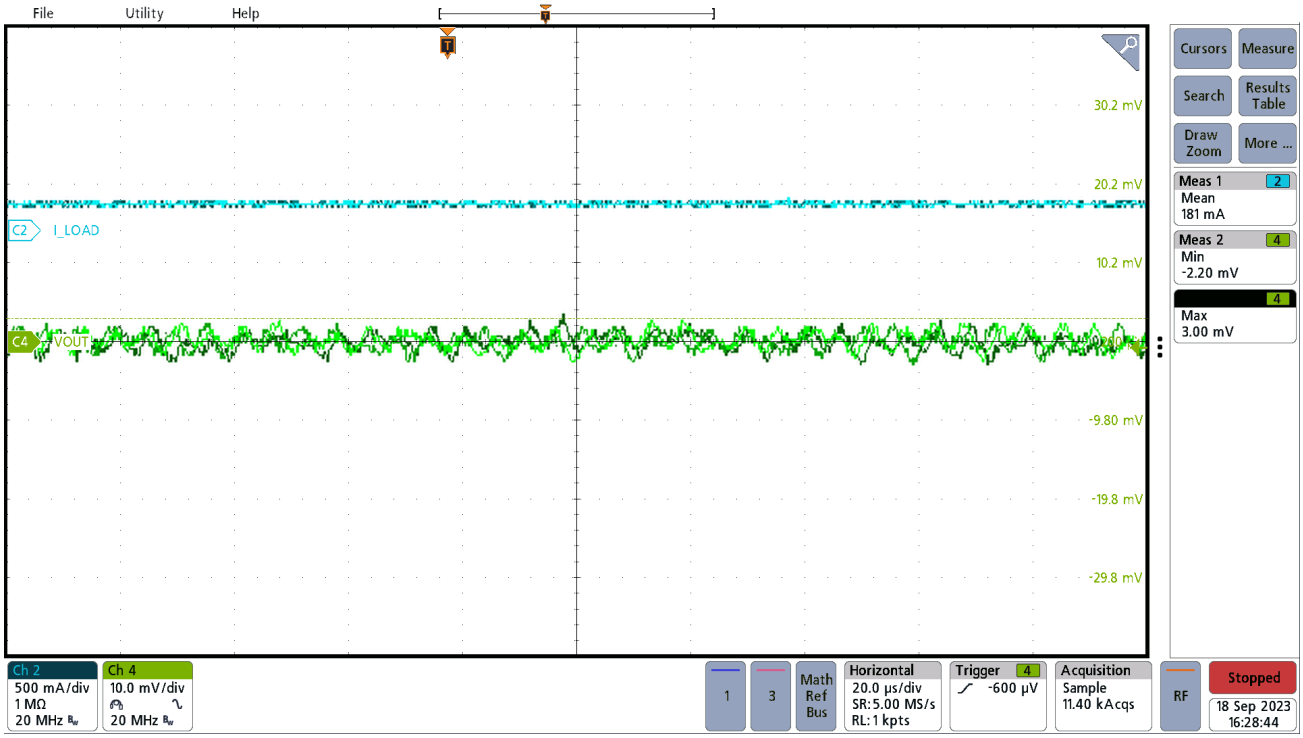


Figure 3-5. LP5912-Q1 Voltage Ripple, 1.8-V Output (VDDA_1P8), 180-mA Load

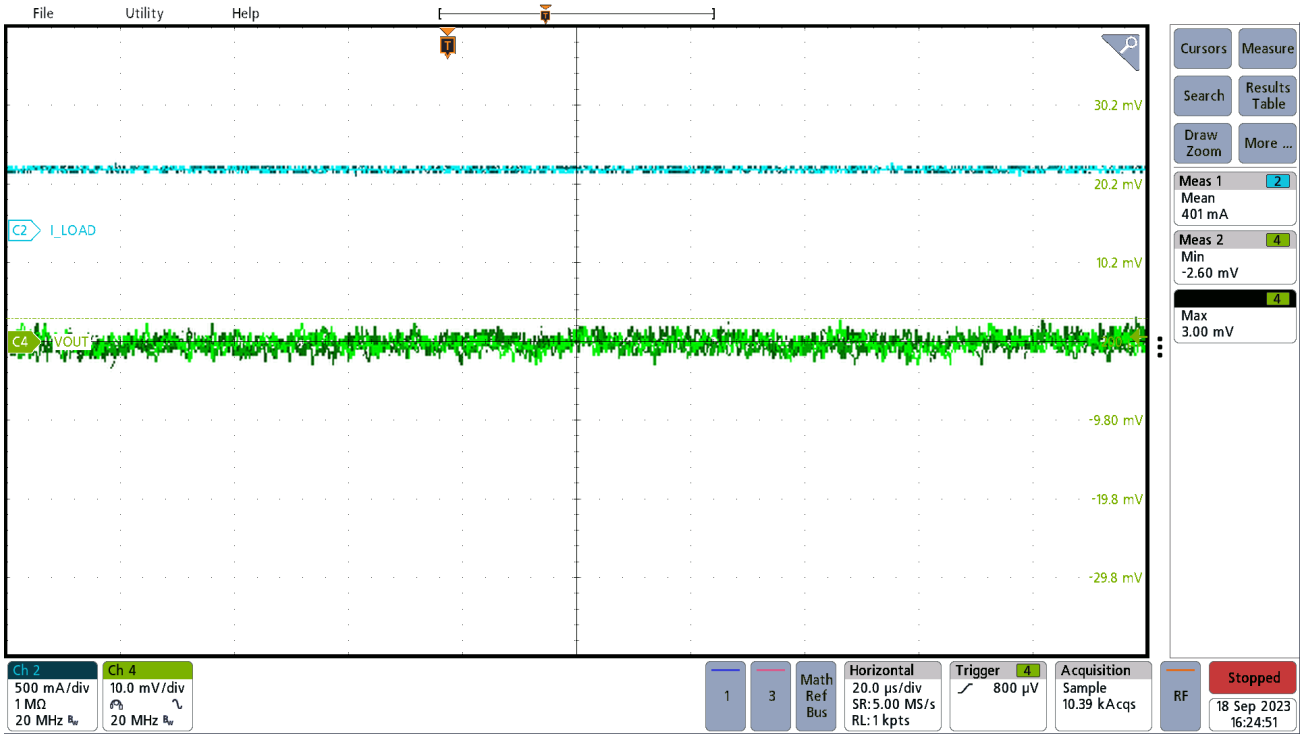


Figure 3-6. TPS628502-Q1 Voltage Ripple, 1.1-V Output (VDDS_DDR), 400-mA Load

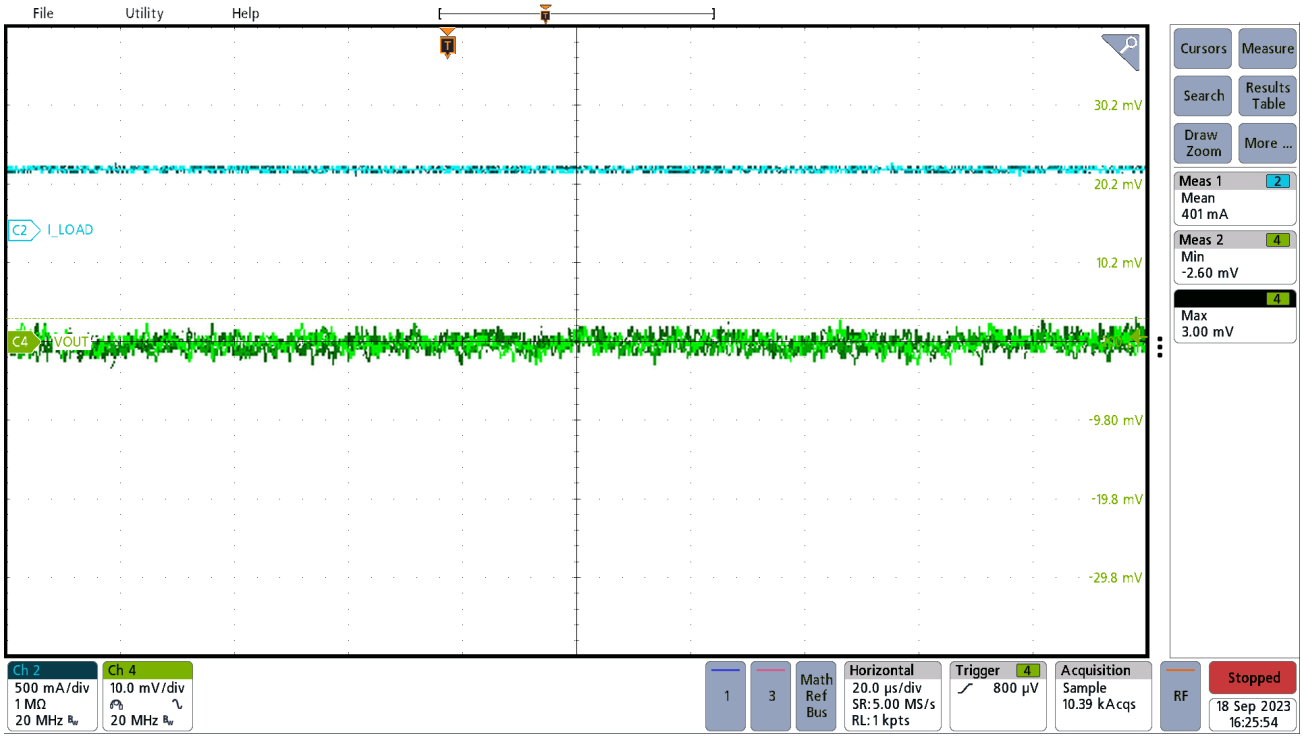


Figure 3-7. TPS628502-Q1 Voltage Ripple, 0.85-V Output (VDDR_CORE), 300-mA Load

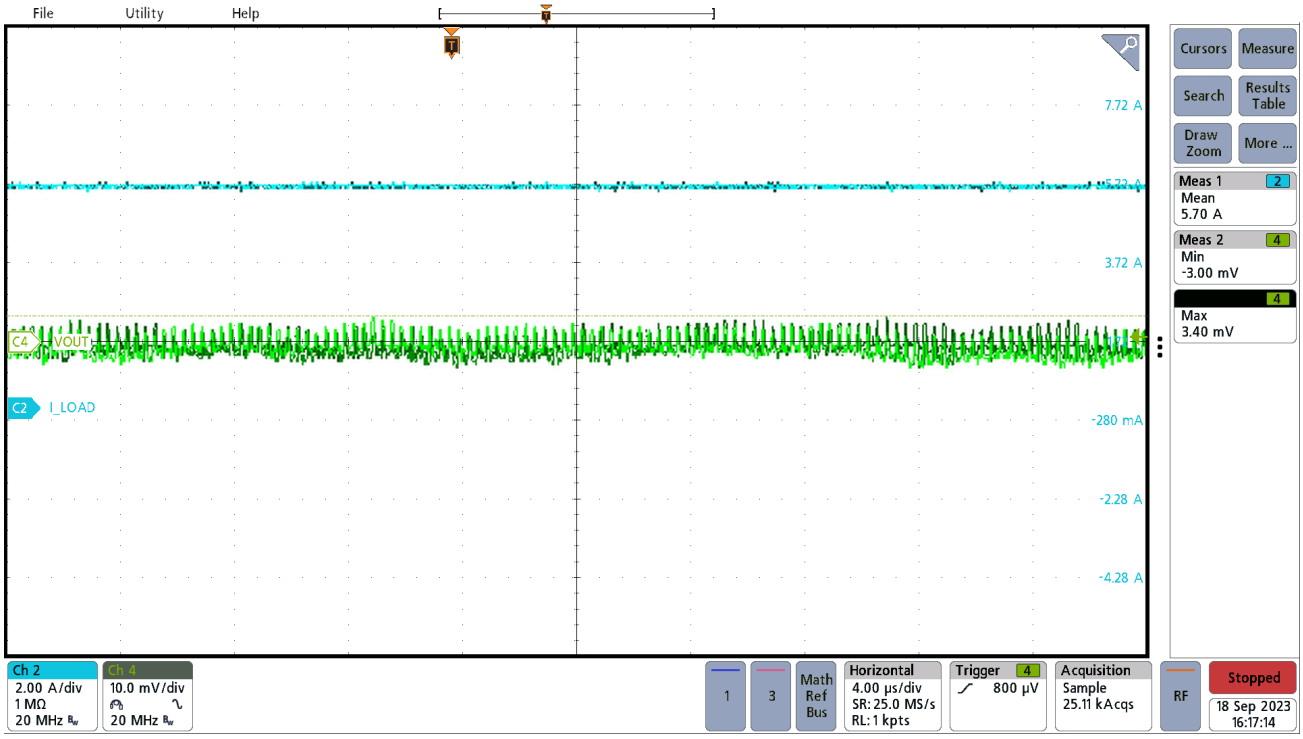


Figure 3-8. TPS62871-Q1 Voltage Ripple, 0.75-V Output (VDD_CORE), 5.7-A Load

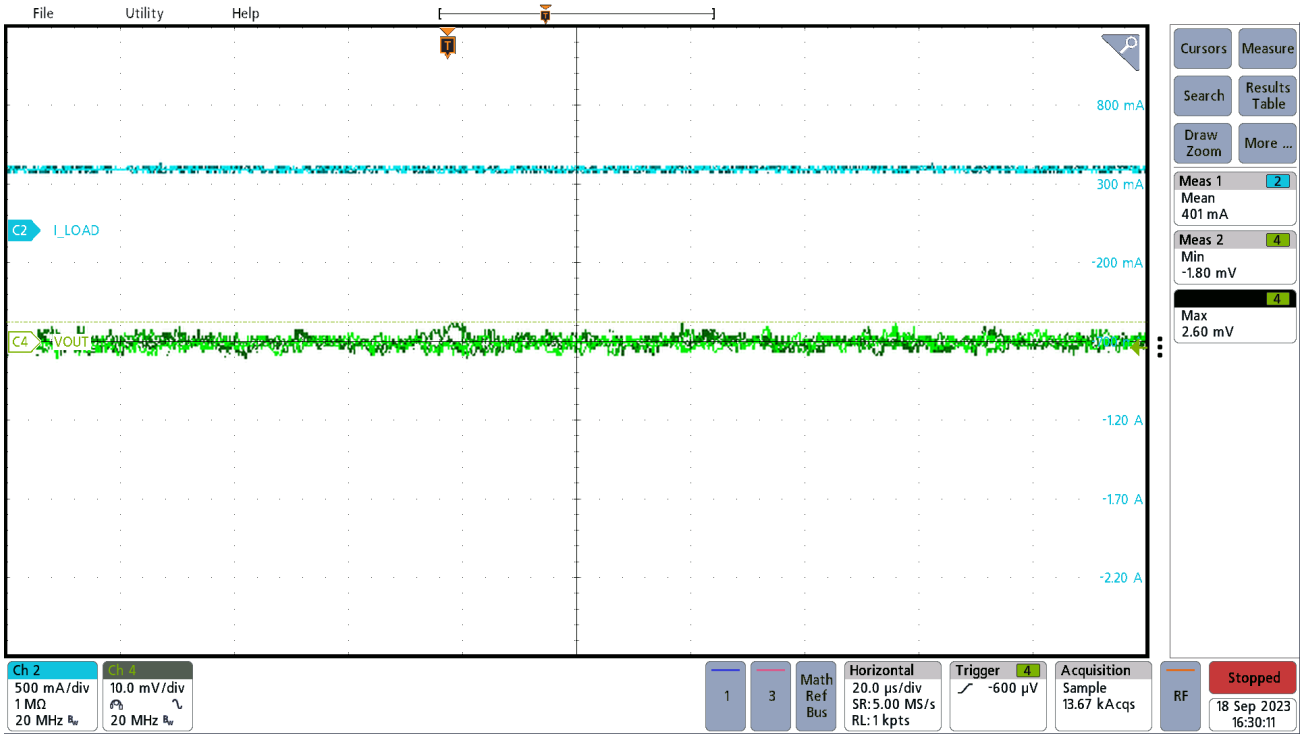


Figure 3-9. TPS745-Q1 Voltage Ripple, 1.8-V Output (VPP), 400-mA Load

3.4 Load Transients

Load transient response was measured for each switching converter and is shown in Figure 3-10 to Figure 3-14. Unless specified, each load was stepped from 25% to 75% of the maximum load of the converter at a slew rate of 1 A / µs.

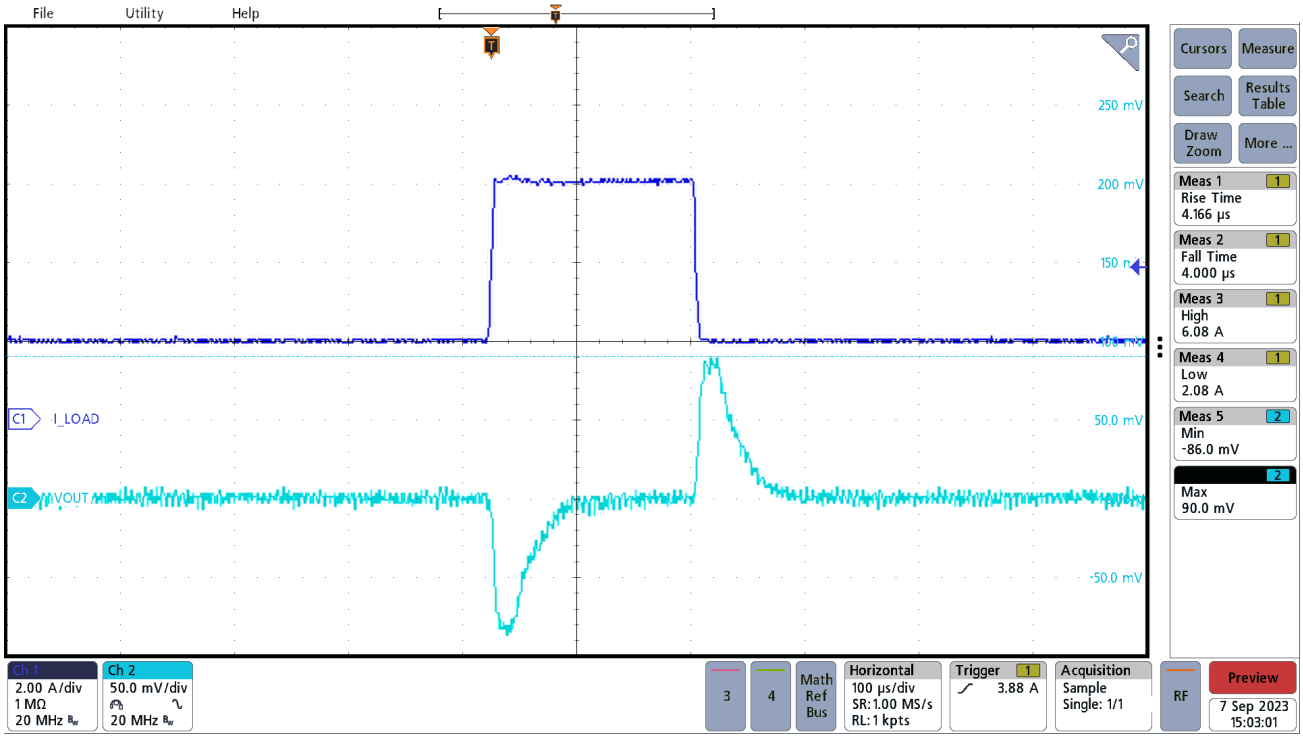


Figure 3-10. LM61480-Q1 Load Transient Response, 12-V Input, 3.3-V Output, 2-A to 6-A Load Step

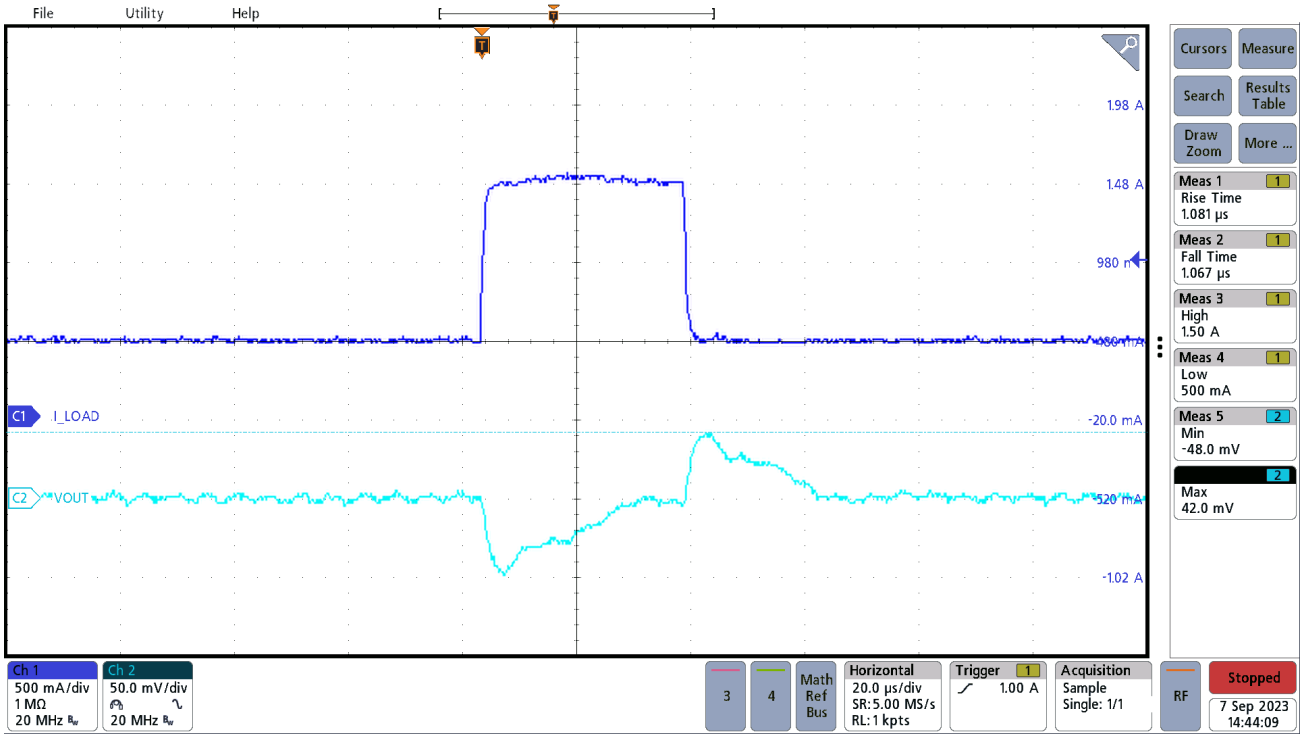


Figure 3-11. TPS628502-Q1 Load Transient Response, 3.3-V Input, 1.8-V Output, 0.5-A to 1.5-A Load Step

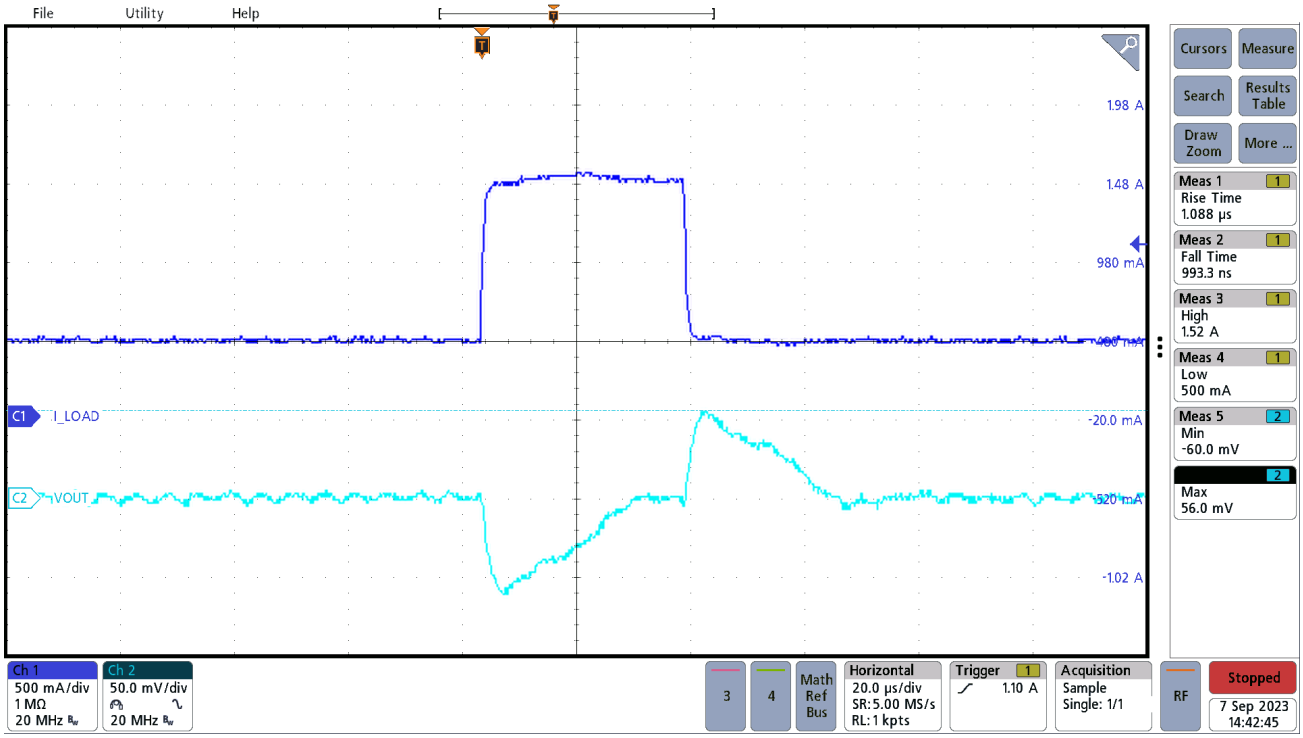


Figure 3-12. TPS628502-Q1 Load Transient Response, 3.3-V Input, 1.1-V Output, 0.5-A to 1.5-A Load Step

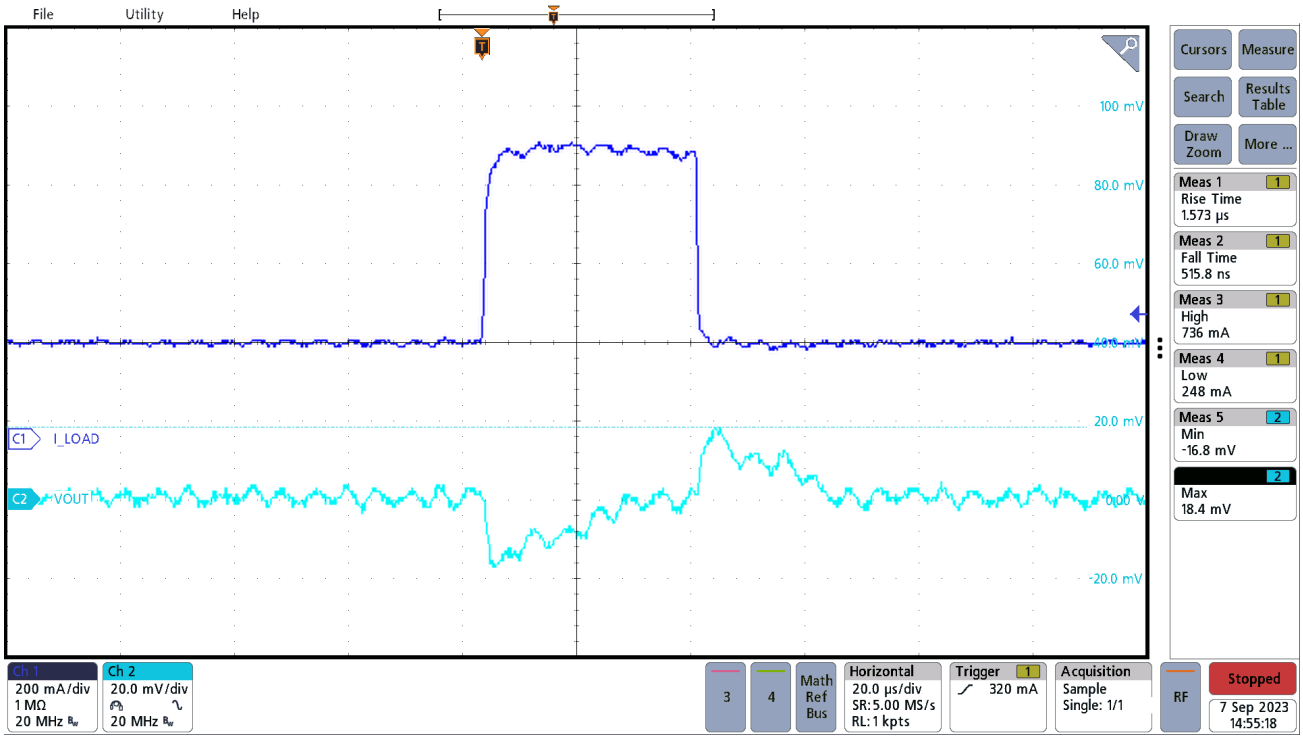


Figure 3-13. TPS628501-Q1 Load Transient Response, 3.3-V Input, 0.85-V Output, 0.25-A to 0.75-A Load Step

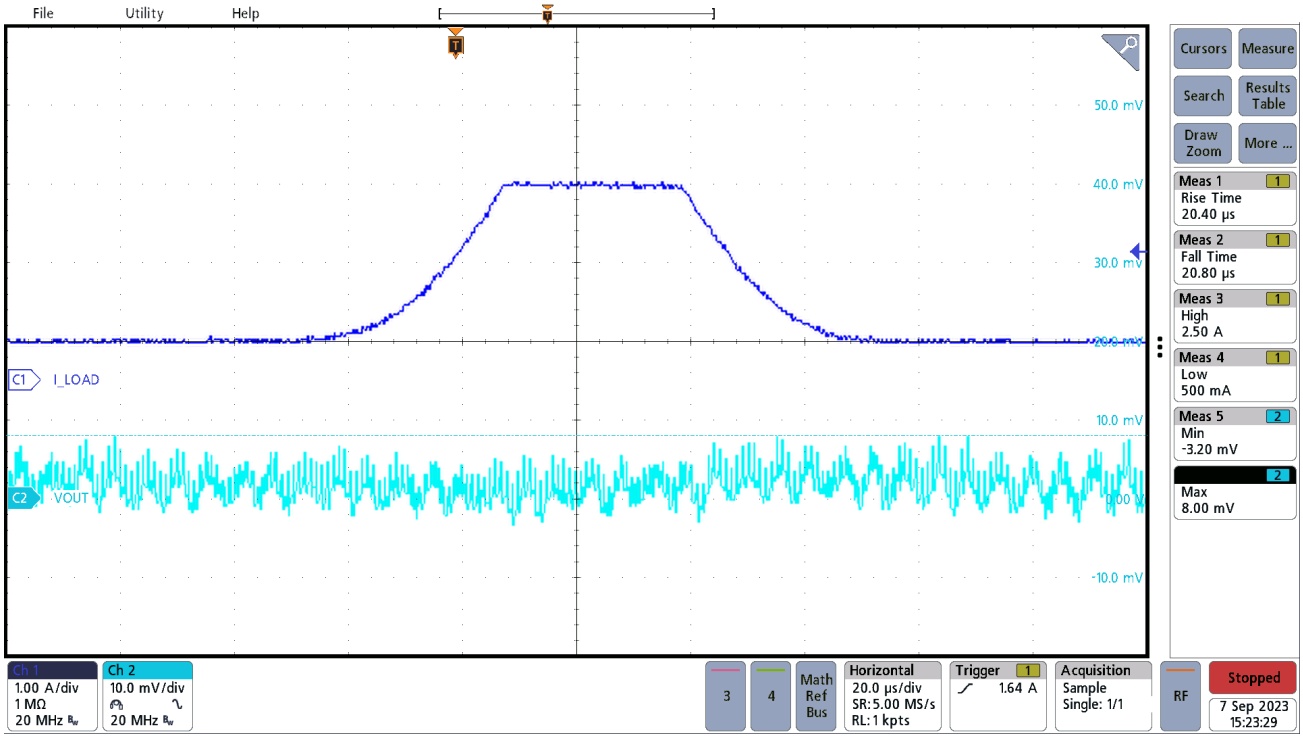


Figure 3-14. TPS62871-Q1 Load Transient Response, 3.3-V Input, 0.75-V Output, 0.1 A / µs Slew Rate, 0.5-A to 2.5-A Load Step

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265