Test Report: PMP31210

4-Phase Buck 700-W Reference Design (Extended Input Voltage Range)

Description

This reference design is a 700-W buck converter using the LM5143A-Q1 device. Due to lowest dead times, ultra-strong drivers, and the ability to adjust the rising edge and falling edge individually, the resulting efficiency is 98%.

Due to the reduced loss, the board area is also greatly reduced, now 150 mm × 125 mm, with a low profile of 12 mm or 15 mm, depending on the inductor selected.

Ample headroom for increased output power is available by using forced cooling or a heat sink mounted to a chassis. Using additional cooling options, the output current can be increased to 60-A continuous and higher.

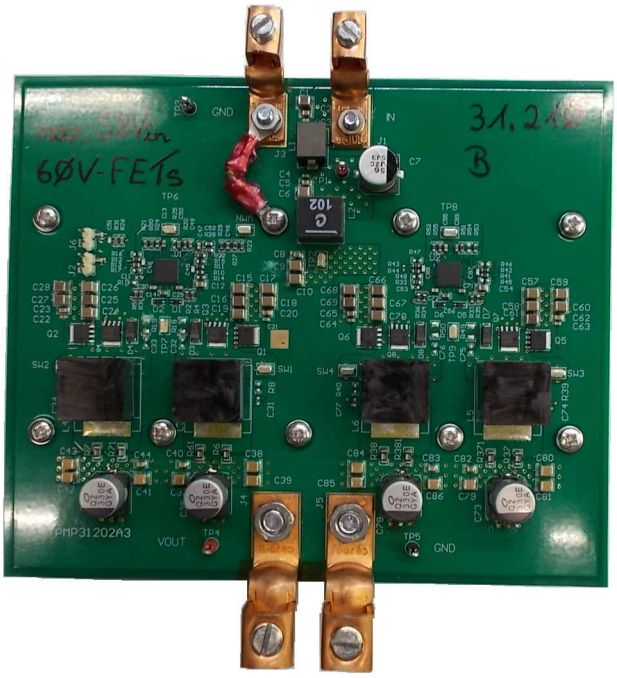
The interleaved operation results in low root mean square (RMS) stress at the input capacitor and reduced ripple at the input and the output. A generic two stage EMI input filter is provided.

Features

- Power supply delivers up to 700-W continuous and up to 1-kW peak output power
- The interleaved four-phase buck topology provides ripple rejection
- The extended input range (compared to PMP31202) makes the design an excellent choice for truck applications
- This reference design is completely built and has completed testing in a lab

Applications

- Aftermarket audio amplifier



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	20 V to 58 V
Output Voltage	13.8 V at 50 A (70 A_{MAX} by current limit)
Switching Frequency	200 kHz
Topology	Four Phases Interleaved Buck Converter
IC	2 × LM5143A-Q1

1.2 Considerations

Unless otherwise indicated, all measurements were done with 24-V input voltage and 50-A output current.

The load used was an electronic load TDI RBL100-120-800, limited to 800 W_{MAX}, squeezed up to 828 W; the source was the SMPS Agilent 6574A, limited to a maximum 35-A input current, squeezed up to 35.8 A.

Efficiency and thermal image measurements up to 60-A continuous current are provided, but with a proper thermal interface there is still some headroom left – the current limitation trips at around 70 A.

Unless otherwise indicated, an air flow of 0.5 meters per second (m/s) to 1 m/s was used for the first measurements.

CAUTION

Make sure the wiring is properly connected. The output current can be as high as 60 A and the input current can be as high as 30 A.

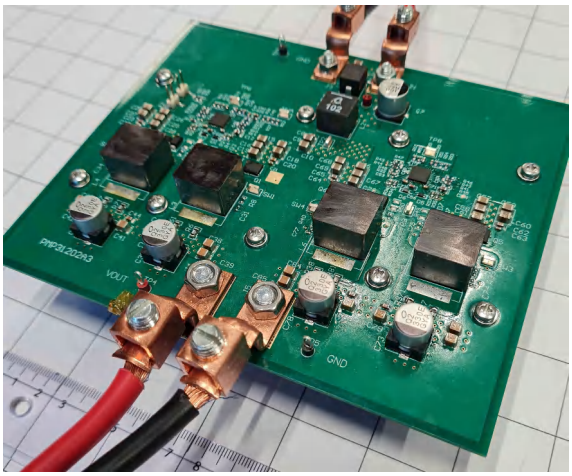


Figure 1-1. Board Image With Connected Cable

WARNING

A 16-mm^2 cable cross section still gets warm and provides a minor voltage drop. Always wear eye protection when working with this reference design, and do not wear watches or rings.

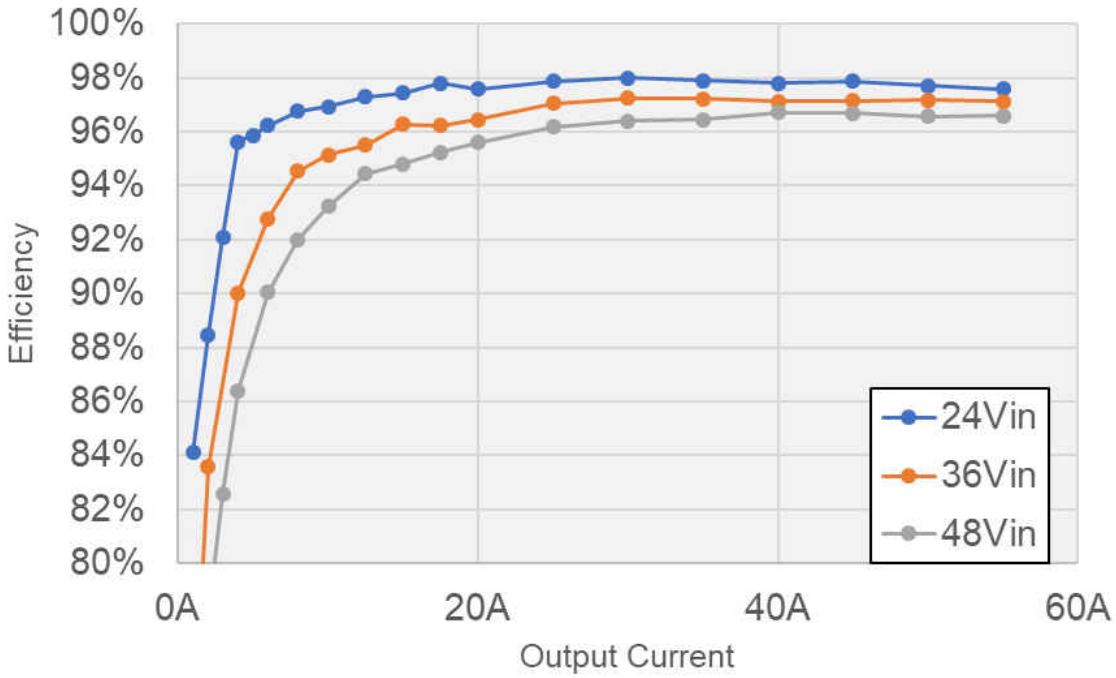
1.3 Dimensions

The size of the board is 156.2 mm × 130.8 mm. The four-layer board was manufactured with 105-µm copper on each layer.

The solder stop cutout for the heat sink is 150 mm × 75 mm to fit for standard heat sinks.

2 Testing and Results

2.1 Efficiency Graph



A minor improvement is still possible by moving towards DCR sensing.

Figure 2-1. Efficiency vs Output Current Without Input Filter

2.2 Loss Graph

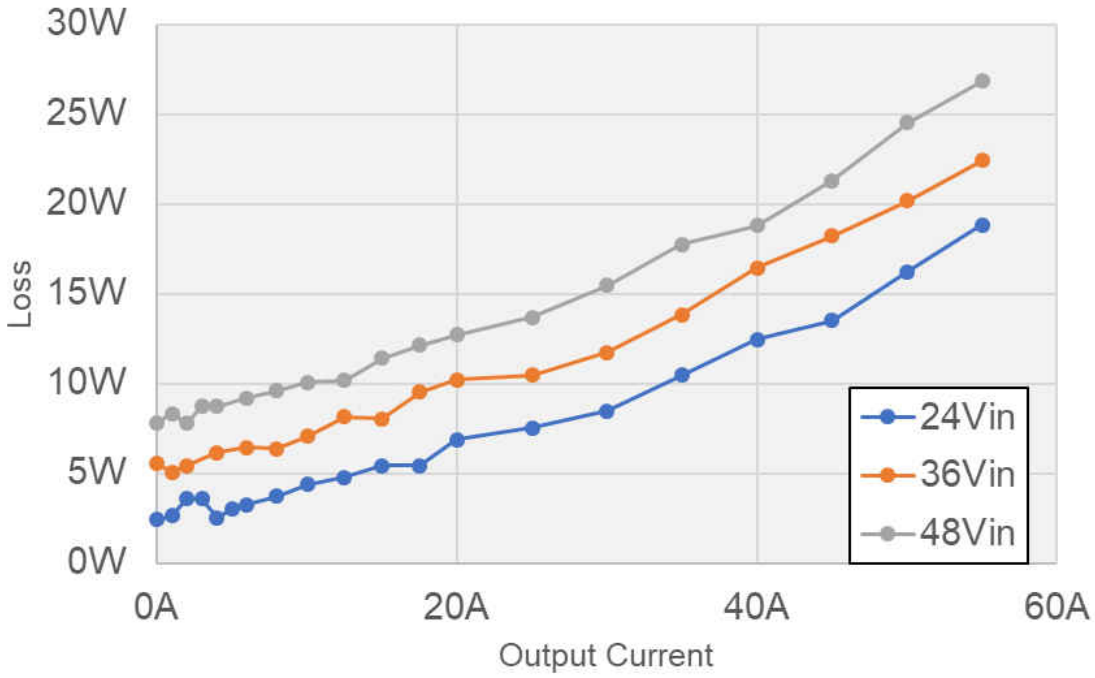


Figure 2-2. Loss vs Output Current

Figure 2-3 shows efficiency and loss depending on the input voltage.

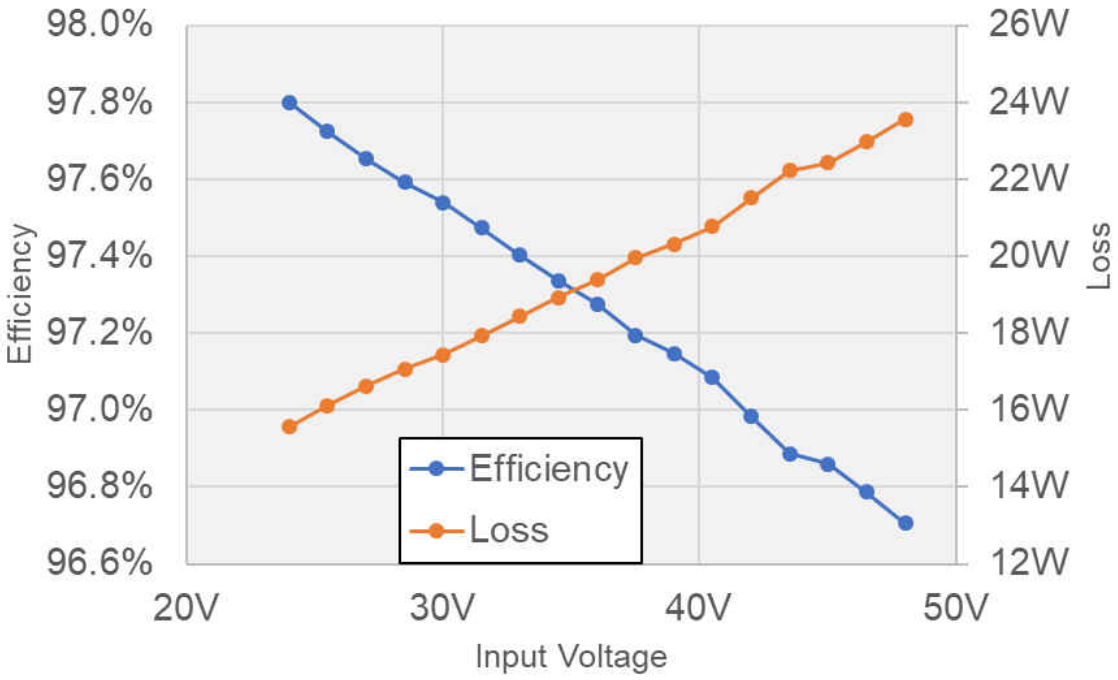


Figure 2-3. Efficiency and Loss vs Input Voltage at Full Load 50 A

2.3 Load Regulation

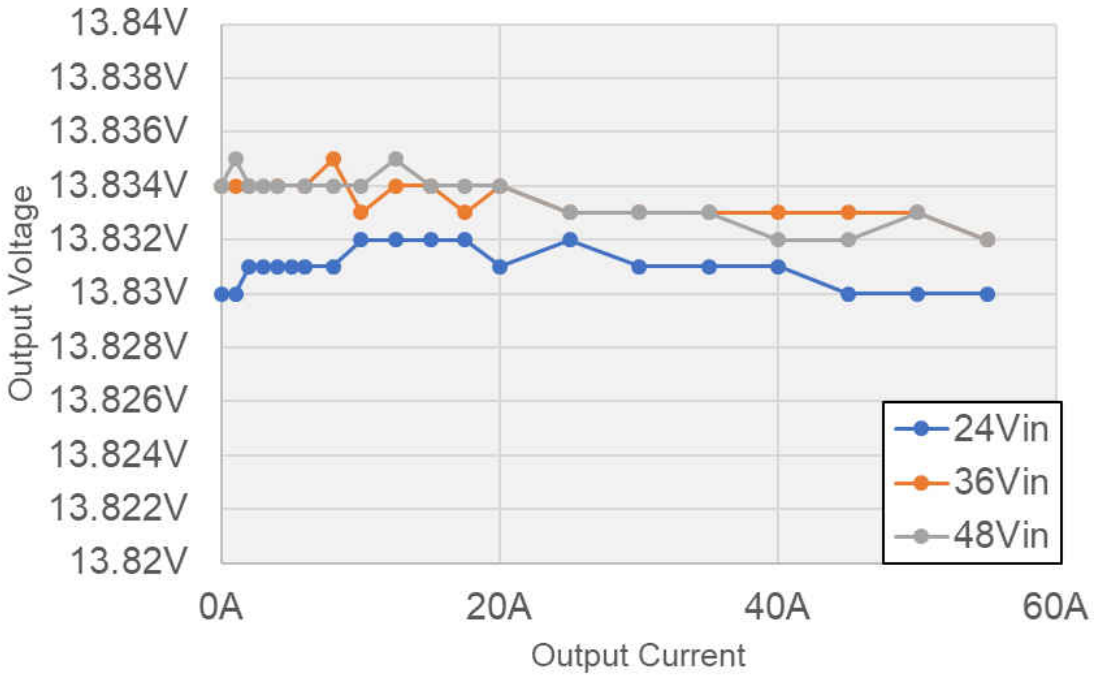


Figure 2-4. Output Voltage vs Output Current

2.4 Thermal Images

All images were taken after around 30 minutes of **continuous** operation and 110% load.

2.4.1 Summary, Hottest Spot High-Side FET Q6, NVMFS5C645NL

Table 2-1. Hot Spot Maximum Temperature

Input Voltage (I_{OUT} = 55 A	Hottest Spot, Horizontal(1)	Hottest Spot, Vertical(2)	Hottest Spot, Vertical With Airflow(3)
24 V	69.1°C	63.9°C	47.4°C
36 V	77.5°C	69.0°C	51.5°C
48 V	85.4°C(4)	77.3°C	56.0°C

(1) Horizontal – ⇒ board flat on the bench, no proper convection = **worst case**
(2) Vertical – ⇒ board upright on the bench, fins vertical = natural convection
(3) Vertical with airflow – ⇒ forced cooling < 0.5 m/s = **best case**
(4) The red cell indicates the highest temperature under the given conditions.

2.4.2 Thermal Images

Table 2-2. Infrared (IR) Images

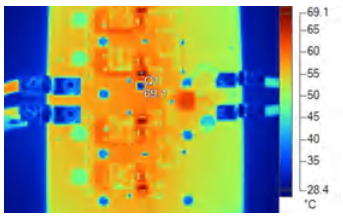
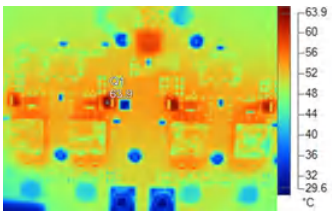
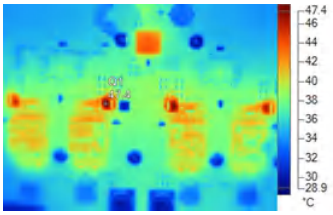
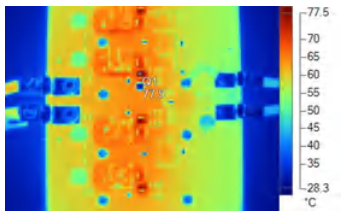
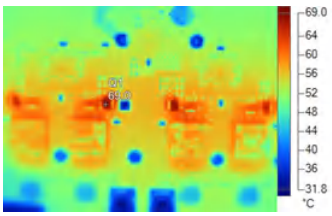
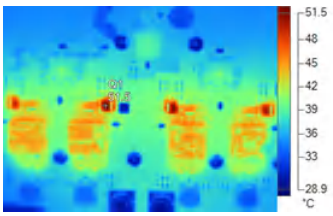
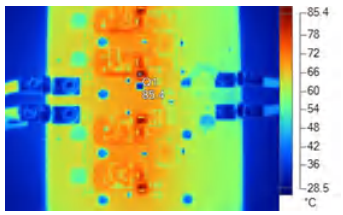
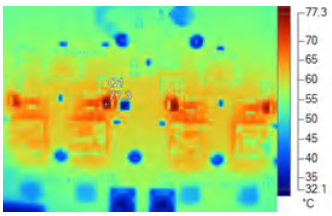
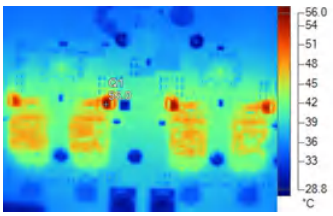
V_{IN}	Horizontal	Vertical	Vertical With Airflow
24 V			
36 V			
48 V			

Figure 2-5 is a graphical representation of the results in Table 2-1.

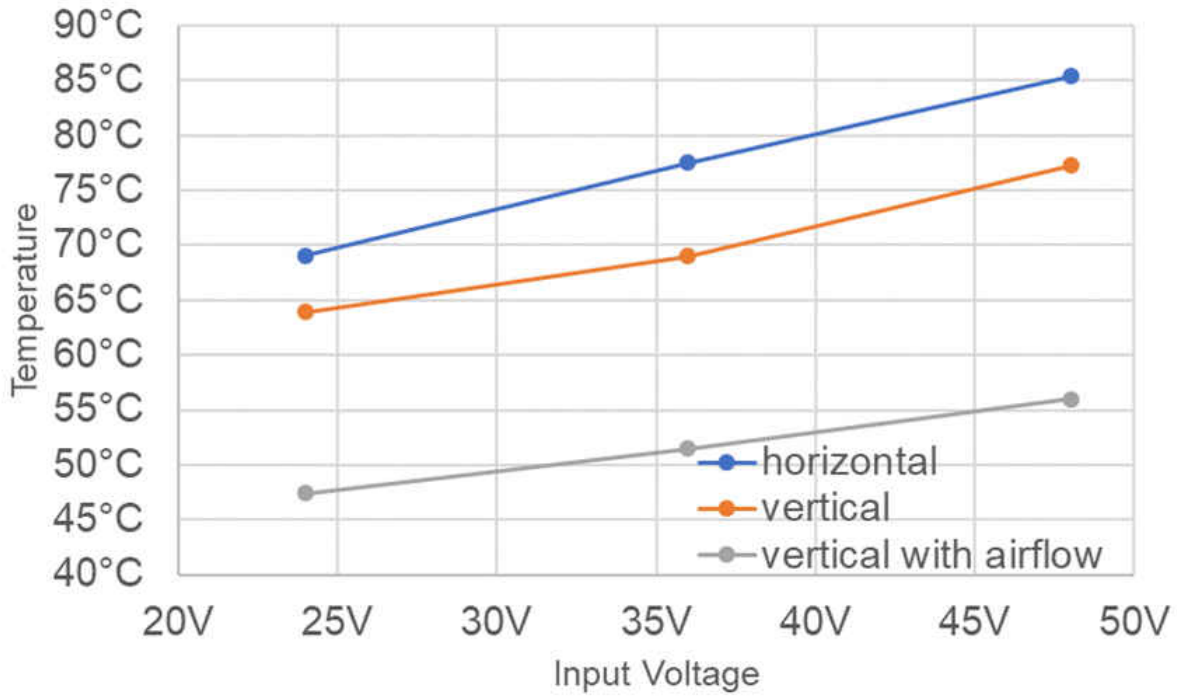


Figure 2-5. Temperature of Hottest Spot vs Input Voltage at 110% Load 55 A

2.4.3 Thermal Mechanics

The aluminum adapter (150 mm × 75 mm × 5 mm) is used by mounting the converter to a chassis, which is the thermal interface. This area is also used for a standard heat sink; 150 mm × 75 mm from stock. The measurement with the heat sink is worst case - the board is horizontal on the bench, with the heat sink upside down. The best case is the board in a vertical position, with fins in a vertical position as well.

Individually, the adapter provides a minor improvement, the board itself is well routed regarding power losses.

Table 2-3. Thermal Comparisons

Input Voltage	Horizontal	Vertical	Vertical with Airflow	Benefit
24 V	69.1°C	63.9°C	47.4°C	–21.7 K
36 V	77.5°C	69.0°C	51.5°C	–9.3 K
48 V	85.4°C	77.3°C	56.0°C	–29.4 K

Note

For output currents of 50-A and higher (continuous), proper orientation of the heat sink is mandatory!

2.5 Bode Plots

2.5.1 Bode Plot Summary, Loop Bandwidth 16 kHz

Table 2-4.

	24 V_{IN}	36 V_{IN}	48 V_{IN}
Loop bandwidth (kHz)	16.1	16	16
Phase margin	63°	61°	60°
Slope (20 dB/decade)	–1.16	–1.15	–1.15
Gain margin (dB)	–15.1	–16	–16.4
Slope (20 dB/decade)	–0.65	–1	–1.37
Roll off frequency (kHz)	76.2	71.7	65

2.5.2 24-V Input Voltage

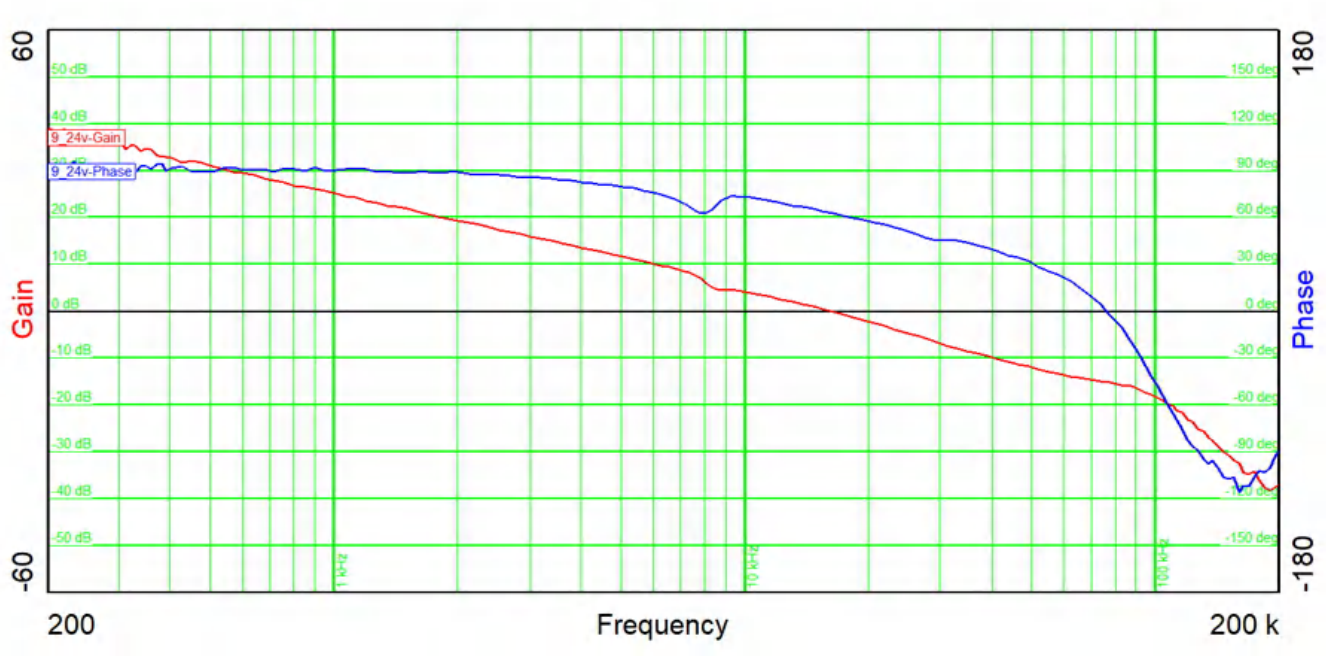


Figure 2-6. Bode Plot at 24-V Input Voltage

2.5.3 36-V Input Voltage

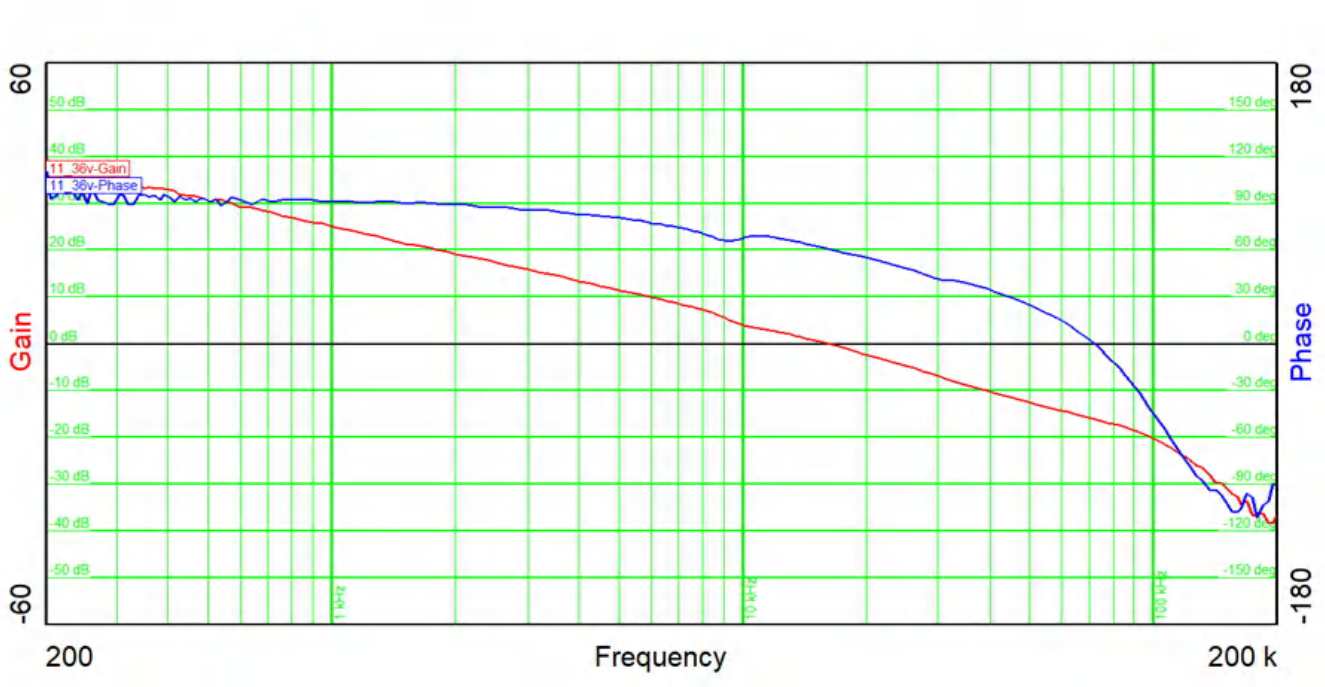


Figure 2-7. Bode Plot at 36-V Input Voltage

2.5.4 48-V Input Voltage

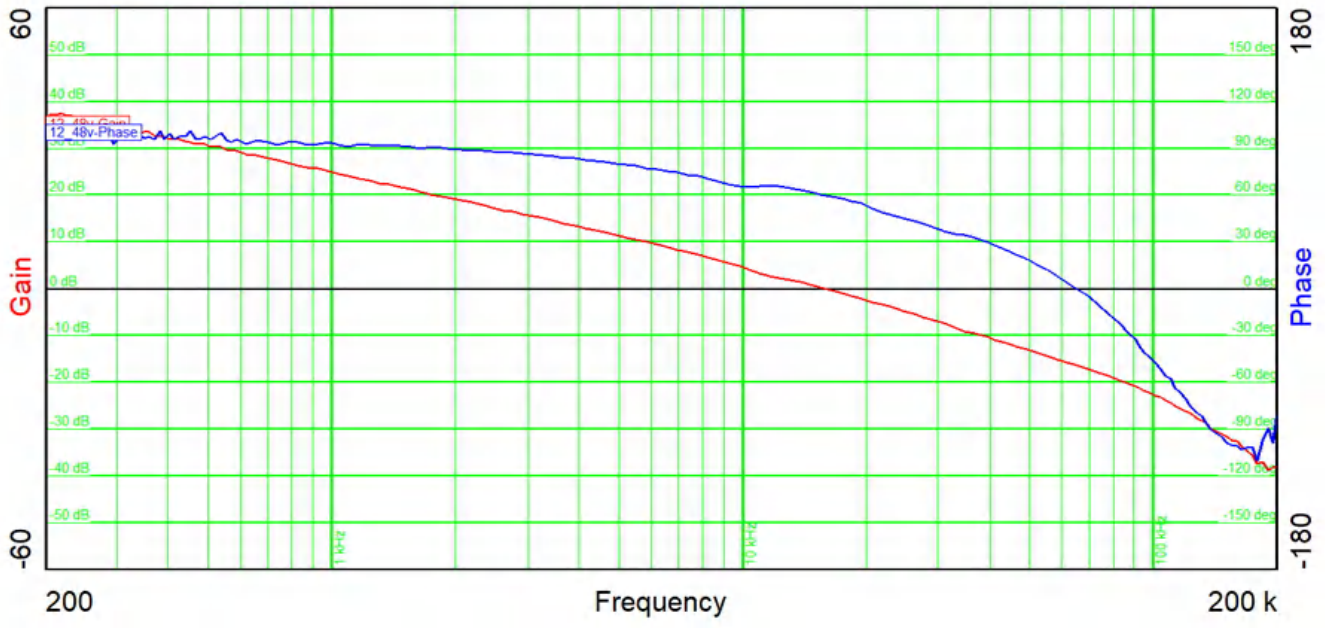


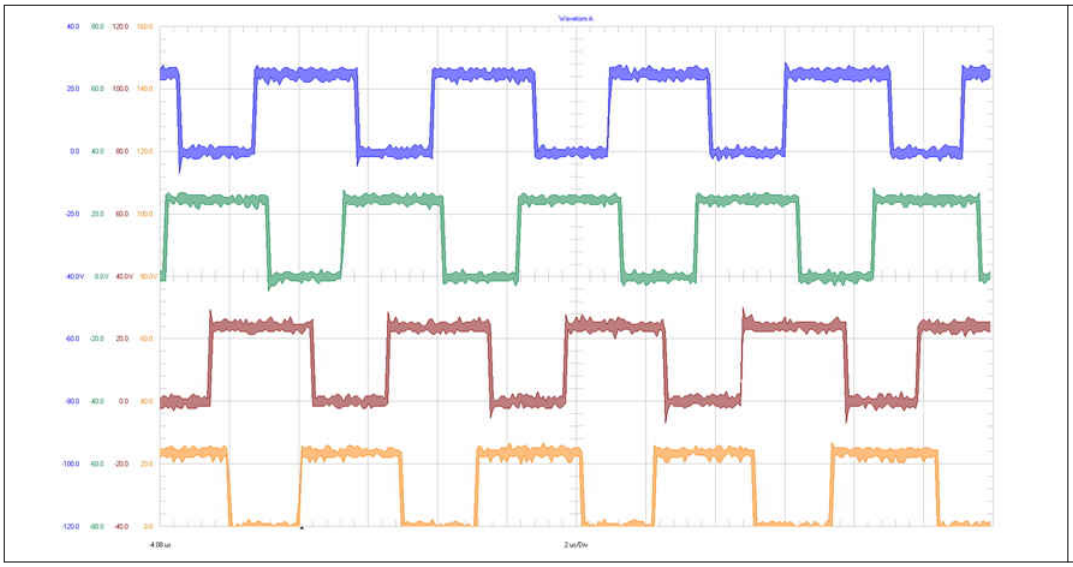
Figure 2-8. Bode Plot at 48-V Input Voltage

3 Waveforms for 2 × LM5143A-Q1 in Four Phase Configuration and Interleaved Operation

3.1 Switching

3.1.1 Overview of the Four Switching Phases

3.1.1.1 24-V Input Voltage



(SW1 to SW4)
20 V / div
2 µs / div
Full bandwidth

Figure 3-1. Four Switching Phases at 0, 90, 180, 270 Degrees Phase Shift at 24 V_{IN}

Primary Controller U1	phase 1(1)	0 degrees
	phase 2(1)	180 degrees
Secondary Controller U2	phase 3(1)	90 degrees
	phase 4(1)	270 degrees

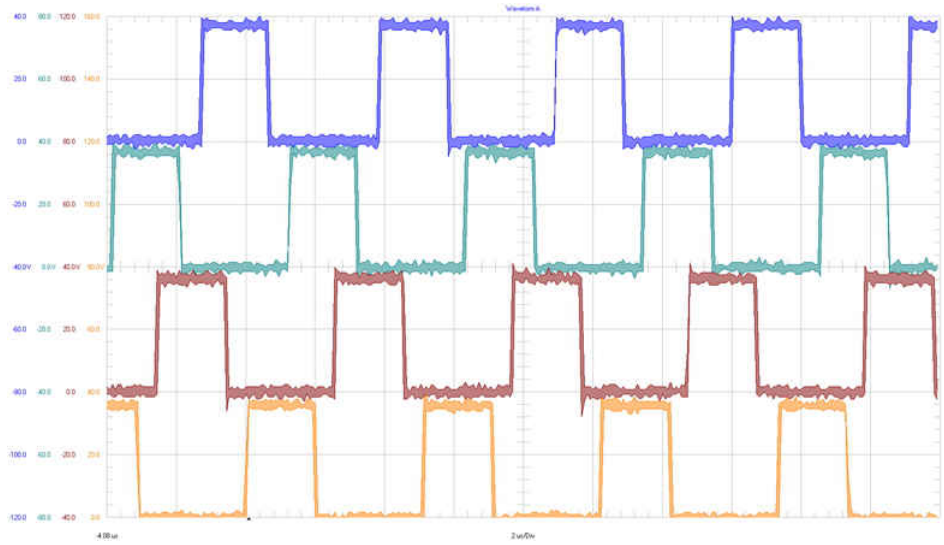
(1) The background color in the table cells correspond to the waveform colors in Figure 3-1.

Figure 3-1 highlights the four phase interleaved operation of the two stacked controllers in primary and secondary configuration. Four phase interleaved operation results in **ripple rejection at 25%, 50% and 75% duty cycle**.

This evidence shows that at 24-V input voltage (duty cycle around 50%) and at 480-V input voltage (duty-cycle around 25%) and around 12-V output voltage, the ripple rejection is best.

This ripple rejection is illustrated in Figure 3-8, output ripple < 10 mV_{PP} and noise < 50 mV_{PP}.

3.1.1.2 36-V Input Voltage

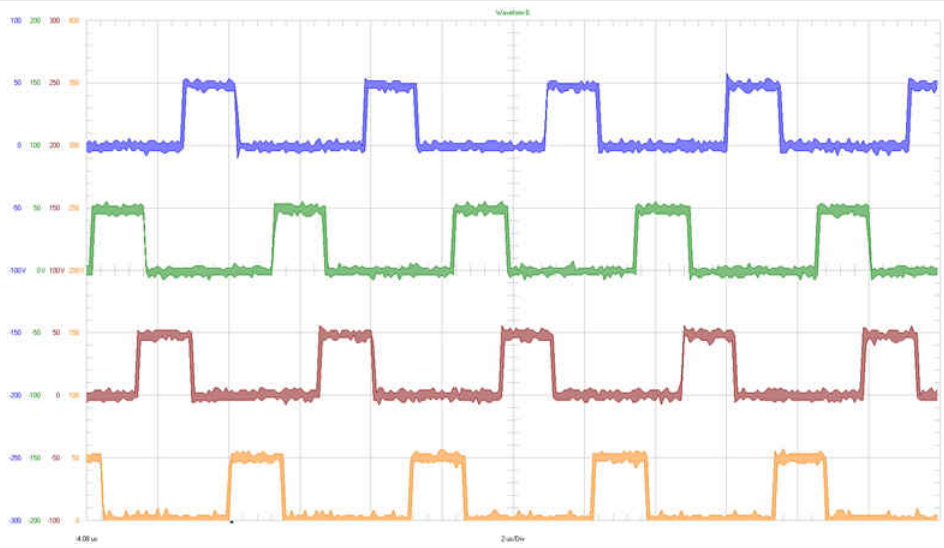


(SW1 to SW4)
20 V / div
2 µs / div
Full bandwidth

Figure 3-2. Four Switching Phases at 0, 90, 180, 270 Degrees Phase Shift at 36 V_{IN}

Primary Controller U1	phase 1(1)	0 degrees
	phase 2(1)	180 degrees
Secondary Controller U2	phase 3(1)	90 degrees
	phase 4(1)	270 degrees

3.1.1.3 48-V Input Voltage



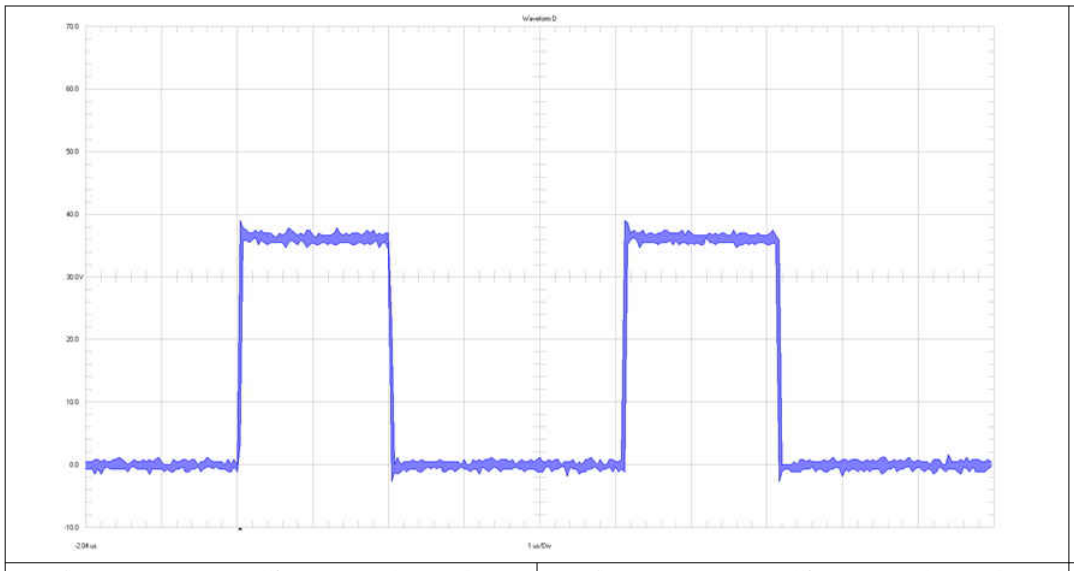
(SW1 to SW4)
50 V / div
2 µs / div
Full bandwidth

Figure 3-3. Four Switching Phases at 0, 90, 180, 270 Degrees Phase Shift at 48 V_{IN}

Primary Controller U1	phase 1(1)	0 degrees
	phase 2(1)	180 degrees
Secondary Controller U2	phase 3(1)	90 degrees
	phase 4(1)	270 degrees

3.1.2 Low-Side FET

3.1.2.1 Switch Node to GND



	10 V / div 1 µs / div Full bandwidth
	10 V / div 100 ns full scale Full bandwidth

Figure 3-4. Waveform Switch Node to GND

3.1.2.2 Low-Side FET Gate to GND

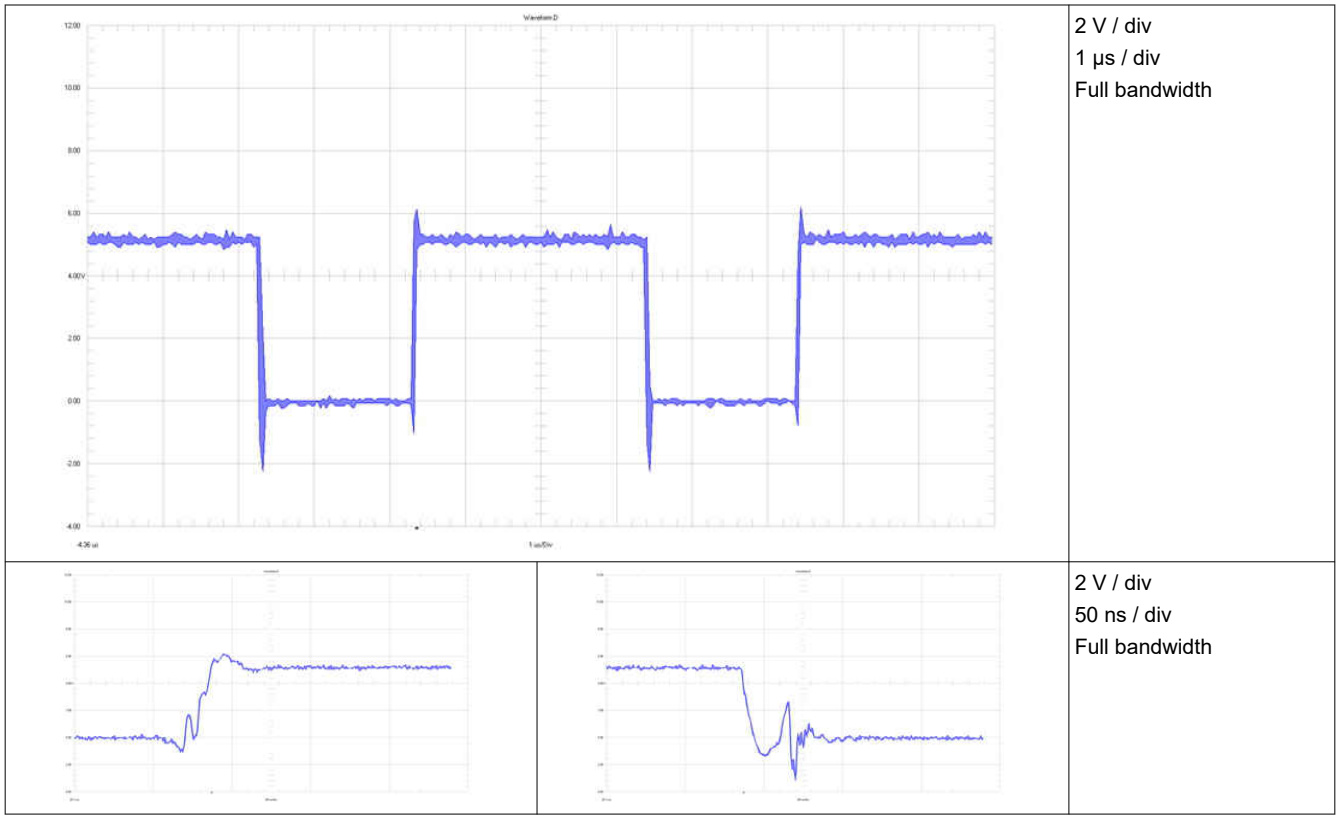
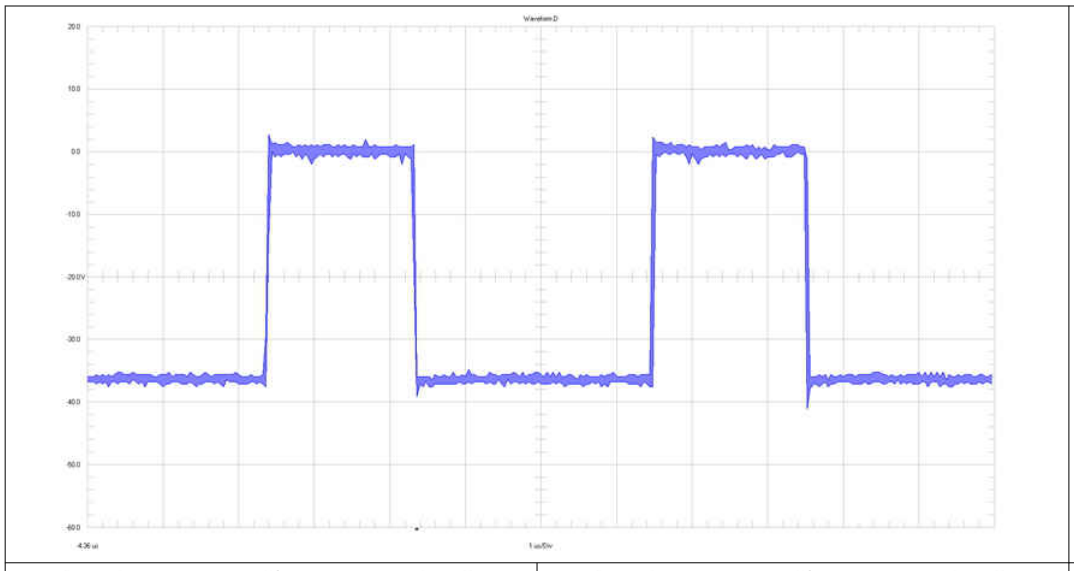


Figure 3-5. Waveform Low-Side FET to GND

3.1.3 High-Side FET

3.1.3.1 Switch Node to V_{IN}



	10 V / div 1 µs / div Full bandwidth
	10 V / div 100 ns full scale Full bandwidth

Figure 3-6. Waveform Switch Node to V_{IN}

3.1.3.2 High-Side FET Gate to Switch Node

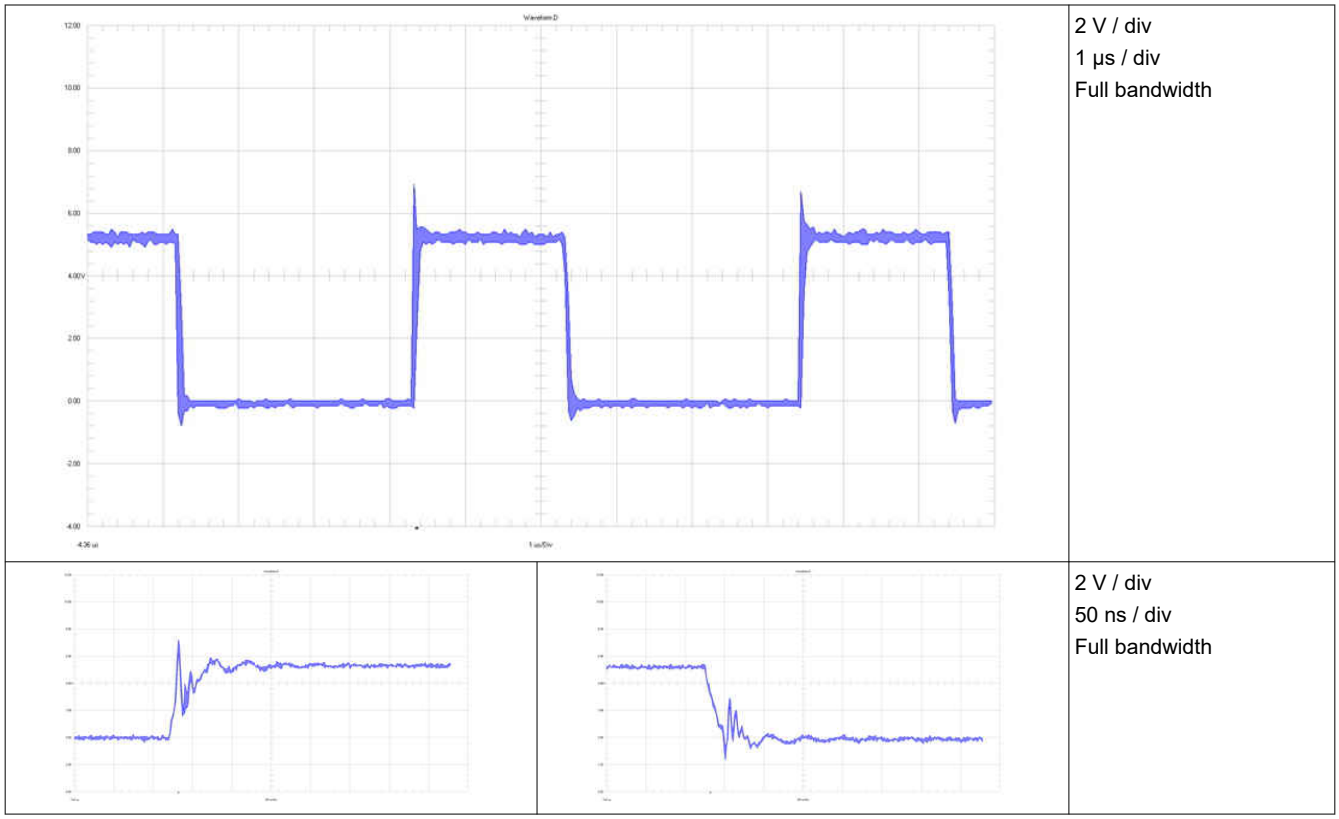


Figure 3-7. Waveform Low-Side FET Gate to Switch Node

3.2 Output Voltage Ripple

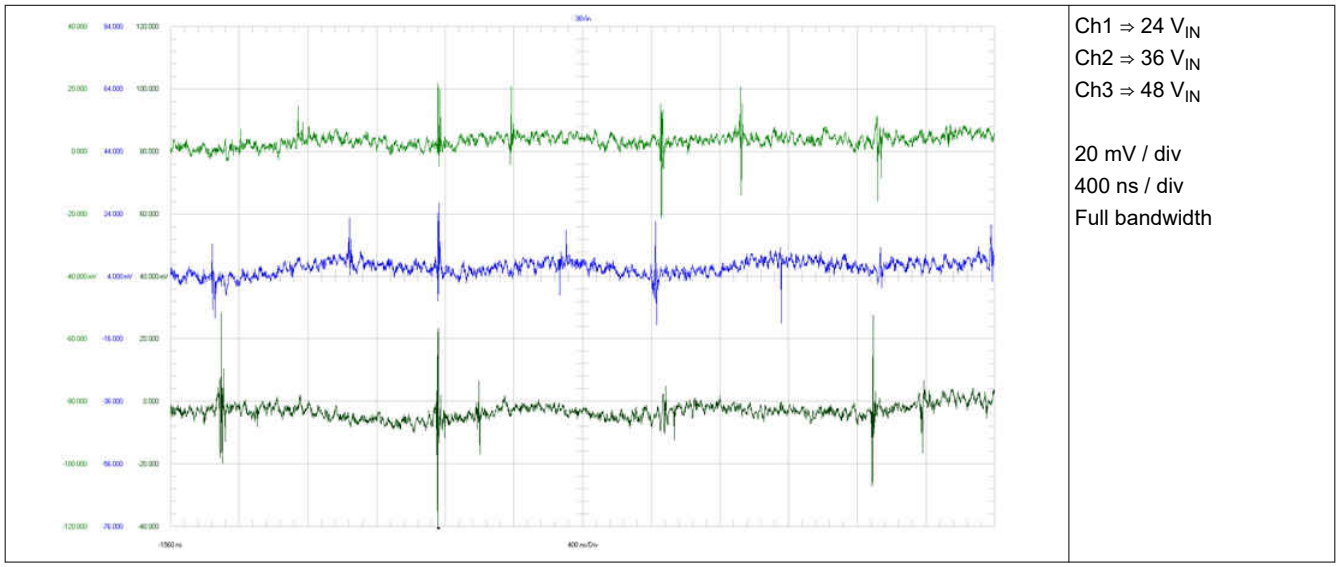


Figure 3-8. Output Voltage Ripple < 10 mV_{PP} (AC Coupled), Noise < 30 mV_{PK}

3.3 Input Voltage Ripple

3.3.1 Board Input

3.3.1.1 24-V Input Voltage

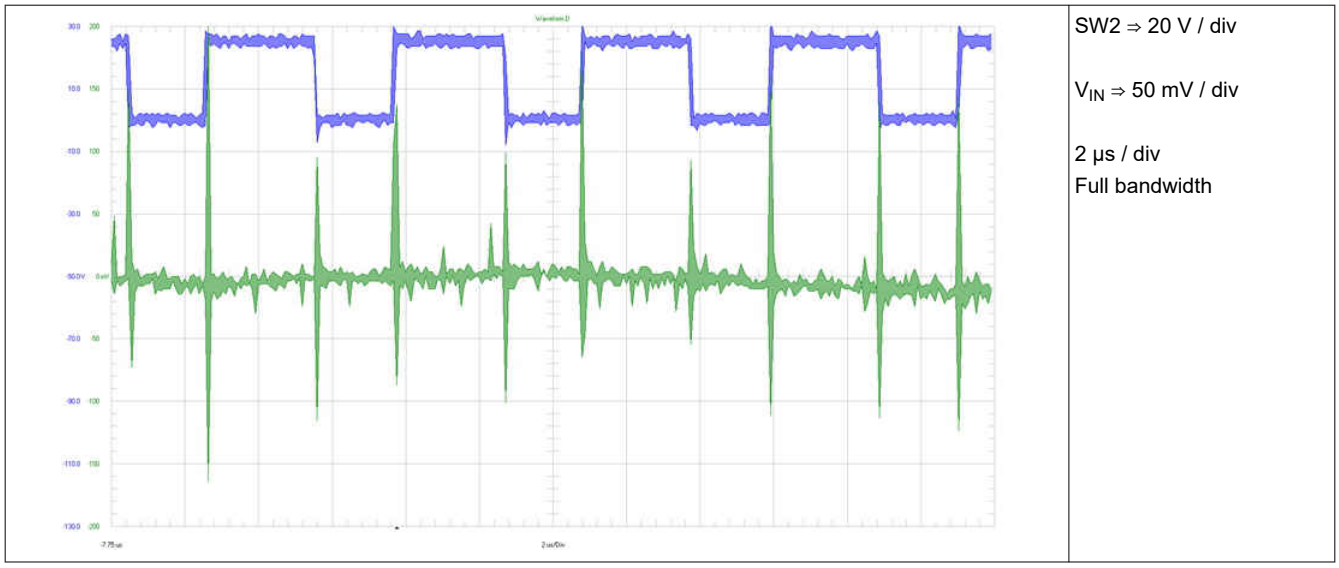


Figure 3-9. Voltage Ripple: Board Input (AC Coupled) at 24-V Input Voltage

3.3.1.2 36-V Input Voltage

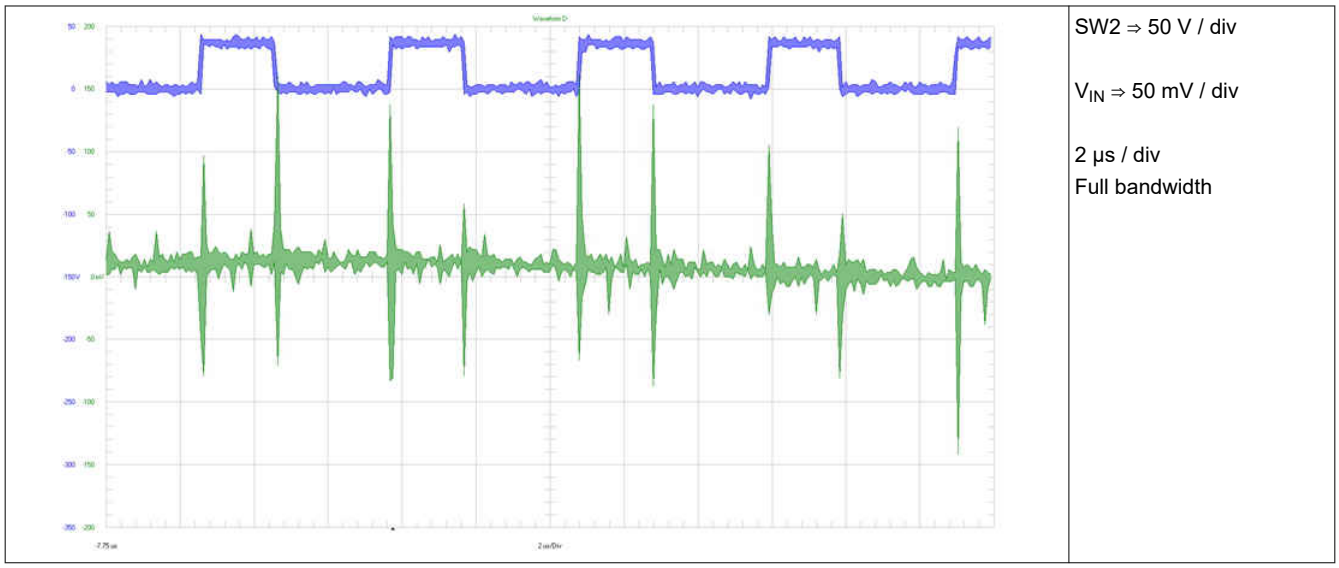


Figure 3-10. Voltage Ripple: Board Input (AC Coupled) at 36-V Input Voltage

3.3.1.3 48-V Input Voltage

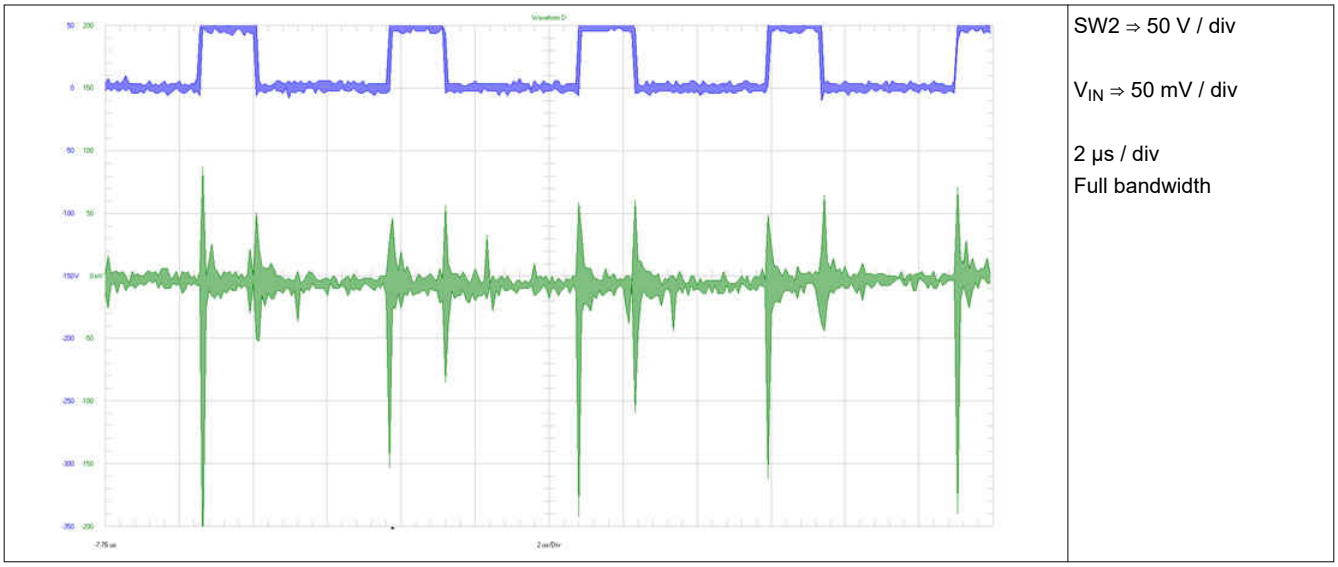


Figure 3-11. Voltage Ripple: Board Input (AC Coupled) at 36-V Input Voltage

3.3.2 Power Stage Input, No Input Filter

3.3.2.1 24-V Input Voltage

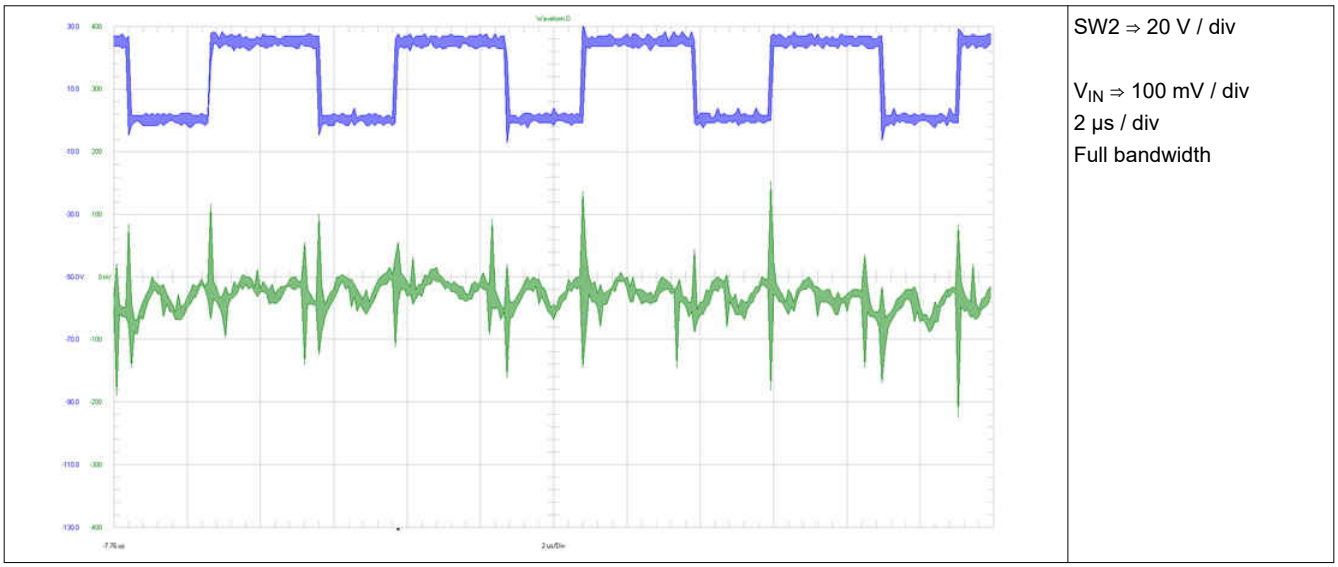


Figure 3-12. Voltage Ripple: Power Stage Input (AC Coupled) at 24-V Input Voltage

3.3.2.2 36-V Input Voltage

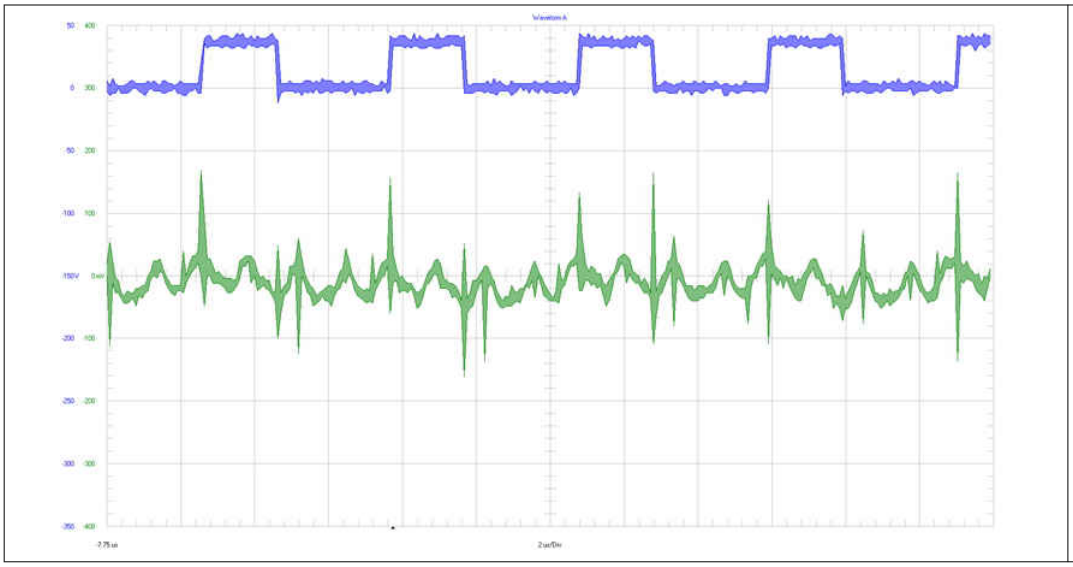


Figure 3-13. Voltage Ripple: Power Stage Input (AC Coupled) at 36-V Input Voltage

3.3.2.3 48-V Input Voltage

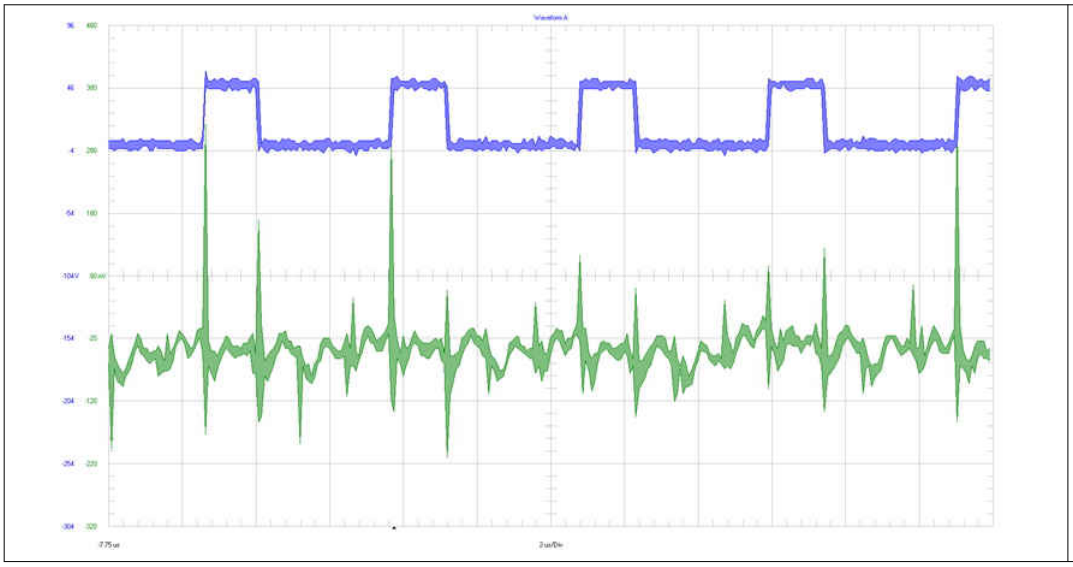


Figure 3-14. Voltage Ripple: Power Stage Input (AC Coupled) at 48-V Input Voltage

3.4 Load Transients

3.4.1 Load Transient 10 A to 50 A (80 %)

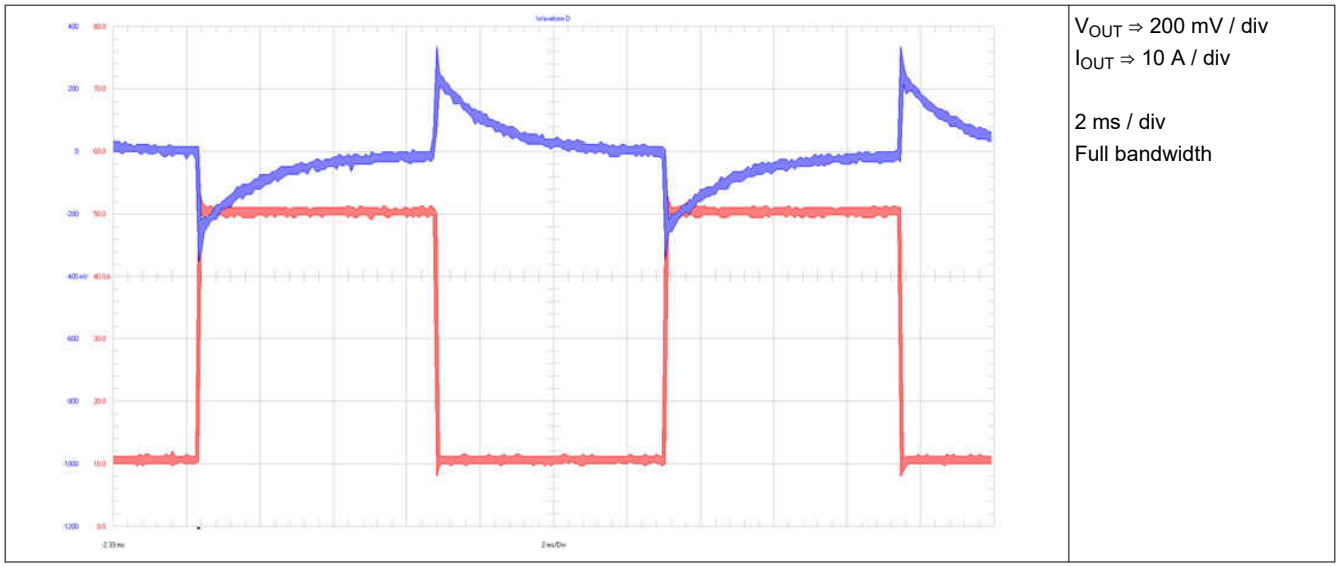


Figure 3-15. Load Transient 10 A to 50 A, Transient Response 350 mV_{PK}

3.4.2 Load Transient 5 A to 50 A (90 %)

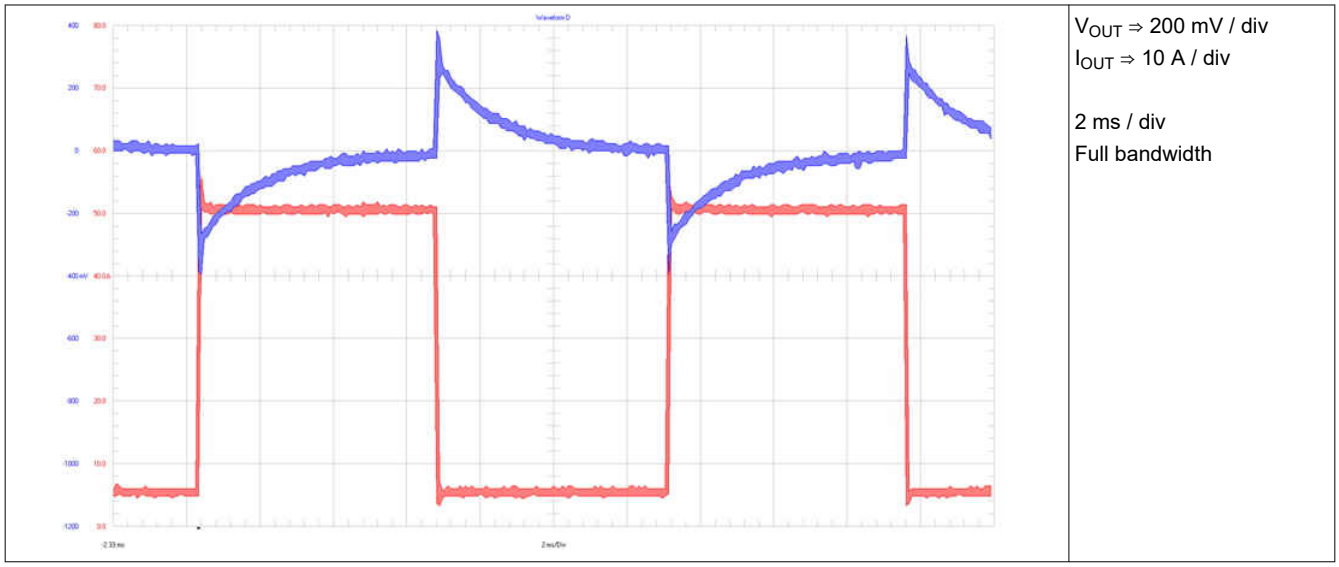
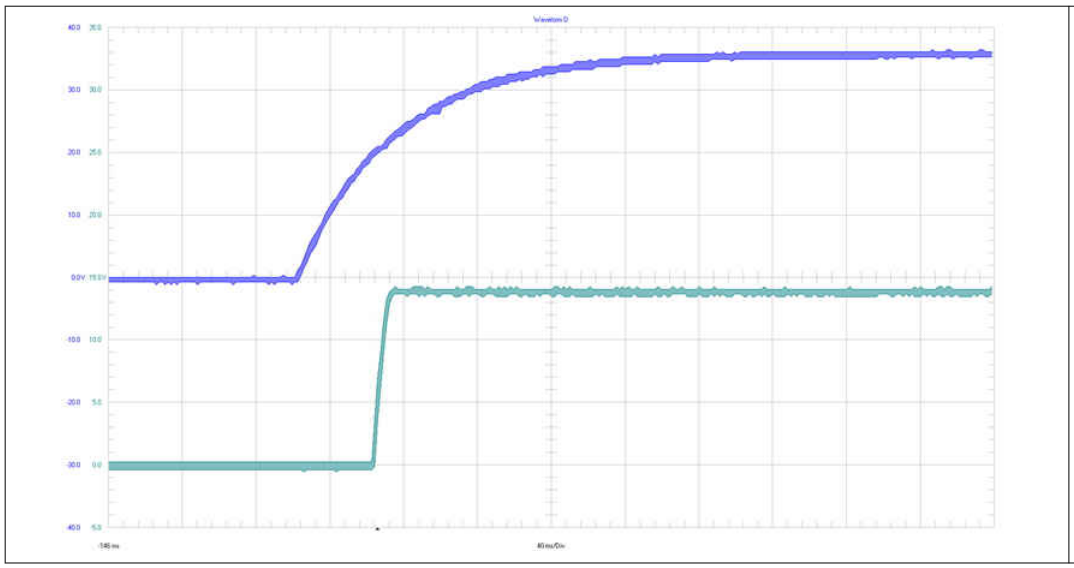


Figure 3-16. Load Transient 5 A to 50 A, Transient Response 400 mV_{PK}, Less Than 3%

3.5 Start-Up Sequence

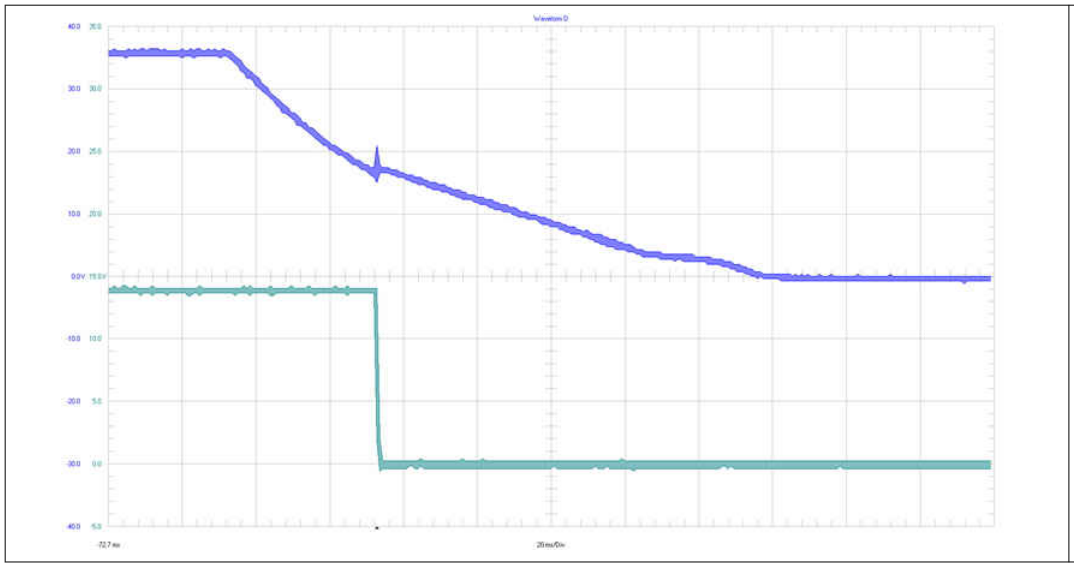


V_{IN} ⇒ 10 V / div
V_{OUT} ⇒ 5 V / div

40 ms / div
20-MHz bandwidth

Figure 3-17. Start-Up (Soft Start 10 ms, set via Capacitor C49 = 330 nF)

3.6 Shutdown Sequence



V_{IN} ⇒ 10 V / div
V_{OUT} ⇒ 5 V / div

20 ms / div
20-MHz bandwidth

Figure 3-18. Shutdown

A Individual Adjusting of the Rising Edge and Falling Edge With LM5143A

The rising edge and falling edge of switch-node waveforms were adjusted by modifying the gate resistors at the high-side FET.

These measurements were done with 24-V input voltage and 50-A output current to prevent FET drain-to-source voltage higher than 60 V_{PP}.

A.1 2.21-Ω High and 4.75-Ω Low Resistor in Before Gate of the High-Side FET

These resistor values are derived from PMP31202.

The 2.21-Ω resistor is connected to the HO pin and the 4.75-Ω resistor is connected to the HOL pin of the LM5143A-Q1.

For reference, see the PMP31210 Schematic.

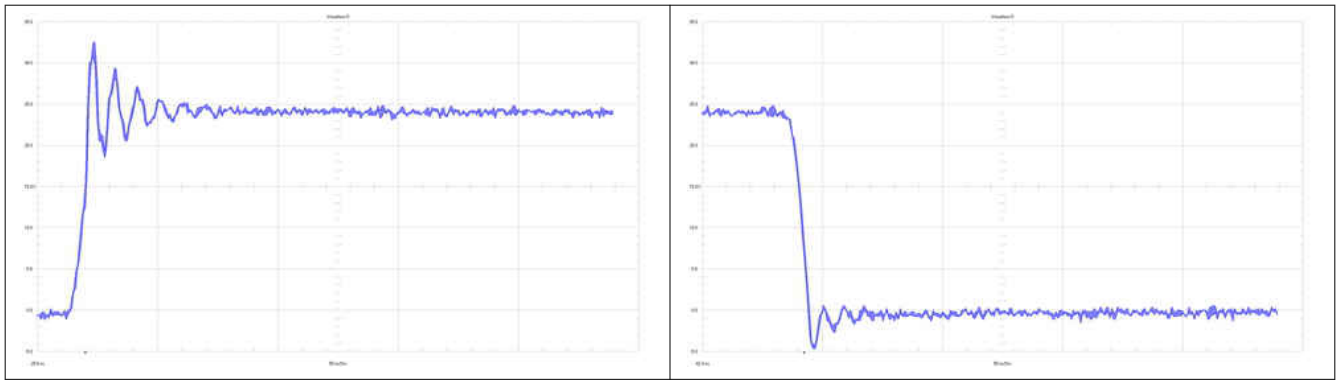


Figure A-1. Waveform at the Switch Node With 2.21-Ω and 4.75-Ω Resistor

A.2 2 × 4.75-Ω Resistors in Before Gate of the High-Side FET

In Figure A-2 the voltage of both the overshoot (OS) and undershoot (US) is less than 5 V_{PK}.

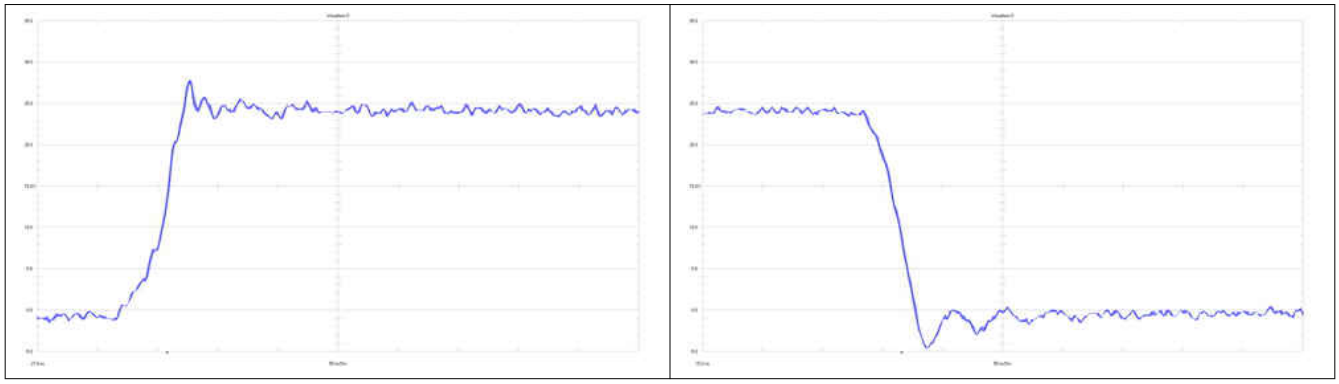


Figure A-2. Waveform at the Switch Node With 4.75-Ω Resistors Each at Rising and Falling Edge

B Measurements Across the Low-Side FETs to Check at All Four Phases

The input voltage was set to 24 V and the output current was adjusted to 50 A.

For reference, see the PMP31210 Schematic.

B.1 FET Q3

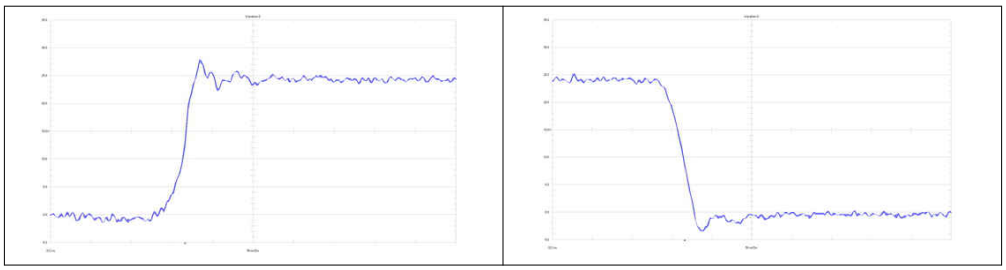


Figure B-1. Waveform at the Switch-Node Q3 Drain to GND

B.2 FET Q4

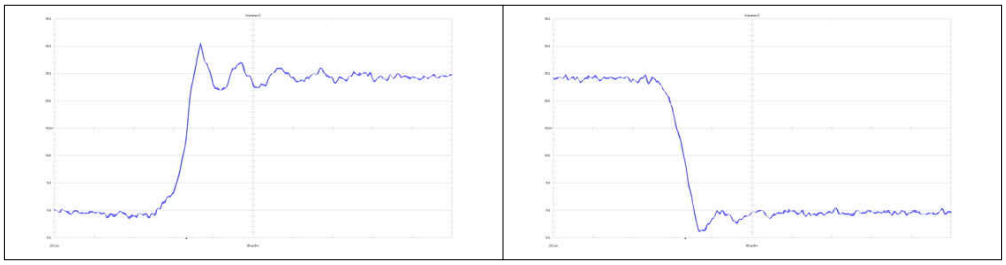


Figure B-2. Waveform at the Switch-Node Q4 Drain to GND

B.3 FET Q7

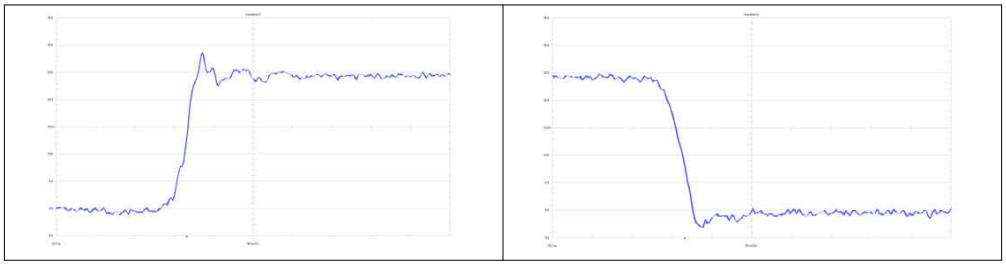


Figure B-3. Waveform at the Switch-Node Q7 Drain to GND

B.4 FET Q8

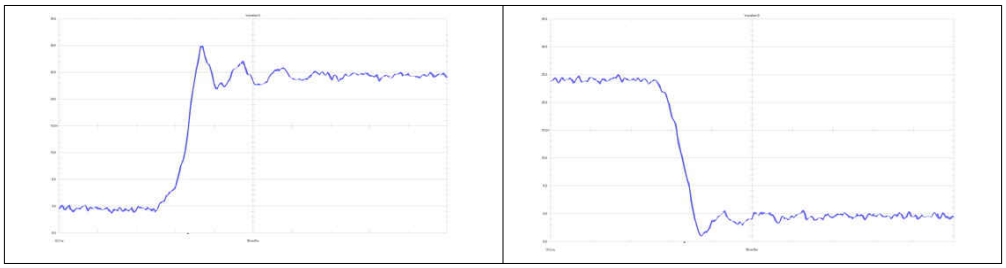


Figure B-4. Waveform at the Switch-Node Q8 Drain to GND

C ON Demand – Assembly of Thermal Interface

Figure C-1. Stack: PCB – Thermal Foil – Adapter - Heat Sink

- Drill the nine holes (diameter 3.5 mm) to Aluminum adapter 150 mm × 75 mm × 5 mm; for correct dimensions use the Altium Designer® file.
- Drill another nine holes (diameter 2.5 mm) to heat sink and cut threads M3
- Add nine holes (diameter 3 mm) to the thermal foil using a punch pliers; so far this is the best choice.
- *Attention*: Less adhesive side of thermal foil (RS) shows towards adapter, strong adhesive side (3M) shows towards the PCB.
- Remove protection foil on less adhesive side **only**, keep protection foil on the other side. Now place the foil at the aluminum adapter.
- Place just the nine screws plus washers at the PCB and place the top down on the PCB, two pieces of tape keep the screws in place, so there are nine *bolts* on the other side, this helps for the next step.
- Remove protection foil at the strong adhesive side of the thermal foil, remove white protection foil at the adapter and place the adapter precisely on PCB.
- Flip by keeping the adapter in place and set the adapter and PCB on top of heat sink, remove tapes and fix the screws. This completes the process

EMI: the adapter and heat sink are floating and provide the shortest connection J3 GND to the screw left of the L2 heat sink. Figure C-2 shows a GND connection.

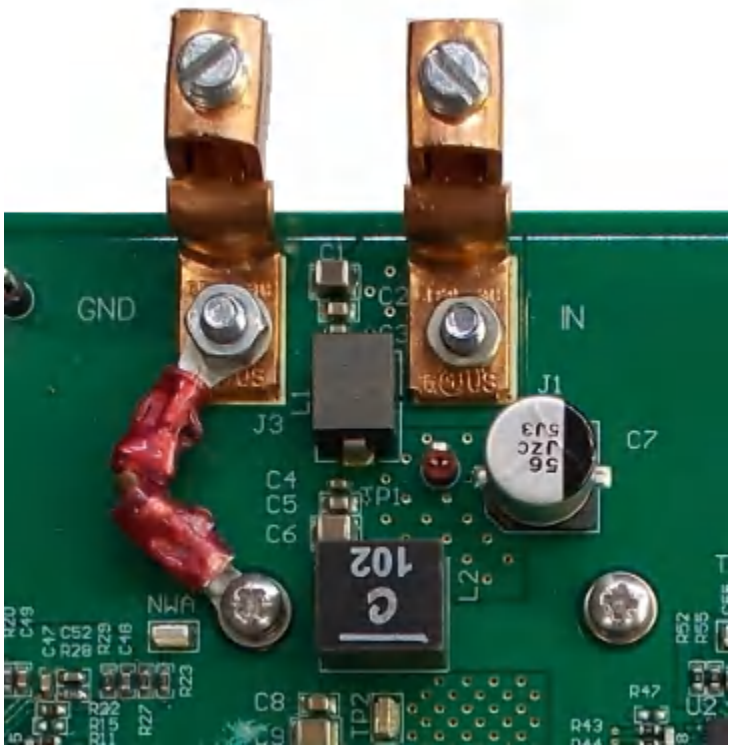
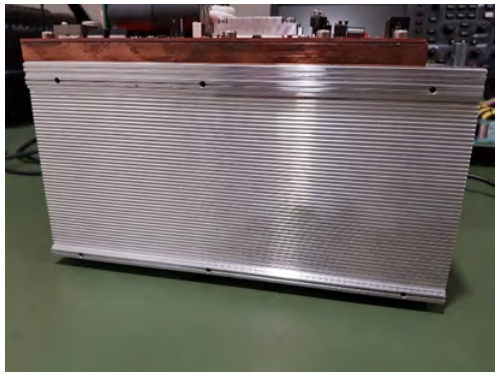


Figure C-2. GND Connection

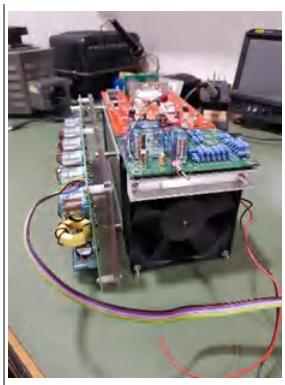
C.1 Thermal Interface Example

The following images provide examples for the best thermal interface, besides water cooling. In these examples, the RF amplifier sinking losses are 300 W and higher.



copper adapter, diameter 10 mm

heat sink, for fan 120 mm × 120 mm



fan in front and back

Figure C-3. Example for Best Thermal Interface

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