Test Report: PMP22589

Ultra-Wide Input, 10-W Isolated Flyback Reference Design

Description

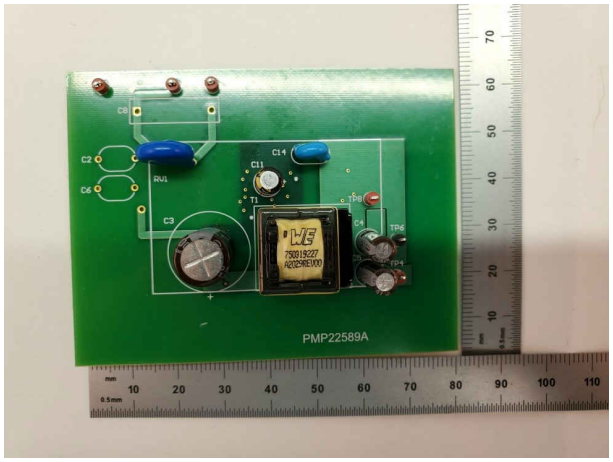
This reference design is a wide-V_{IN}, low-power flyback design that can take dual inputs from 19 VDC to 60 VDC and 85 VAC to 275 VAC. It is designed to provide 24 V at 420 mA to the output load.

Features

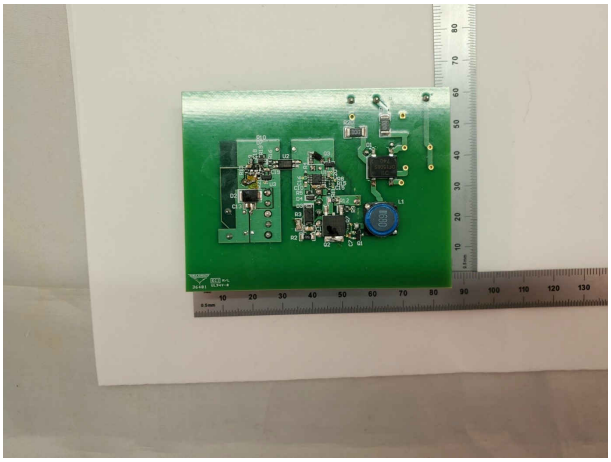
- Ultra-wide input
- Small form factor
- Excellent regulation over wide input

Applications

- AC charging (pile) station



Board Photo (Top)



Board Photo (Bottom)

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	19 VDC to 60 VDC or 85 VAC to 275 VAC
Output Voltage	24 V
Output Current	420 mA

1.2 Required Equipment

Working with this design requires the following equipment:

- DC voltage source
- AC voltage source
- AC/DC power meter
- Electronic load
- Multimeters
- Oscilloscope

2 Testing and Results

2.1 DC Input Efficiency and Voltage Regulation Graphs

Figure 2-1 and Figure 2-2 show the DC input efficiency and DC input Vout regulation graphs.

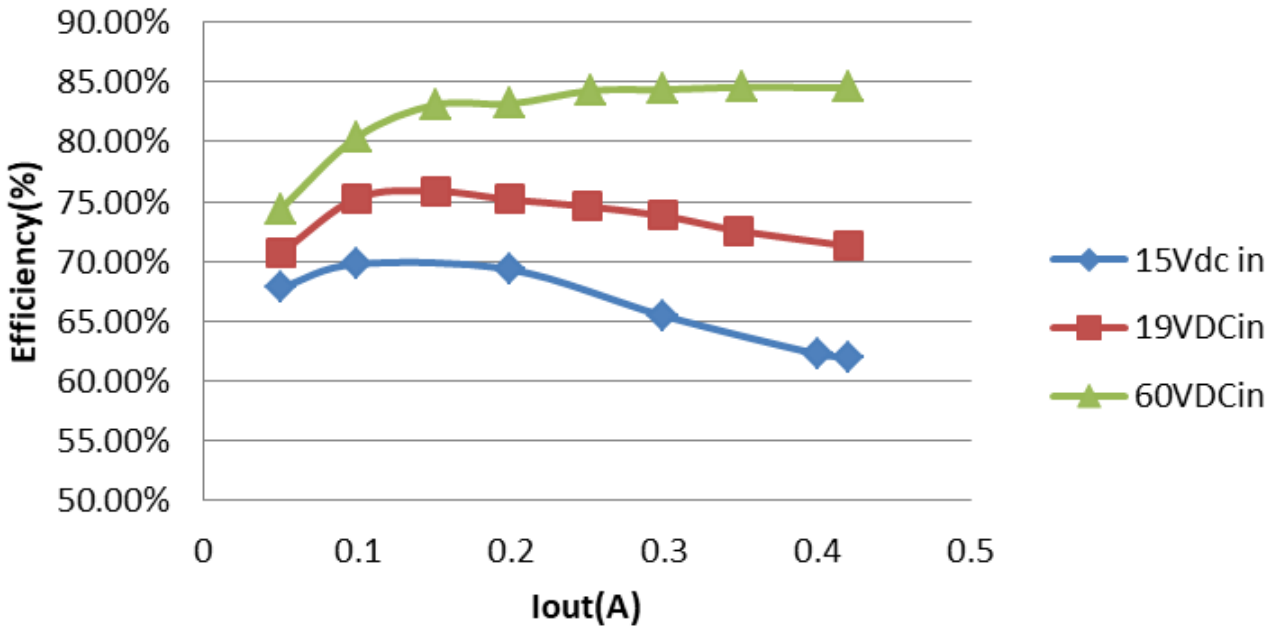


Figure 2-1. DC Input Efficiency

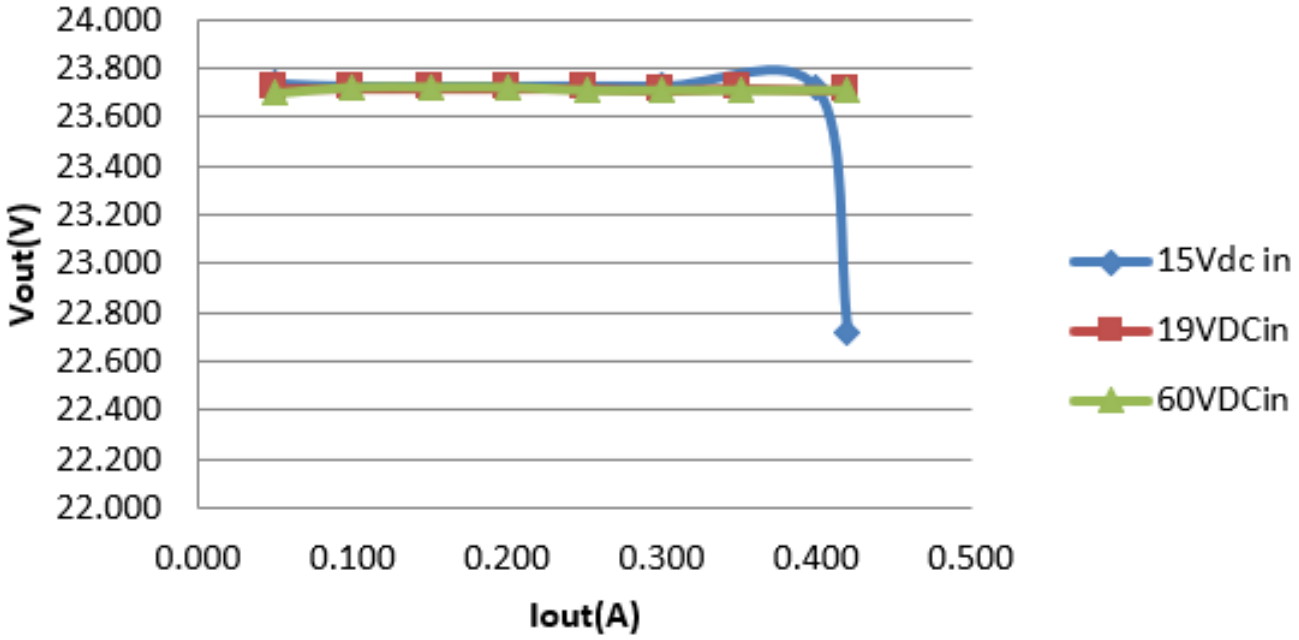


Figure 2-2. DC Input Vout Regulation

2.2 DC Input Efficiency and Voltage Regulation Data

Table 2-1 through Table 2-3, show the DC Input Efficiency and Voltage Regulation Data at 15 VDC, 19 VDC, and 60 VDC, respectively.

Table 2-1. 15 VDC

Vin (VDC)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Ploss (W)
15.038	0.017	0.258	23.740	0.000	0.000	0.000	0.258
15.028	0.116	1.750	23.730	0.050	1.187	0.678	0.564
15.011	0.227	3.400	23.730	0.100	2.373	0.698	1.027
15.080	0.454	6.845	23.730	0.200	4.746	0.693	2.099
15.047	0.722	10.869	23.720	0.300	7.116	0.655	3.753
15.000	0.973	14.590	22.720	0.400	9.088	0.623	5.502
15.014	0.983	14.760	21.800	0.420	9.156	0.620	5.604

Table 2-2. 19 VDC

Vin (VDC)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Ploss (W)
19.138	0.012	0.231	23.720	0.000	0.000	0.000	0.231
19.129	0.088	1.678	23.720	0.050	1.186	0.707	0.492
19.119	0.165	3.150	23.720	0.100	2.372	0.753	0.778
19.104	0.247	4.720	23.720	0.151	3.582	0.759	1.138
19.094	0.330	6.310	23.720	0.200	4.744	0.752	1.566
19.090	0.416	7.944	23.710	0.250	5.928	0.746	2.017
19.075	0.505	9.640	23.720	0.300	7.116	0.738	2.524
19.000	0.600	11.401	23.710	0.349	8.275	0.726	3.126
19.081	0.732	13.970	23.720	0.420	9.962	0.713	4.008

Table 2-3. 60 VDC

Vin (VDC)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Ploss (W)
60.140	0.004	0.227	23.700	0.000	0.000	0.000	0.227
60.140	0.027	1.595	23.720	0.050	1.186	0.744	0.409
60.140	0.049	2.950	23.720	0.100	2.372	0.804	0.578
60.130	0.072	4.310	23.720	0.151	3.582	0.831	0.728
60.130	0.095	5.700	23.710	0.200	4.742	0.832	0.958
60.120	0.118	7.089	23.710	0.252	5.975	0.843	1.114
60.120	0.140	8.430	23.710	0.300	7.113	0.844	1.317
60.110	0.164	9.840	23.710	0.351	8.322	0.846	1.518
60.110	0.196	11.780	23.710	0.420	9.958	0.845	1.822

2.3 AC Input Efficiency and Voltage Regulation Graphs

Figure 2-3 and Figure 2-4 show the AC input efficiency and voltage regulation graphs.

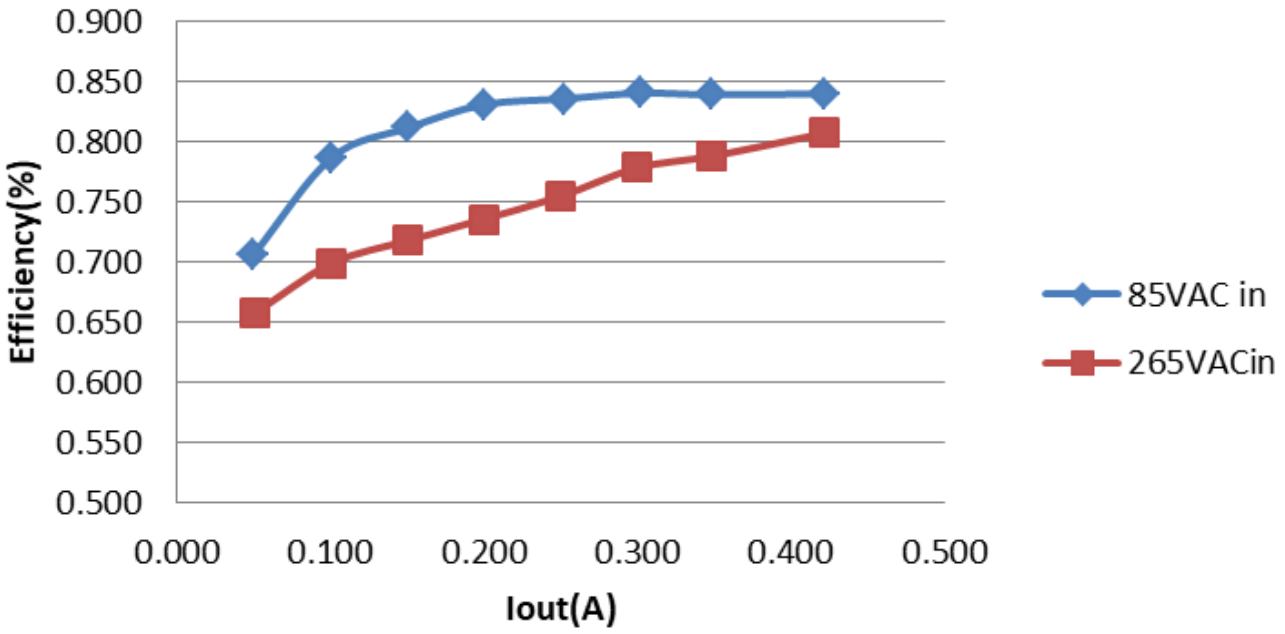


Figure 2-3. AC Input Efficiency

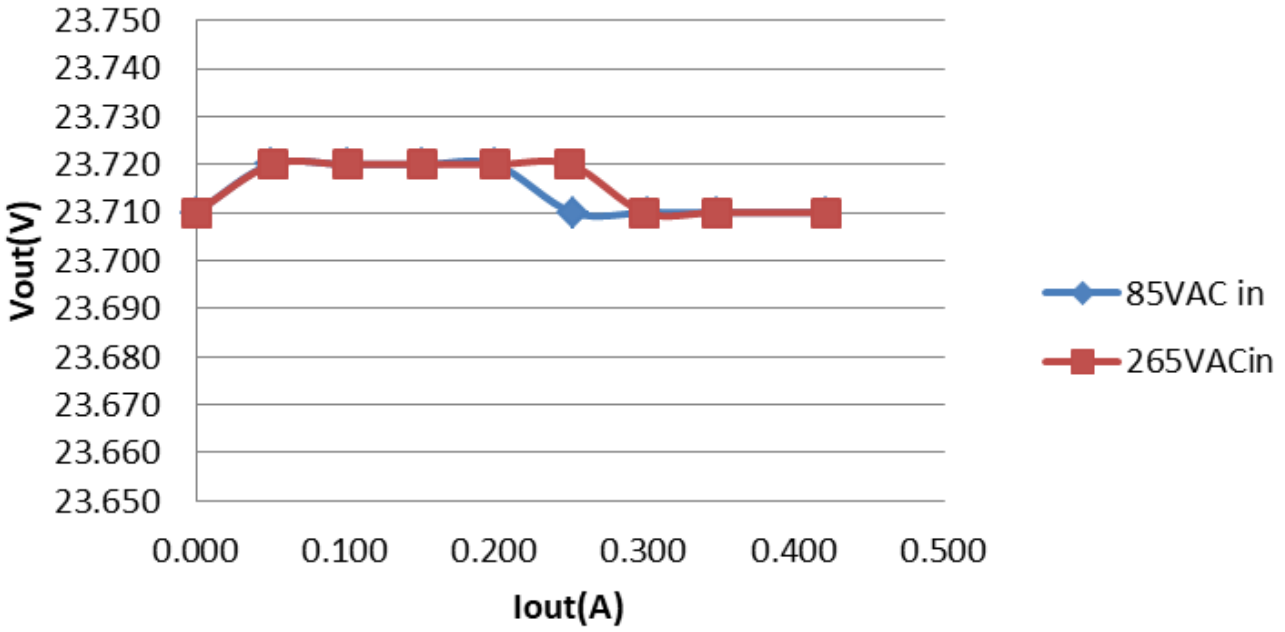


Figure 2-4. AC Input Vout Regulation

2.4 AC Input Efficiency and Voltage Regulation Data

Table 2-4 and Table 2-5 show the AC input efficiency and voltage regulation data at 85 VAC and 265 VAC, respectively.

Table 2-4. 85 VAC

Vin (VAC)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Ploss (W)
85.000	0.348	23.710	0.000	0.000	0.000	0.348
85.000	1.680	23.720	0.050	1.186	0.706	0.494
85.150	3.045	23.720	0.101	2.396	0.787	0.649
85.150	4.413	23.720	0.151	3.582	0.812	0.831
85.150	5.710	23.720	0.200	4.744	0.831	0.966
85.150	7.150	23.710	0.252	5.975	0.836	1.175
85.150	8.520	23.710	0.302	7.160	0.840	1.360
85.150	9.860	23.710	0.349	8.275	0.839	1.585
85.150	11.914	23.710	0.422	10.006	0.840	1.908

Table 2-5. 265 VAC

Vin (VAC)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Ploss (W)
265.000	1.080	23.710	0.000	0.000	0.000	1.080
265.000	1.840	23.720	0.051	1.210	0.657	0.630
265.000	3.428	23.720	0.101	2.396	0.699	1.032
265.000	4.990	23.720	0.151	3.582	0.718	1.408
265.000	6.450	23.720	0.200	4.744	0.736	1.706
265.000	7.860	23.720	0.250	5.930	0.754	1.930
265.000	9.140	23.710	0.300	7.113	0.778	2.027
265.000	10.500	23.710	0.349	8.275	0.788	2.225
265.000	12.400	23.710	0.422	10.006	0.807	2.394

2.5 Thermal Images

Figure 2-5 through Figure 2-7 were taken at 19 VDCin; full load, 15 minute soak, room temperature, no airflow, and no heat sink.

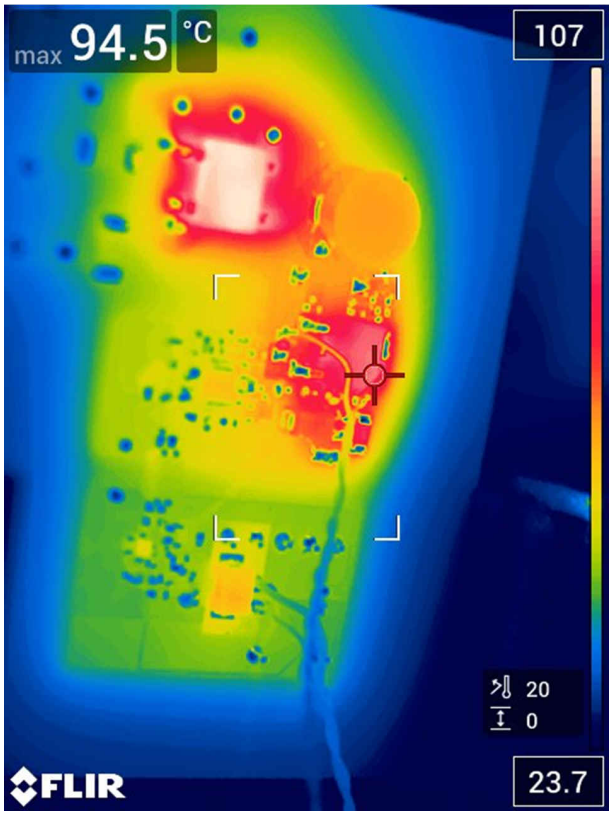


Figure 2-5. Back of the Board Showing Q2, D3, and R2 at About 94.5°C

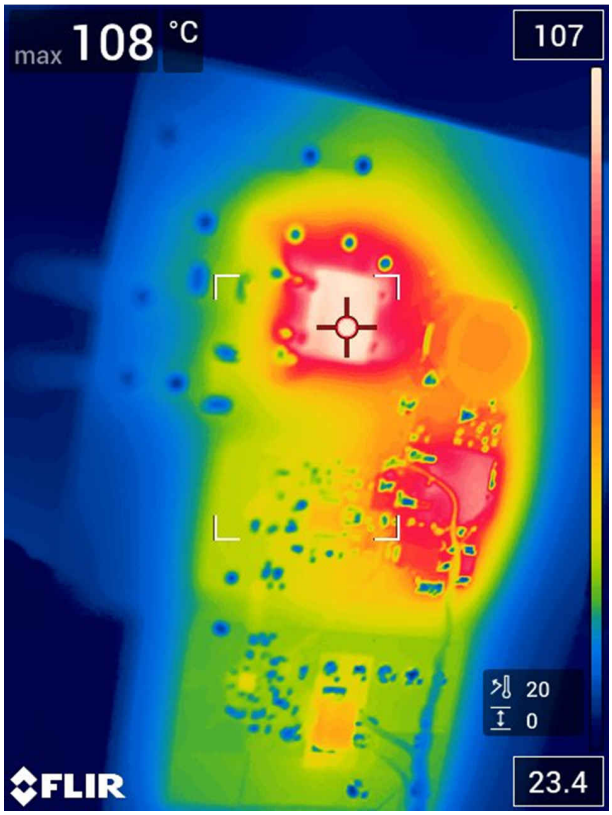


Figure 2-6. Dbridge = 108°C

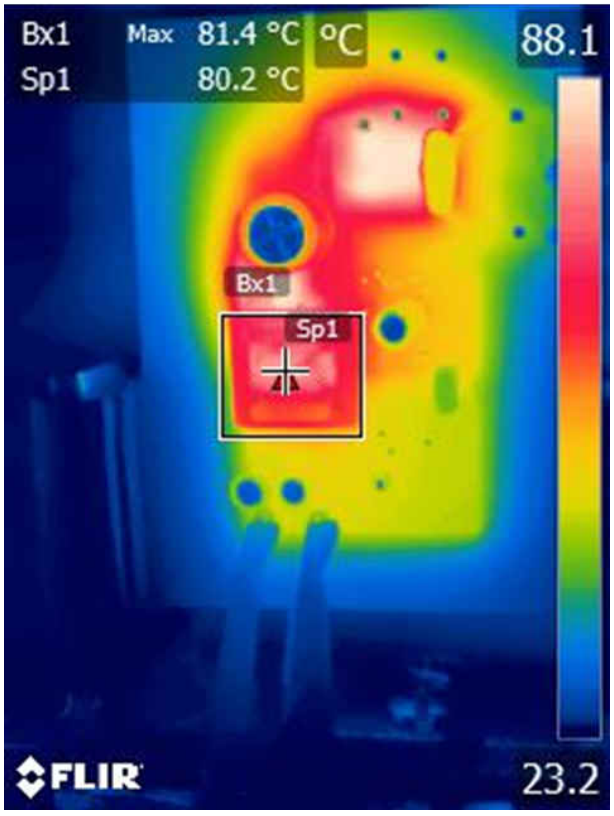


Figure 2-7. Front of the Board – Transformer Showing 80°C

Figure 2-8 and Figure 2-9 were taken at 85 VACin; full load, 15 minute soak, room temperature, no airflow, and no heat sink.

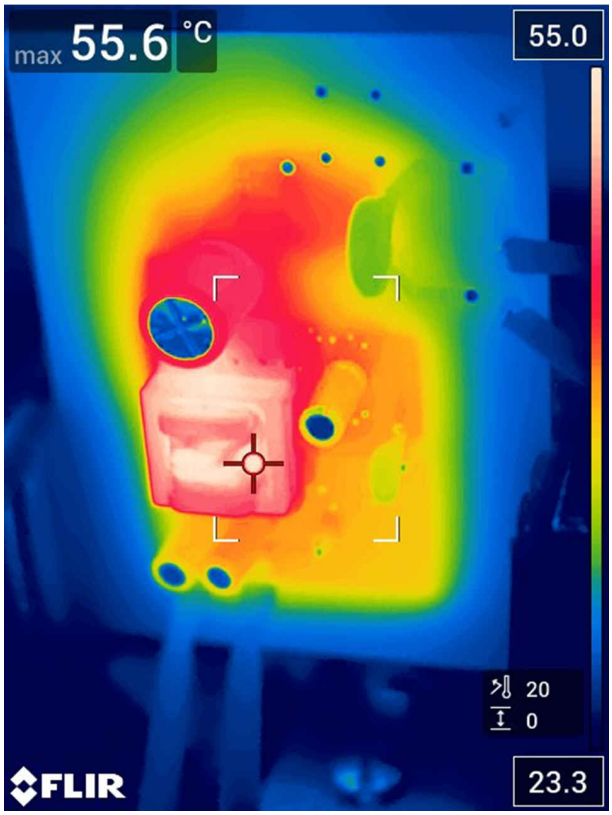


Figure 2-8. Front of the Board - Transformer Showing 55°C

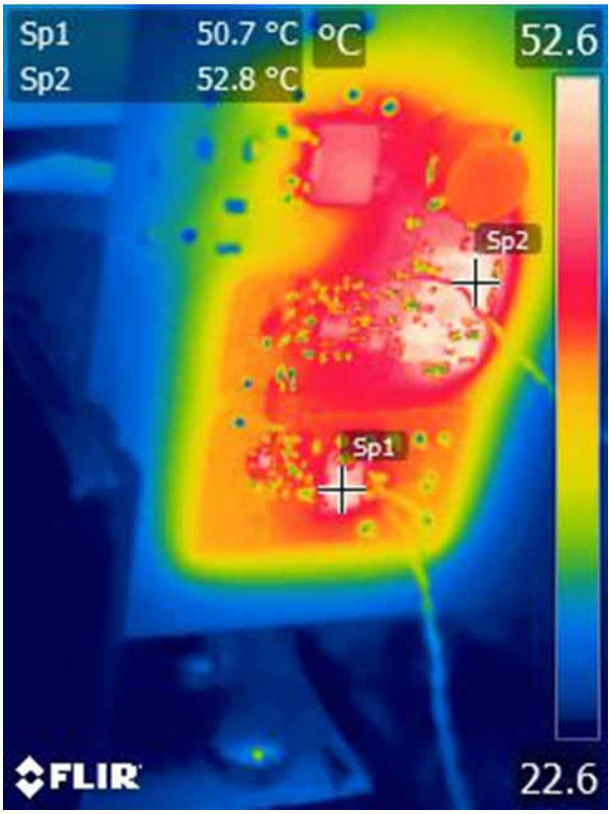


Figure 2-9. Bottom of Board Showing Dout = 50.7°C; Qpri = 52.8°C

Figure 2-10 and Figure 2-11 were taken at 275 VACin; full load, 15 minute soak, room temperature, no airflow, and no heat sink.

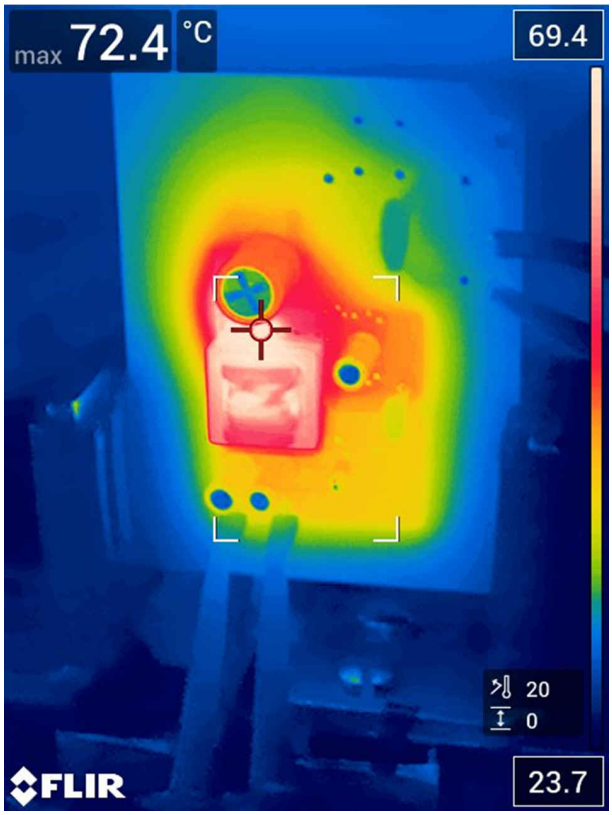


Figure 2-10. Top of Board Showing XFMER = 72.4°C

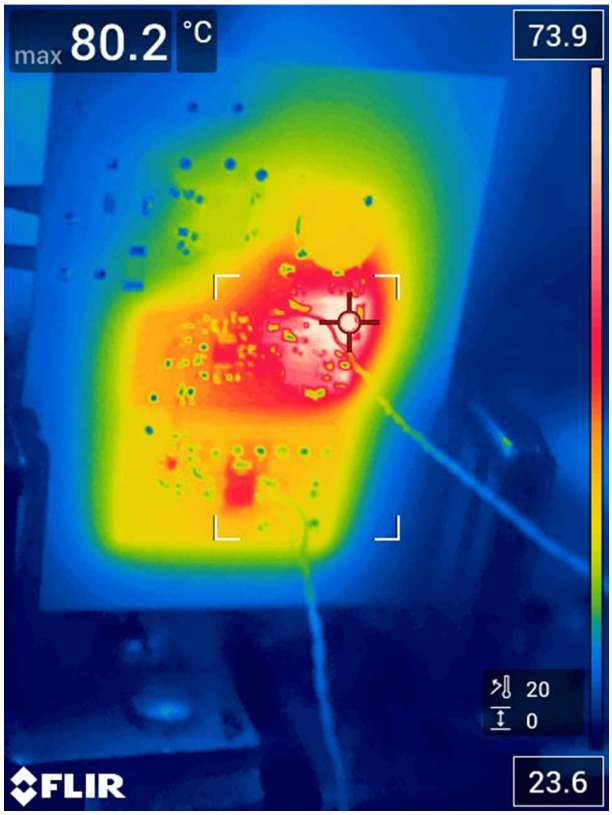


Figure 2-11. Bottom of Board Showing Q2 at 80°C

2.6 Bode Plots

The following image illustrates the PMP22589 bode plot.

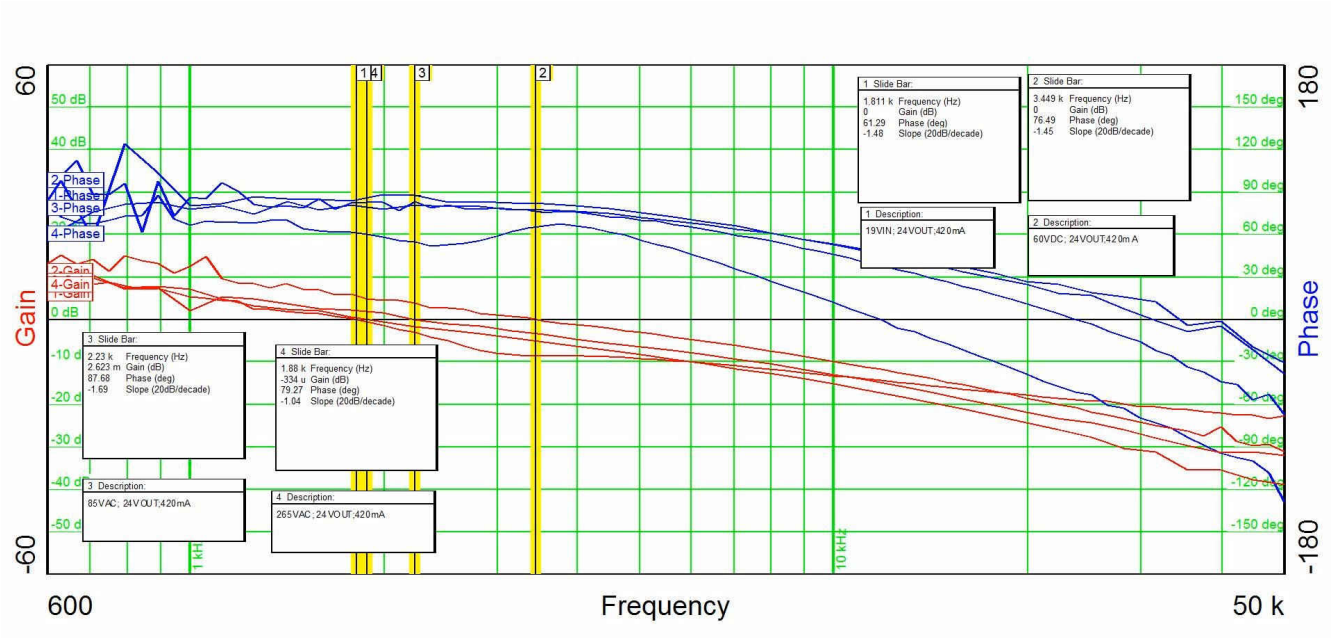


Figure 2-12. Bode Plot

3 Waveforms

3.1 Switch-Node Waveforms

Figure 3-1. 19 VDCin; 24 V_{OUT} at 0 mA

Figure 3-2. 19 VDCin; 24 V_{OUT} at 420 mA

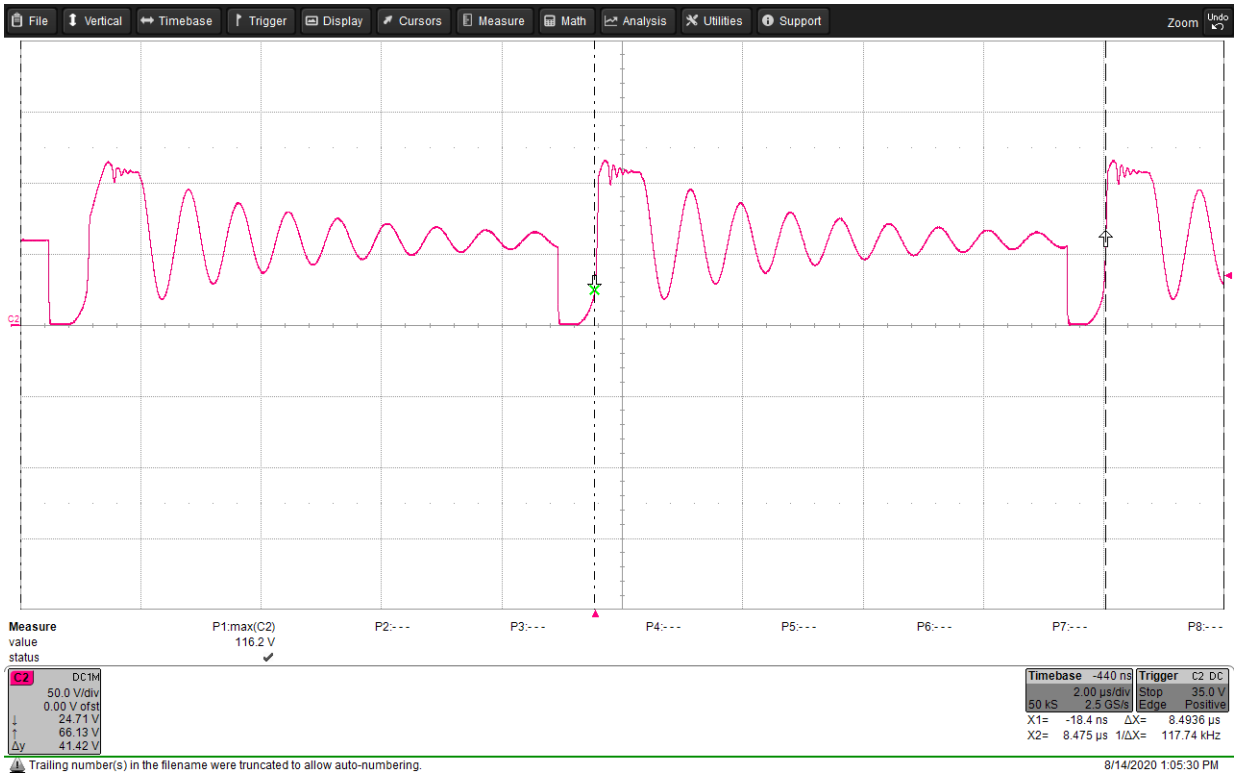


Figure 3-3. 60 VDCin; 24 V_{OUT} at 0 mA

Figure 3-4. 60 VDCin; 24 V_{OUT} at 420 mA

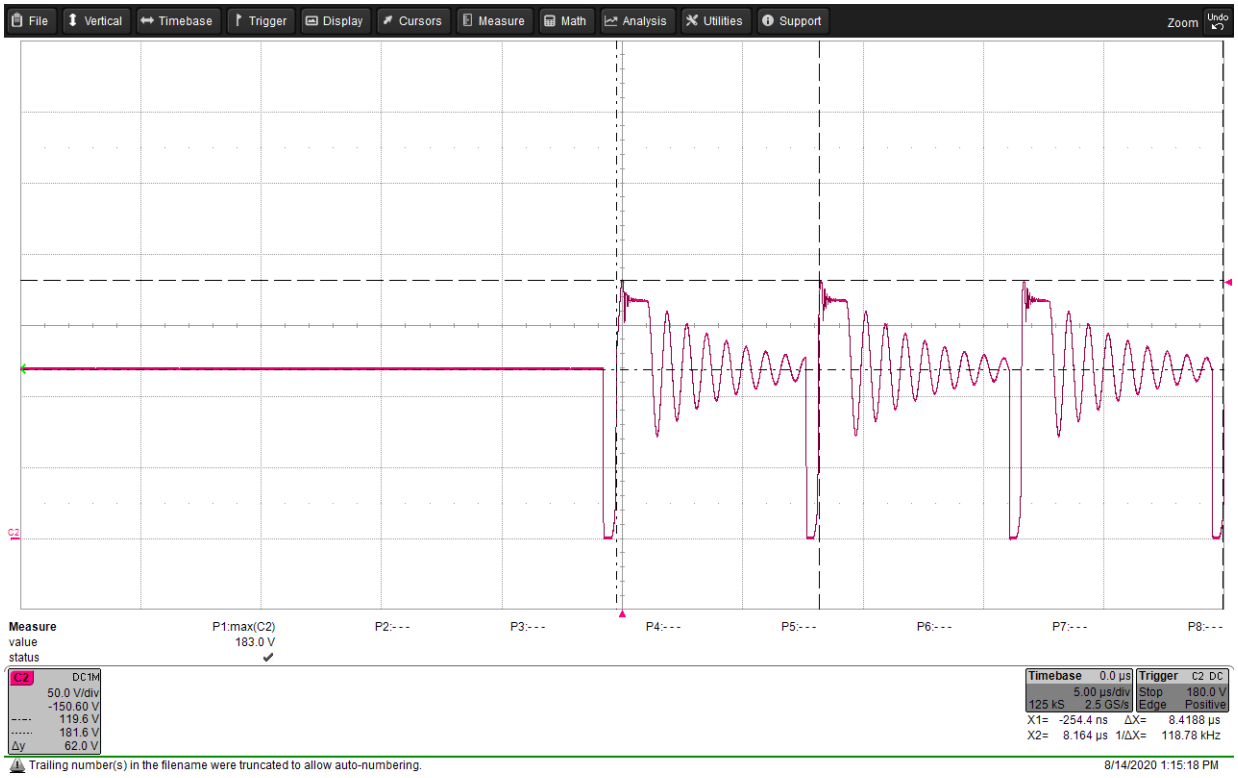


Figure 3-5. 85 VACin; 24 V_{OUT} at 0 mA

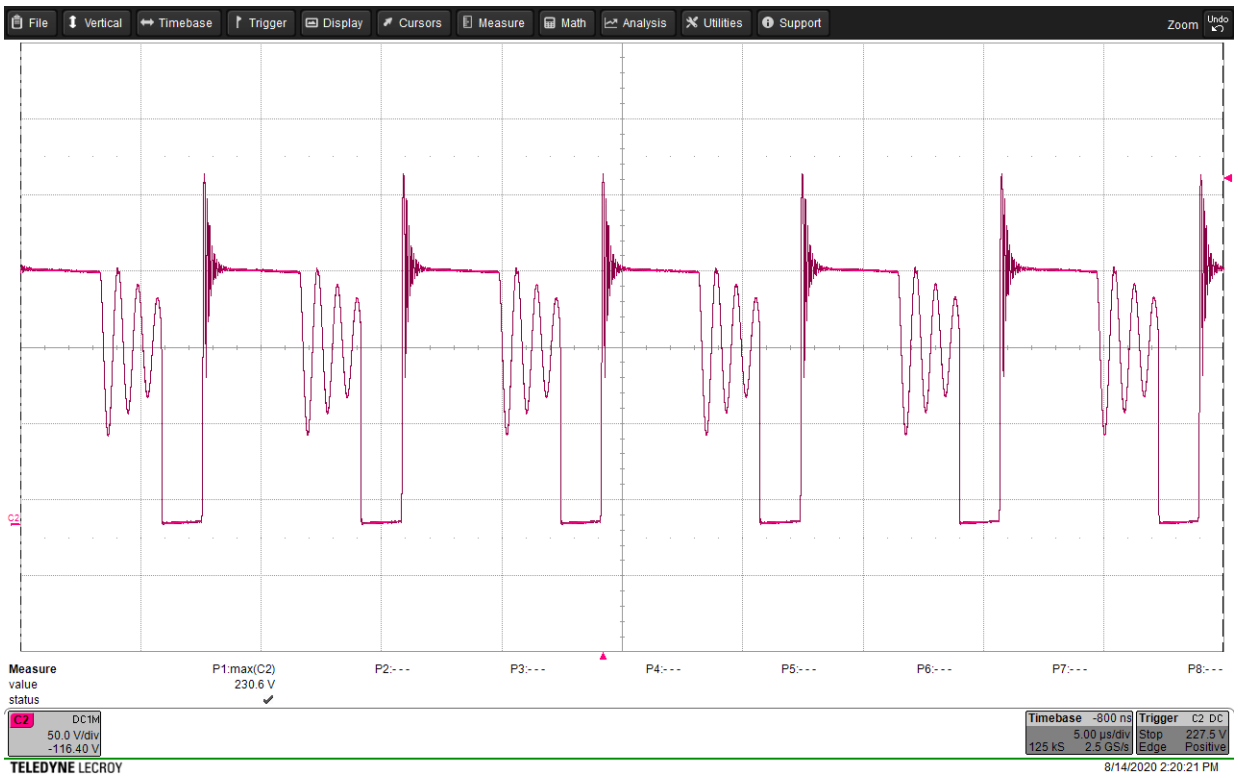


Figure 3-6. 85 VACin; 24 V_{OUT} at 420 mA

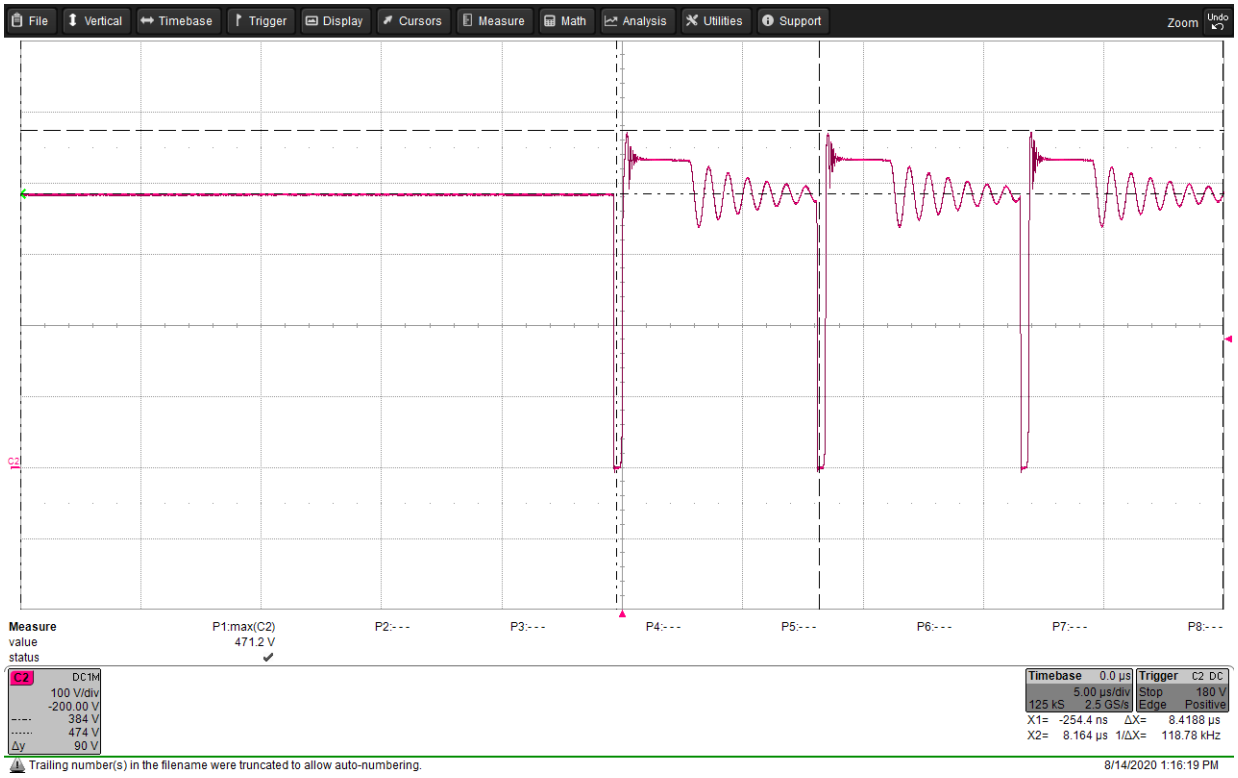


Figure 3-7. 275 VACin; 24 V_{OUT} at 0 mA

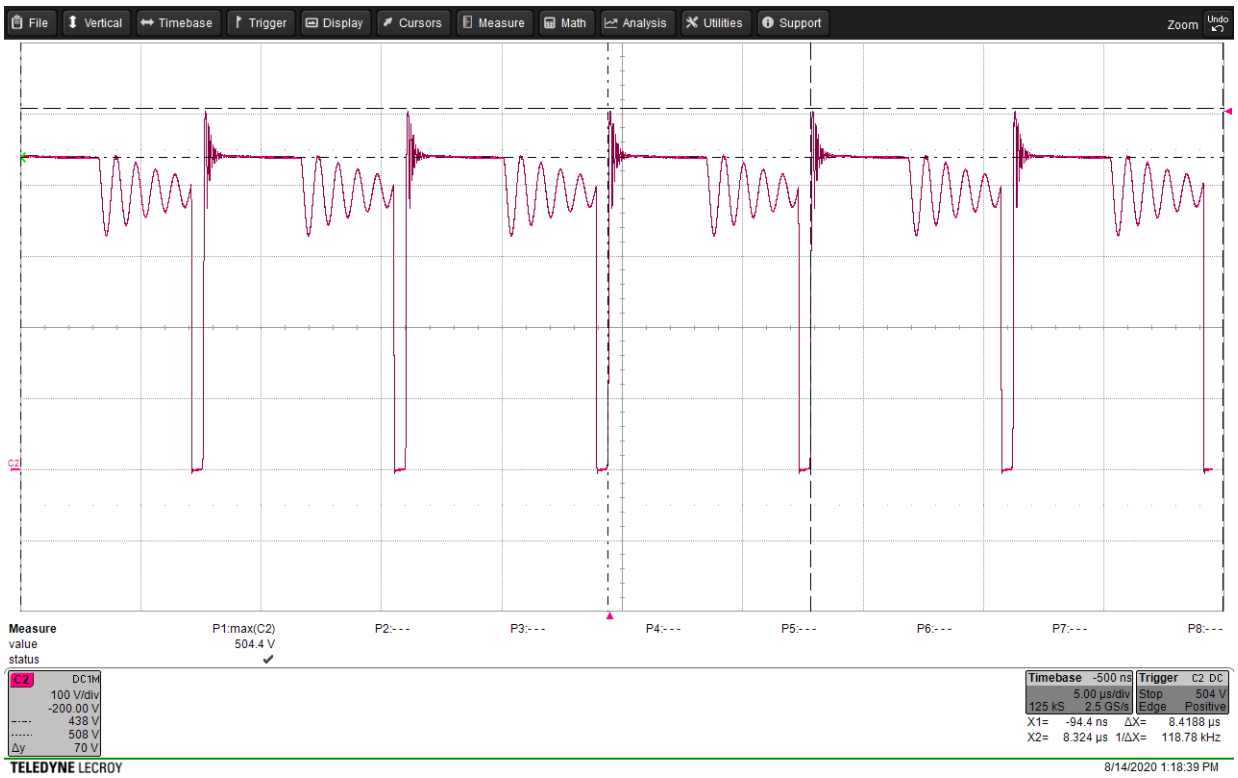


Figure 3-8. 275 VACin; 24 V_{OUT} at 420 mA

3.2 Output Voltage Ripple

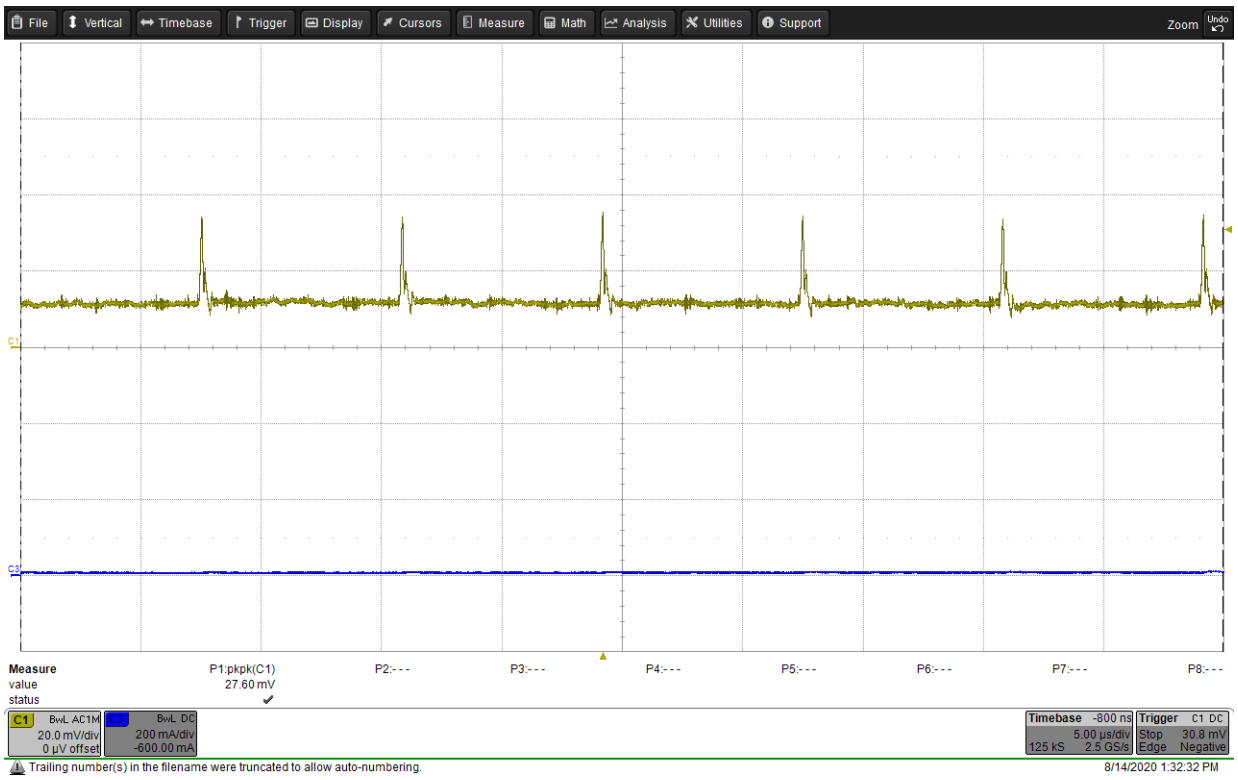


Figure 3-9. 19 VDCin; 24 V_{OUT} at 0 mA

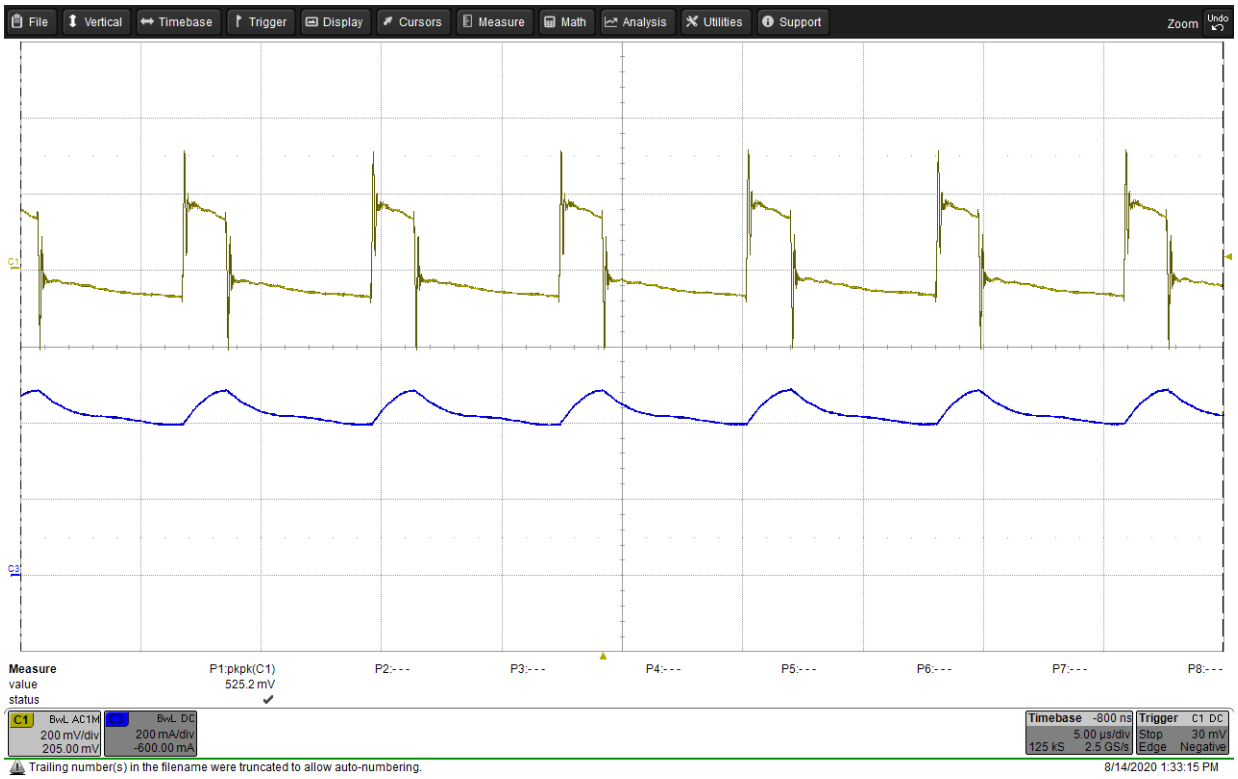


Figure 3-10. 19 VDCin; 24 V_{OUT} at 420 mA

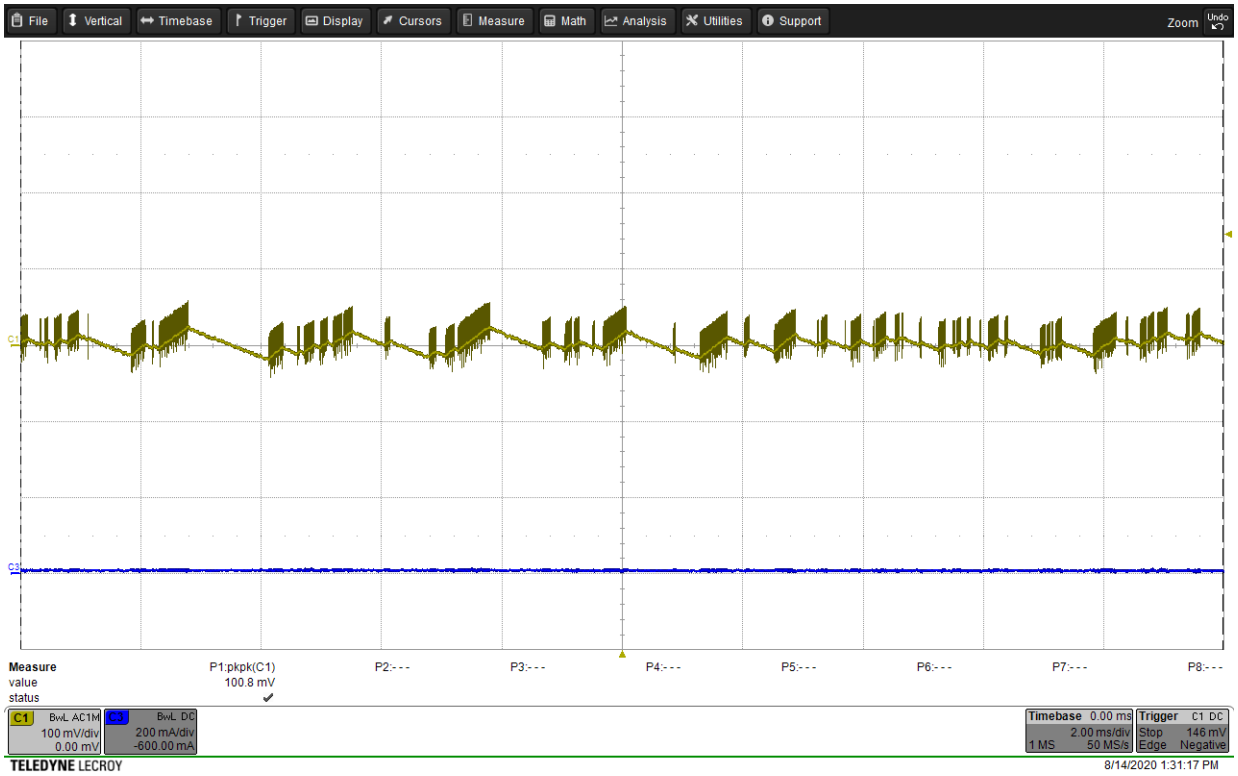


Figure 3-11. 60 VDCin; 24 V_{OUT} at 0 mA

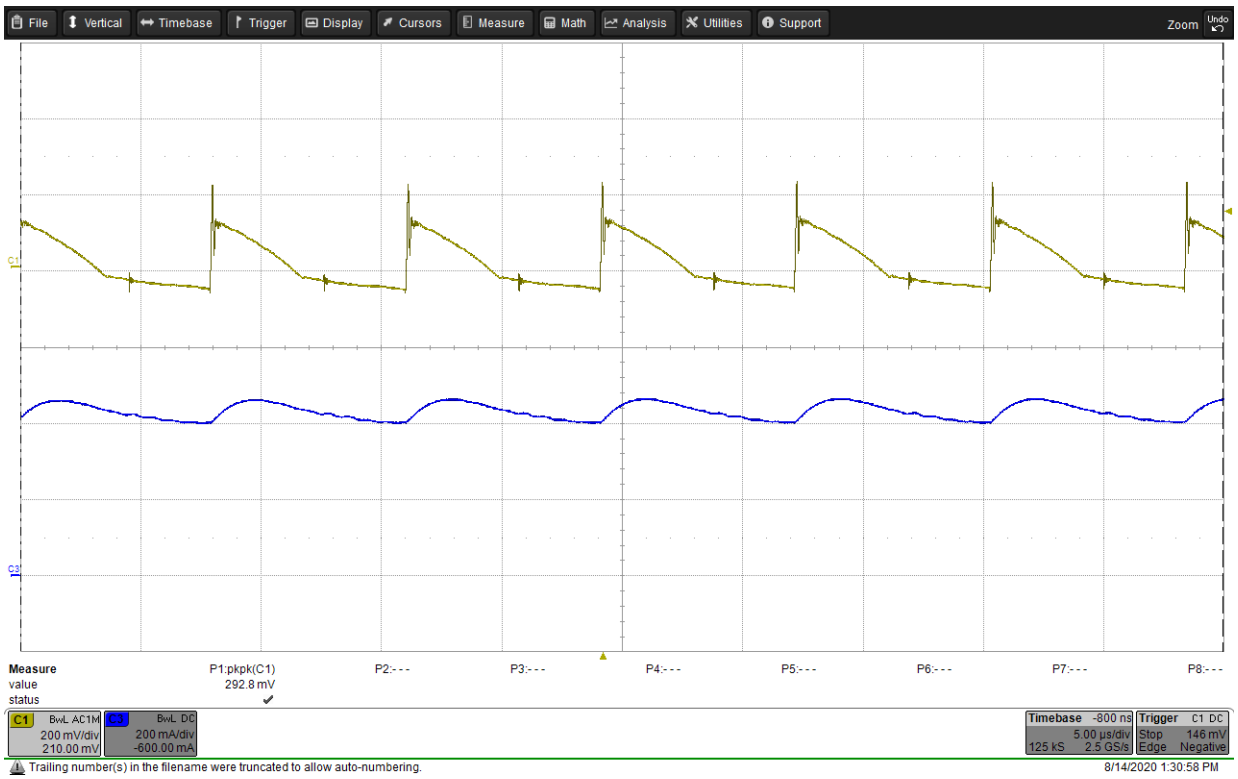


Figure 3-12. 60 VDCin; 24 V_{OUT} at 420 mA

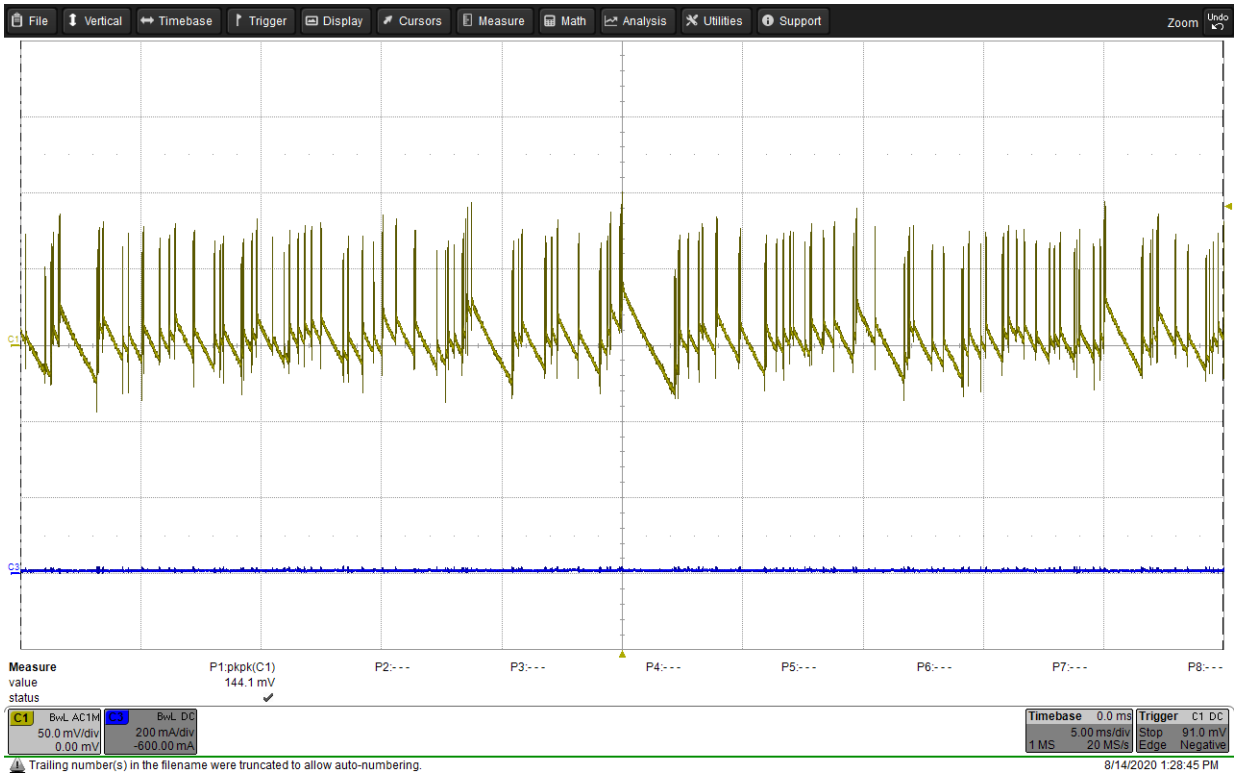


Figure 3-13. 85 VACin; 24 V_{OUT} at 0 mA

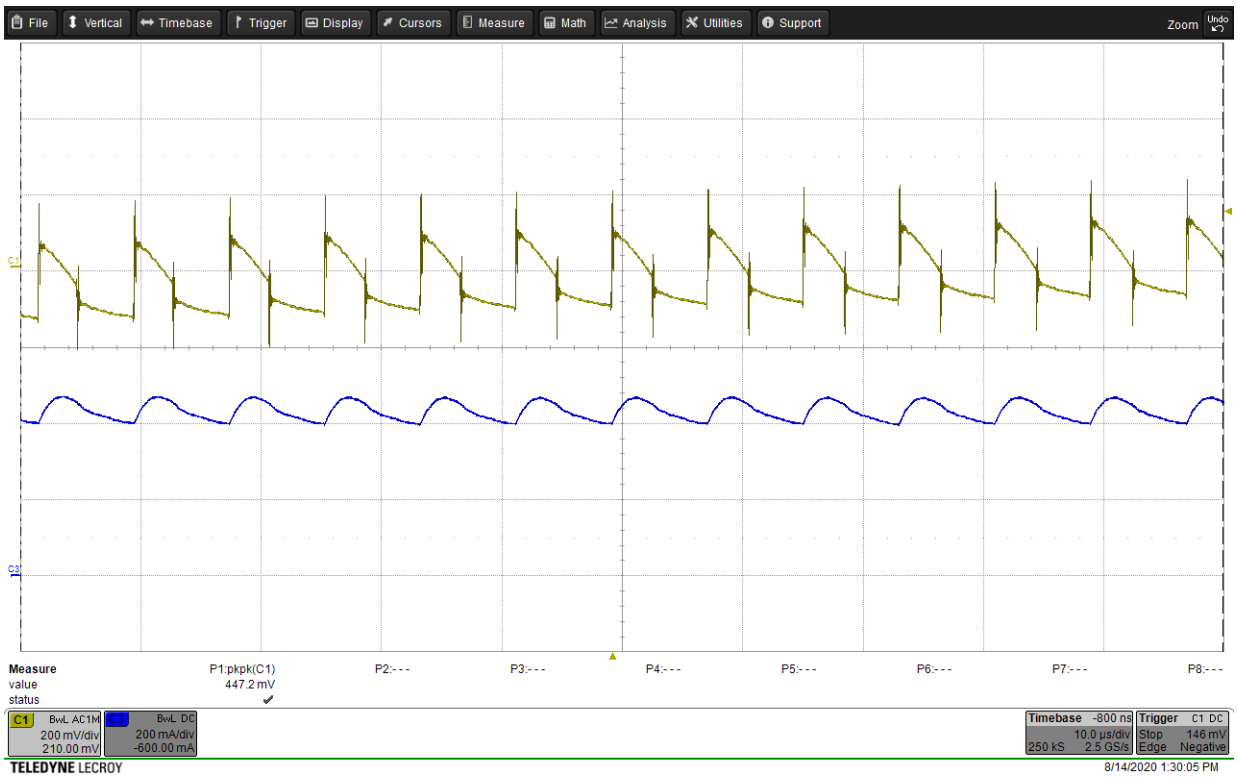


Figure 3-14. 85 VACin; 24 V_{OUT} at 420 mA

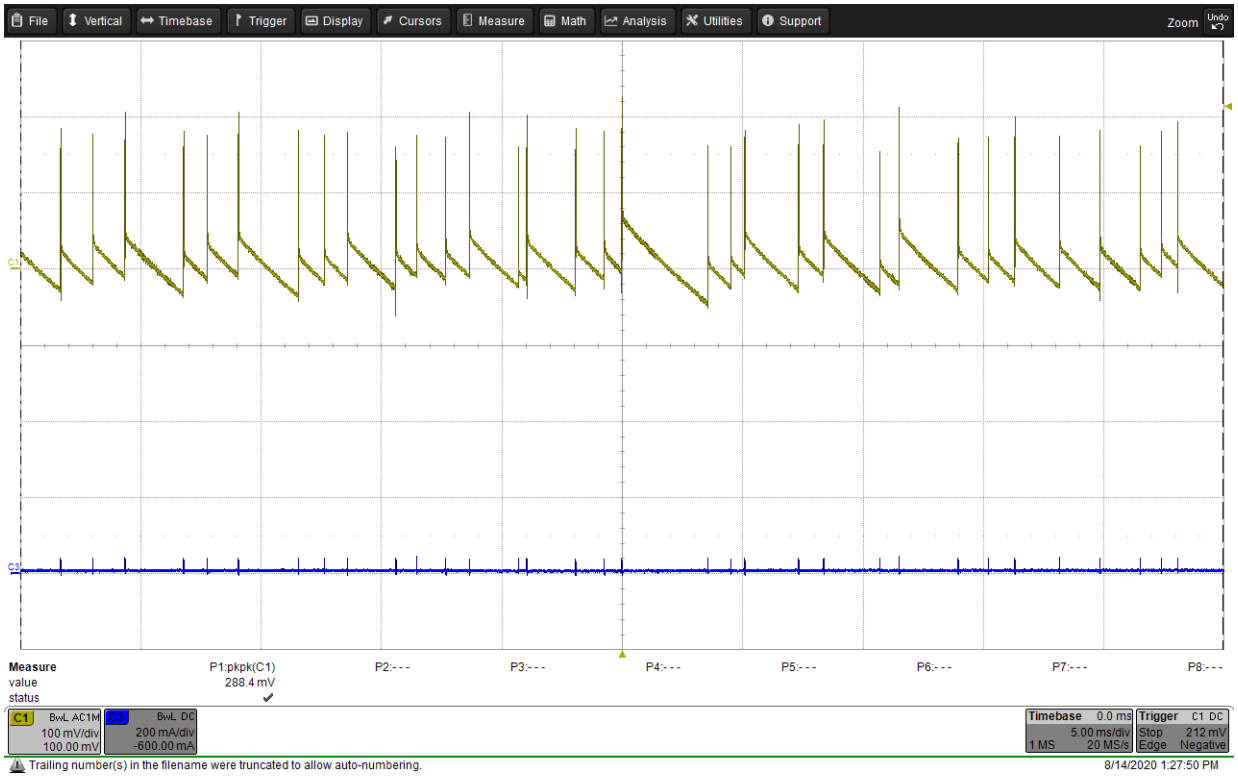


Figure 3-15. 275 VACin; 24 V_{OUT} at 0 mA

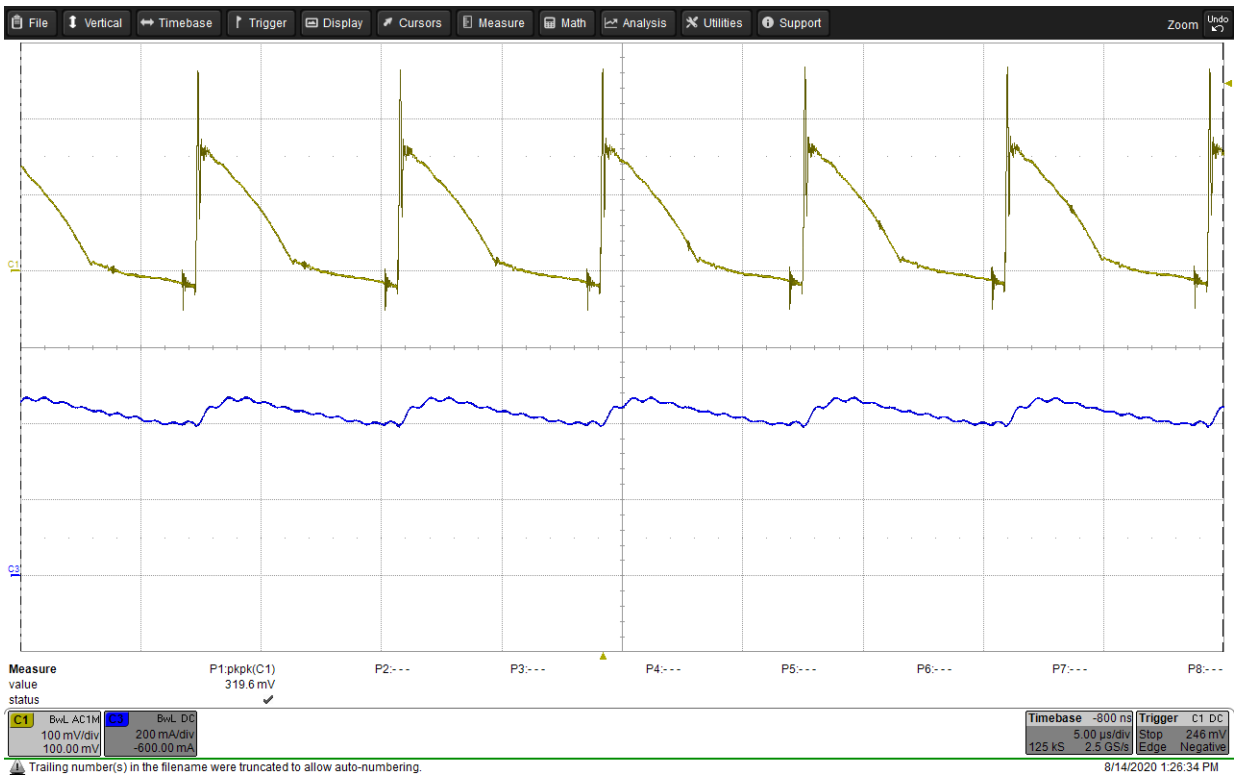
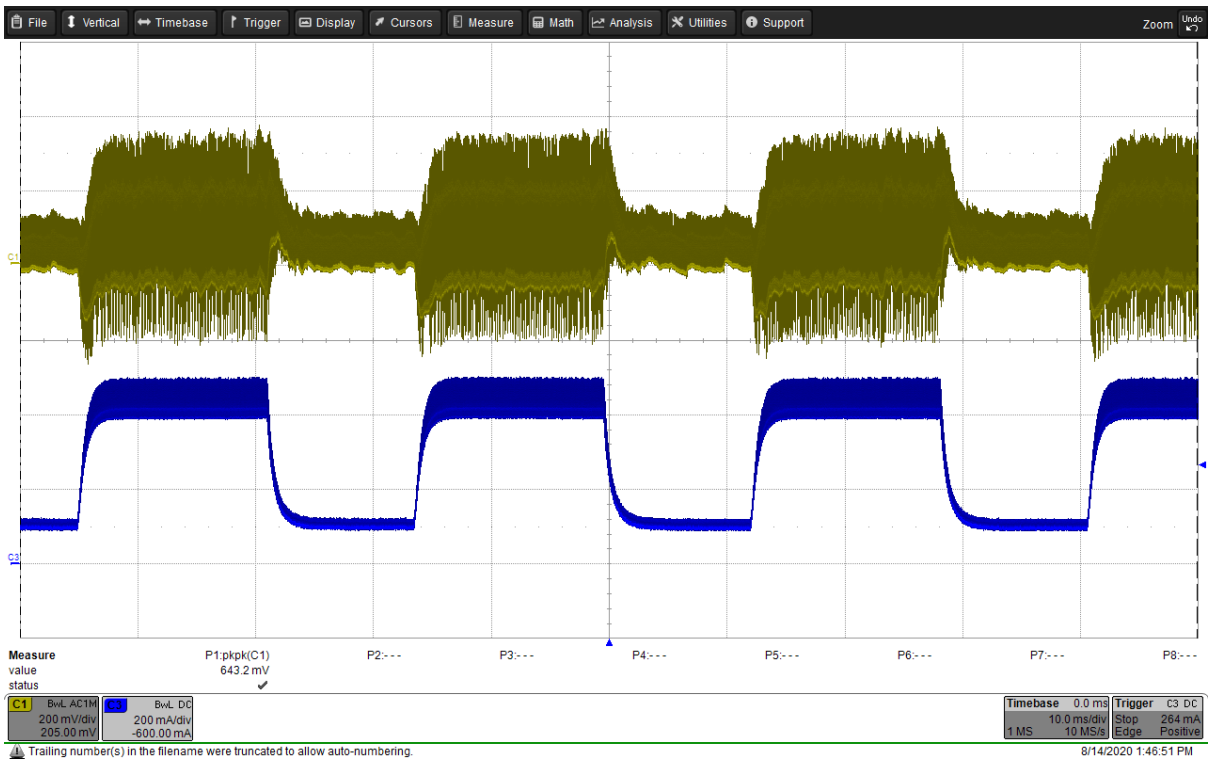


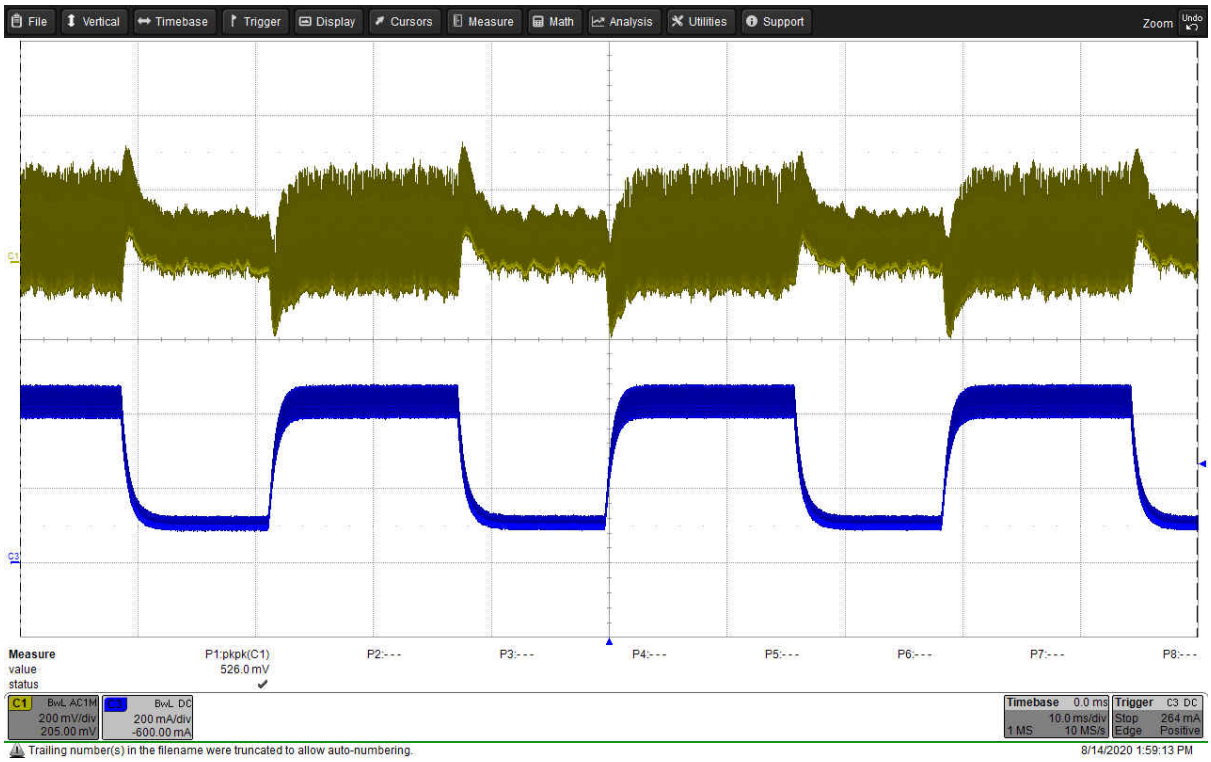
Figure 3-16. 275 VACin; 24 V_{OUT} at 420 mA

3.3 Transient Response



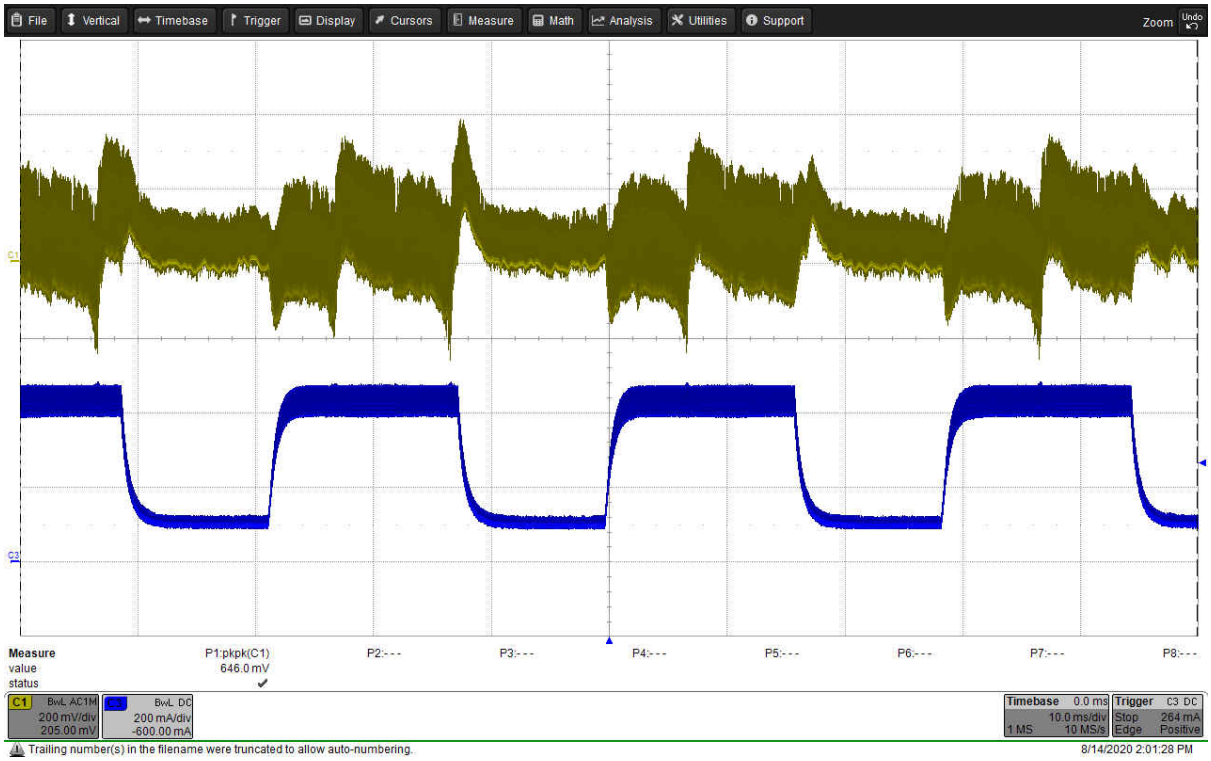
Load is stepping from 100 mA to 420 mA using an E-load. Vout is AC coupled showing a pk-to-pk deviation of 643.2 mV.

Figure 3-17. 19 VDCin



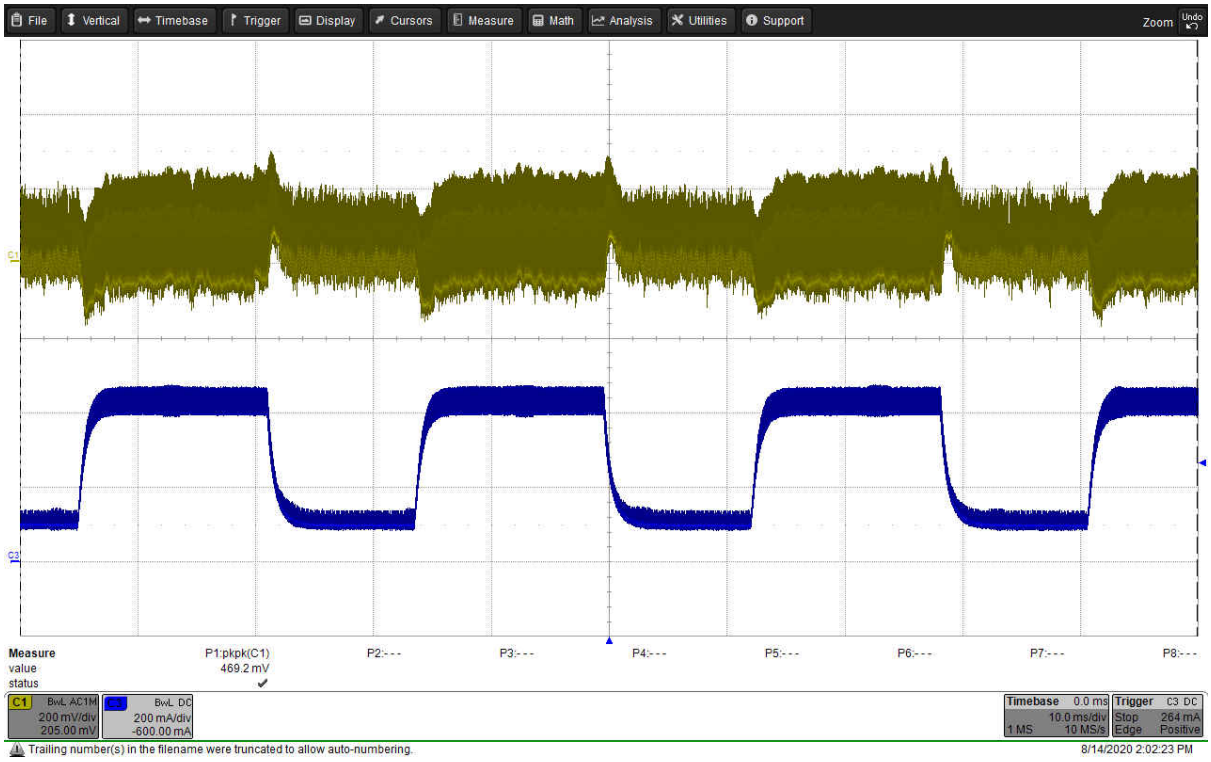
Load is stepping from 100 mA to 420 mA using an E-load. Vout is AC coupled showing a pk-to-pk deviation of 526 mV.

Figure 3-18. 60 VDCin



Load is stepping from 100 mA to 420 mA using an E-load. Vout is AC coupled showing a pk-to-pk deviation of 646 mV.

Figure 3-19. 85 VACin



Load is stepping from 100 mA to 420 mA using an E-load. Vout is AC coupled showing a pk-to-pk deviation of 469.2 mV.

Figure 3-20. 265 VACin

3.4 Start-up

The following waveforms were created with 19 VDC in start-up

Figure 3-21. No Load

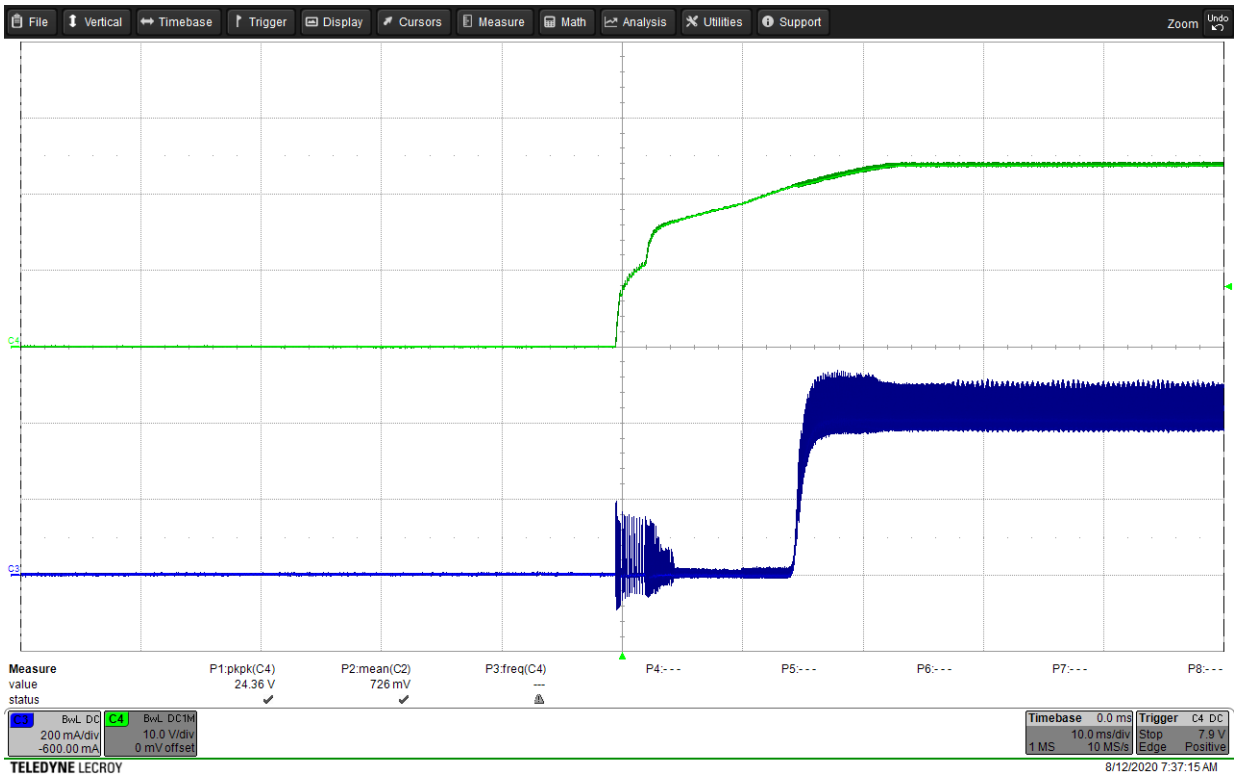


Figure 3-22. 420-mA Load

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