Test Report: PMP23069

3-kW, 180-W/in³ Single-Phase Totem-Pole Bridgeless PFC Reference Design With 16-A Maximum Input

Description

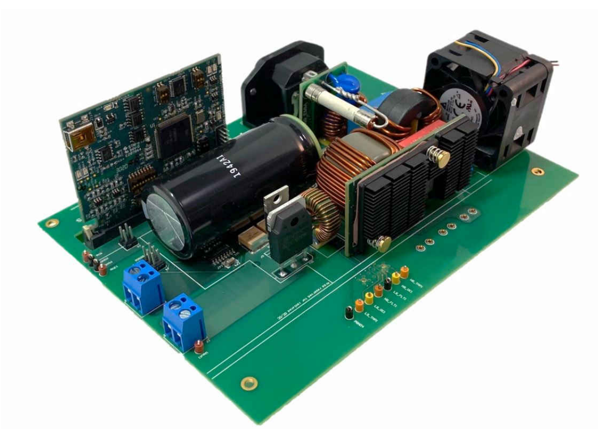
This reference design is a GaN based 3-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The supply is designed to support a maximum input current of 16-A_{RMS} and peak power of 3.6 kW. The power stage is followed by a baby boost converter, which helps to greatly reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN device with integrated driver and protection, enables higher efficiency and reduces power supply size and complexity. The F28004x or F28002x C2000 controller is used for all the advanced controls including fast relay control, baby boost operation during AC drop out event, reverse current flow protection, and communication between the PFC and house-keeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

Features

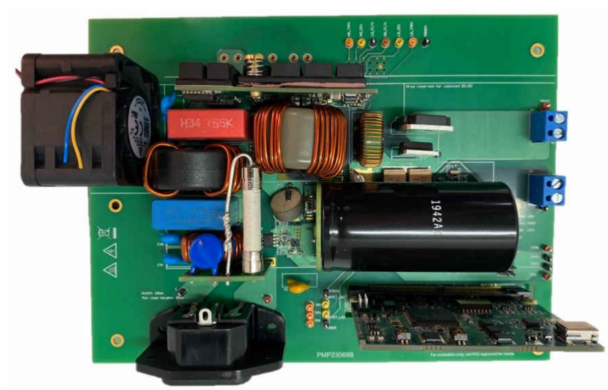
- > 180 W/in³ power density in an x-y dimension of less than 68-mm × 121-mm space and maximum height of 32 mm
- Peak efficiency of 98.7%
- Semiconductor relay increases power density and reliability
- GaN optimized with driver integration

Application

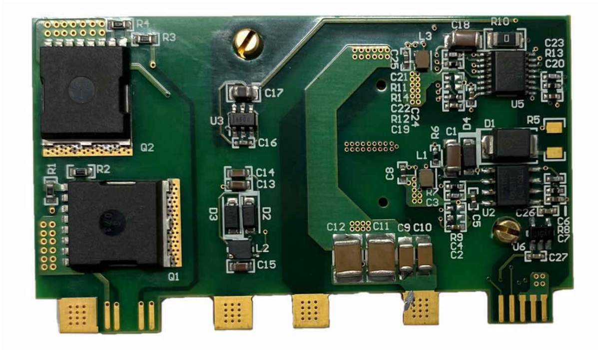
- Merchant network and server PSU
- Merchant telecom rectifiers



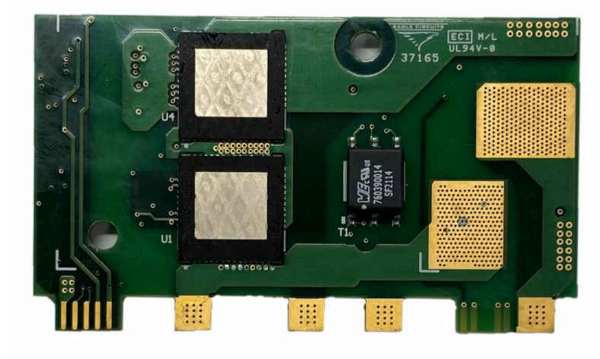
Board Side View



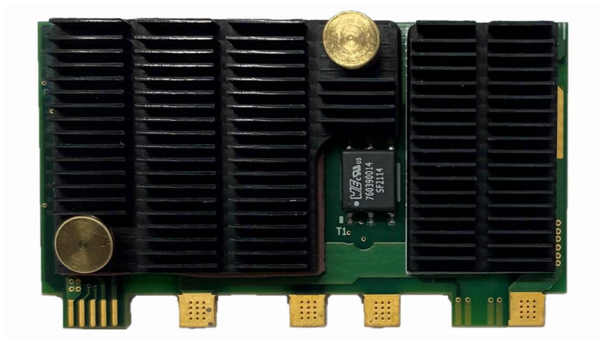
Board Top View



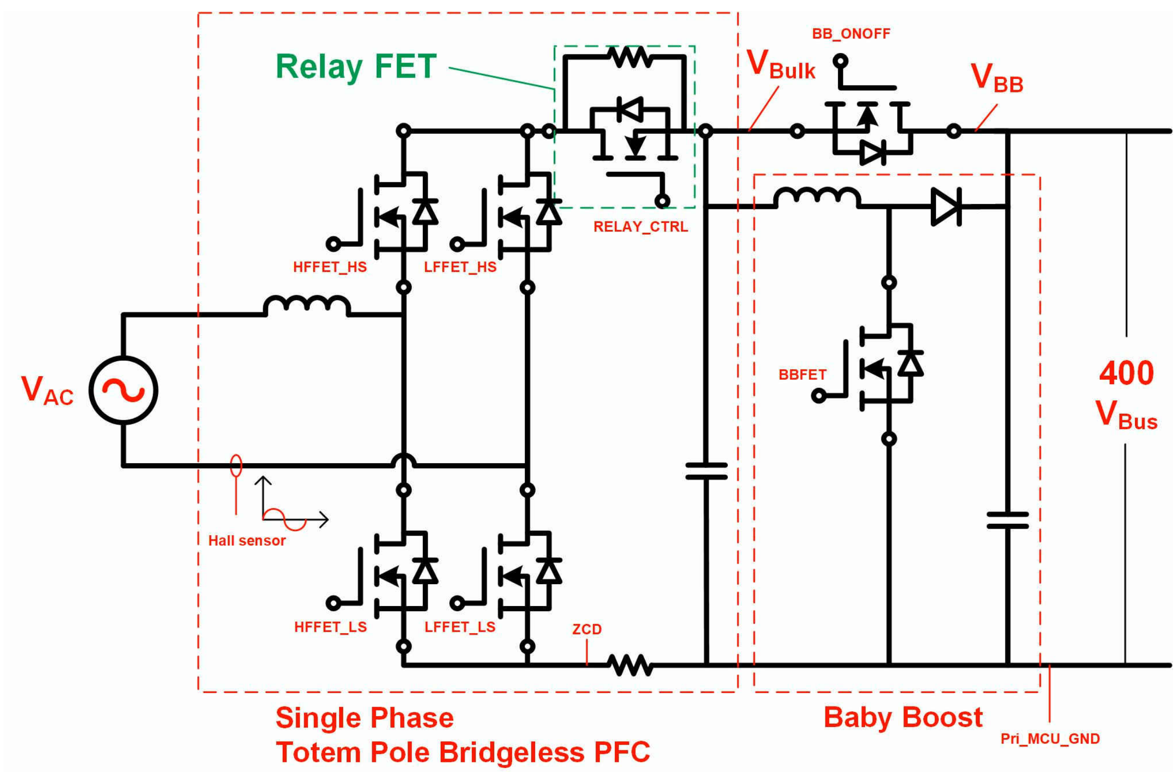
FET Daughter Card Top View



FET Daughter Card Bottom View



FET Daughter Card Bottom View With Heat Sinks



Totem Pole PFC Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications	Units
Input Voltage	85–265	VAC
Line Frequency	47–63	Hz
Input Current (Max)	16	A_{RMS}
Output Voltage	380	VDC
High Line Output Power	3	kW
Low Line Output Power	1.5	kW

1.2 Considerations

Due to the totem-pole topology, the PFC ground (PGND) is floating. This can lead to common-mode current issues with improper test equipment setups. Use differential voltage probes when using an oscilloscope. Use isolated sources for the 12Vp and 12V1 auxiliary supplies. TI recommends using the PMP20306 isolated bias supply reference design.

1.3 Dimensions

Figure 1-1 illustrates the power supply with a maximum component height of 32 mm (image shown is not to scale).

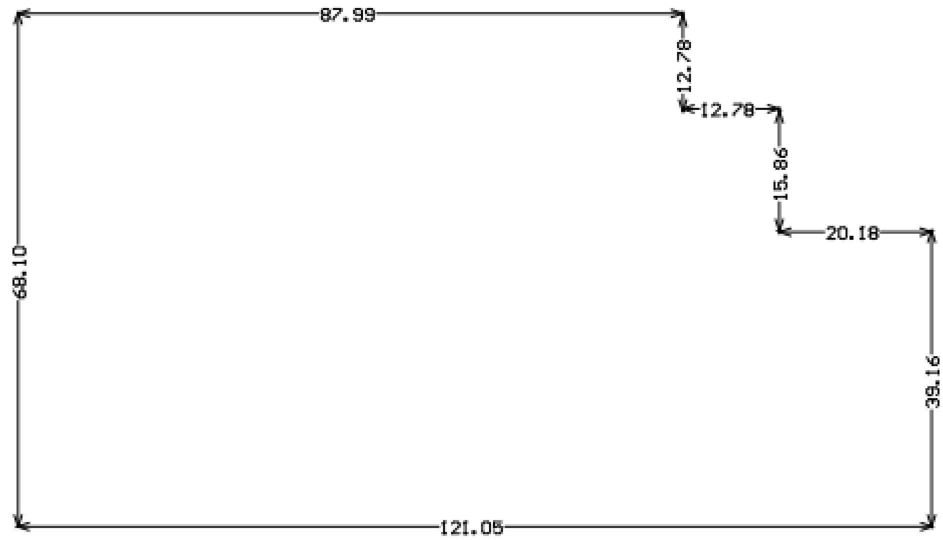


Figure 1-1. Power-Supply Dimensions

Figure 1-2 shows the FET daughter card dimensions (image shown is not to scale).

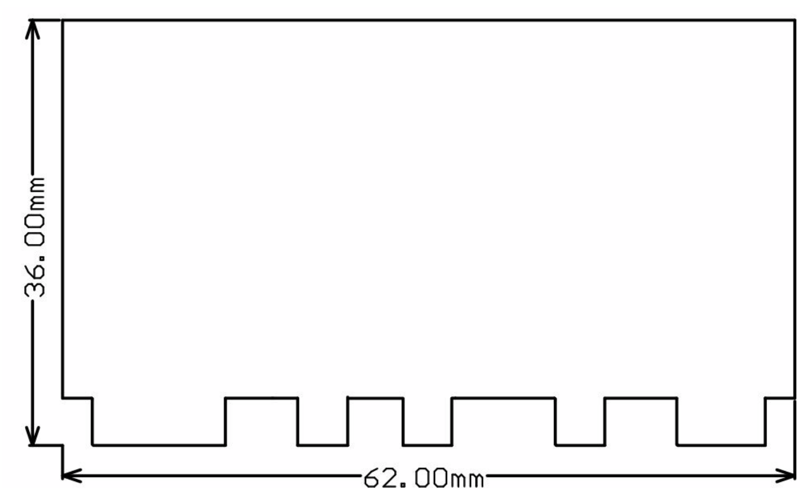


Figure 1-2. FET Daughter Card Dimensions

2 Testing and Results

2.1 Efficiency Graphs

Conditions

- Frequency: 65 kHz
- GaN Slew Rate: 100 V/ns
- Output: 380 V
- PFC Inductor: PAL6585.254NL
- Power analyzer: WT3000E
- Relay and BB bypass FETs shorted
- Auxiliary supply not included

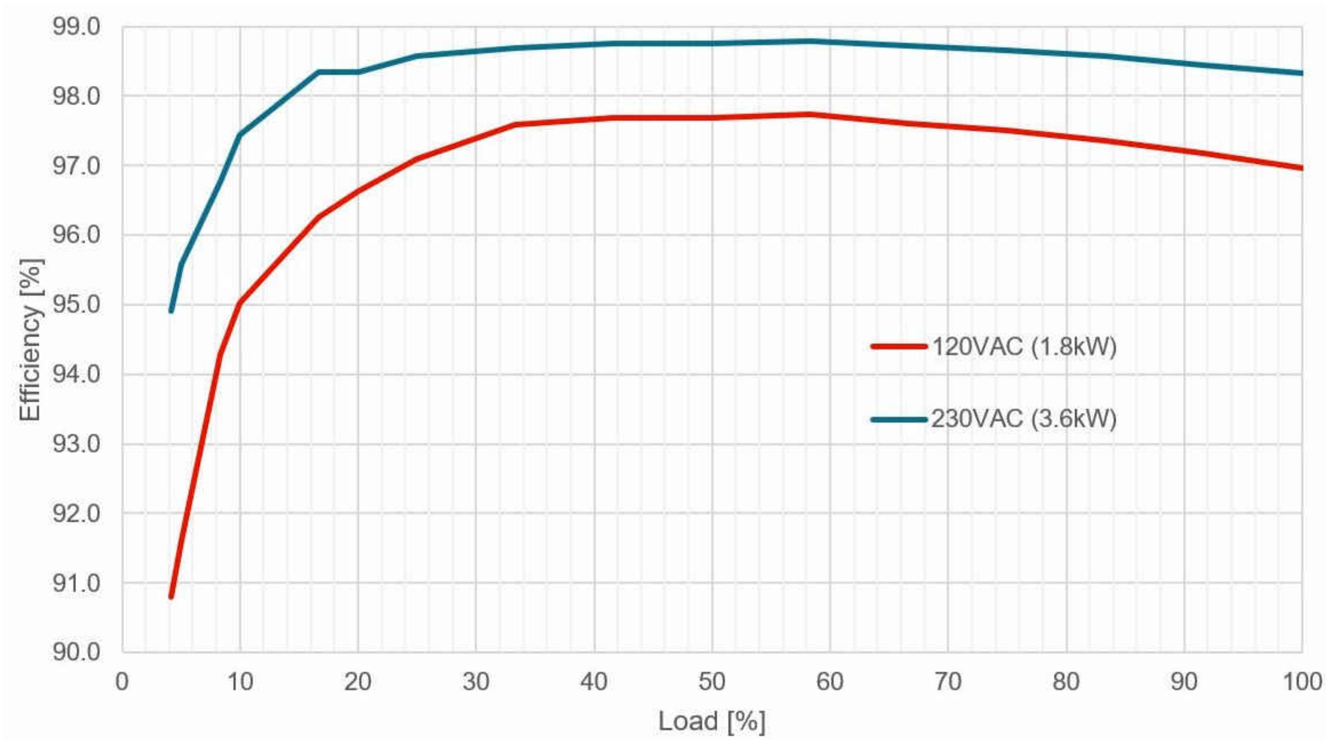


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

Table 2-1 and Table 2-2 display the 120 VAC and 230 VAC efficiency data.

Table 2-1. 120 VAC Efficiency

% Load	Input Voltage (V_{RMS})	Input Current (A_{RMS})	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)
4%	120.05	0.77	88.13	382.28	0.21	80.02	90.80
5%	120.04	0.85	98.32	282.81	0.24	90.16	91.61
8%	119.97	1.30	145.08	382.43	0.38	145.08	94.29
10%	119.93	21.58	186.84	382.75	0.46	177.51	95.02
17%	119.77	2.59	308.30	382.32	0.78	296.78	96.26
20%	119.68	3.14	375.26	382.84	0.95	362.49	96.64
25%	119.66	3.87	462.25	382.37	1.17	448.82	97.09
33%	119.46	5.16	615.39	382.42	1.57	600.56	97.59
42%	119.36	6.47	770.37	382.33	1.97	752.50	97.68
50%	119.15	7.79	925.95	382.54	2.36	904.51	97.69
58%	119.04	9.09	1080.44	382.21	2.76	1055.87	97.73
67%	118.87	10.43	1237.97	382.51	3.16	1208.33	97.61
75%	118.75	11.57	1371.55	382.34	3.50	1337.42	97.51
83%	118.60	13.12	1552.80	382.57	3.95	1511.82	97.36
92%	118.37	14.49	1713.16	382.87	4.35	1664.92	97.18
100%	118.23	15.88	1874.88	383.03	4.75	1818.05	96.97

Table 2-2. 230 VAC Efficiency

% Load	Input Voltage (V_{RMS})	Input Current (A_{RMS})	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)
4%	230.21	0.72	153.16	382.23	0.38	145.37	94.91
5%	230.19	0.85	185.33	382.79	0.46	177.21	95.58
8%	230.10	1.36	307.08	382.33	0.77	297.13	96.76
10%	230.06	1.64	371.96	382.78	0.95	362.51	97.44
17%	229.90	2.67	610.42	382.19	1.57	600.31	98.34
20%	229.88	3.2	732.46	382.68	1.88	720.73	98.35
25%	229.79	4.00	917.31	382.41	2.36	904.25	98.58
33%	229.58	5.34	1223.96	382.38	3.16	1207.92	98.69
41%	229.47	6.68	1530.36	382.43	3.95	1511.31	98.76
50%	230.05	7.99	1837.48	382.32	4.75	1814.72	98.76
58%	229.94	9.32	2142.20	382.00	5.54	2116.28	98.79
67%	229.82	10.68	2454.77	382.57	6.33	2423.00	98.72
75%	229.59	12.04	2763.84	382.63	7.13	2726.59	98.66
83%	229.46	13.41	3074.80	382.56	7.92	3030.79	98.57
92%	228.55	14.80	3379.92	382.95	8.69	3327.10	98.44
100%	228.31	16.18	3692.35	382.88	9.48	3630.65	98.33

2.2.1 THD Optimization

Conditions

- Frequency: 100 kHz
- Maximum load: 3 kW
- GaN Slew Rate: 100 V/ns
- Output: 385 V
- Power analyzer: WT3000E

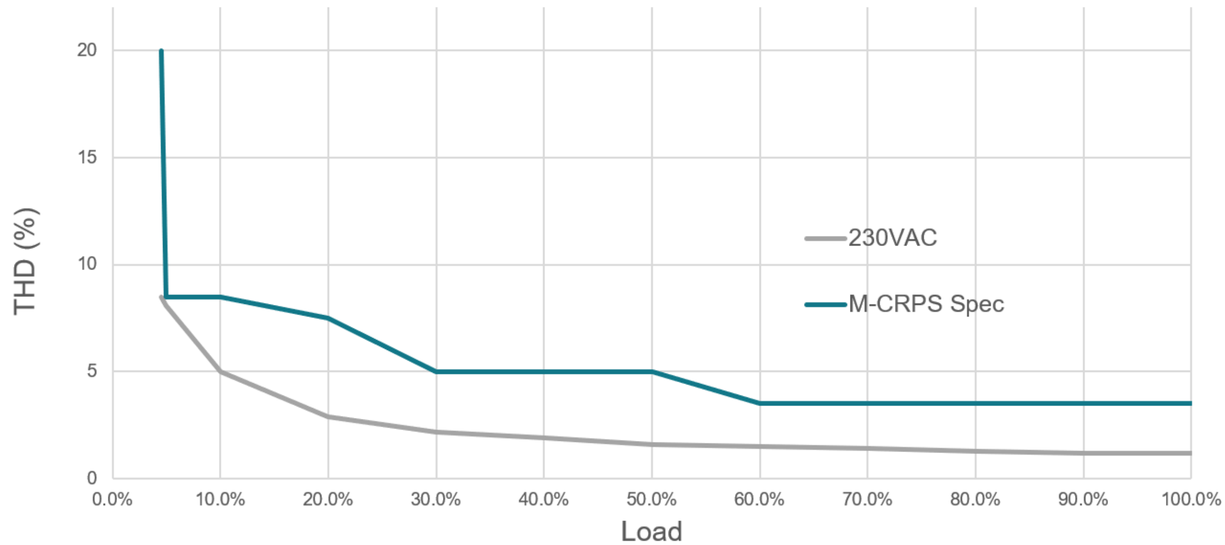


Figure 2-2. THD

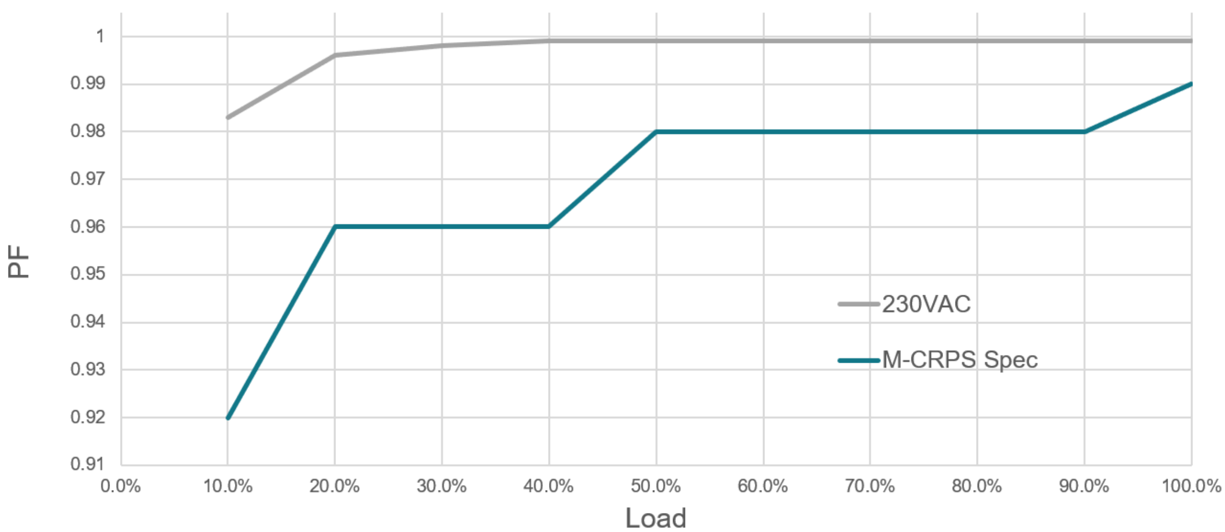


Figure 2-3. Power Factor

2.3 Thermal Images

Conditions

- Same as efficiency test
- Input: 230 VAC
- Output: 380 V, 3.6 kW
- Frequency: 65 kHz
- Slew rate: 100 V/ns
- Dead-time: 100 ns
- Fan: FFB0412EN-00
  - Air-speed: 33 LFM, 6 m/s
- Time: 30 minutes

Table 2-3. Heat Sink and Thermal Interface

GaN Heat Sink	GaN TIM	Silicon Heat Sink	Silicon TIM
S08EDR03-A	T-Work9000	S08EDR08	Tgard TNC-4(1)

(1) Silicon TIM used in room temperature test is LI2000A-150-150-0.2. Not recommended for worst case conditions. Contact TI for heat-sink drawings.

Note

The thermal design is based on 16-A_{RMS} input current.

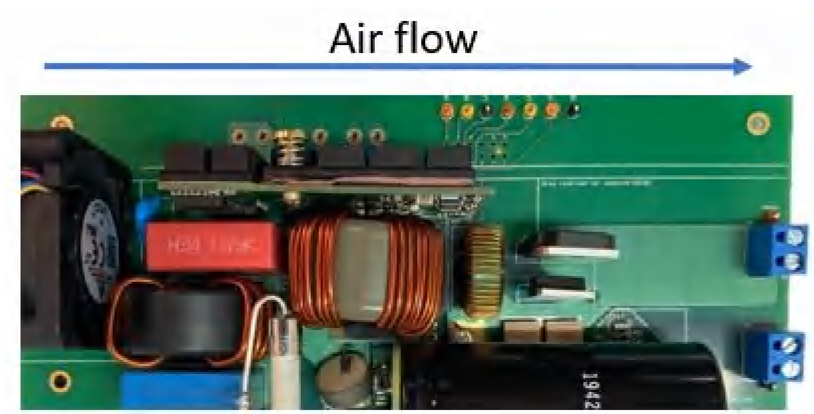


Figure 2-4. Test Setup

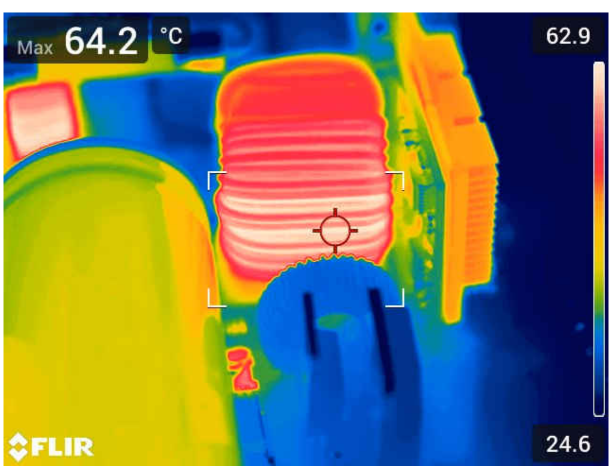


Figure 2-5. PFC Inductor

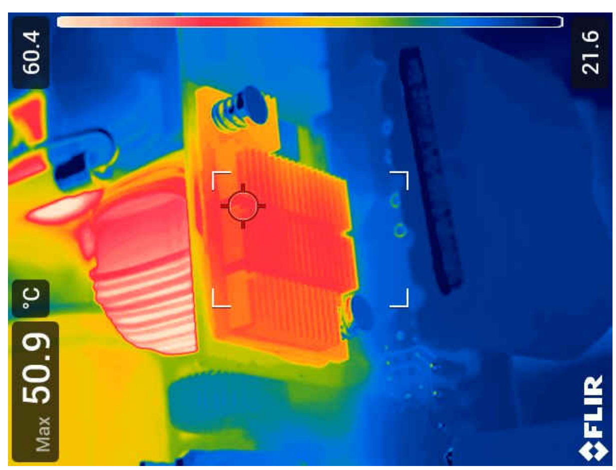


Figure 2-6. Backside of FET Card

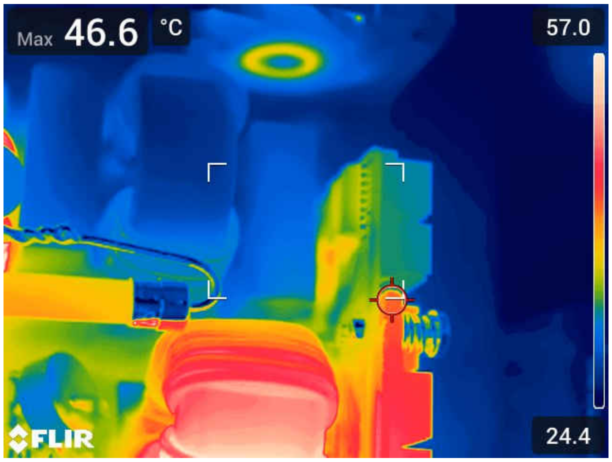


Figure 2-7. LF Silicon FETs

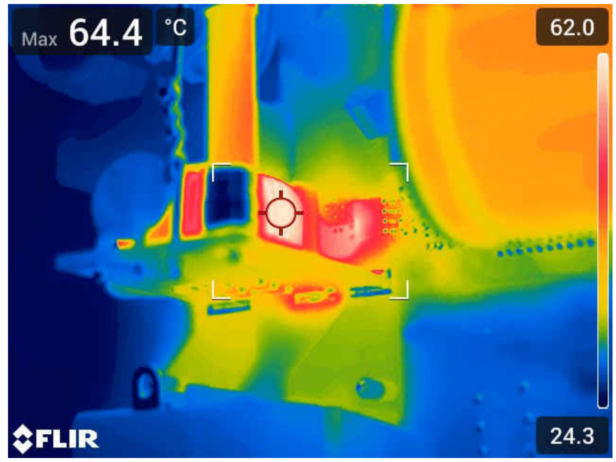


Figure 2-8. Common-Mode Choke and Hall Sensor

2.3.1 Low-Side GaN Junction Temperature

Using the LMG3522 internal temperature reporting, the PWM signal from the TEMP pin is measured to calculate the die temperature. Measurements are taken under the same conditions as the thermal images, see the following tables.

Table 2-4. LS PWM Temperature Reading (65 kHz)

Condition	Temperature (°C)
Minimum	63.91
Average	66.57
Maximum	68.95

Table 2-5. LS PWM Temperature Reading (100 kHz)

Condition	Temperature (°C)
Minimum	77.66
Average	78.70
Maximum	80.16

2.4 Thermal Mechanical Design

2.4.1 Design Parameters

- Power Device: LMG3522R030 GaN top cooled | IPT60R022S7 Infineon bottom cooled
- Ambient temperature: 55°C
- Airflow: 12 m/s
- Daughter card PCB: 62 mm × 36 mm, 69 mil, 6 layer, 1-oz copper, FR4 High tg
- GaN Cooling: Top side Heat sink 40 mm × 29 mm × 6 mm, Aluminum, Z40-6.3B
- GaN Thermal Interface Material (TIM1): T-work9000 at 50 psi (R = 0.031(°C in^2) / W) 1 mm
- Low frequency FETs Cooling: Bottom side Heat sink 17.5 mm × 29 mm × 7 mm, Aluminum, Z35-6.3B
- Low frequency FETs Adhesive Type (TIM2): Tgard TNC-4 at 25–35 psi (R = 0.3(°C in^2) / W) 0.127 mm

2.4.2 Thermal Resistance Calculation

- T_A = 25°C (measured from GaN TEMP_PWM)
- T_J = 67°C (measured from GaN TEMP_PWM)
- Power loss = 7.5 W (at below operating condition and Tj = 67°C)
- $R_{\theta JA}$ = (67°C – 25°C) / 7.5 W = 5.6°C/W

2.4.3 Heat-Sink Diagrams

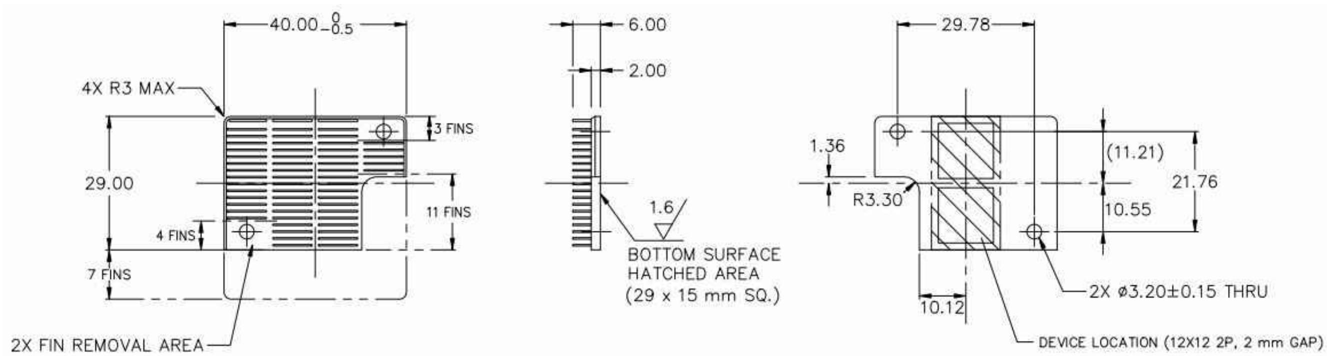


Figure 2-9. S08EDR03-A (Alpha Novatech)

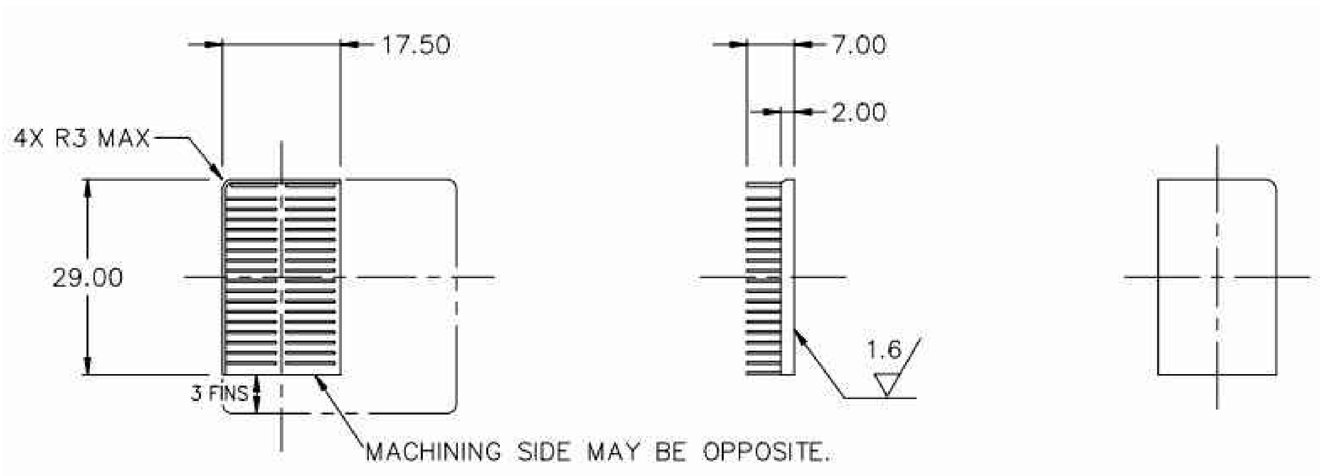


Figure 2-10. S08EDR08 (Alpha Novatech)

2.5 EMI

EMI is represented in the following image.

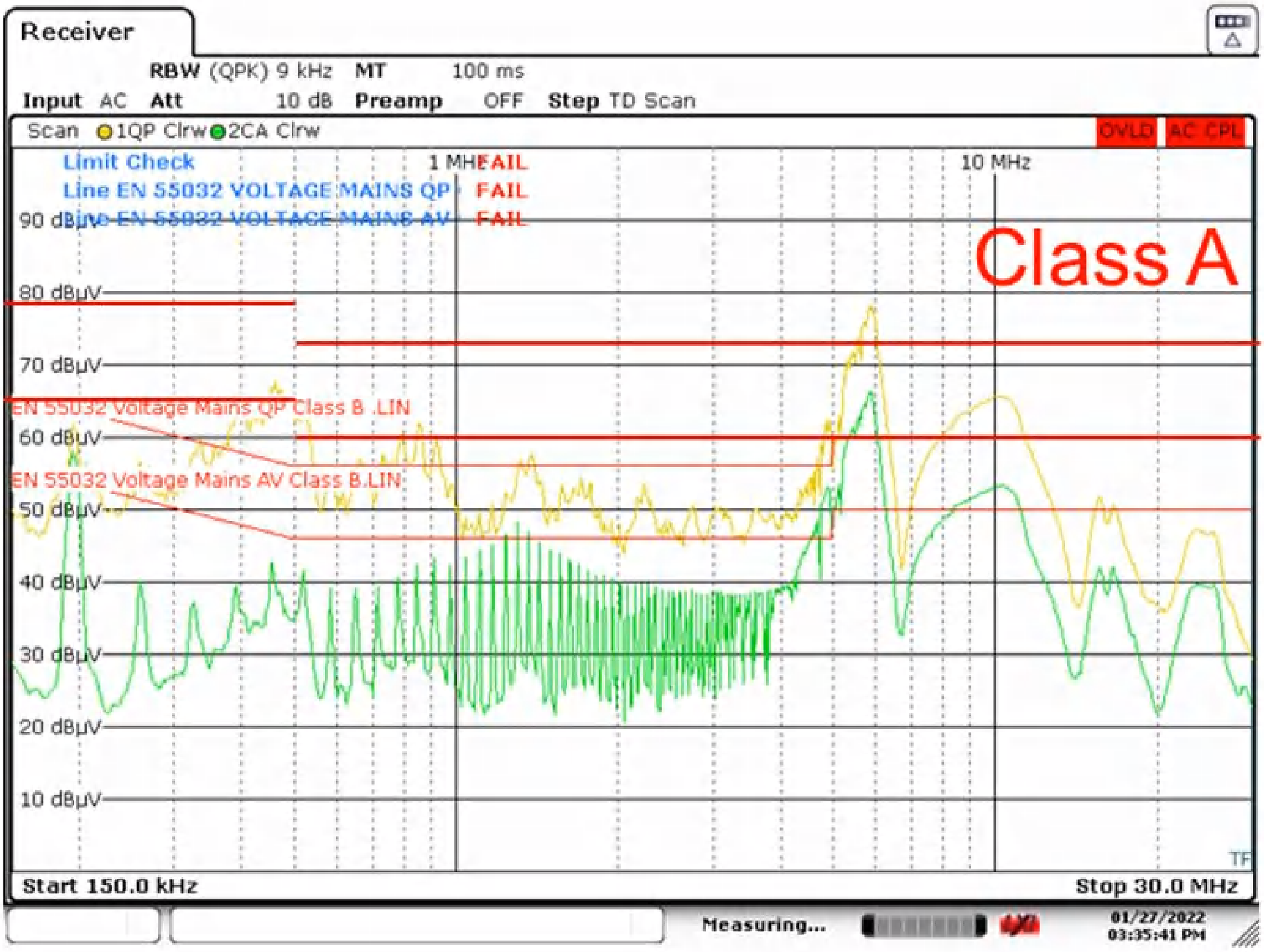


Figure 2-11. 230 VAC, Line, 400 W, X-cap: C44 = 1.97 µF, C45 = 3 µF

3 Waveforms

3.1 AC Drop

Test data in the following images are taken from PMP23031 single-phase CCM TTPL PFC.

C1 = IAC, C2 = BB Bypass, C3 = VBB

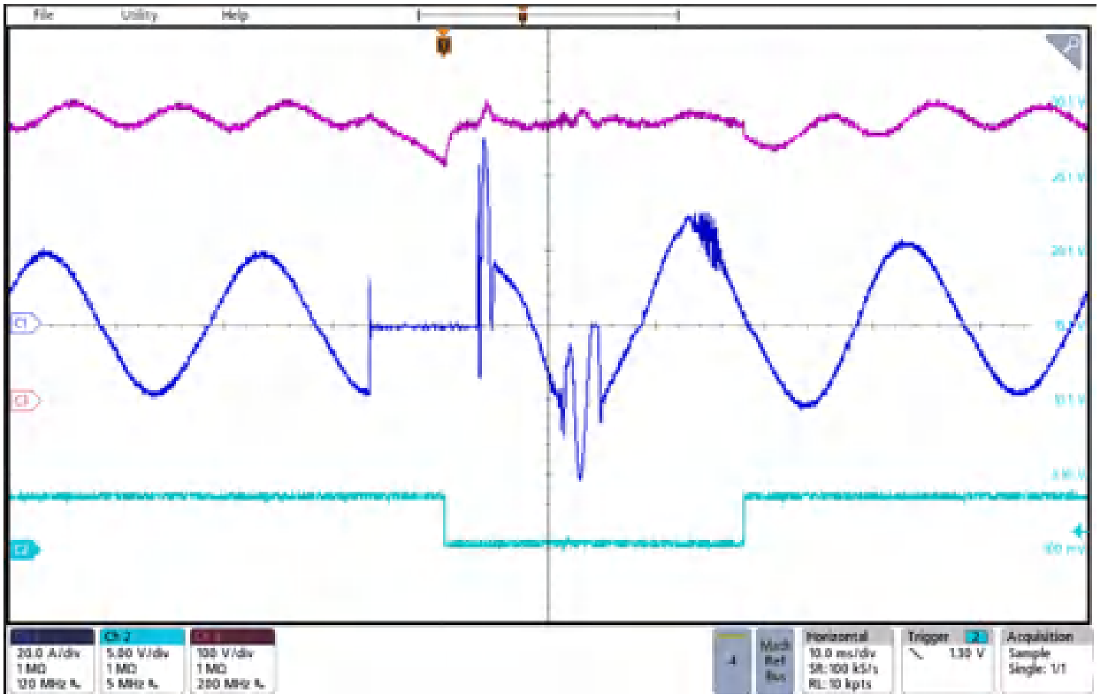


Figure 3-1. 230 VAC, 3 kW, 10-ms Drop, Return at 90 Degrees

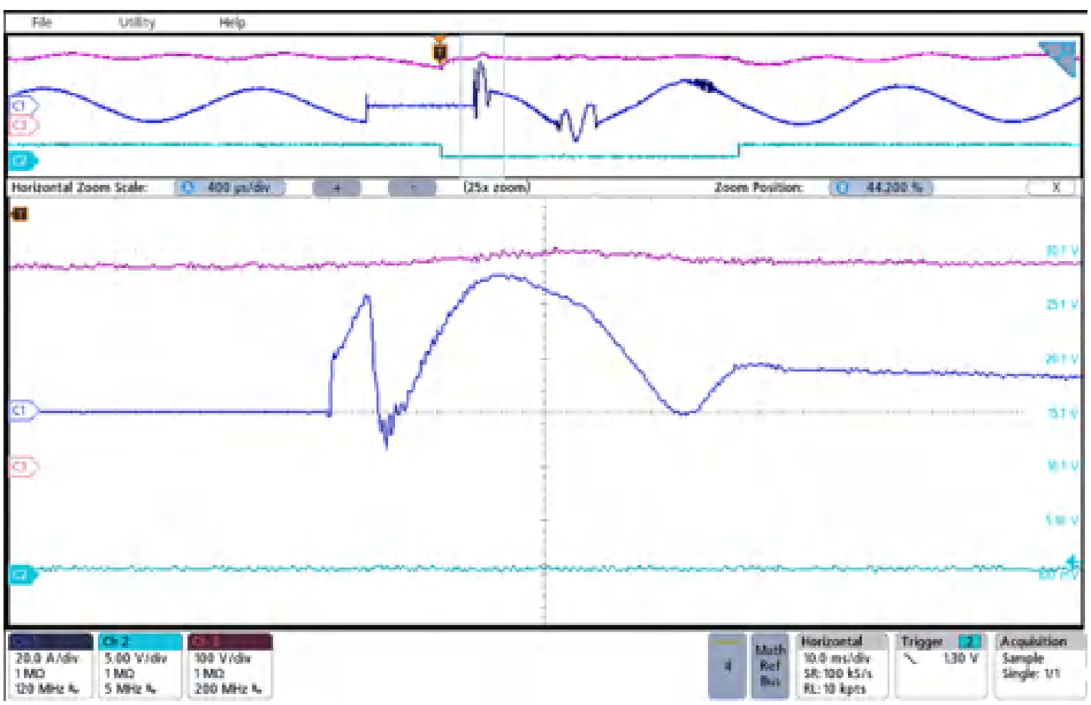


Figure 3-2. 230 VAC, 3 kW, 10-ms Drop, Return at 90 Degrees (Zoom)

3.2 Load Transients

The waveforms in Figure 3-3 through Figure 3-8 were captured at 120 VAC with slew rate = 1 A/µs.

C2 = VAC, C3 = V_{OUT}, C4 = IAC

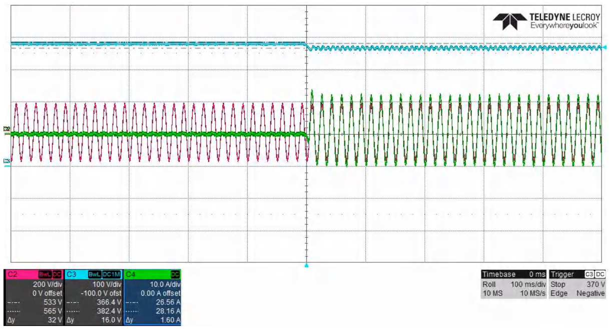


Figure 3-3. 120 VAC, 0% to 50% Load

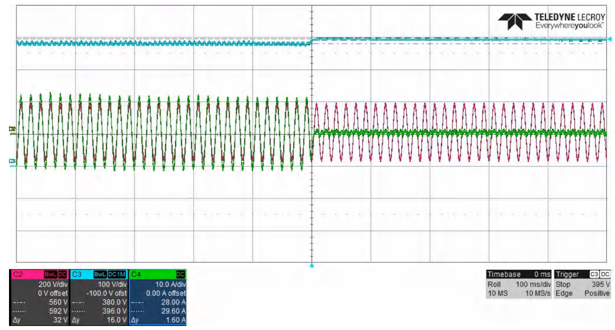


Figure 3-4. 120 VAC, 50% to 0% Load

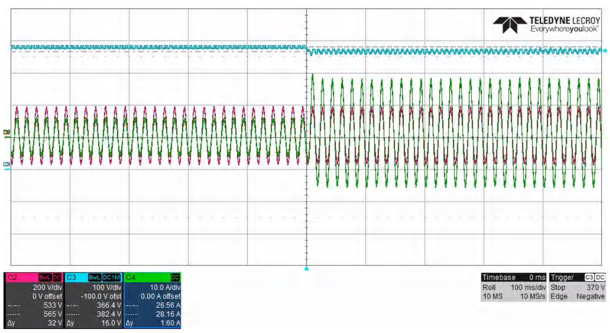


Figure 3-5. 120 VAC, 25% to 75% Load

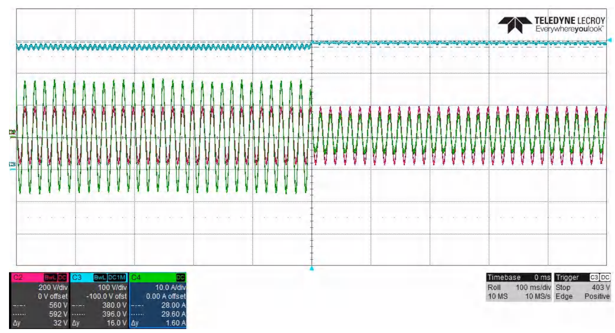


Figure 3-6. 120 VAC, 75% to 25% Load

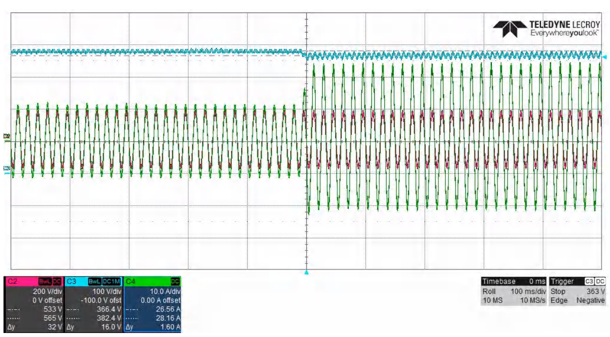


Figure 3-7. 120 VAC, 50% to 100% Load

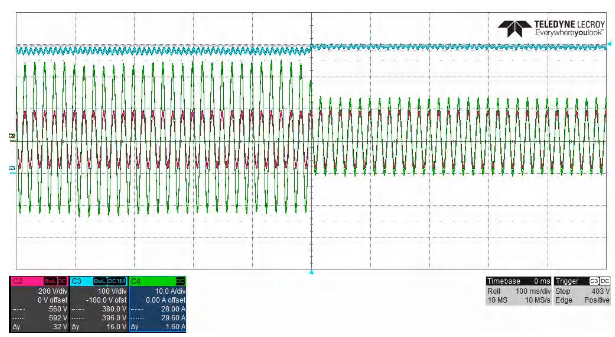


Figure 3-8. 120 VAC, 100% to 50% Load

The waveforms in Figure 3-9 through Figure 3-14 were captured at 230 VAC with slew rate = 1 A/µs.

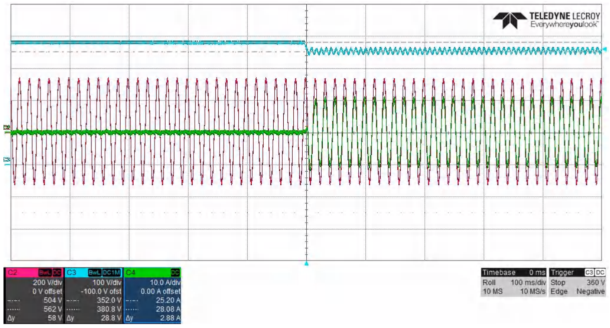


Figure 3-9. 230 VAC, 0% to 50% Load

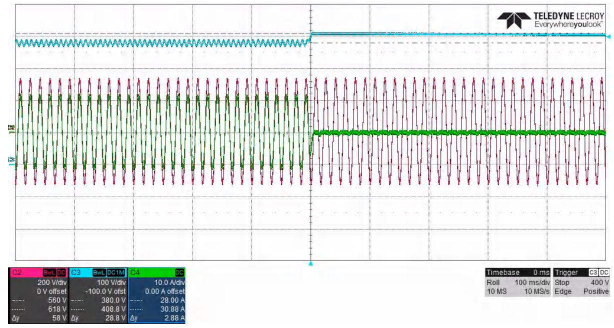


Figure 3-10. 230 VAC, 50% to 0% Load

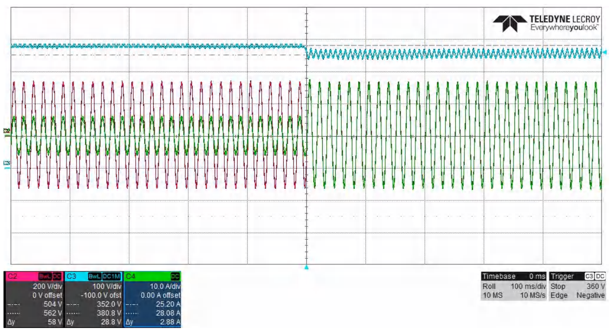


Figure 3-11. 230 VAC, 25% to 75% Load

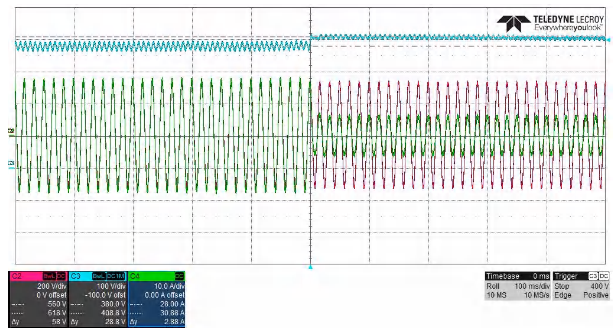


Figure 3-12. 230 VAC, 75% to 25% Load

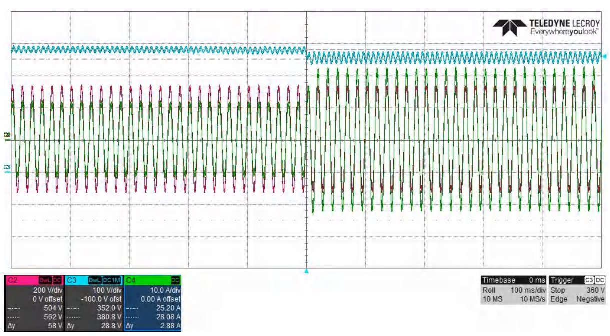


Figure 3-13. 230 VAC, 50% to 100% Load

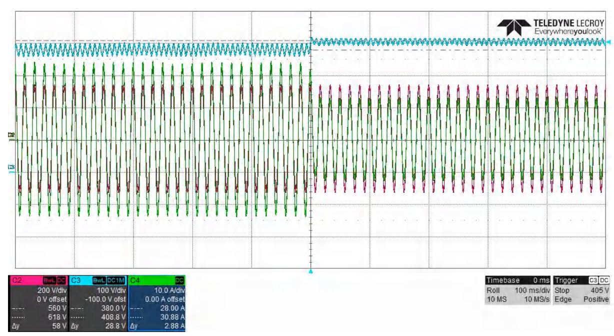


Figure 3-14. 230 VAC, 100% to 50% Load

3.3 Start-Up Sequence

The waveforms in Figure 3-15 and Figure 3-16 were captured at 120 VAC, no load.

C2 = VAC, C3 = V_{OUT}, C4 = IAC

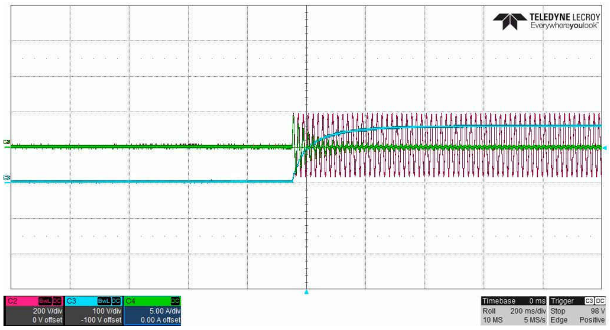


Figure 3-15. AC On

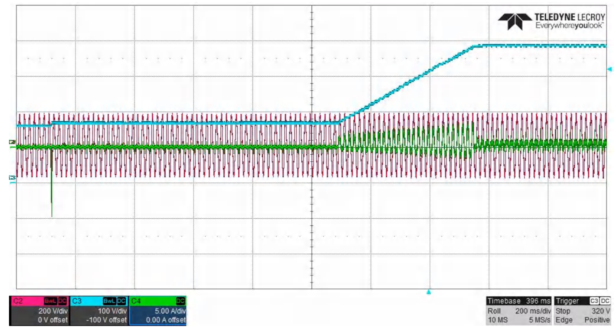


Figure 3-16. Relay On

The waveforms in Figure 3-17 and Figure 3-18 were captured at 230 VAC, no load.

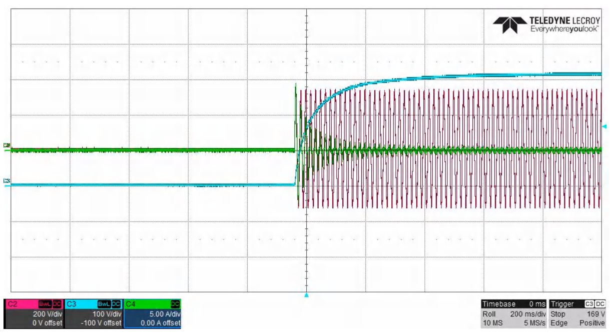


Figure 3-17. AC On

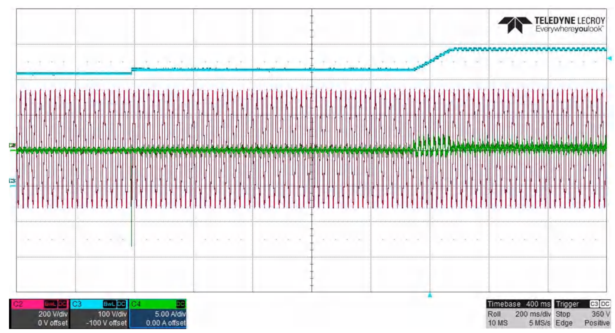


Figure 3-18. Relay On

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