Test Report: PMP22339

High-Voltage, 800-W SEPIC Converter Reference Design for Server Battery Backup Charging

1 Description

This Discontinuous Conduction Mode (DCM), non-isolated, 800-W SEPIC converter battery charger provides an adjustable output voltage and current. The output voltage can be adjusted from 282 V to 400 V by setting an external DC voltage between 0 V to 3 V. The output charging current can be adjusted between 0 A to 2 A by adjusting the duty cycle of a PWM input. It operates over an input voltage range of 340 Vdc–420 Vdc. Independent voltage and current feedback loops are used to maintain regulation.

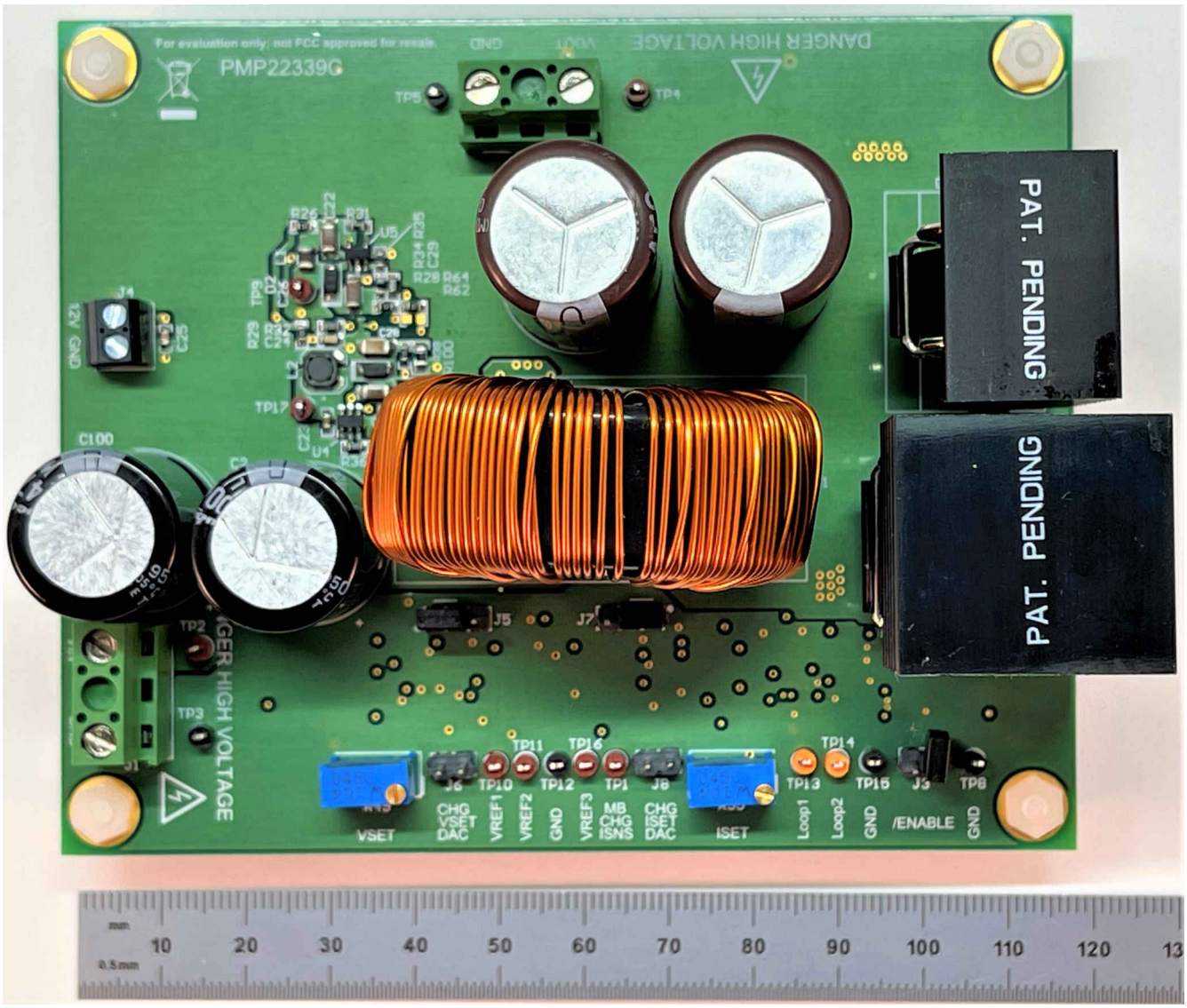

Figure 1-1. Top Photo

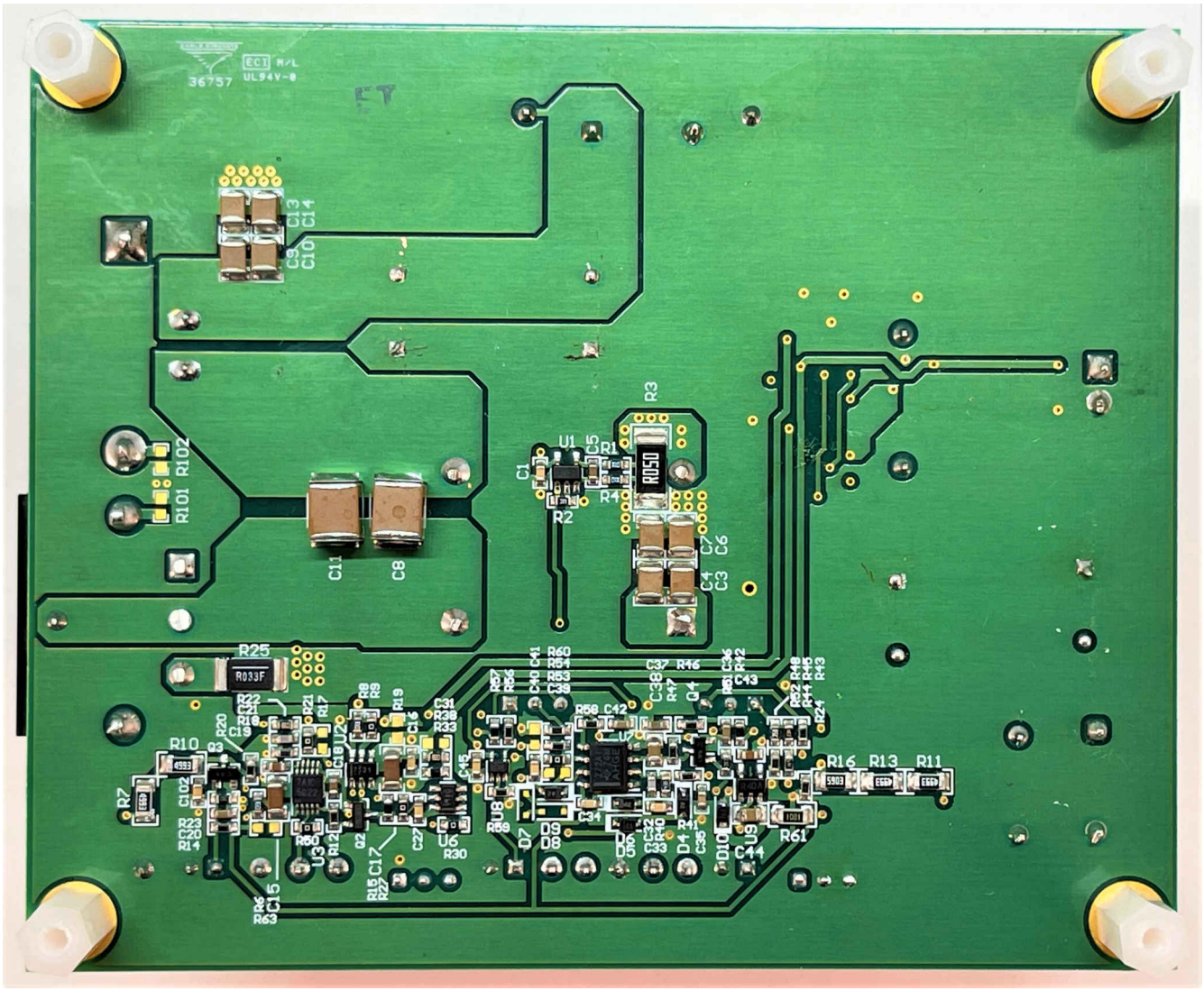

Figure 1-2. Bottom Photo

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	340 V–420 V, after > 335-V startup
Output voltage	282 V–400 V, (CHG VSET DAC = 0 Vdc–3 Vdc)
Output current	0 A–2 A, (CHG ISET DAC = 0% to 100%, 100 kHz, 2.5 V)
Switching frequency	100 kHz
Isolation	No

2.2 Required Equipment

- Li-Ion batteries or load (active or resistive), 400 V, 2 A, 800 W minimum
- Input source power supply, adjustable, 0 V–500 V, 1000 W, 3 A minimum
- Oscilloscope and high-voltage probes
- Digital multimeters
- 12-V bias supplies, 100 mA minimum
- Function generator, adjustable frequency, amplitude and duty cycle

3 Testing and Results

3.1 Thermal Images

The following images show the operating temperature of the board with 400-Vdc input and 400 V at 2-A output at room temperature with approximately 200 LFM to 400 LFM of air flow.

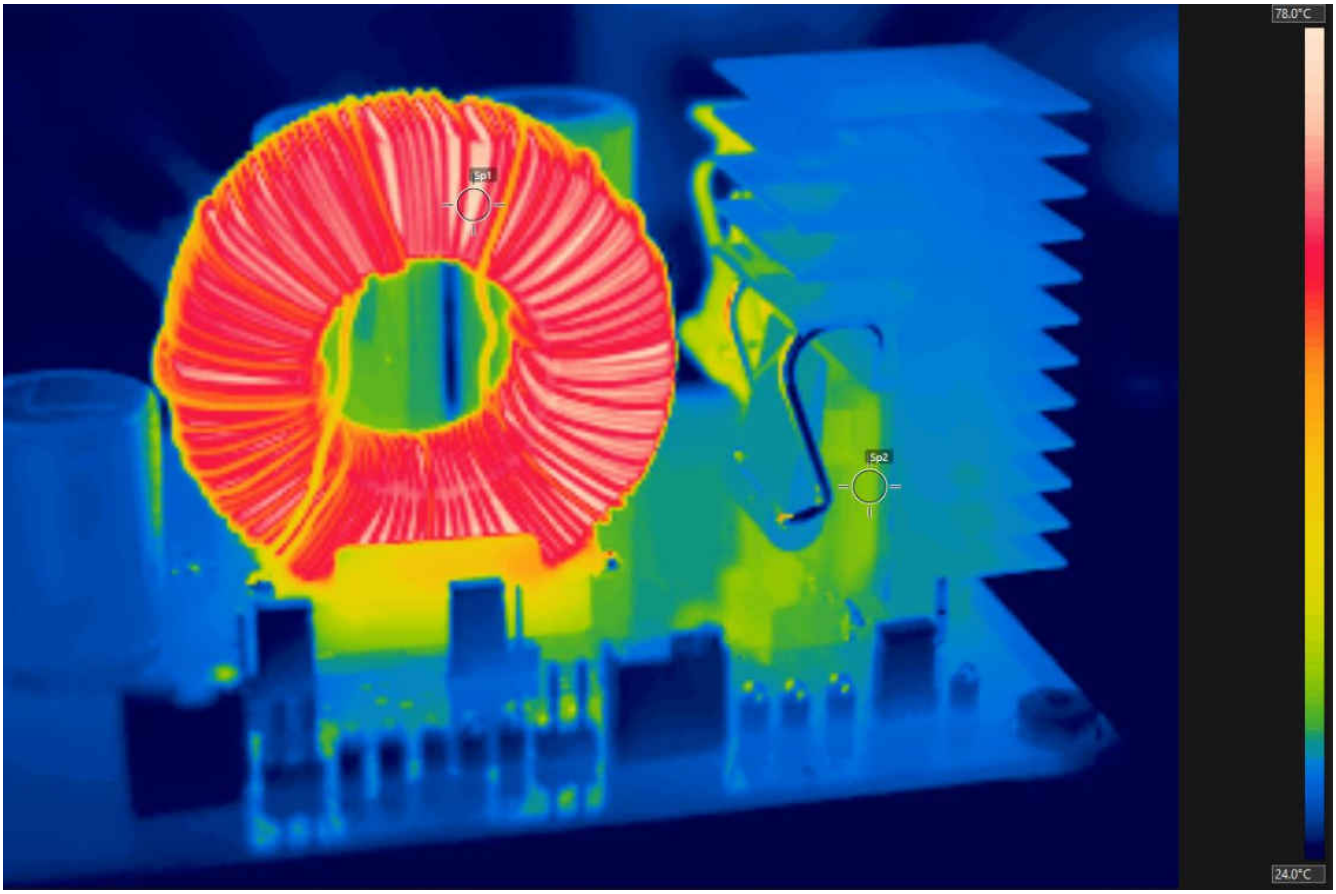

Figure 3-1. Front Thermal Image

Measurement Location	Temperature (°C)
Sp1	75.6
Sp2	37.1

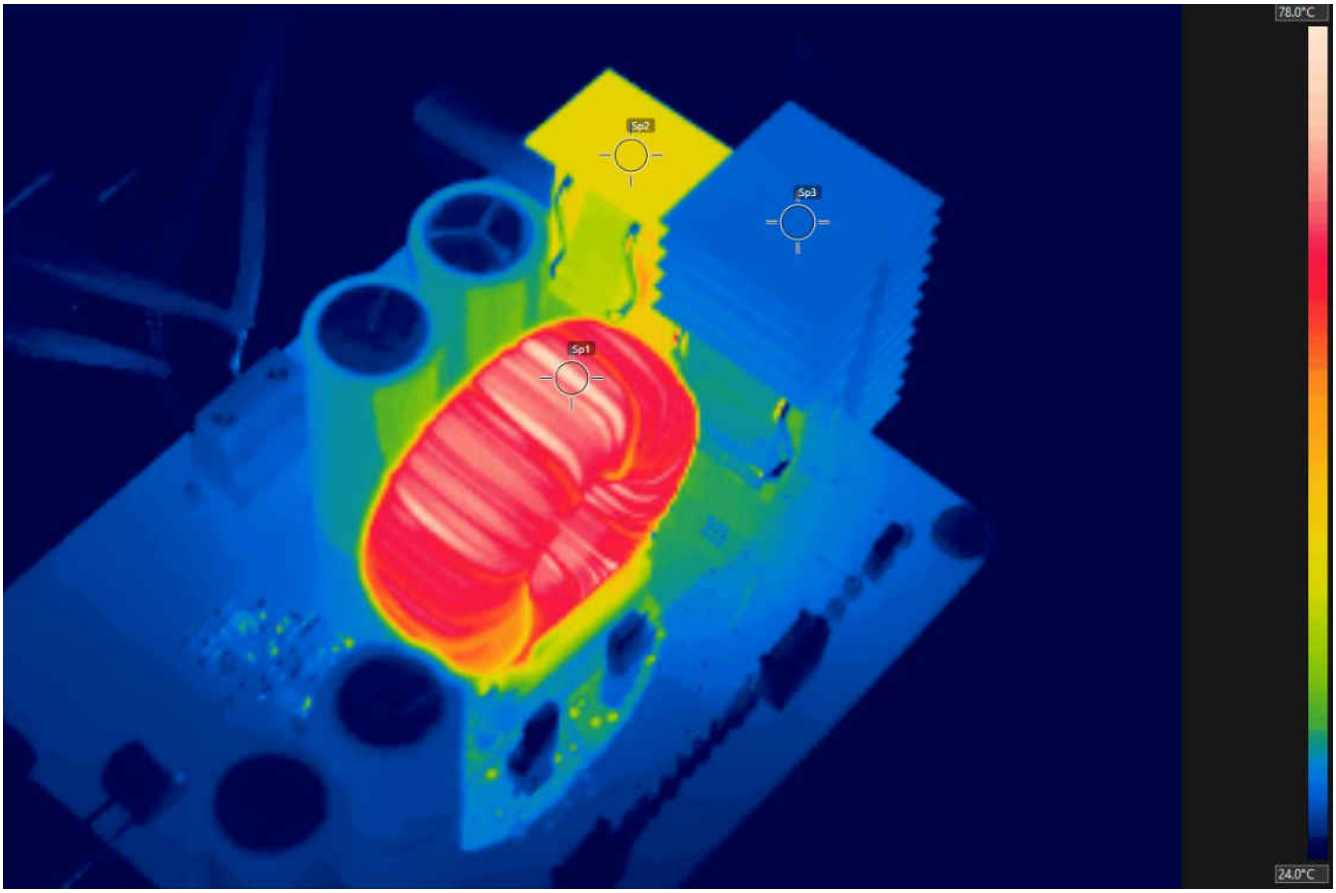

Figure 3-2. Top Thermal Image

Measurement Location	Temperature (°C)
Sp1	75.9
Sp2	47.6
Sp3	29.2

3.2 Efficiency and Power Dissipation Graph

This graph displays the efficiency and power dissipation of the converter at three different input and output voltage conditions.

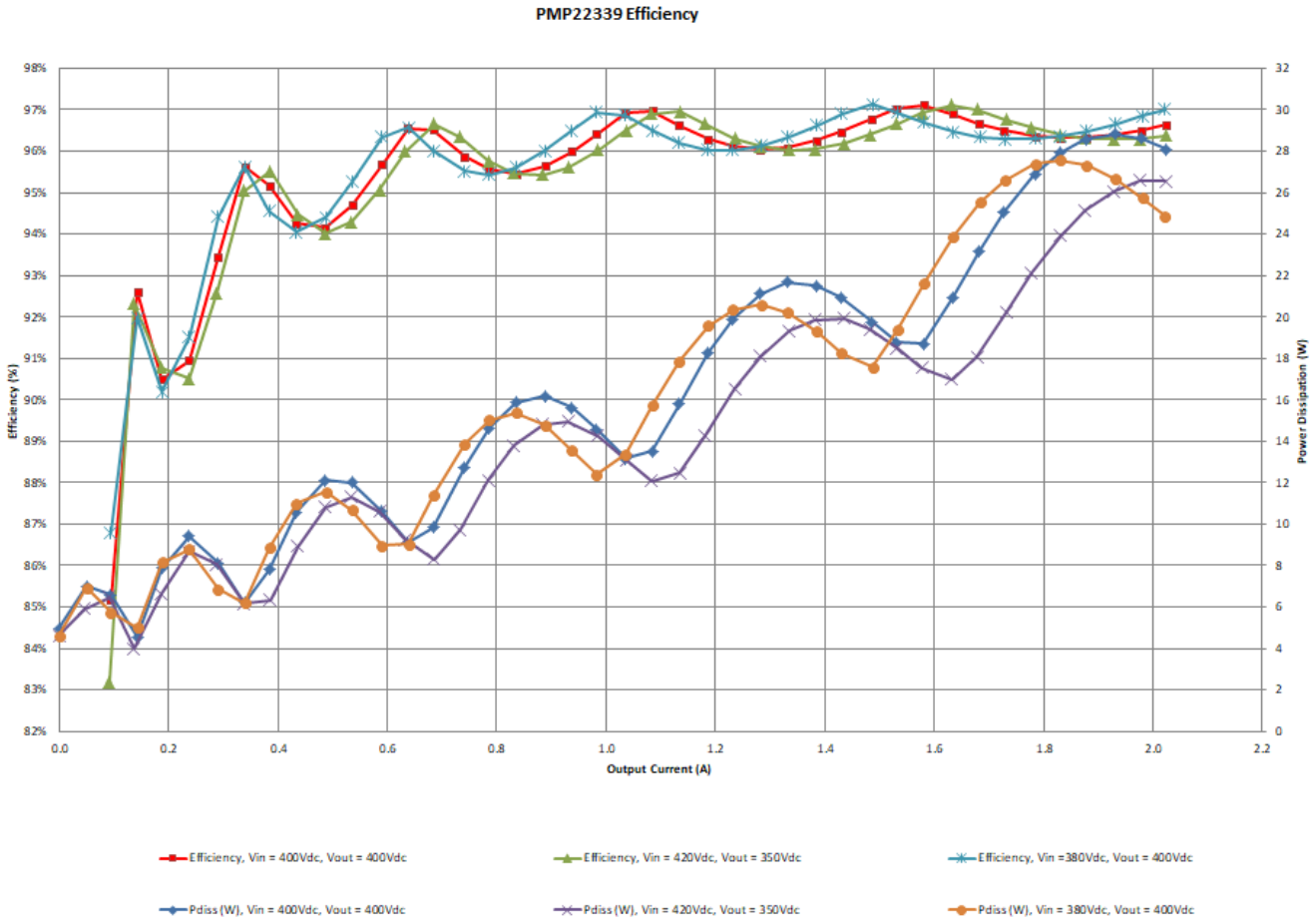

Figure 3-3. Efficiency and Power Dissipation Graph

3.3 Efficiency and Power Dissipation Data

Vin	Iin	Vout	Iout	Po	Pin	Efficiency, Vin = 400Vdc, Vout = 400Vdc	Pdiss (W), Vin = 400Vdc, Vout = 400Vdc
400.111	0.0124	399.6	0.0000	0.000	4.968	0.0%	4.97
400.109	0.0678	399.6	0.0504	20.119	27.121	74.2%	7.00
400.108	0.1107	399.6	0.0944	37.714	44.286	85.2%	6.57
400.108	0.1540	399.6	0.1428	57.075	61.631	92.6%	4.56
400.108	0.2073	399.6	0.1878	75.047	82.930	90.5%	7.88
400.107	0.2600	399.6	0.2368	94.631	104.045	91.0%	9.41
400.106	0.3102	399.6	0.2903	115.992	124.109	93.5%	8.12
400.112	0.3543	399.6	0.3393	135.569	141.777	95.6%	6.21
400.105	0.4037	399.5	0.3847	153.714	161.529	95.2%	7.82
400.109	0.4594	399.5	0.4336	173.232	183.797	94.3%	10.57
400.109	0.5166	399.5	0.4871	194.603	206.704	94.1%	12.10
400.108	0.5651	399.5	0.5358	214.082	226.083	94.7%	12.00
400.106	0.6149	399.5	0.5892	235.417	246.038	95.7%	10.62
400.106	0.6601	399.5	0.6382	254.986	264.094	96.6%	9.11
400.105	0.7073	399.5	0.6837	273.157	283.013	96.5%	9.86
400.105	0.7712	399.5	0.7404	295.809	308.561	95.9%	12.75
400.104	0.8212	399.5	0.7858	313.938	328.574	95.5%	14.64
400.104	0.8729	399.5	0.8346	333.395	349.259	95.5%	15.86
400.102	0.9269	399.5	0.8879	354.689	370.865	95.6%	16.18
400.102	0.9743	399.5	0.9367	374.190	389.803	96.0%	15.61
400.102	1.0169	399.5	0.9821	392.300	406.868	96.4%	14.57
400.100	1.0666	399.5	1.0353	413.585	426.763	96.9%	13.18
400.101	1.1162	399.5	1.0841	433.082	446.585	97.0%	13.50
400.100	1.1706	399.5	1.1329	452.561	468.357	96.6%	15.80
400.099	1.2300	399.5	1.1862	473.823	492.114	96.3%	18.29
400.099	1.2794	399.5	1.2317	492.005	511.899	96.1%	19.89
400.099	1.3332	399.5	1.2825	512.320	533.424	96.0%	21.10
400.098	1.3834	399.5	1.3313	531.809	553.476	96.1%	21.67
400.099	1.4362	399.5	1.3846	553.102	574.614	96.3%	21.51
400.099	1.4799	399.5	1.4298	571.165	592.095	96.5%	20.93
400.099	1.5333	399.5	1.4864	593.744	613.488	96.8%	19.74
400.098	1.5762	399.4	1.5318	611.846	630.614	97.0%	18.77
400.097	1.6247	399.5	1.5805	631.328	650.042	97.1%	18.71
400.097	1.6834	399.5	1.6337	652.601	673.511	96.9%	20.91
400.098	1.7376	399.5	1.6824	672.043	695.222	96.7%	23.18
400.096	1.7873	399.5	1.7275	690.032	715.104	96.5%	25.07
400.095	1.8484	399.5	1.7840	712.646	739.532	96.4%	26.89
400.095	1.8961	399.5	1.8292	730.707	758.636	96.3%	27.93
400.095	1.9464	399.5	1.8779	750.155	778.753	96.3%	28.60
400.095	2.0001	399.5	1.9311	771.409	800.226	96.4%	28.82
400.096	2.0482	399.5	1.9797	790.857	819.473	96.5%	28.62
400.095	2.0900	399.3	2.0239	808.107	836.211	96.6%	28.10

Figure 3-4. Efficiency and Power Dissipation at V_{IN} = 400 Vdc, V_{OUT} = 400 Vdc

Vin	Iin	Vout	Iout	Po	Pin	Efficiency, Vin = 420Vdc, Vout = 350Vdc	Pdiss (W), Vin = 420Vdc, Vout = 350Vdc
420.107	0.0110	349.9	0.0000	0.000	4.606	0.0%	4.61
420.108	0.0526	349.9	0.0462	16.171	22.100	73.2%	5.93
420.108	0.0919	349.9	0.0918	32.120	38.612	83.2%	6.49
420.106	0.1234	349.8	0.1368	47.864	51.852	92.3%	3.99
420.106	0.1717	349.8	0.1871	65.464	72.123	90.8%	6.66
420.106	0.2180	349.8	0.2369	82.891	91.578	90.5%	8.69
420.106	0.2588	349.8	0.2877	100.662	108.725	92.6%	8.06
420.111	0.2958	349.8	0.3376	118.110	124.261	95.1%	6.15
420.100	0.3367	349.8	0.3863	135.133	141.459	95.5%	6.33
420.108	0.3844	349.8	0.4361	152.548	161.472	94.5%	8.92
420.106	0.4311	349.8	0.4868	170.276	181.104	94.0%	10.83
420.106	0.4720	349.8	0.5346	186.998	198.304	94.3%	11.31
420.105	0.5127	349.8	0.5854	204.755	215.368	95.1%	10.61
420.105	0.5483	349.8	0.6322	221.105	230.349	96.0%	9.24
420.105	0.5907	349.8	0.6858	239.849	248.144	96.7%	8.30
420.104	0.6330	349.8	0.7325	256.199	265.939	96.3%	9.74
420.104	0.6817	349.8	0.7841	274.260	286.375	95.8%	12.11
420.102	0.7246	349.8	0.8309	290.604	304.393	95.5%	13.79
420.102	0.7717	349.8	0.8846	309.386	324.188	95.4%	14.80
420.100	0.8108	349.7	0.9311	325.652	340.616	95.6%	14.96
420.100	0.8539	349.8	0.9849	344.471	358.729	96.0%	14.26
420.100	0.8941	349.8	1.0364	362.491	375.603	96.5%	13.11
420.099	0.9304	349.7	1.0830	378.785	390.879	96.9%	12.09
420.098	0.9745	349.8	1.1348	396.889	409.365	97.0%	12.48
420.098	1.0176	349.7	1.1814	413.179	427.479	96.7%	14.30
420.097	1.0676	349.8	1.2350	431.946	448.491	96.3%	16.55
420.096	1.1101	349.8	1.2816	448.254	466.344	96.1%	18.09
420.095	1.1577	349.8	1.3353	467.018	486.357	96.0%	19.34
420.096	1.1978	349.7	1.3819	483.308	503.178	96.1%	19.87
420.095	1.2425	349.8	1.4354	502.036	521.951	96.2%	19.92
420.095	1.2800	349.8	1.4820	518.322	537.738	96.4%	19.42
420.095	1.3190	349.8	1.5314	535.624	554.101	96.7%	18.48
420.094	1.3555	349.8	1.5780	551.906	569.437	96.9%	17.53
420.094	1.3988	349.8	1.6315	570.622	587.619	97.1%	17.00
420.095	1.4400	349.8	1.6780	586.878	604.945	97.0%	18.07
420.093	1.4898	349.8	1.7316	605.630	625.838	96.8%	20.21
420.094	1.5331	349.8	1.7781	621.900	644.025	96.6%	22.13
420.094	1.5818	349.8	1.8315	640.576	664.513	96.4%	23.94
420.093	1.6217	349.8	1.8759	656.135	681.277	96.3%	25.14
420.094	1.6684	349.8	1.9294	674.828	700.881	96.3%	26.05
420.093	1.7084	349.8	1.9759	691.102	717.678	96.3%	26.58
420.091	1.7437	349.0	2.0228	705.962	732.517	96.4%	26.55

Figure 3-5. Efficiency and Power Dissipation at V_{IN} = 420 Vdc, V_{OUT} = 350 Vdc

Vin	Iin	Vout	Iout	Po	Pin	Efficiency, Vin =380Vdc, Vout = 400Vdc	Pdiss (W), Vin = 380Vdc, Vout = 400Vdc
380.099	0.0121	399.6	0.0000	0.000	4.611	0.0%	4.61
380.100	0.0714	399.6	0.0506	20.219	27.150	74.5%	6.93
380.098	0.1146	399.6	0.0946	37.803	43.555	86.8%	5.75
380.098	0.1635	399.6	0.1431	57.168	62.157	92.0%	4.99
380.098	0.2192	399.6	0.1881	75.151	83.320	90.2%	8.17
380.098	0.2724	399.6	0.2371	94.725	103.522	91.5%	8.80
380.098	0.3234	399.6	0.2905	116.075	122.937	94.4%	6.86
380.093	0.3732	399.6	0.3395	135.645	141.853	95.6%	6.21
380.099	0.4280	399.6	0.3849	153.810	162.664	94.6%	8.85
380.098	0.4849	399.6	0.4338	173.336	184.317	94.0%	10.98
380.097	0.5427	399.6	0.4873	194.708	206.270	94.4%	11.56
380.096	0.5916	399.6	0.5361	214.199	224.879	95.3%	10.68
380.096	0.6432	399.5	0.5895	235.528	244.488	96.3%	8.96
380.095	0.6950	399.5	0.6385	255.106	264.155	96.6%	9.05
380.093	0.7489	399.5	0.6840	273.279	284.650	96.0%	11.37
380.093	0.8151	399.5	0.7407	295.938	309.796	95.5%	13.86
380.091	0.8659	399.5	0.7861	314.080	329.116	95.4%	15.04
380.091	0.9180	399.5	0.8349	333.561	348.918	95.6%	15.36
380.091	0.9725	399.5	0.8883	354.872	369.634	96.0%	14.76
380.090	1.0207	399.5	0.9371	374.388	387.954	96.5%	13.57
380.090	1.0653	399.5	0.9825	392.509	404.917	96.9%	12.41
380.090	1.1238	399.5	1.0357	413.769	427.153	96.9%	13.38
380.089	1.1812	399.5	1.0845	433.261	448.969	96.5%	15.71
380.087	1.2382	399.5	1.1333	452.742	470.605	96.2%	17.86
380.088	1.2987	399.5	1.1867	474.062	493.635	96.0%	19.57
380.087	1.3486	399.5	1.2321	492.220	512.566	96.0%	20.35
380.088	1.4027	399.5	1.2831	512.572	533.165	96.1%	20.59
380.087	1.4532	399.5	1.3319	532.119	552.323	96.3%	20.20
380.087	1.5067	399.5	1.3852	553.380	572.685	96.6%	19.31
380.086	1.5516	399.5	1.4305	571.490	589.722	96.9%	18.23
380.087	1.6093	399.5	1.4870	594.086	611.659	97.1%	17.57
380.086	1.6618	399.5	1.5325	612.251	631.635	96.9%	19.38
380.086	1.7190	399.5	1.5812	631.692	653.353	96.7%	21.66
380.085	1.7809	399.5	1.6345	653.007	676.897	96.5%	23.89
380.084	1.8364	399.5	1.6832	672.475	697.994	96.3%	25.52
380.084	1.8867	399.5	1.7283	690.528	717.108	96.3%	26.58
380.084	1.9483	399.5	1.7850	713.145	740.518	96.3%	27.37
380.083	1.9963	399.5	1.8301	731.201	758.756	96.4%	27.56
380.083	2.0468	399.5	1.8789	750.663	777.969	96.5%	27.31
380.083	2.1010	399.5	1.9321	771.932	798.570	96.7%	26.64
380.083	2.1498	399.5	1.9807	791.345	817.099	96.8%	25.75
380.081	2.1864	398.7	2.0218	806.138	831.021	97.0%	24.88

Figure 3-6. Efficiency and Power Dissipation at V_{IN} = 380 Vdc, V_{OUT} = 400 Vdc

3.4 Current Regulation

This graph displays the measured output current versus CHG ISET DAC at an input voltage of 400 Vdc. A PWM signal is provided at J8 with a frequency of 100 kHz, an amplitude of 2.5 V, and a duty cycle varying between 0% and 100%. A constant resistance mode load of 200 Ω is used and V_{OUT} is allowed to vary with the current control.

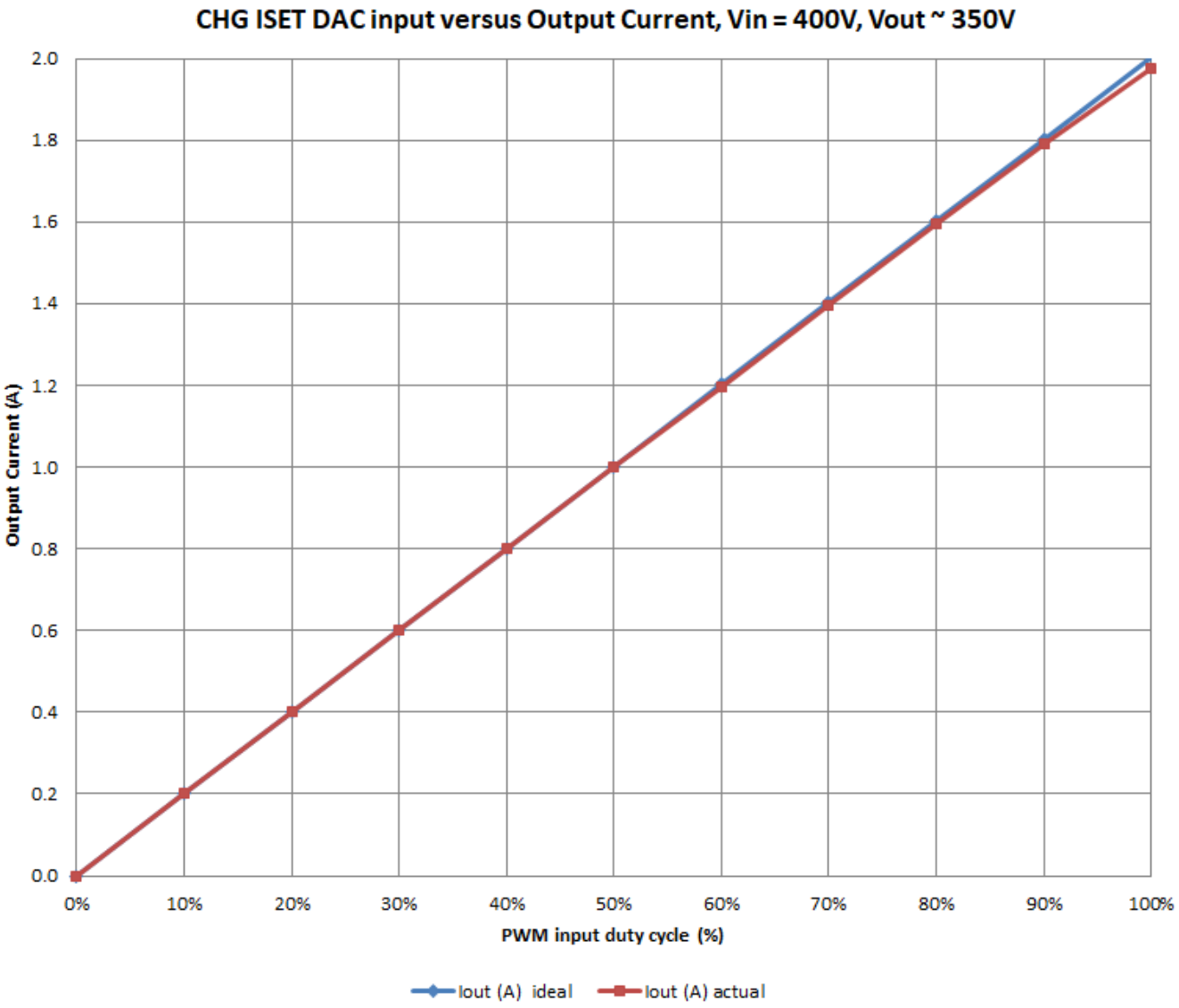

Figure 3-7. CHG ISET DAC Accuracy Curve

Duty Cycle	VREF3 TP14 (V)	Iout (A) actual	Iout (A) ideal	Iout error (%)
0.999	1.9975	1.9754	2.0009	-1.3
0.900	1.7997	1.7923	1.8030	-0.6
0.800	1.5997	1.5944	1.6027	-0.5
0.700	1.3997	1.3961	1.4023	-0.4
0.600	1.1997	1.1976	1.2020	-0.4
0.500	0.9998	0.9988	1.0017	-0.3
0.400	0.7999	0.7997	0.8013	-0.2
0.300	0.6002	0.6004	0.6010	-0.1
0.200	0.4009	0.4004	0.4007	-0.1
0.100	0.2006	0.2013	0.2003	0.5
0.002	0.0039	0.0041	0.0032	27.0

Figure 3-8. CHG ISET DAC Accuracy Table

3.5 Voltage Regulation

This graph displays the measured output voltage versus CHG VSET DAC at an input voltage of 400 Vdc. A DC voltage ranging from 0 V–3 V is applied at J6 and a constant resistance mode load is used with the resistance equal to V_{OUT} ideal at each setpoint.

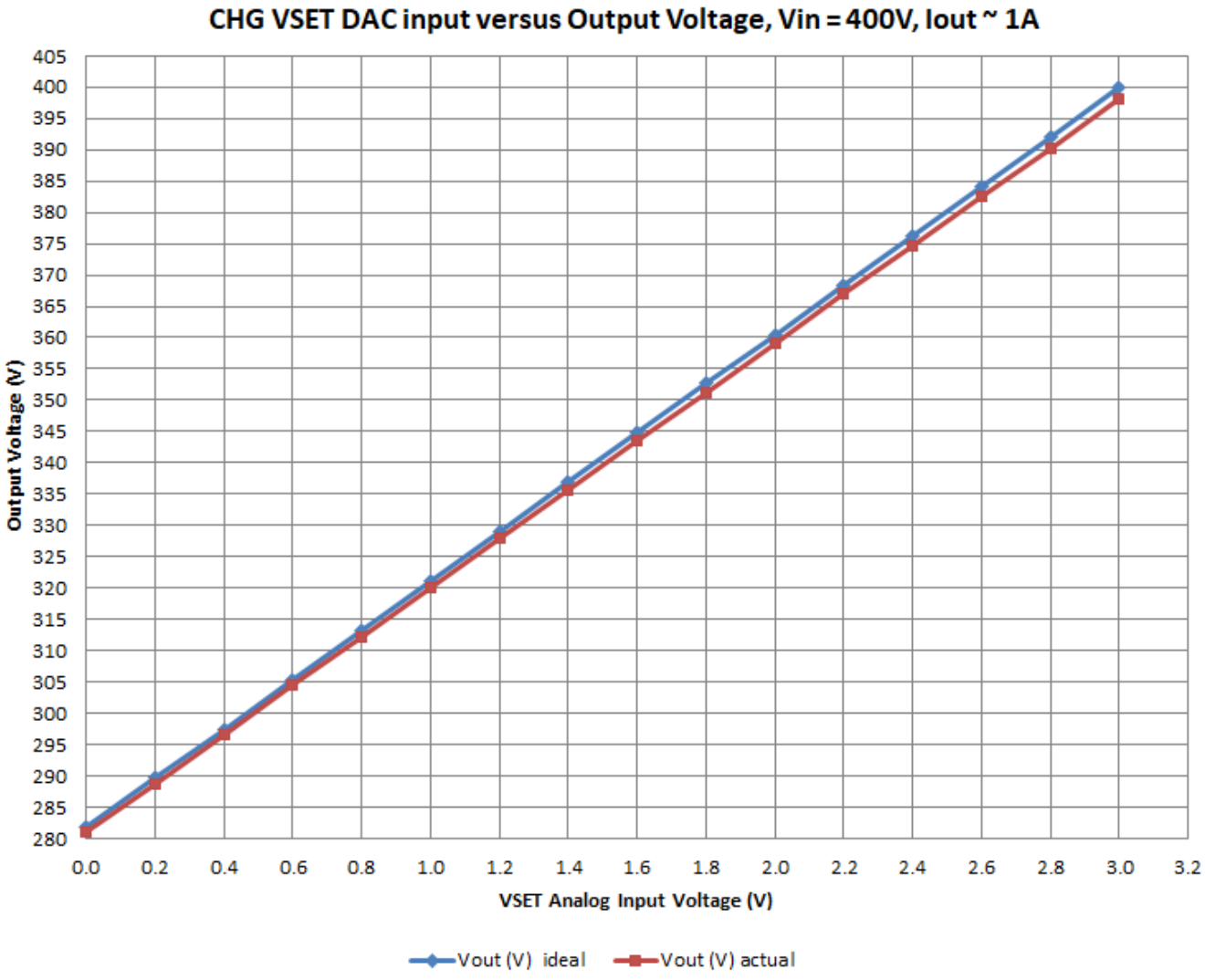

Figure 3-9. CHG VSET DAC Accuracy Curve

VDAC	VREF1 TP11 (V)	Vout (V) actual	Vout (V) ideal	Vout error (%)
0.000	1.762	281.0	281.7322	-0.3
0.200	1.811	288.8	289.6093	-0.3
0.400	1.861	296.6	297.4863	-0.3
0.600	1.910	304.4	305.3633	-0.3
0.800	1.959	312.2	313.2404	-0.3
1.000	2.008	320.0	321.1174	-0.3
1.200	2.057	327.8	328.9944	-0.4
1.400	2.106	335.7	336.8715	-0.4
1.600	2.156	343.5	344.7485	-0.4
1.800	2.205	351.3	352.6255	-0.4
2.000	2.254	359.1	360.5026	-0.4
2.200	2.303	366.9	368.3796	-0.4
2.400	2.352	374.7	376.2566	-0.4
2.600	2.401	382.5	384.1337	-0.4
2.800	2.450	390.3	392.0107	-0.4
3.000	2.500	398.1	399.8878	-0.5

Figure 3-10. CHG VSET DAC Accuracy Table

4 Waveforms

4.1 Start-up

The following figures show the output voltage start-up waveform (YELLOW), the $\overline{\text{ENABLE}}$ waveform (BLUE), and the output current waveform (RED) under two different output conditions.

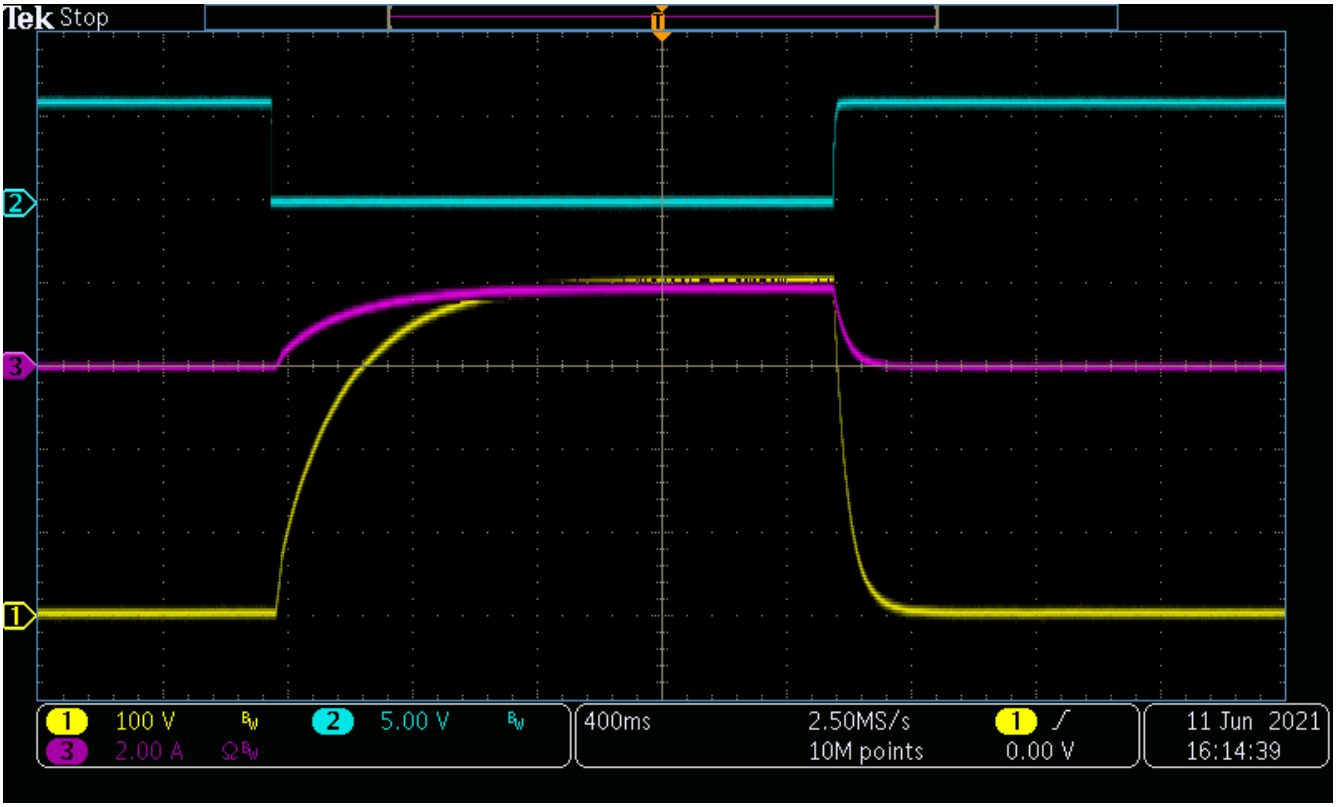

Figure 4-1. V_{IN} = 400 V and V_{OUT} = 400 V at 2 A. Resistive Load (V_{OUT}: 100 V/DIV, $\overline{\text{ENABLE}}$: 5 V/DIV, I_{OUT}: 2 A/DIV, 400 ms/DIV, BWL = 20 MHz)

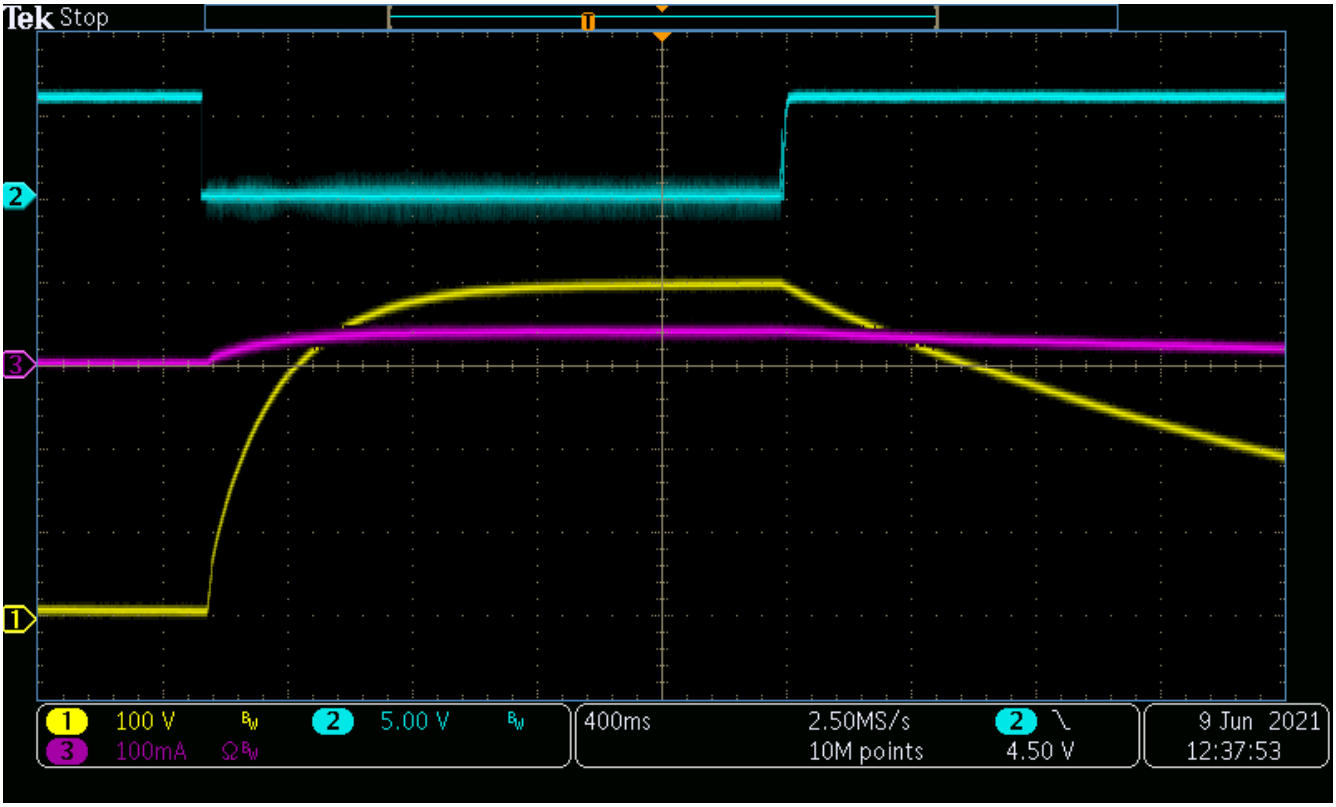

Figure 4-2. V_{IN} = 400 V and V_{OUT} = 400 V at 40 mA. Resistive Load (V_{OUT}: 100 V/DIV, $\overline{\text{ENABLE}}$: 5 V/DIV, I_{OUT}: 100 mA/DIV, 400 ms/DIV, BWL = 20 MHz)

4.2 Switch Node

The following figures show the FET switch node voltage (YELLOW) at TP7 under various input and output conditions.

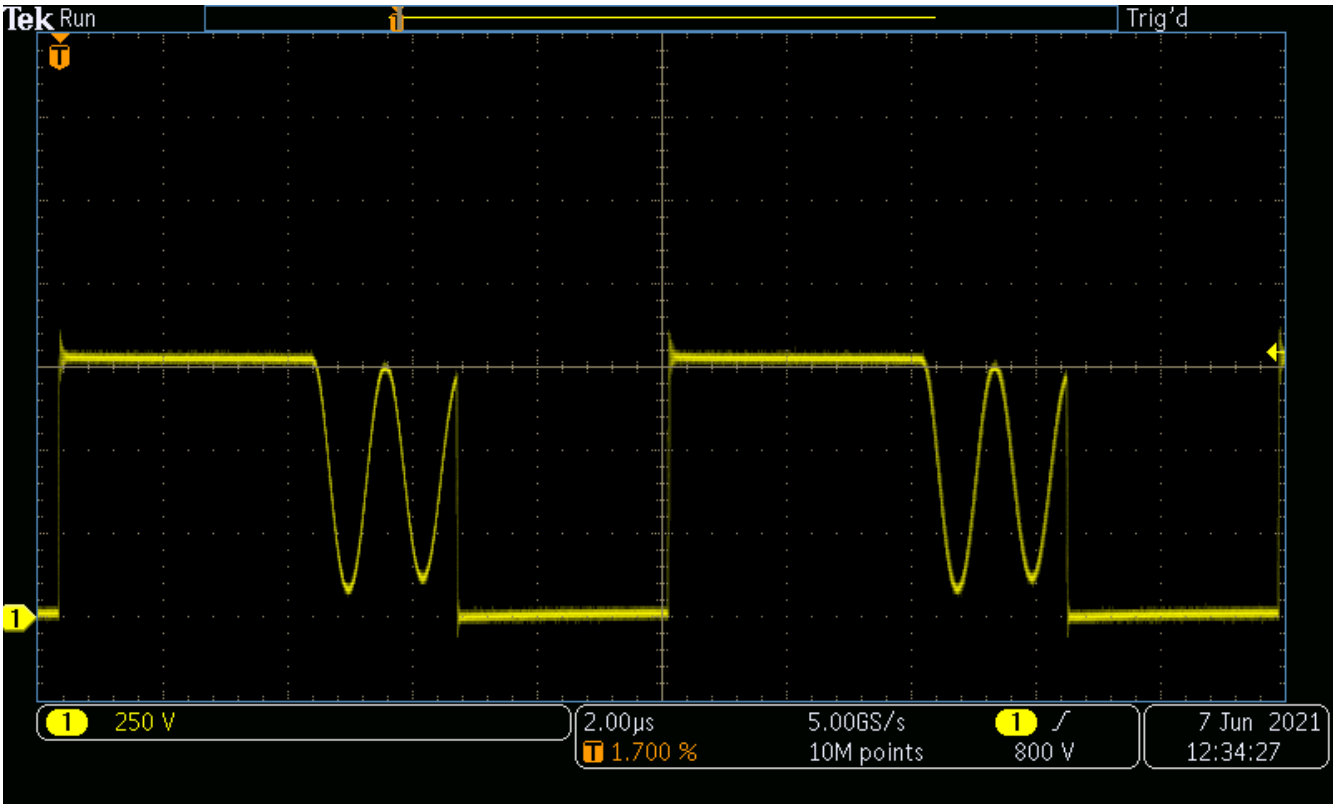

Figure 4-3. V_{IN} = 420 V and V_{OUT} = 350 V at 2 A. Resistive Load (V_{OUT}: 250 V/DIV, 2 µs/DIV, BWL = 800 MHz)

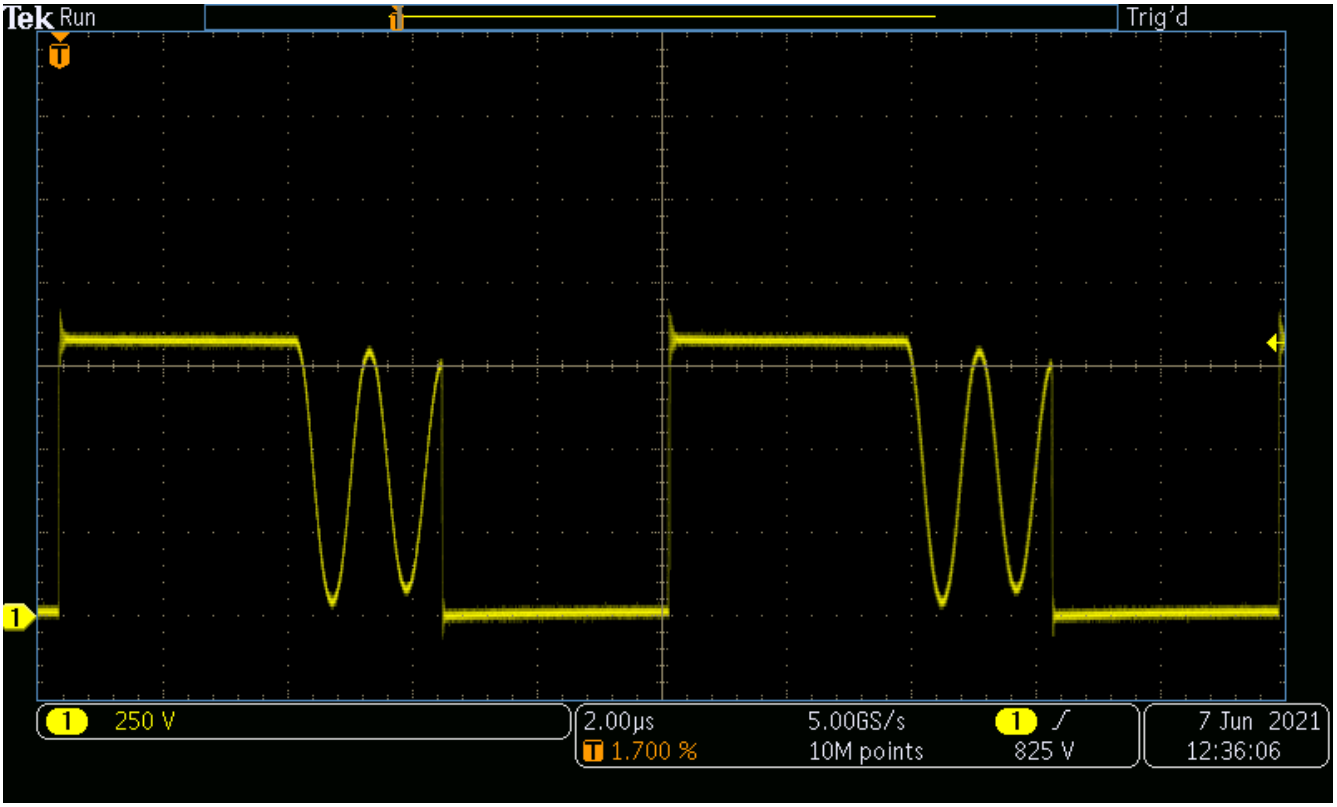

Figure 4-4. V_{IN} = 420 V and V_{OUT} = 400 V at 2 A.
Resistive Load (V_{OUT}: 250 V/DIV, 2 µs/DIV, BWL = 800 MHz)

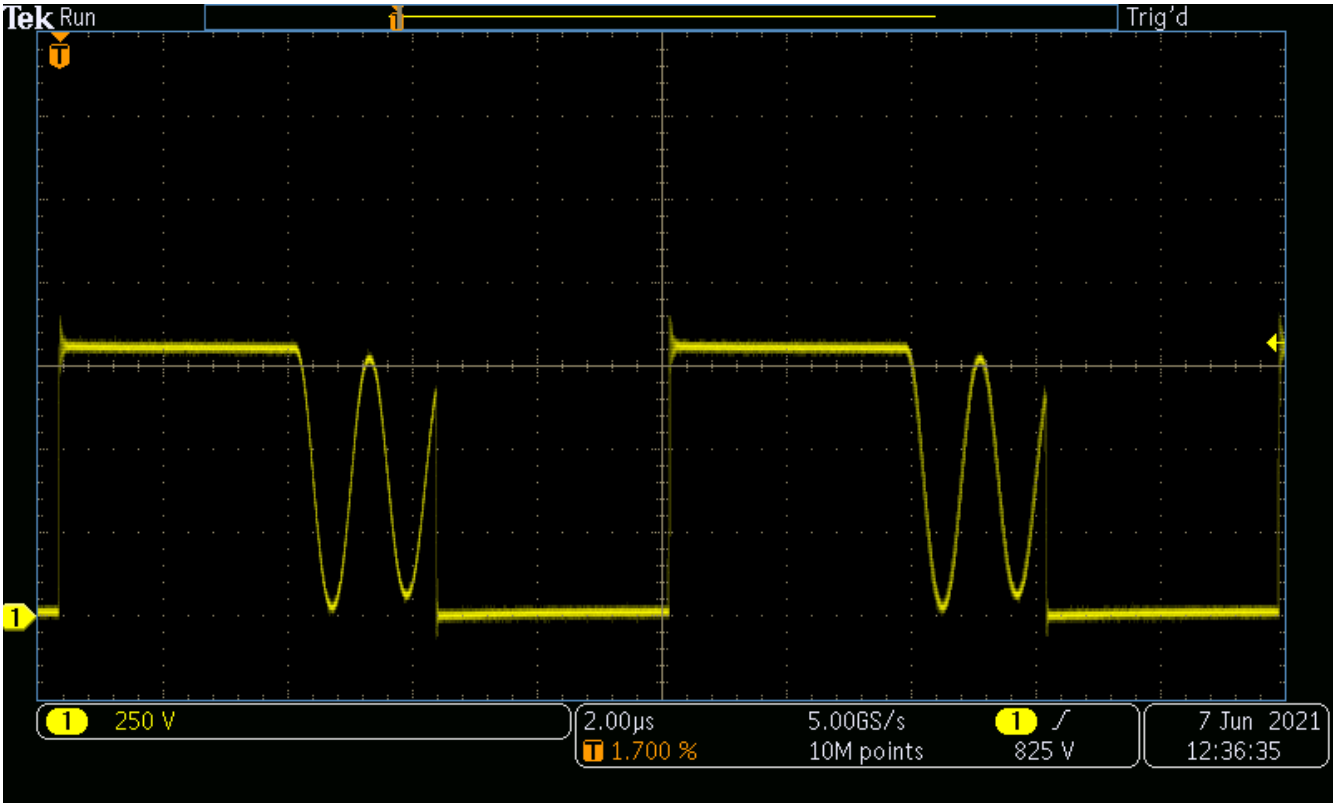

Figure 4-5. V_{IN} = 400 V and V_{OUT} = 400 V at 2 A.
Resistive Load (V_{OUT}: 250 V/DIV, 2 µs/DIV, BWL = 800 MHz)

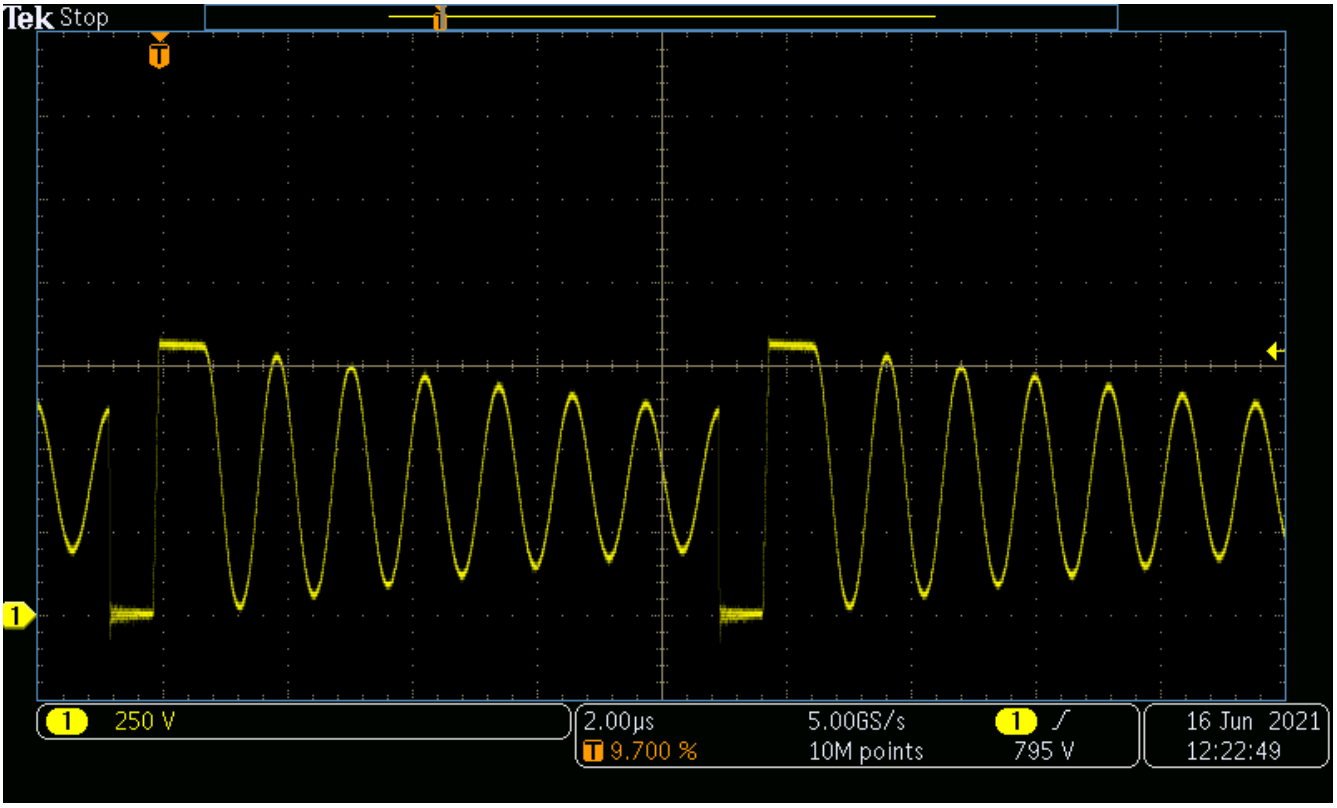

Figure 4-6. V_{IN} = 400 V and V_{OUT} = 400 V at 70 mA.
Resistive Load (V_{OUT}: 250 V/DIV, 2 µs/DIV, BWL = 800 MHz)

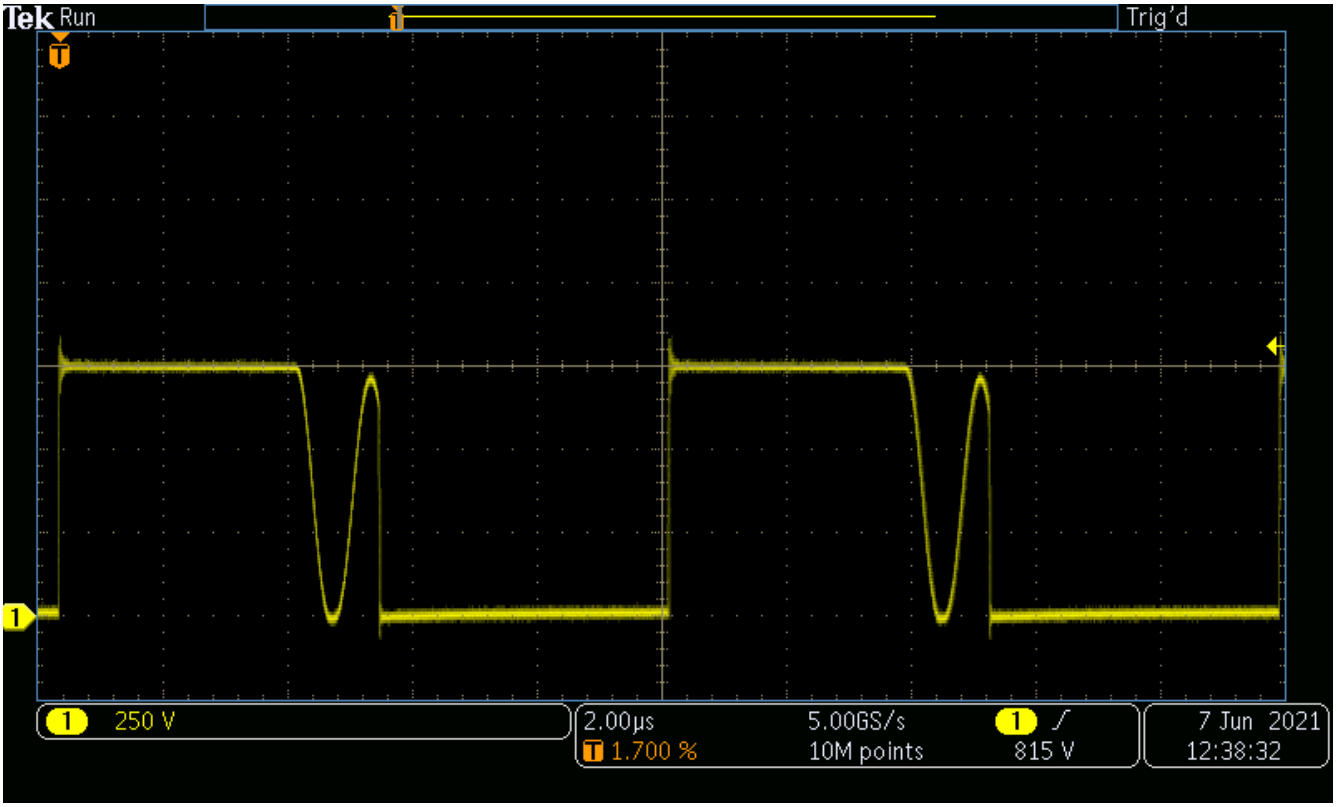

Figure 4-7. V_{IN} = 340 V and V_{OUT} = 400 V at 2 A.
Resistive Load (V_{OUT}: 250 V/DIV, 2 µs/DIV, BWL = 800 MHz)

The following figure shows the FET switch node rise time of 22.8 ns at TP7.

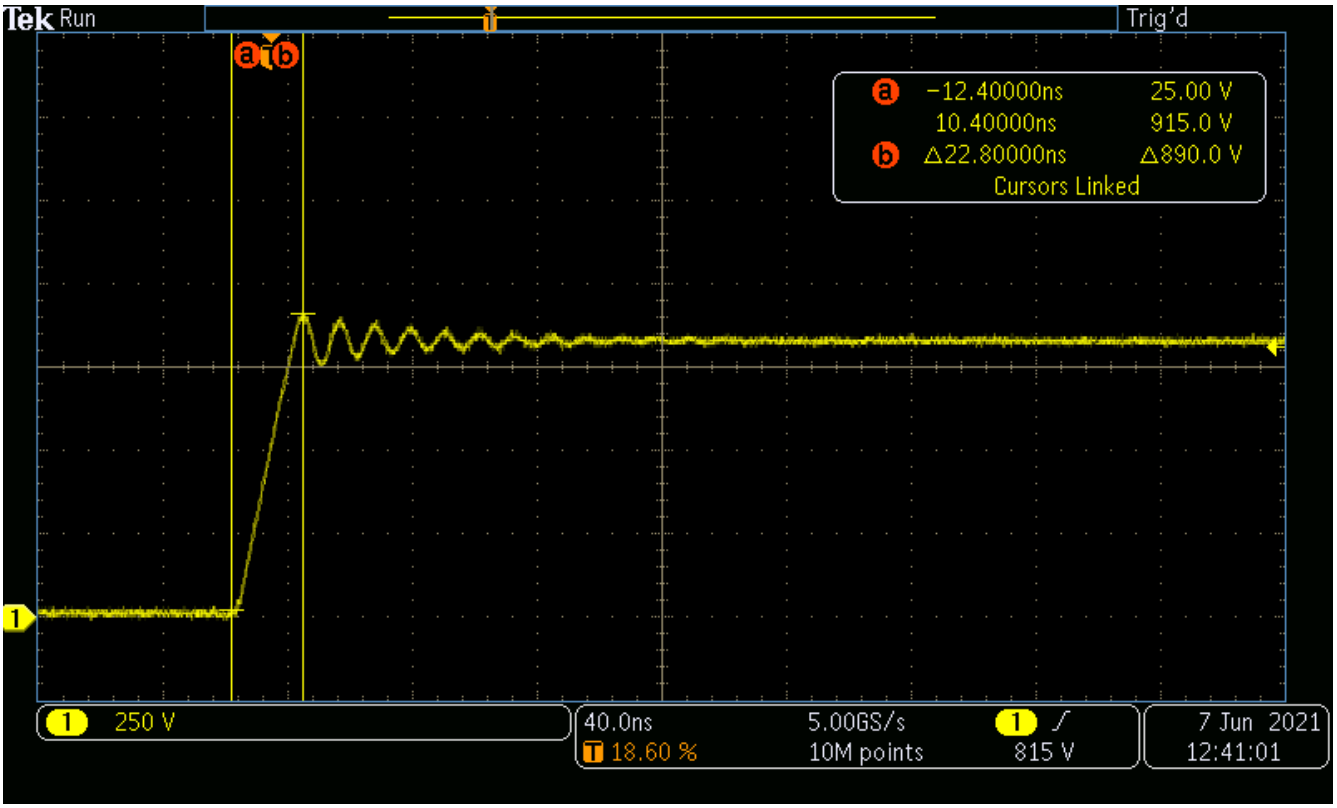

Figure 4-8. V_{IN} = 400 V and V_{OUT} = 400 V at 2 A. Resistive Load (V_{OUT}: 250 V/DIV, 40 ns/DIV, BWL = 800 MHz)

4.3 Output Voltage Ripple

The output ripple voltage is shown in the following figure. The ripple was measured tip and barrel across ceramic output capacitors C10 and C14.

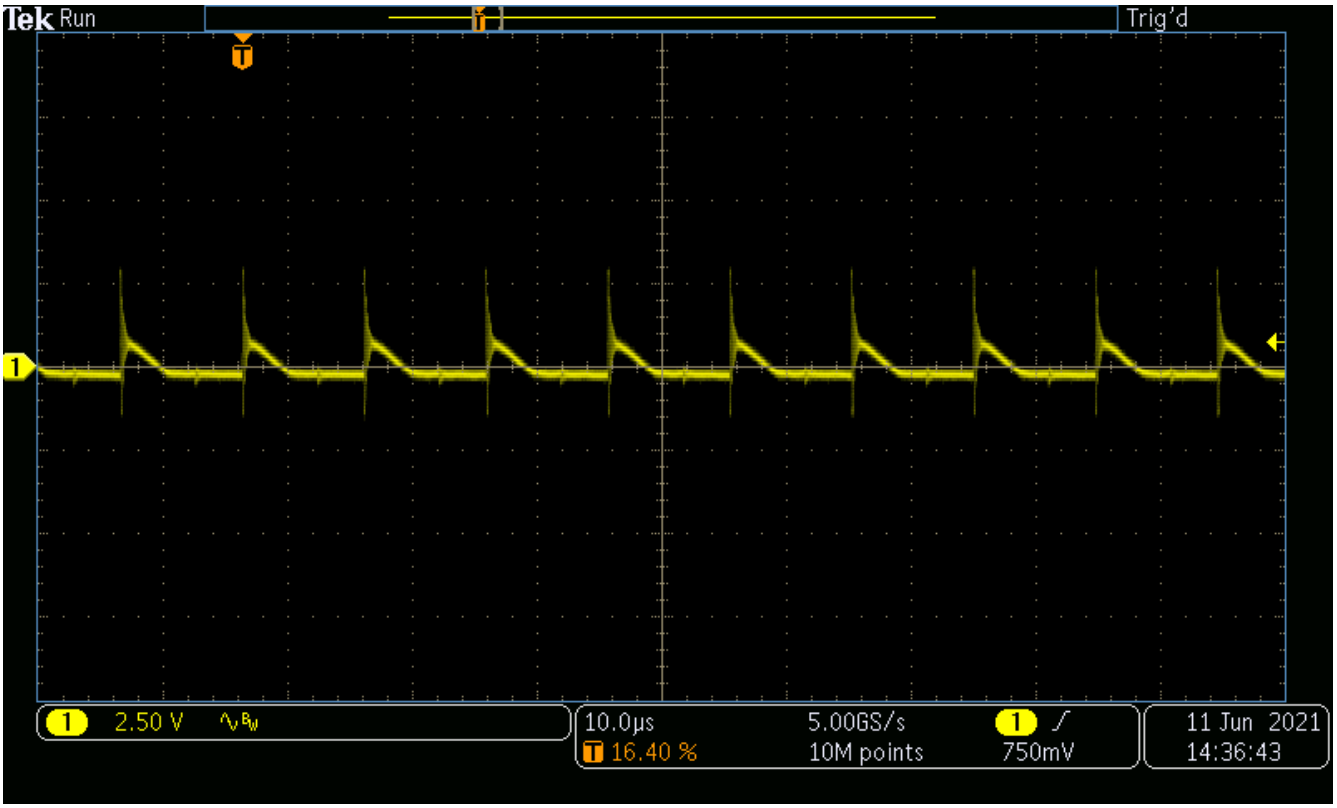

Figure 4-9. V_{IN} = 400 V and V_{OUT} = 400 V at 2 A. Resistive Load (V_{OUT}: 2.5 V/DIV, 10 µs/DIV, BWL = 20 MHz)

4.4 Current Loop to Voltage Loop Transition

The following figure shows the transition between the current loop control mode and the voltage loop control mode.

In the beginning state, the board is set to 1 A of output current and 400 V of output voltage. The resistive load is set to 270 Ω. In this state, the load is attempting to draw more current than the 1 A current limit allows. This means that the output voltage is limited to 270 V and the current loop is in control.

In the end state, the board output current setting is changed from 1 A to 2 A. The increased current limit is more than the current draw of the load. This allows the output voltage to rise up to the commanded 400 V and the voltage control loop takes over.

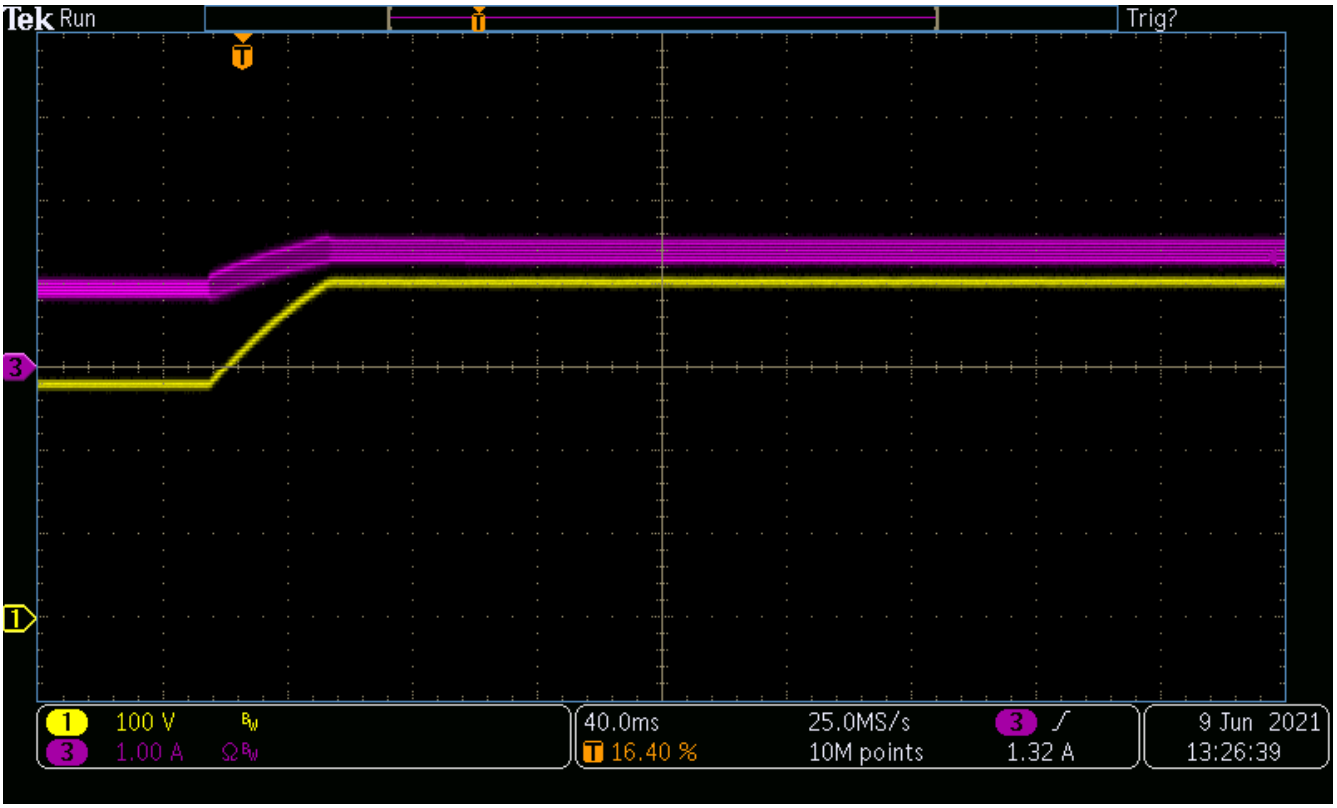

Figure 4-10. V_{IN} = 400 V, V_{OUT} = 400 V. Resistive Load = 270 Ω (V_{OUT}: 100 V/DIV, I_{OUT}: 1 A/DIV, 40 ms/DIV, BWL = 20 MHz)

4.5 Voltage Loop to Current Loop Transition

The following figure shows the transition between the voltage loop control mode and the current loop control mode.

In the beginning state, the board is set to 440 mA of output current and 282 V of output voltage. The resistive load is set to 800 Ω. In this state, the load is drawing less current than the 440 mA current limit. This means that the output voltage is regulated at 282 V and the voltage loop is in control.

In the end state, the board output voltage setting is changed from 282 V to 400 V. The current control loop limits the output current to 440 mA and the output voltage is limited to less than 400 V.

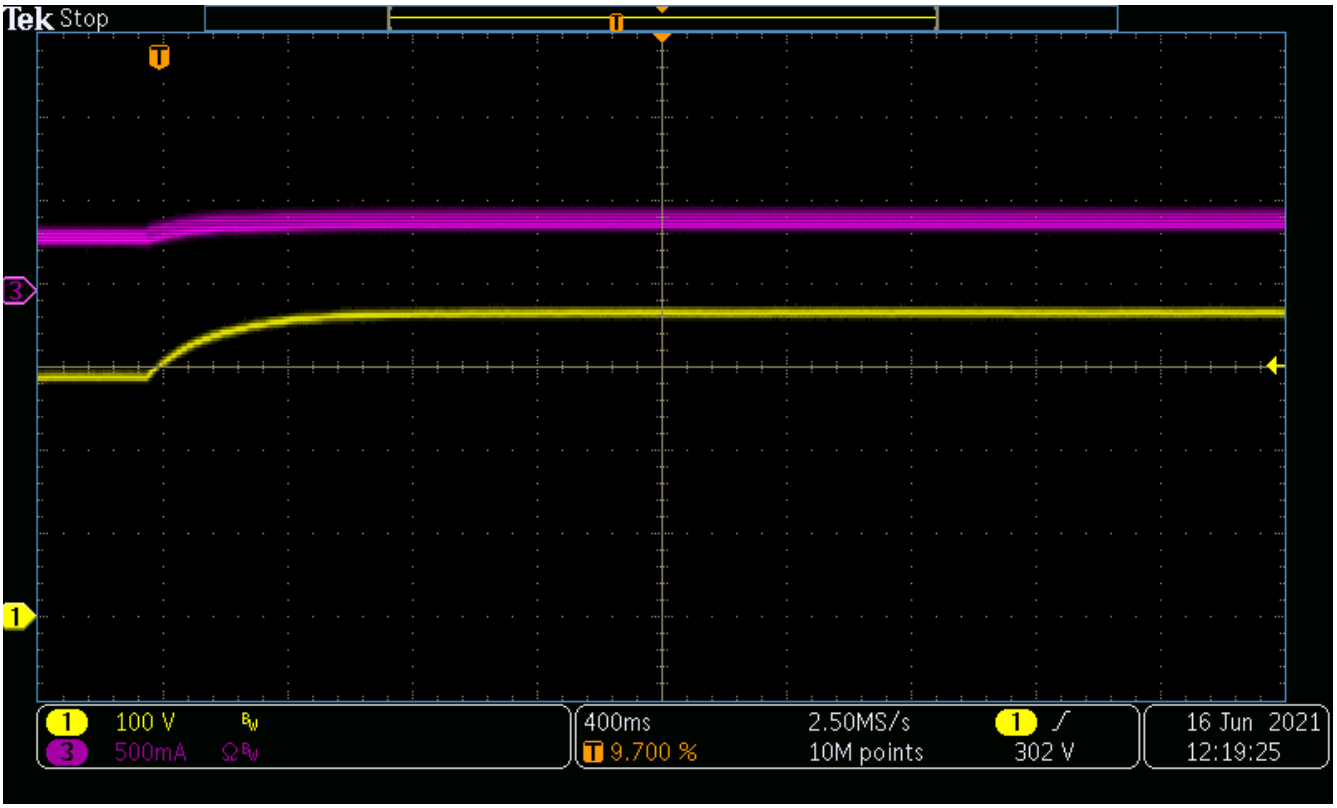

Figure 4-11. V_{IN} = 400 V, I_{OUT} = 0.44 A. Resistive Load = 800 Ω (V_{OUT}: 100 V/DIV, I_{OUT}: 500 mA/DIV, 400 ms/DIV, BWL = 20 MHz)

4.6 Bias Voltage Start-up

This board uses +18 V (BLUE), +12 V (RED), and –5 V (GREEN) bias rails to operate. The following figure shows the start-up behaviors of the +18 V, –5 V, and EN-drv (YELLOW) signals when the external 12-V bias is applied at J4. The start-up speed of the bias rails is determined by the start-up speed of the external 12-V bias.

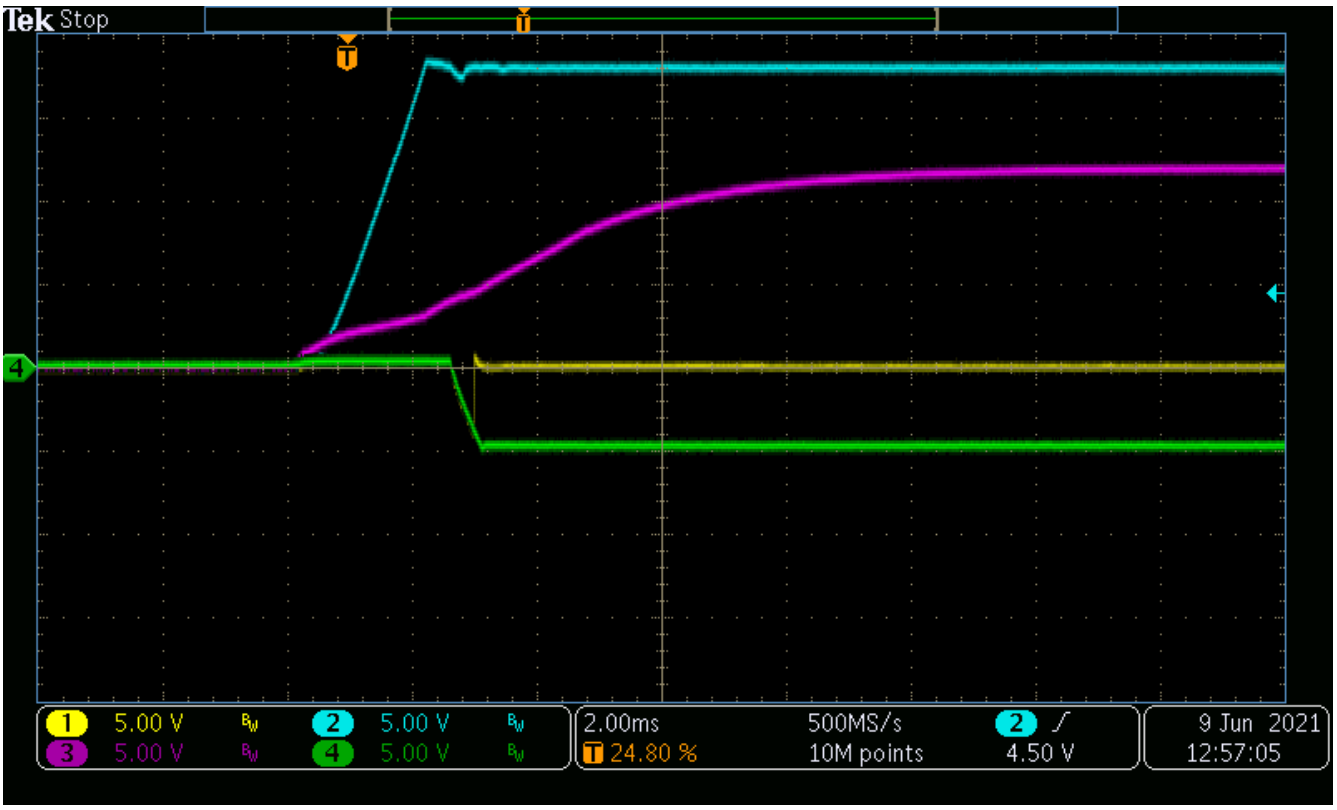

Figure 4-12. (+18 V: 5 V/DIV, +12 V: 5 V/DIV, –5 V: 5 V/DIV, EN-drv: 5 V/DIV, 200 ms/DIV, BWL = 20 MHz)

4.7 Bias Voltage Switch Nodes

The +18-V and –5-V rails are converted from an external 12-V bias signal. The following figures show the switching behaviors of these bias converters.

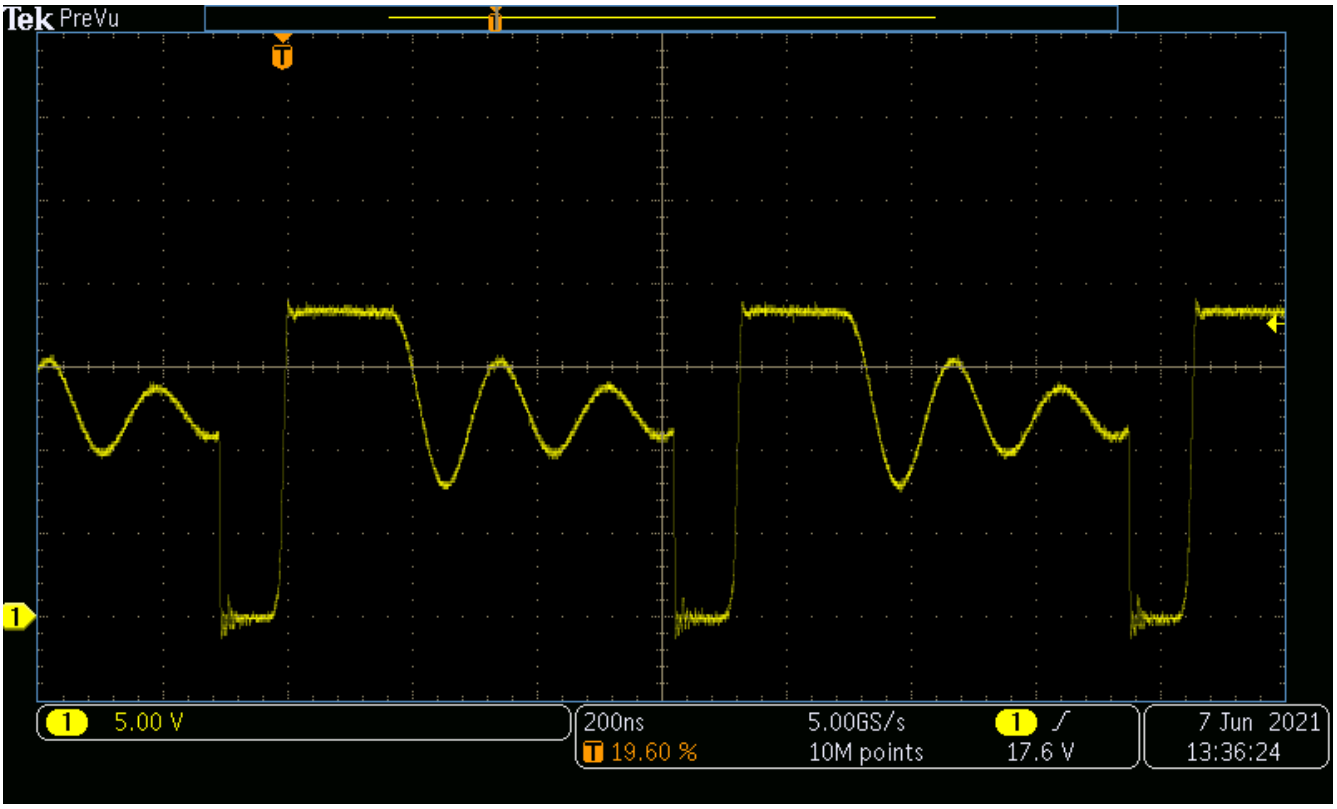

Figure 4-13. +18 V Boost Converter Switch Node at TP9, V_{IN} = 400 V and V_{OUT} = 400 V at 2 A (5 V/DIV, 200 ns/DIV, BWL = 800 MHz)

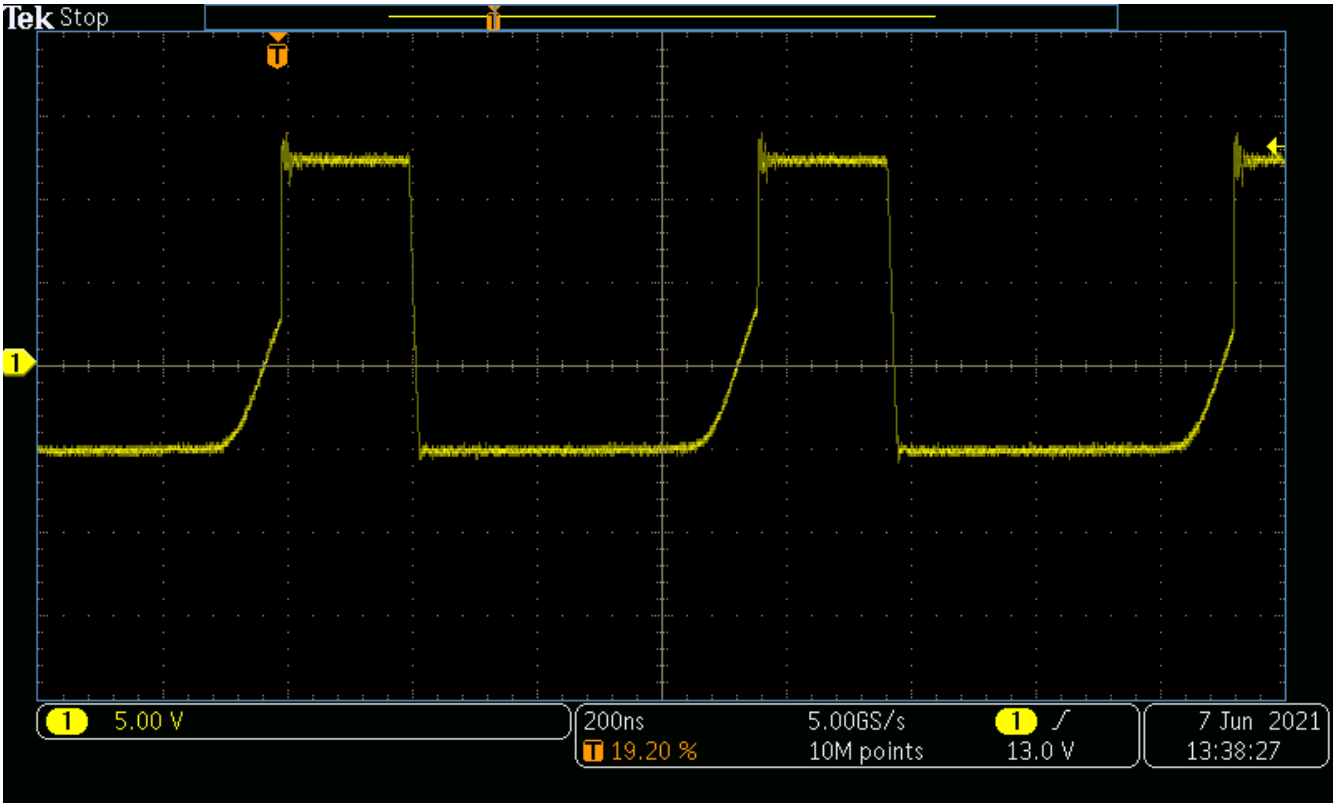

Figure 4-14. –5 V Inverting Buck-Boost Converter Switch Node at TP17, V_{IN} = 400 V and V_{OUT} = 400 V at 2 A (5 V/DIV, 200 ns/DIV, BWL = 800 MHz)

4.8 Output Current Sense Signal

The average of the MB CHG ISNS signal (on TP1) can be used to monitor the output current of the power supply. The following figures show the signal shape for varying output conditions.

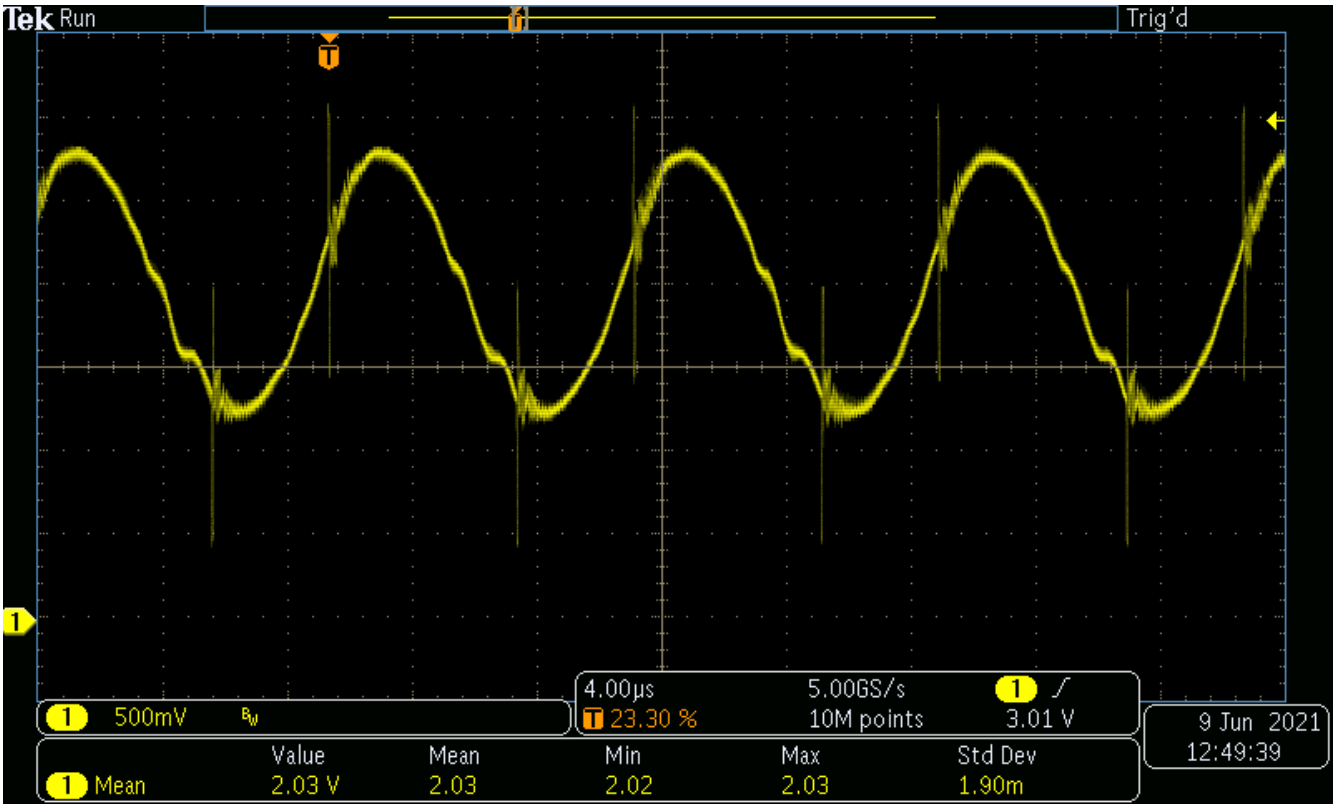

Figure 4-15. V_{IN} = 400 V, V_{OUT} = 400 V, I_{OUT} = 2 A. I_mean = 2.03 V (500 mV/DIV, 4 µs/DIV, BWL = 20 MHz)

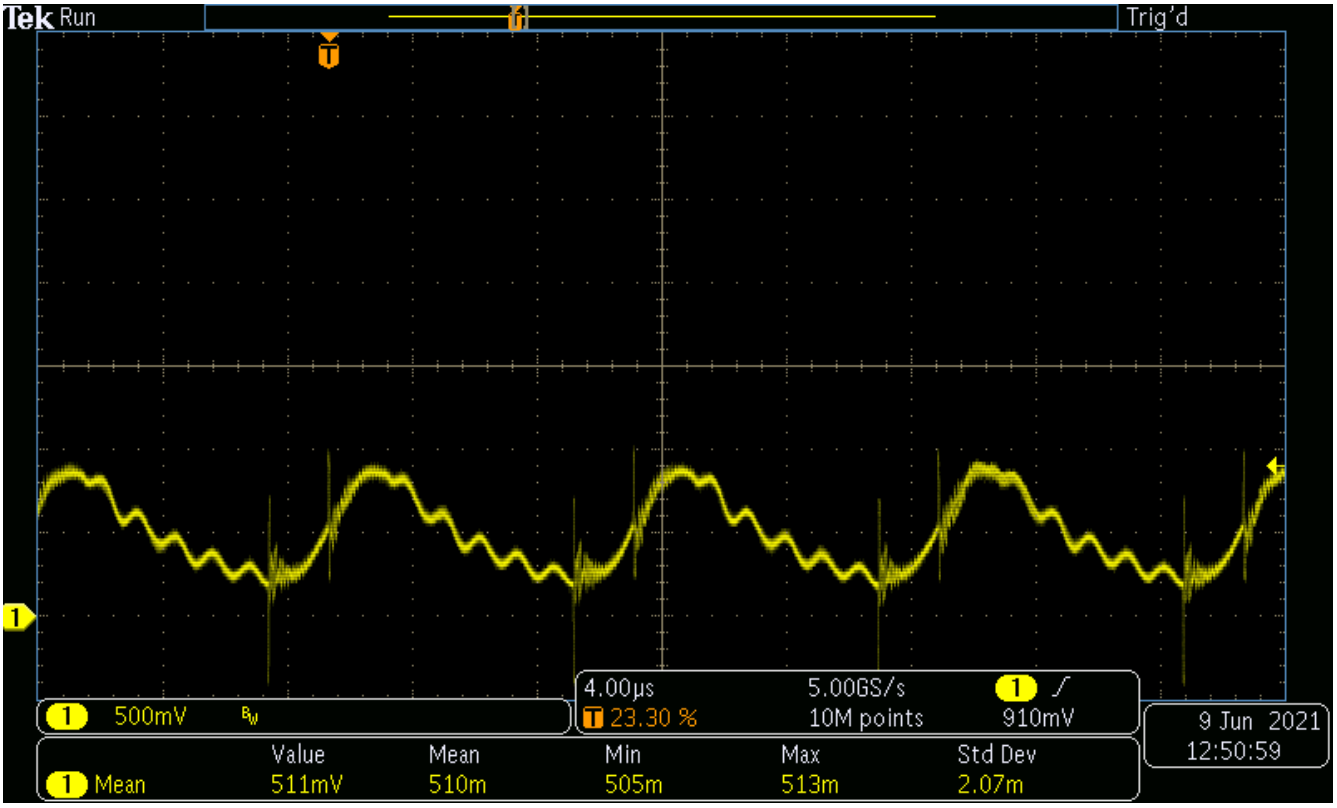

Figure 4-16. V_{IN} = 400 V, V_{OUT} = 400 V, I_{OUT} = 500 mA. I_mean = 511 mV (500 mV/DIV, 4 µs/DIV, BWL = 20 MHz)

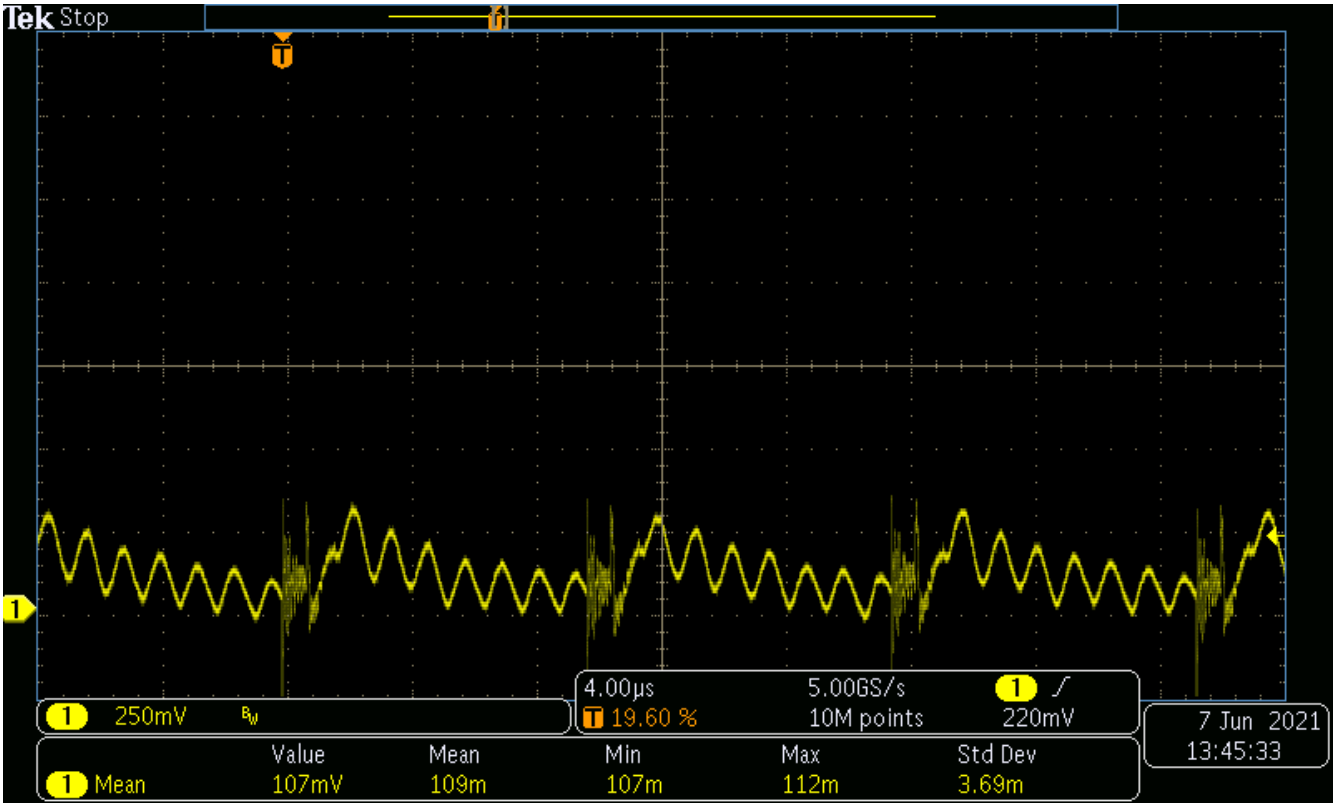

Figure 4-17. V_{IN} = 400 V, V_{OUT} = 400 V, I_{OUT} = 100 mA. I_mean = 107 mV (500 mV/DIV, 4 µs/DIV, BWL = 20 MHz)

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