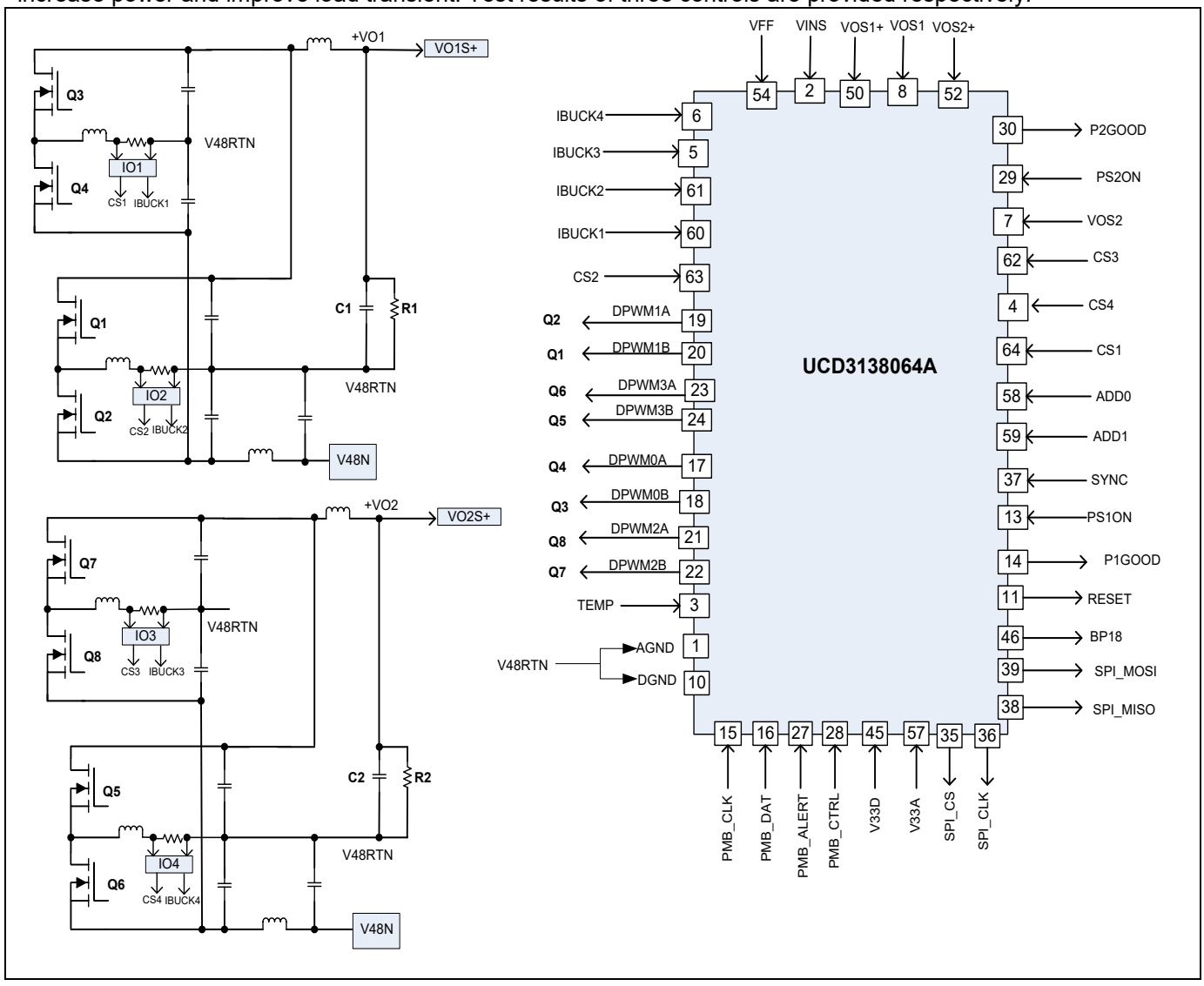
Test Report: PMP20587
Inverting Buck Boost Reference Design

Description

This reference design is to use UCD3138064A as a digital controller to control two-phase two-rail inverting buck-boost. This non-isolated converter is used for wireless radio power. The input voltage is from -35V to -60V. There are two outputs. The output voltage is adjustable from 30V to 56V. The default output voltage of rail 1 is 32V and max current is 8.5A; the default output voltage of rail2 is 48V and max current is 5.5A. With some component changes and firmware changes, the hardware can be used for current mode control or transition mode control to increase power and improve load transient. Test results of three controls are provided respectively.



1 System Specification

1.1 Board Dimension:

245mm x 136mm x 25mm (L x W x H).

1.2 Input Characteristics (Two-Phase Two-Rail under Voltage Mode Control)

Parameter	Symbols	Conditions	Min	TYP	MAX	Units
Input Voltage Range	V_{in}	Normal Operating	-36	-48	-62	V
Max Input Voltage	V_{inmax}	Continuous			-65	V
Input Current	I_{in}	Vin=33V, Full Load, both Rail ON No Load		15 0.1		A
Under Voltage Lockout	V_{off} V_{on}	V_{in} Decreasing V_{in} Increasing		-34 -36		V V

1.3 ***Output Characteristics.*** All specifications at Vin=48V and 25°C ambient unless otherwise noted.

Parameter	Symbols	Conditions	Min	TYP	MAX	Units
Rail1 Output Voltage Setpoint	V_{O1}	4A on output	18	28	56	V
Rail2 Output Voltage Setpoint	V_{O2}	2A on output	18	52	56	V
Line Regulation	Reg_{line}	All outputs; $38 \leq V_{in} \leq 72$; $I_O=I_{Omax}$			0.5	%
Load Regulation	Reg_{load}	voltage droop; $0 \leq I_O \leq I_{Omax}$; V_{in}=48V			0.5	%
Ripple and Noise(1)	V_n	5Hz to 20MHz			100	mV_{pp}
Rail1 Output Current	I_{O1}		0		8	A
Rail2 Output Current	I_{O2}		0		4.5	A
Rail1 Efficiency	η_1	Vo=28V, Vin =-48V, Io=4A		95		%
Rail2 Efficiency	η_2	Vo=52V, Vin =-48V , Io=2.5A		95		%
Output Adjust Range	V_{adj}		18		56	V
Transient Response Overshoot/Undershoot	V_{tr}	90% Load Step at 1A/uS With 500uF electrolytic cap on the output		±3%		V
Output Rise Time	t_{start}	10% to 90% of Vout		50		mS

Overshoot		At Startup			1	%
Switching Frequency	fs	Over V_{in} and I_O ranges		150		kHz
Current Sharing Accuracy	I_{share}	10% - full load		+/-5		%
Loop Phase Margin	φ	50% - Full load		60		degree
Loop Gain Marin	G	50% - Full load		10		dB

Notes: (1) Ripple and noise are measured with 10uF Tantalum capacitor and 0.1uF ceramic capacitor across output

1.4 ***Output Characteristics.*** All specifications at Vin=48V and 25°C ambient unless otherwise noted.

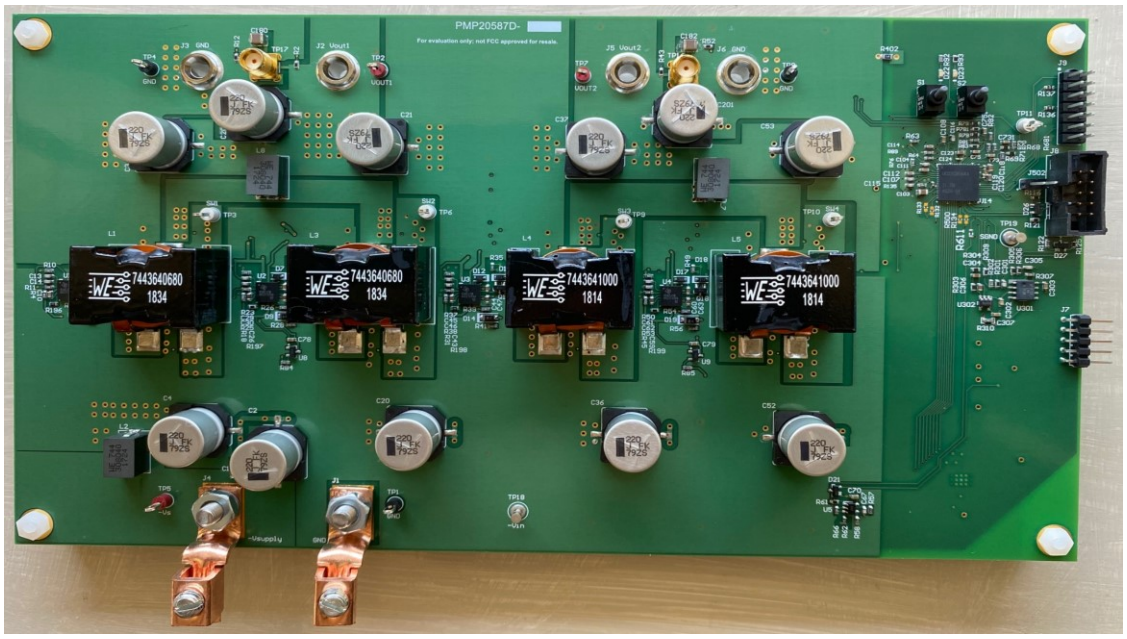
Parameter	Symbols	Fault Response	Min	TYP	MAX	Units
Input Over Voltage	V_{IN_OV}	Restart when Vin is normal		65		V
Input Under Voltage	V_{IN_uV}	Restart when Vin is normal		36		V
Output Over Voltage Slow Shutdown	$V_{O\_OV\_S}$	Restart when Fault is gone		3V higher than Vsetting		V
Output Over Voltage Fast Shutdown	$V_{O\_OV\_F}$	3 Times Retry, reset by ON/OFF Signal		4V higher than Vsetting		V
Output Under Voltage	V_{O_UV}	Restart when Fault is gone		20		V
Output Over current Level 1 shut down	$I_{O\_OC\_1}$	SD with Delay. Restart when Fault is gone		10		A
Output Over current Level 2 shut down	$I_{O\_OC\_2}$	SD without Delay. Restart when Fault.		16		A
Short circuit Protection		Restart when Fault is gone				
Over temperature Protection	T_{OT}	Restart when Fault is gone		65		Degree

2 Test Results under Voltage Mode Control

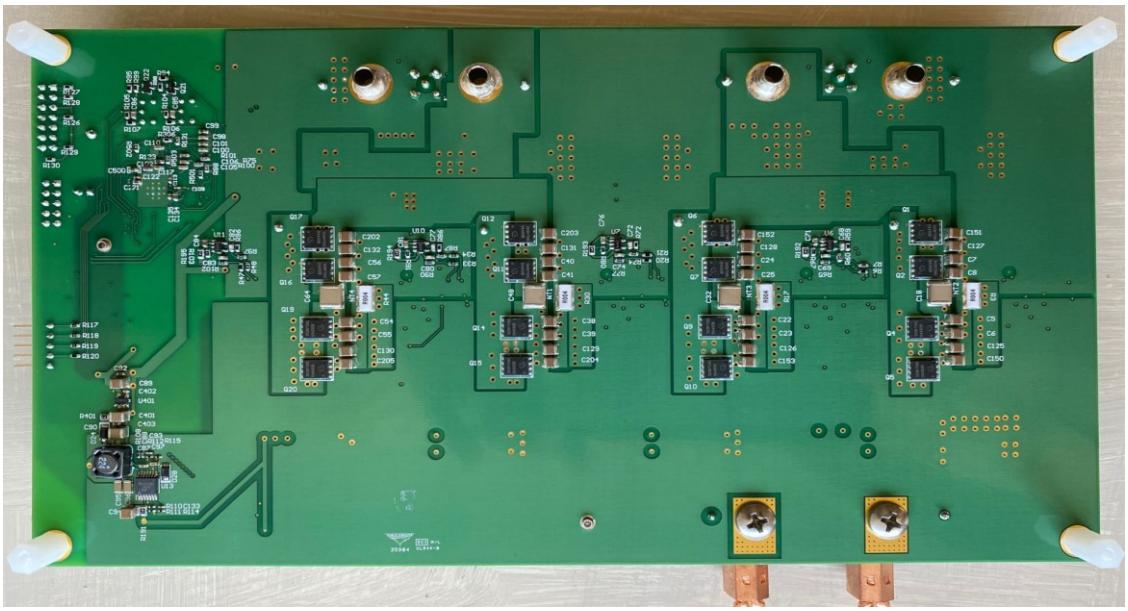
2.1 Board Photos

The photographs below show the top and bottom view of the PMP20587 board.

2.1.1 Top Side



2.1.2 Bottom Side



2.2 Prebias Start up

This test is to evaluate if the module can start up without output voltage dip and reverse current. At light load, output voltage don't discharge fast enough, the output voltage need start up from the remaining voltage of output cap.

At zero load, use SW1 or SW2 to turn on Rail1 or Rail2, then turn off the Rail1 or Rail2. Before the voltage falls to zero voltage, turn on Rail1 and Rail2 at different moment for different Prebias voltage startup. The waveforms are taken from the board shown as below.

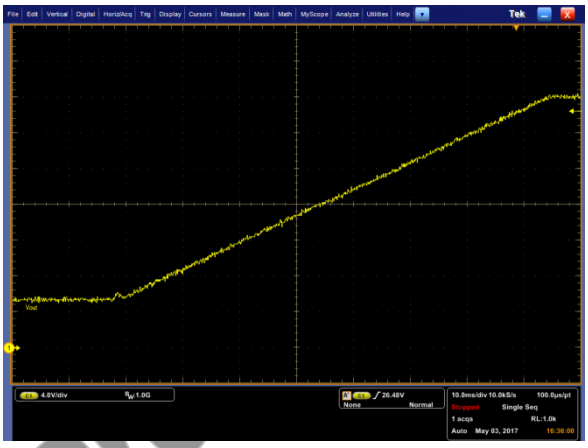


Figure 2-1: Vout =28V, Prebias voltage = 5V

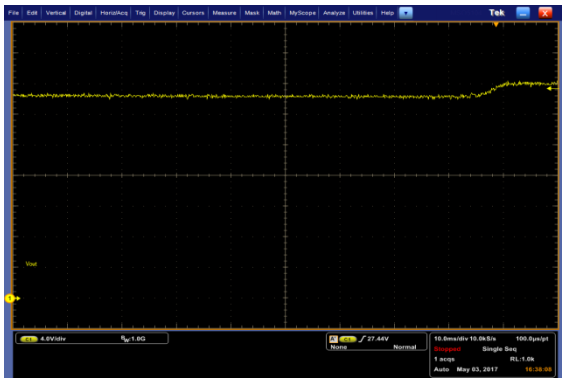


Figure 2-2: Vout =28V, Prebias voltage = 25V

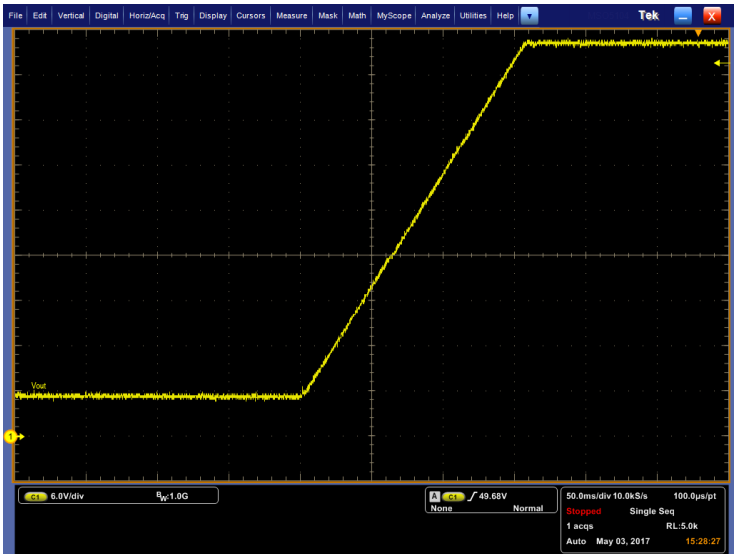


Figure 2-3: Vout =52V, Prebias voltage = 5V

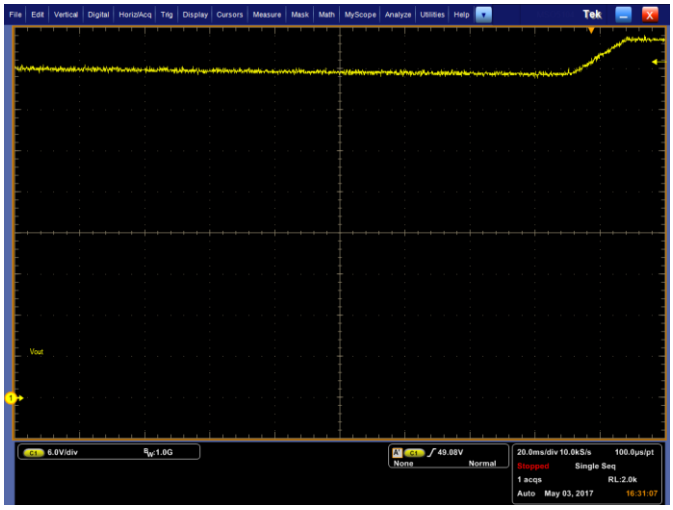


Figure 2-4: Vout =52V, Prebias voltage = 48V

2.3 Output Voltage Ripple

The output voltage ripple can be measured by using BNC cable which effectively reduces the switching noise coupling. The switching voltage ripple is measured by using short time scale and non-periodic ripple is measured by using long time scale. Each ripple should meet the requirement. TP16 and TP17 are BNC plug on the board, shown at Figure 3-1.

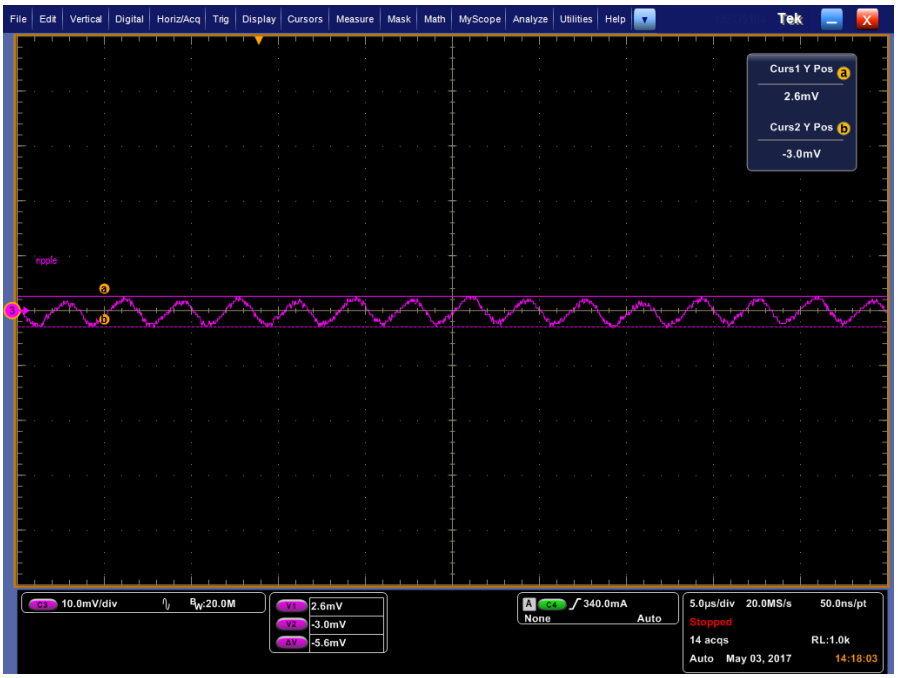


Figure 2-5 Vout =28V, Vin =36V, Iout = 0A. Vpp = 5.6mV

Figure 2-6: Vout =28V, Vin =36V, Iout = 0A. Vpp = 31mV

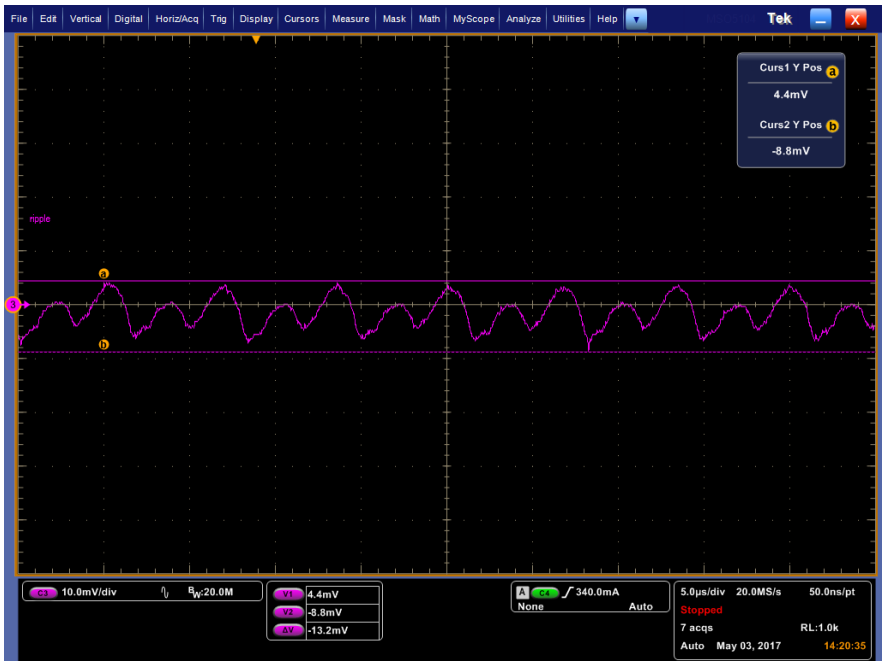


Figure 2-7: Vout =28V, Vin =36V, Iout = 0A. Vpp = 3.8mV

Figure2-8: Vout =28V, Vin =36V, Iout = 8A. Vpp = 32mV

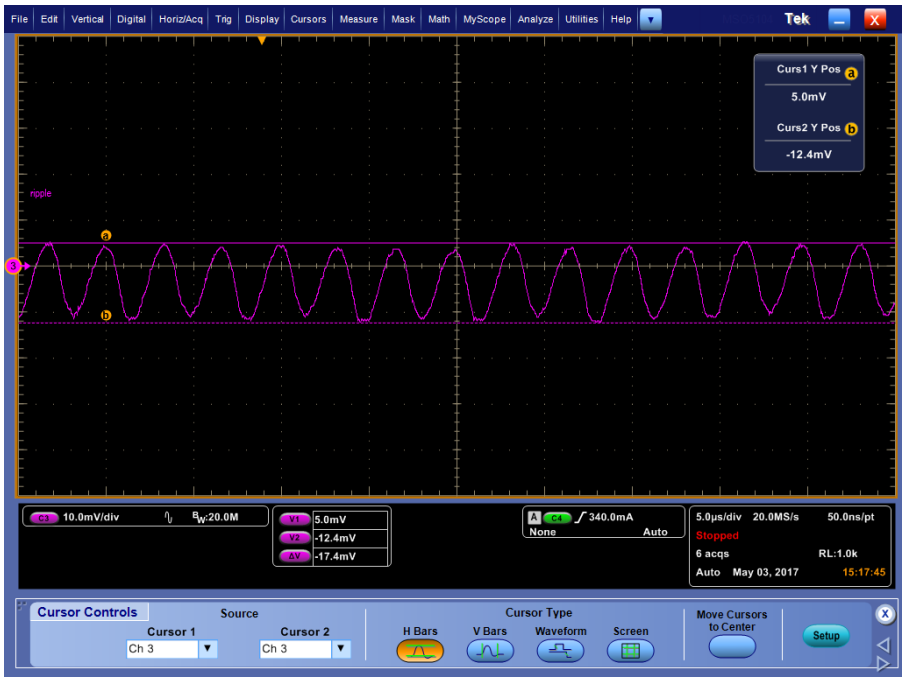


Figure 2-9: Vout =52V, Vin =60V, Iout = 0A, Vpp = 17mV

Figure 2-10: Vout =52V, Vin =60V, Iout = 0A, Vpp = 44mV

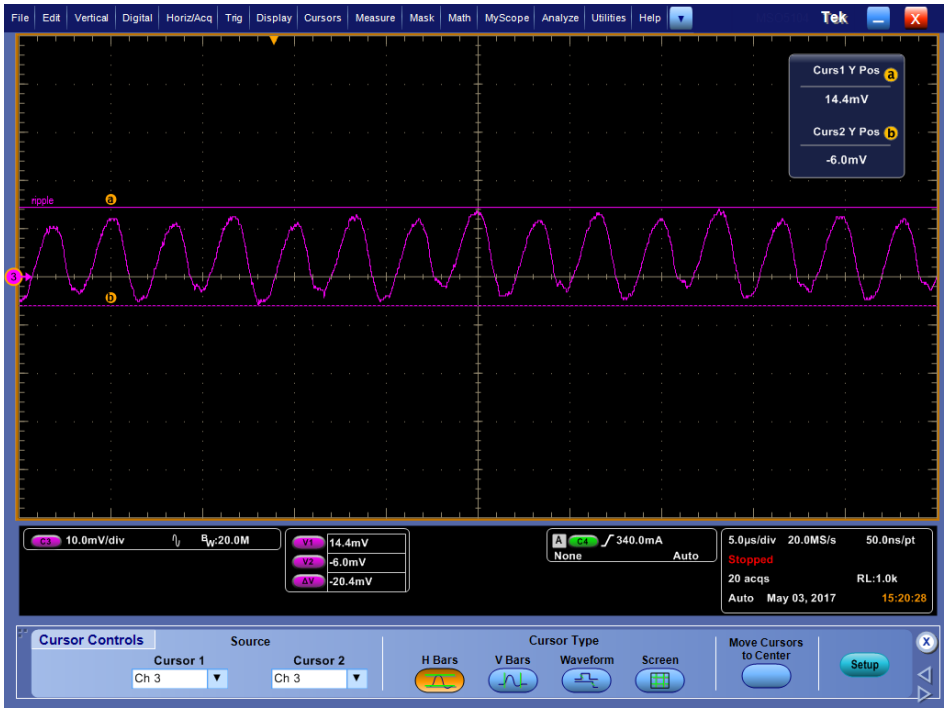


Figure 2-11: Vout =52V, Vin =60V, Iout = 4.5A, Vpp = 20mV

Figure 2-12: Vout =52V, Vin =60V, Iout = 4.5A, Vpp = 52mV

2.4 Load Transient Test

Use the same test setup as 6.2, scope the output voltage variation at different load steps. The largest step from 0.1A to full load is conducted. With non-linear control, the voltage variation is greatly reduced. The output capacitance can reduce the voltage undershoot and overshoot.

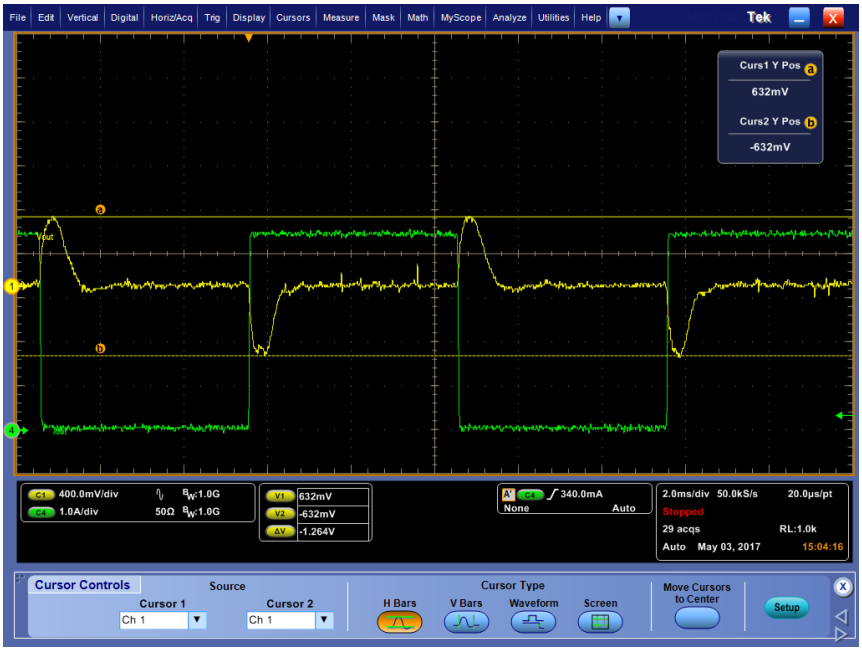


Figure 2-13**: Vout =52V, I_load = 0.1A-4.5A-0.1A. Vpp = 1.26V, Vin =48V**

Figure 2-14**: Vout =28V, I_load = 0.1A-8A-0.1A. Vpp = 1.1V, Vin =48V**

2.5 Load Regulation

The voltage changes when load current varies. There is more voltage drop when the load current is increased, the control loop should be capable to compensate the voltage drop. The ripple voltage also affects the output voltage because of digital sampling system. Use a voltage multiple to connect the output voltage test pins TP2 and TP4 for Rail1, and TP7 and TP8 for the Rail2. Record the voltage reading from the multi-meter when load current changes.

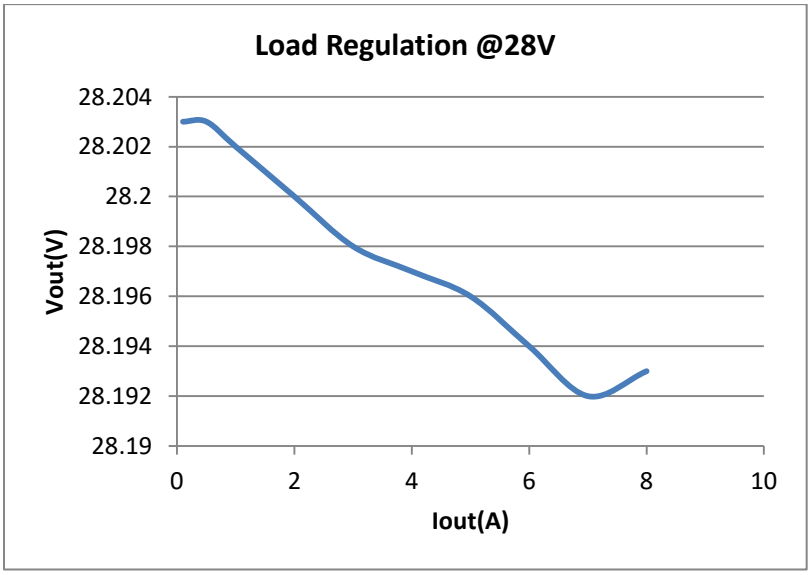


Figure 2-15: Vout = 28V. Voltage variation: 11mV

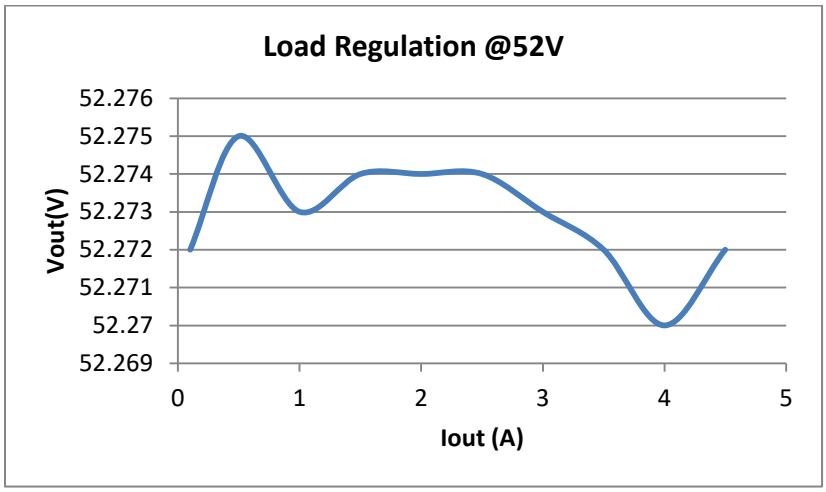


Figure 2-16: Vout = 52V. Voltage variation: 5mV

2.6 Line Regulation

The voltage changes when input voltage varies. At different input voltage, the ripple pattern is changed. This ripple voltage can change the output voltage because of digital sampling system. Use the same test setup as 6.4, vary input voltage and record the voltage reading from the multi-meter.

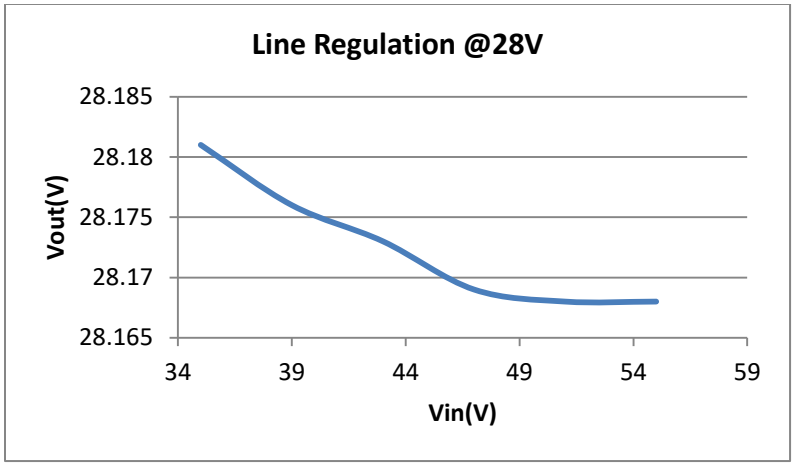


Figure 2-17: Vout = 28V, Iout =8A. Voltage variation: 12mV

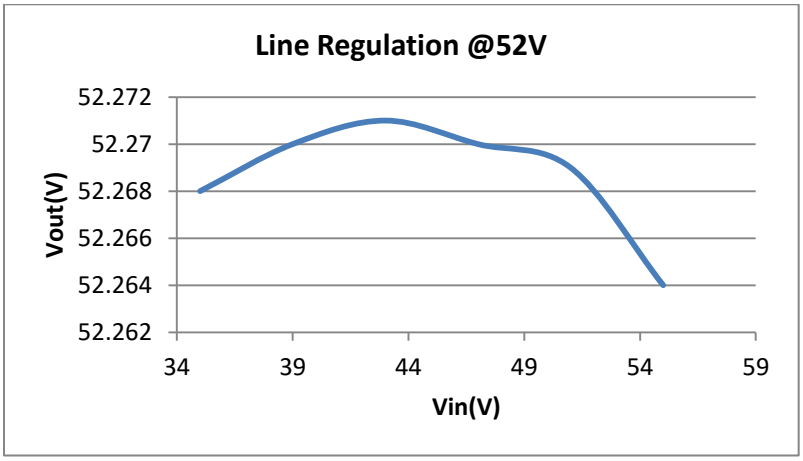


Figure 2-18: Vout = 52V, Iout =4.5A Voltage variation: 7mV

2.7 Efficiency Measurement

Power efficiency is calculated from output power divided by input power. Measure input voltage and output voltage at the points close to the terminals of the board, and input current and load current can be read from power source and electronic load if the instruments are already calibrated with good accuracy. Many parameters can affect power efficiency such as input voltage, output voltage, load current, deadtime,, power components, switching frequency. Next, power efficiency is measured as an example. Vin =48V at three different switching frequency.

Table 2-1 Efficiency Measurement

	Efficiency	100KHz	150KHz	200KHz
48Vin	28Vout @4A	0.961	0.947	0.94
	28Vout @8A	0.964	0.955	0.943
	52Vout @2.25A	0.94	0.96	0.943
	52Vout @4.5A	0.966	0.957	0.953

2.8 Bode Plot

The control loop should provide enough phase margin and gain margin for the converter so that the converter is stable at all conditions. The loop bandwidth is important to reduce output voltage disturbance at load transient. With UCD3138 unique non-linear control, the converter can meet the both criterions. Lower loop bandwidth is adopted during normal operation and higher loop bandwidth is switched during load transient to reduce output voltage overshoot or undershoot. The loop compensation is switched by internal hardware control to reduce the latency.

The Veable machine is used to measure the bode plot. To measure Rail1 bode plot, P1 is connected to VOUT1(TP2), P2 is connected RS1+ through black wire shown at Figure 6-20. GND is connected to TP4. Refer to Veable machine user guide for more information. Figure 6-21 is Bode plot when Vin =48V, Vout =52V for three different load conditions. The Bandwidth is relatively low in order to provide large phase margin and gain margin. Non-linear control is enabled to have fast load response.

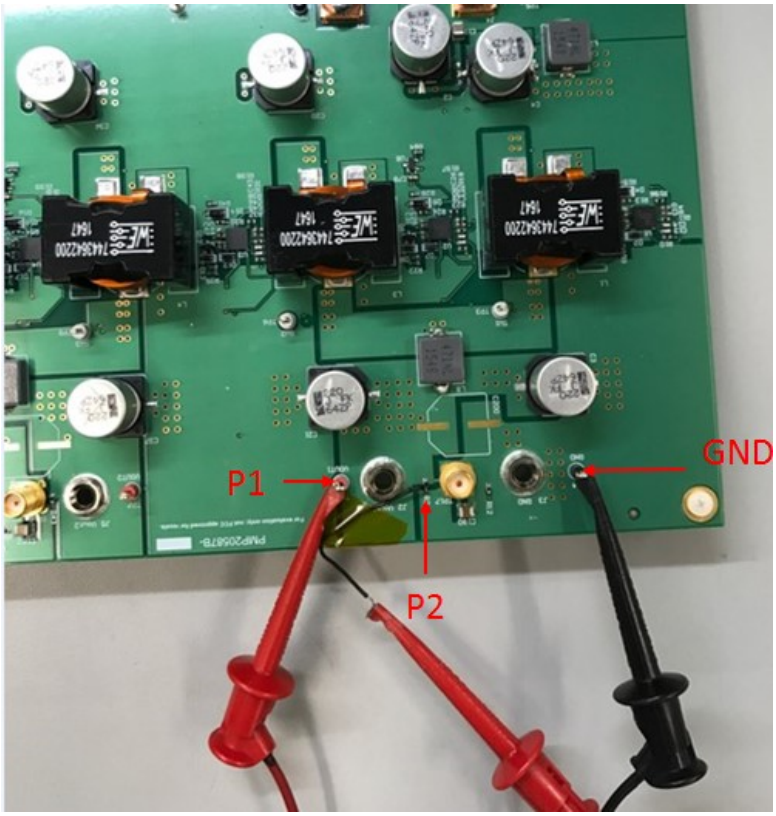


Figure 2-19 Bode Plot Measurement Setup

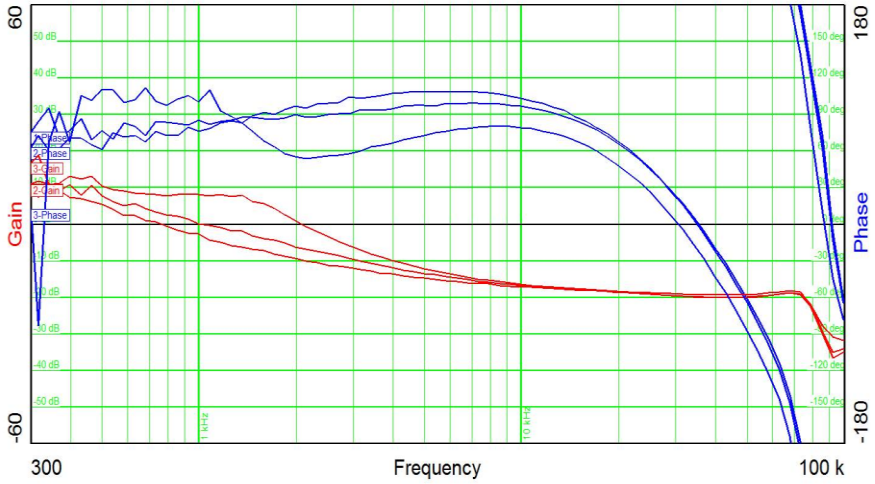


Figure 2-20 Bode Plot Measurement for 0A, Half, Full Load (Vin =48V, Vout =52V)

2.9 Input voltage Feedforward

During input voltage large transient, the converter should suppress the output voltage disturbance from feedforward control loop. The voltage control loop can't respond to input voltage change fast enough, the output voltage can overshoot to trigger over voltage protection or undershoot to trigger under voltage protection. The converter has implemented feedforward function. It detects input voltage quick change, and modifies the duty cycle quickly to reduce output voltage disturbance. The duty cycle can be updated within a couple of switching cycle after the input voltage transient is detected. The best performance can be achieved when the converter is tested in the system. The Non-linear gains of feedforward need to be optimized during the system integration.

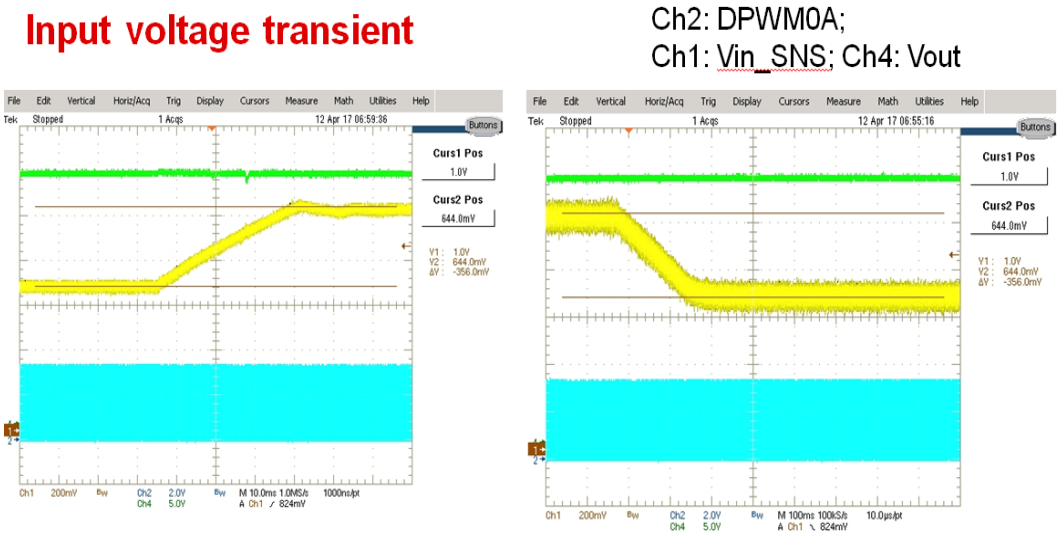


Figure 2-21 Input voltage feedforward

3 Test Results under Current Mode Control

3.1 Description

At voltage mode control, loop bandwidth is normally lower because inherited RHPZ of power stage reduces phase margin and makes the crossover frequency lower. Hence, load response is slower than current mode control. In current mode control, inductor current is taken control and two-order system is changed to a single order system. The phase is boosted by 90 degree so that control loop bandwidth is higher.

The firmware is modified to implement average current mode control for rail 1. Max output power is increased to 600W for this rail. Next, test results are provided from Section 3.2 .

3.2 Prebias Start up

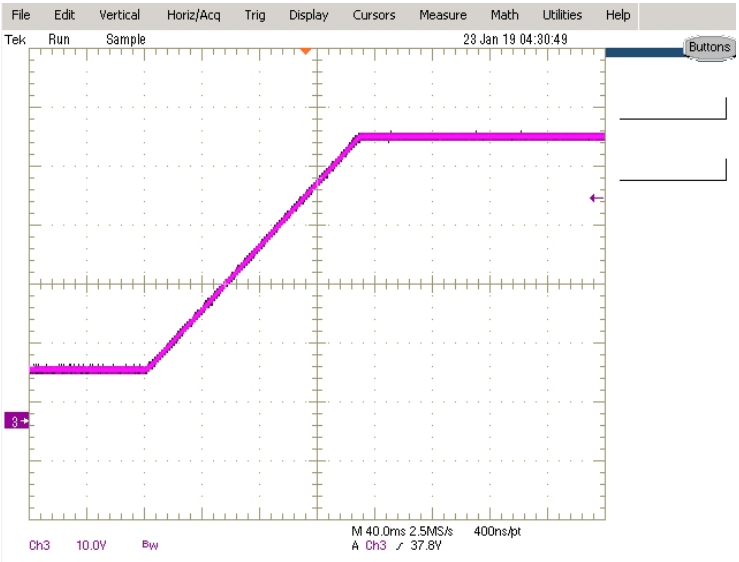


Figure 3-1 Vin =48V, Vout =48V

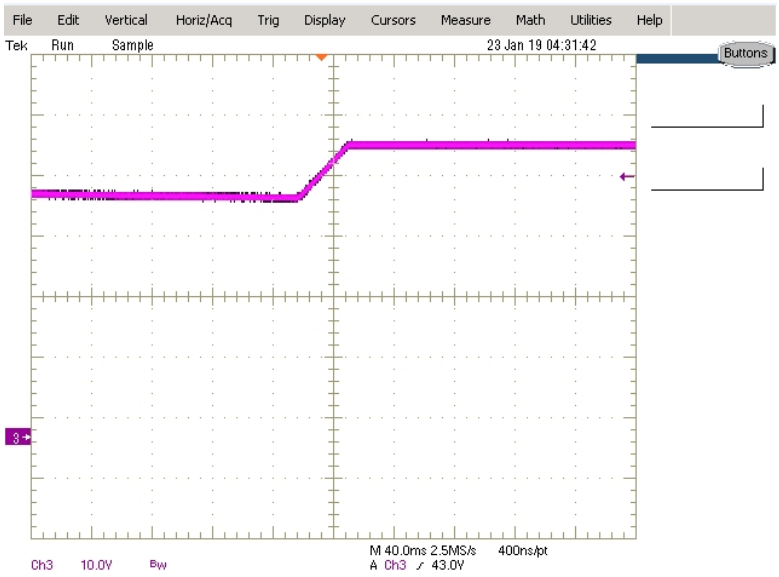


Figure 3-2 Vin =48V, Vout =48V

3.3 Voltage ripple

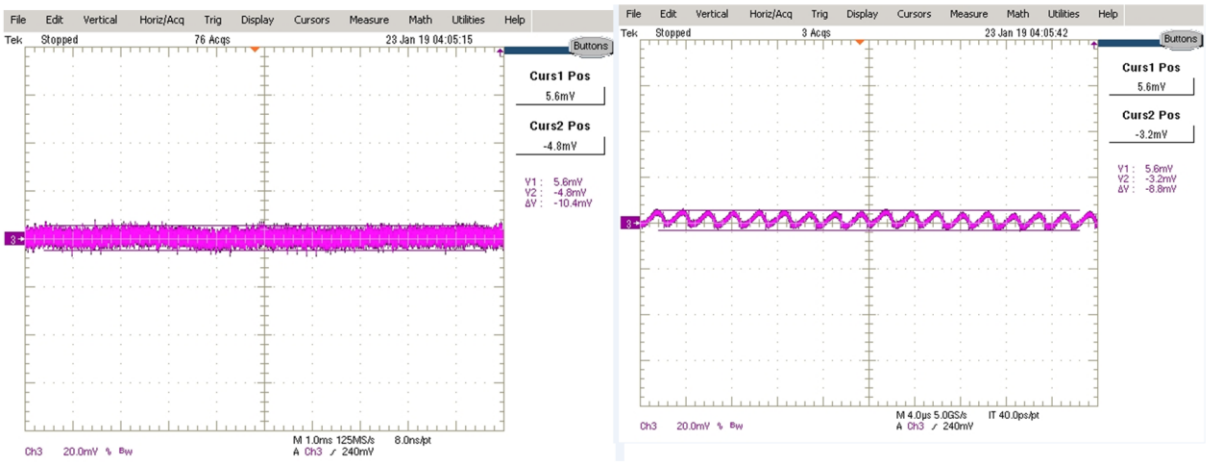


Figure 3-3 Vin =48V, Vout =48V, Iout =0A

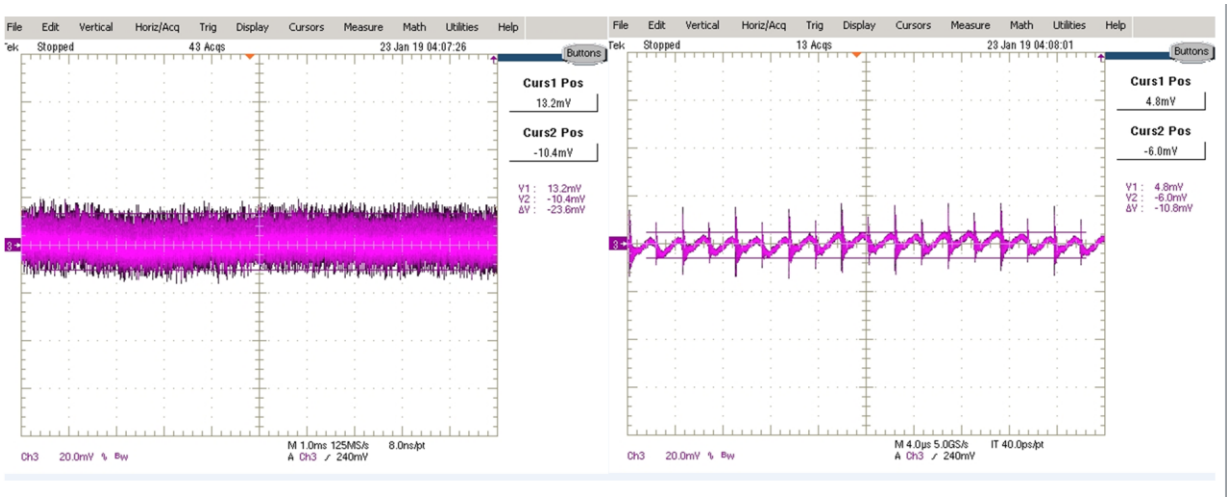


Figure 3-4 Vin =48V, Vout =48V, Iout =12A

3.4 Load transient

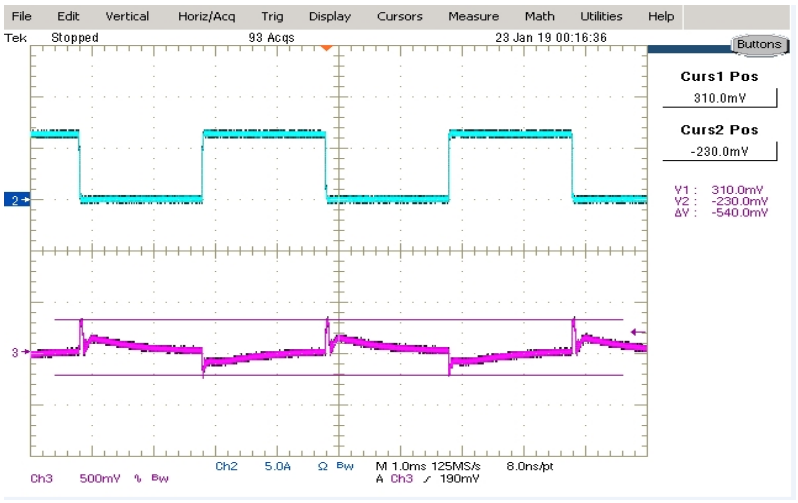


Figure 3-5 Vin =48V, Vout =48V, Iout =0 A-6.3A

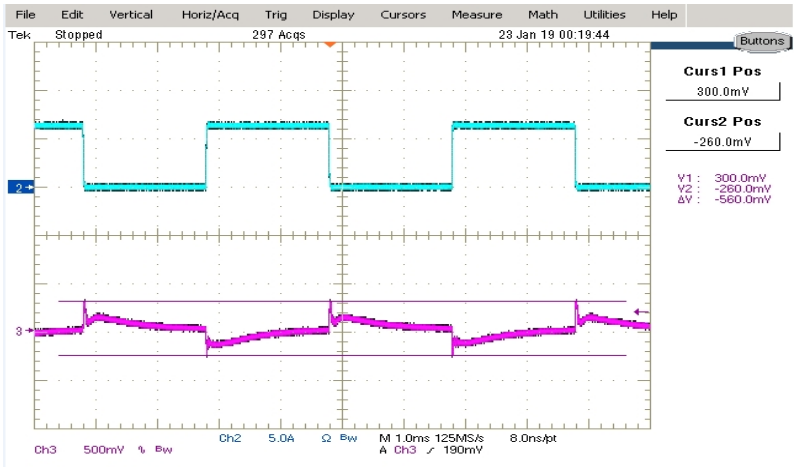


Figure 3-6 Vin =48V, Vout =48V, Iout =6.3 A-12.5A

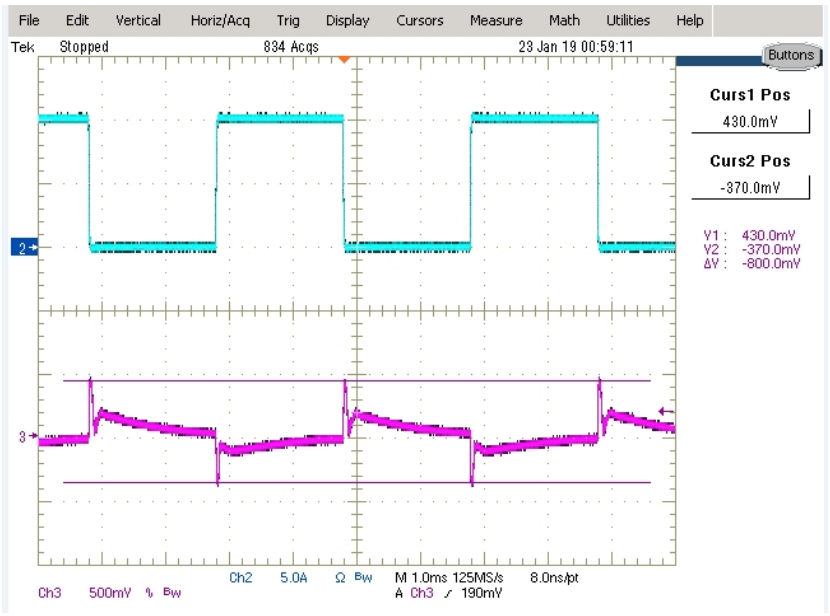


Figure 3-6 Vin =48V, Vout =30V, Iout =0A-10A

3.5 Line Transient

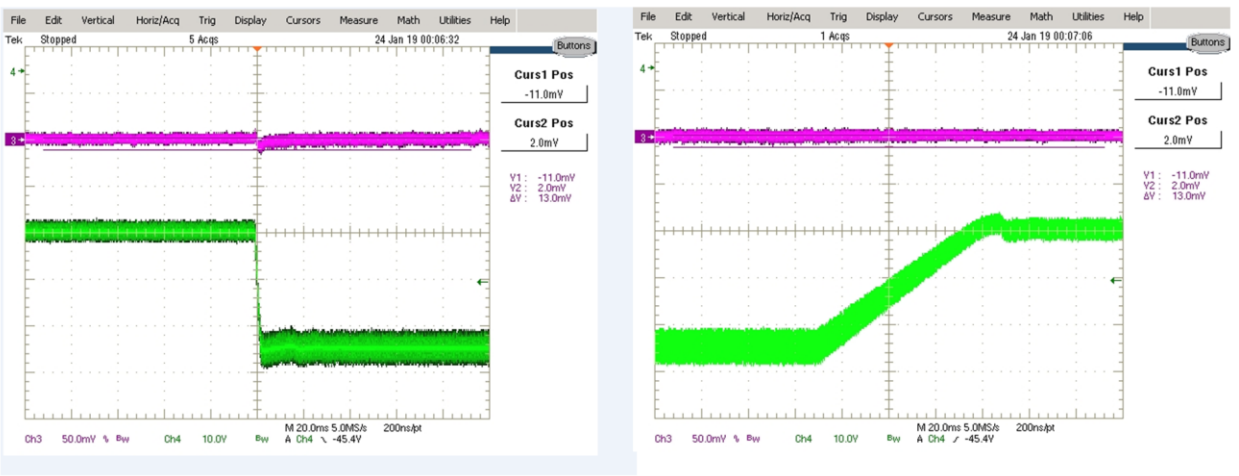


Figure 3-7 Vout =30V, Iout =0A, Vin = 37V – 60V – 37V

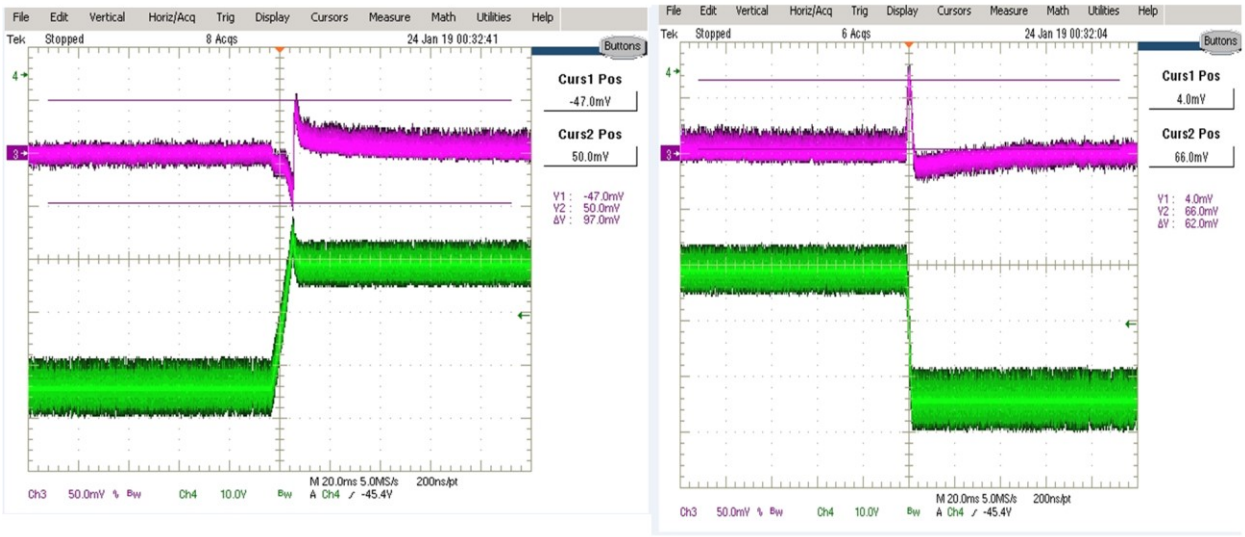


Figure 3-8 Vout =30V, Iout =12A, Vin = 37V – 60V – 37V

3.6 Bode Plot

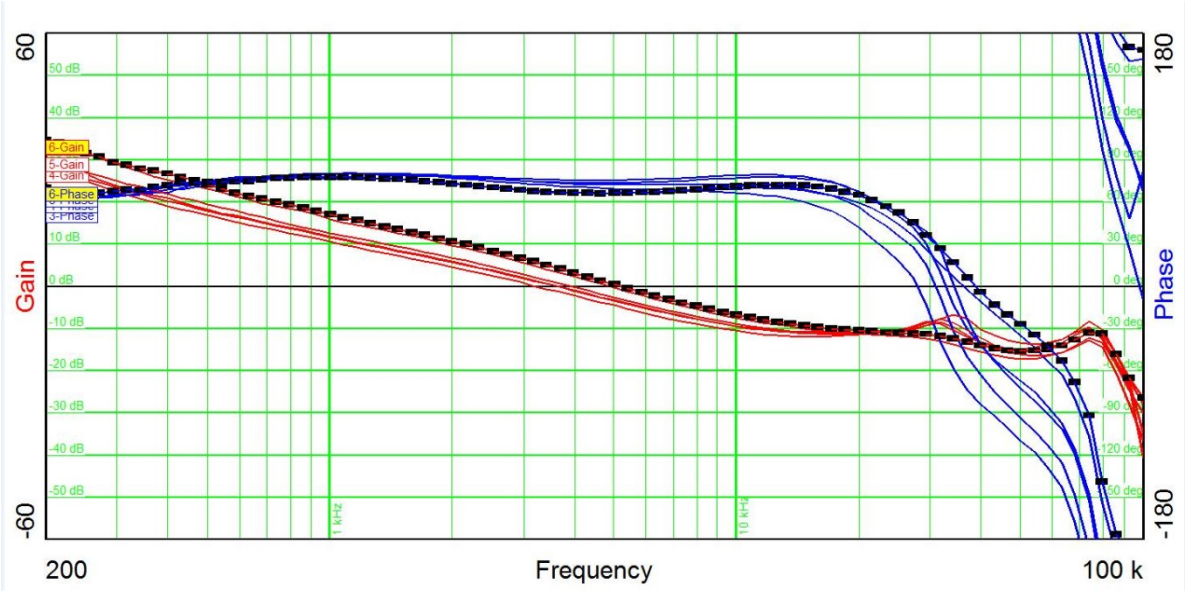


Figure 3-9 Vout =48V, Iout =0A- 13A @ Vin = 37V – 60V

3.7 Current balancing between two phases

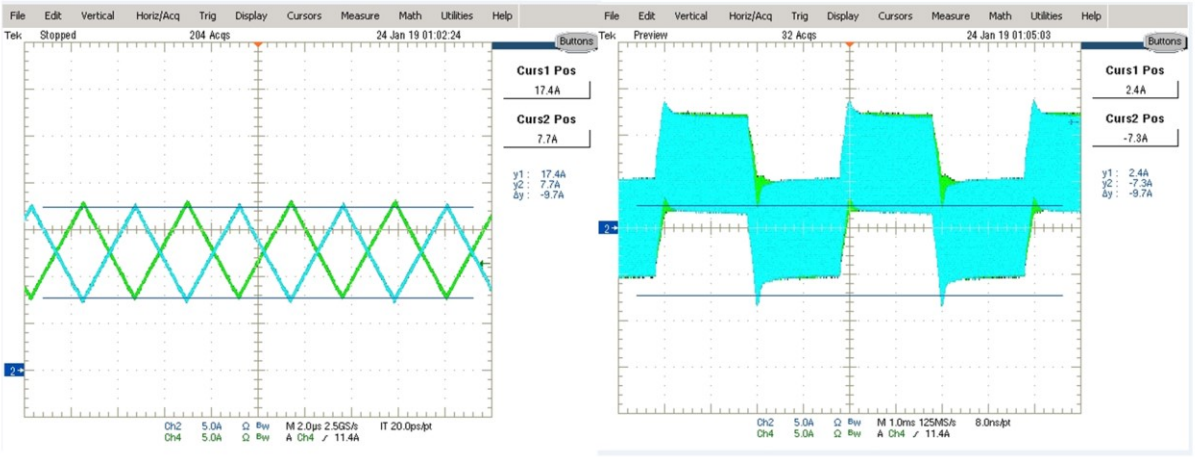


Figure 3-10 Vout =48V, Vin = 48V, Iout =0A to 6A to A

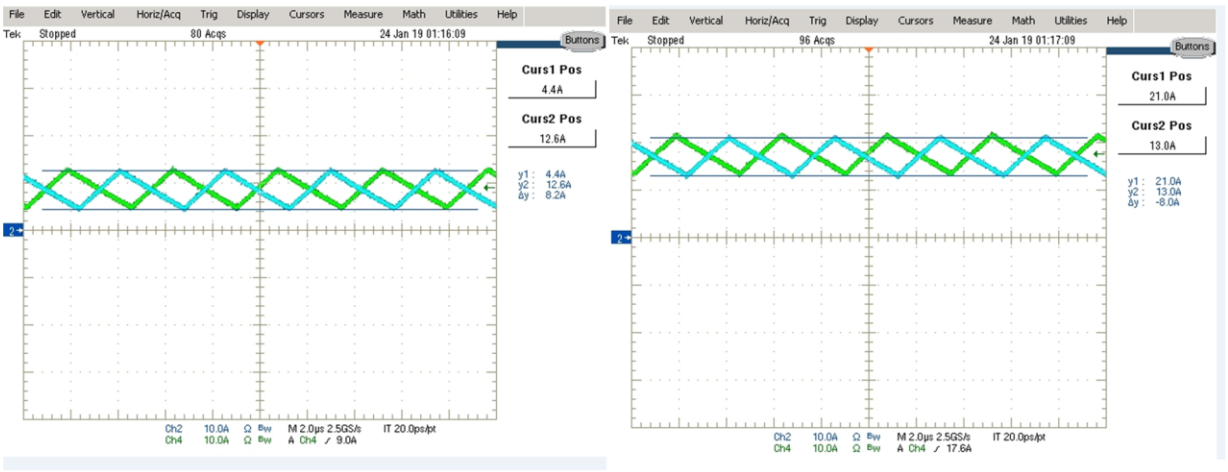


Figure 3-11 Vout =30V, Vin = 48V, Iout =10A and 20A

4 Test Results under Transition Mode Control

4.1 Description

Some components are modified so that the converter can be operated under transition mode. In transition mode operation, power MOSFETs are turned on under zero voltage, and this can significantly reduce switching losses. Higher voltage is applied on the power MOSFETs than other topologies in -48V telecom converter, ZVS operation provides great benefits over hard switching, and hence it brings higher efficiency by 2% over hard switching mode. Interleaved transition mode is implemented further to increase output power to 900W. The test results are provided from Section 4.2.

4.2 MOSFETs Temperature Comparison

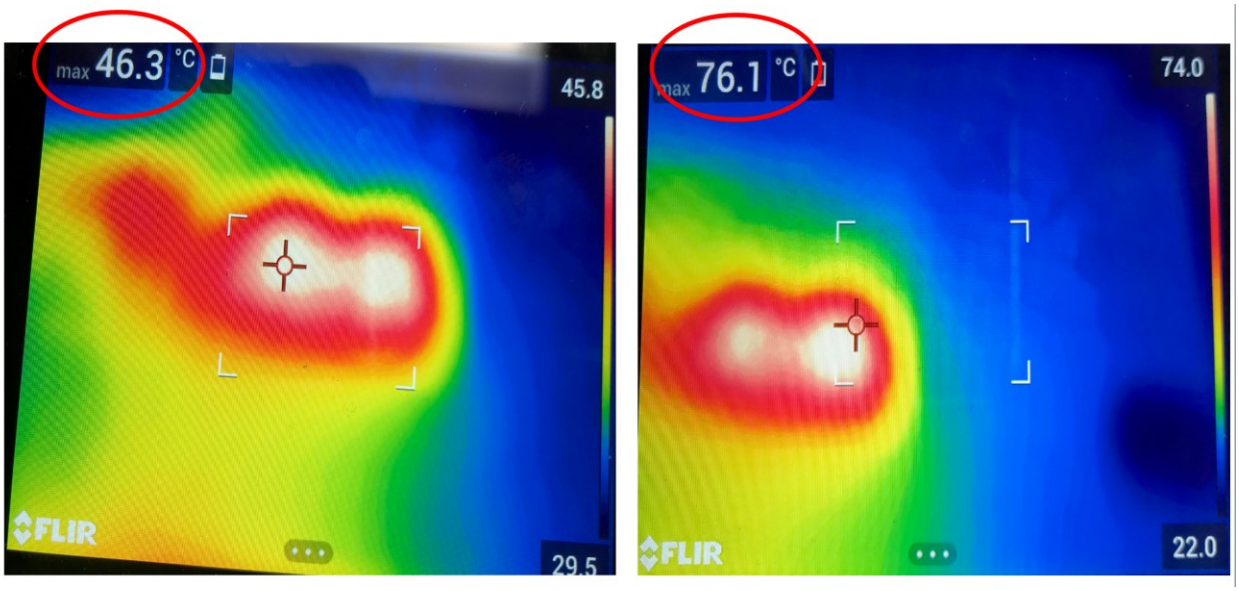


Figure 4-1 Top MOSFETs temperature @ TM IBB (Left) and @ HS IBB (Right) when Po =600W

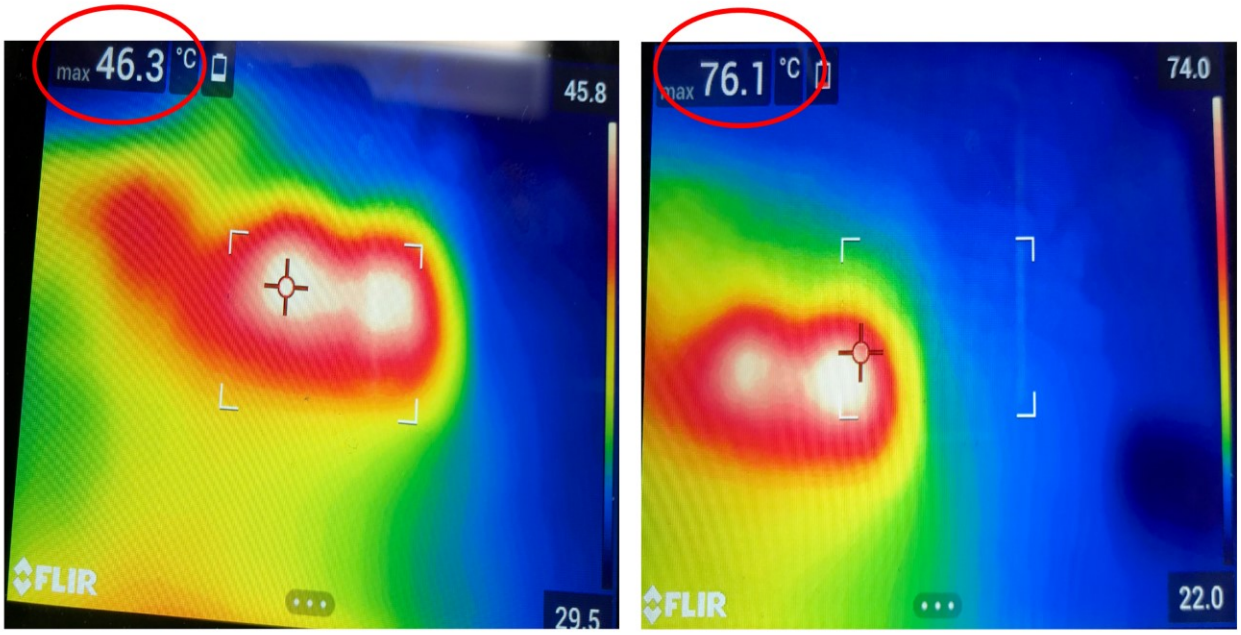


Figure 4-2 Bottom MOSFETs temperature @ TM IBB (Left) and @ HS IBB (Right) when Po =600W

4.3 Power Efficiency Comparison

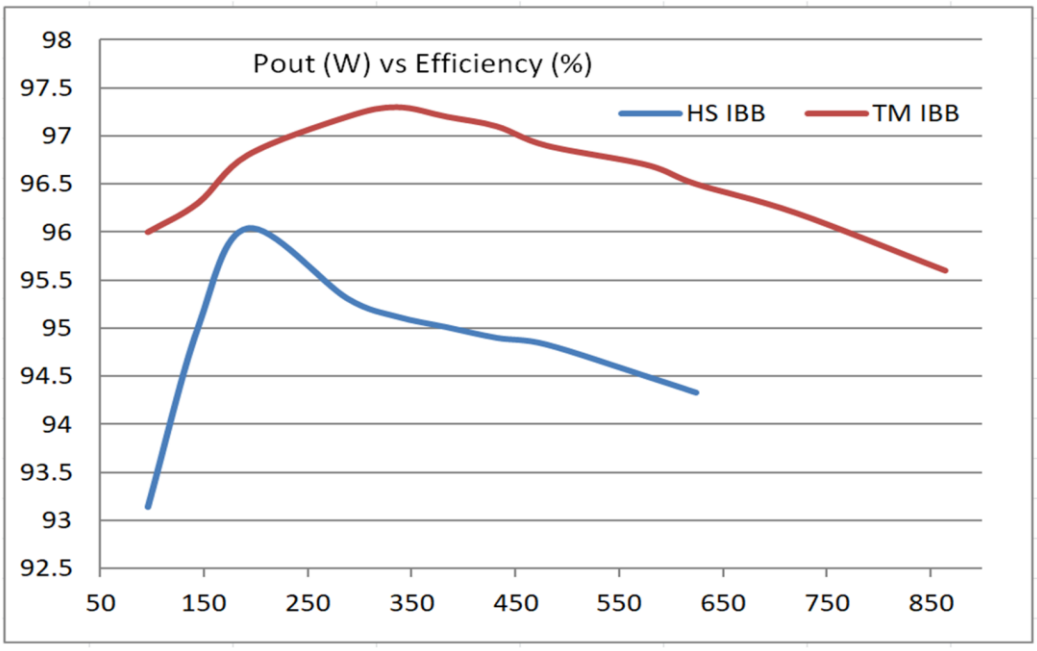


Figure 4-3. Power Efficiency of TM IBB and HS IBB

4.4 Prebias Start up

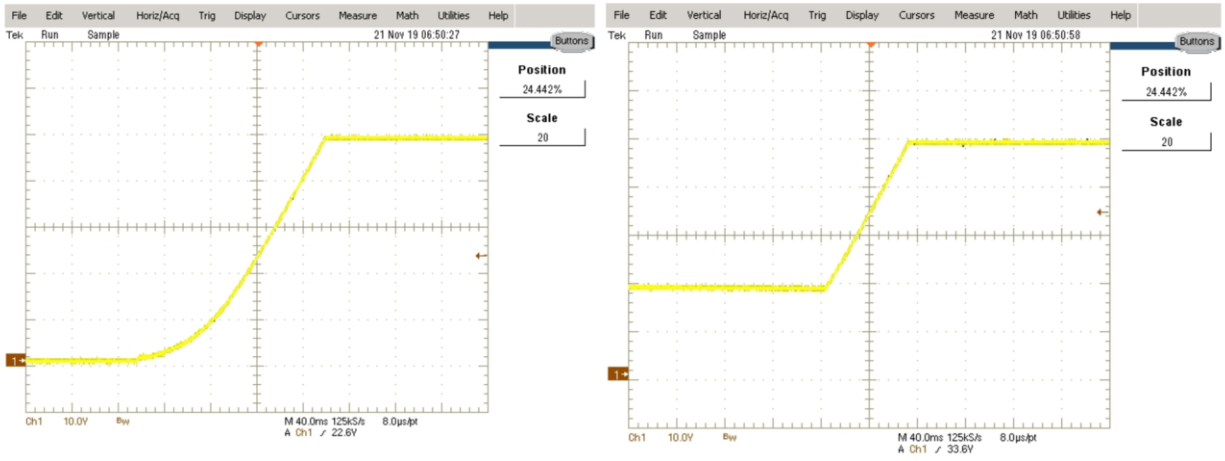


Figure 4-4 Vin =48V, Vout =48V, Iout =0A

4.5 Load Transient

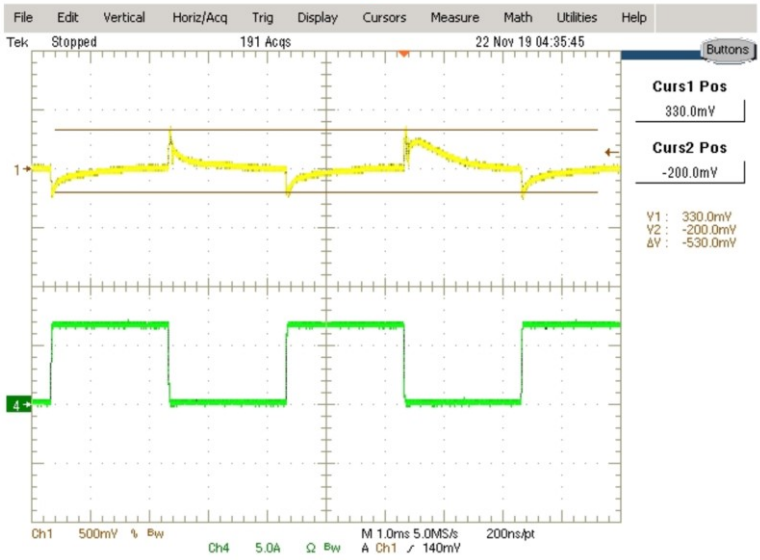


Figure 4-5 Vin =48V, Vout =48V, Iout =0A-6.5A-0A

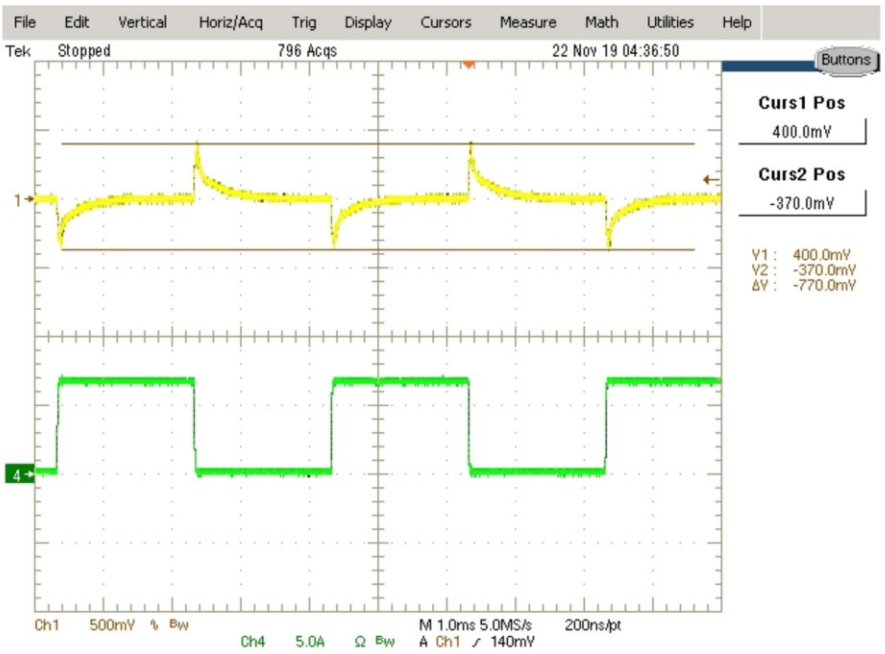


Figure 4-6 Vin =48V, Vout =48V, Iout =6.5A-13A-6.5A

4.6 Line Transient

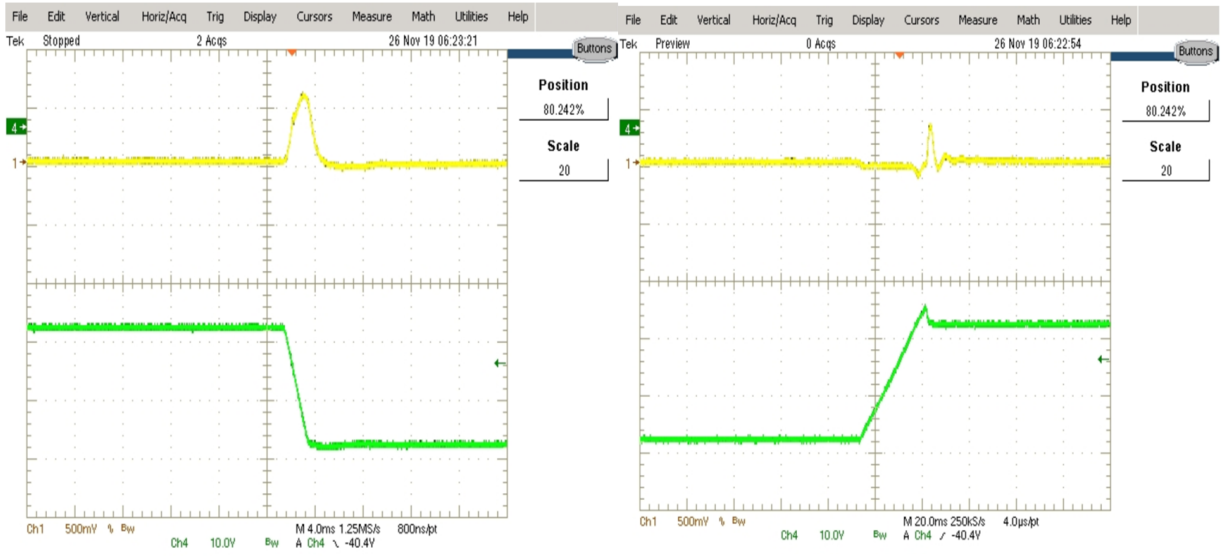


Figure 4-7 Vout =48V, Iout =0A, Vin =35V-60V-35V

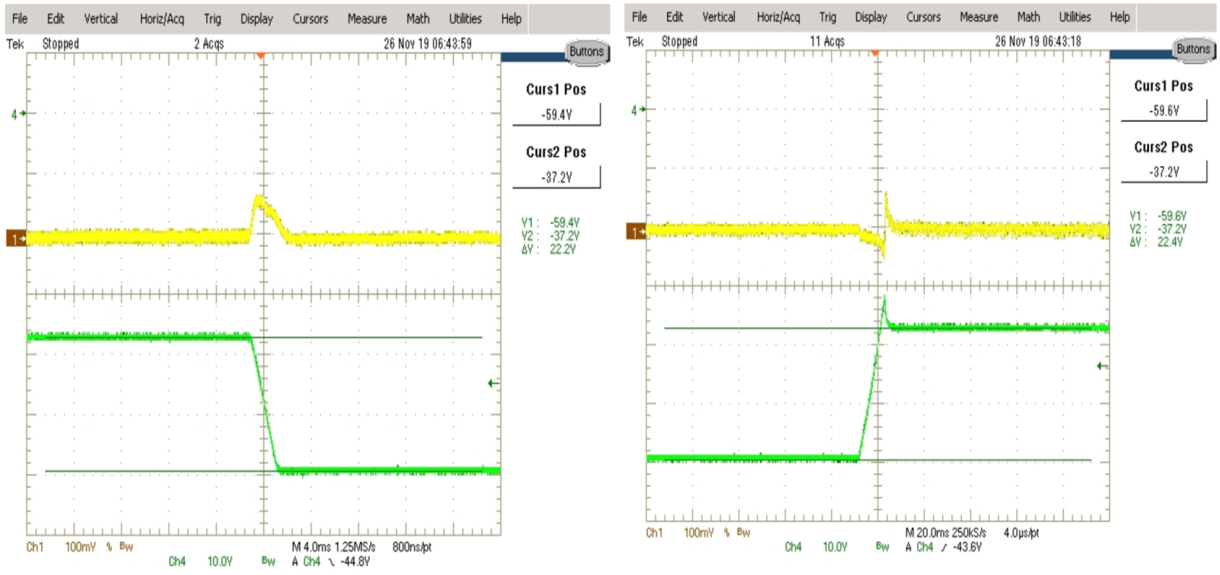


Figure 4-8 Vout =48V, Iout =9A, Vin =35V-60V-35V

4.7 Voltage Ripple

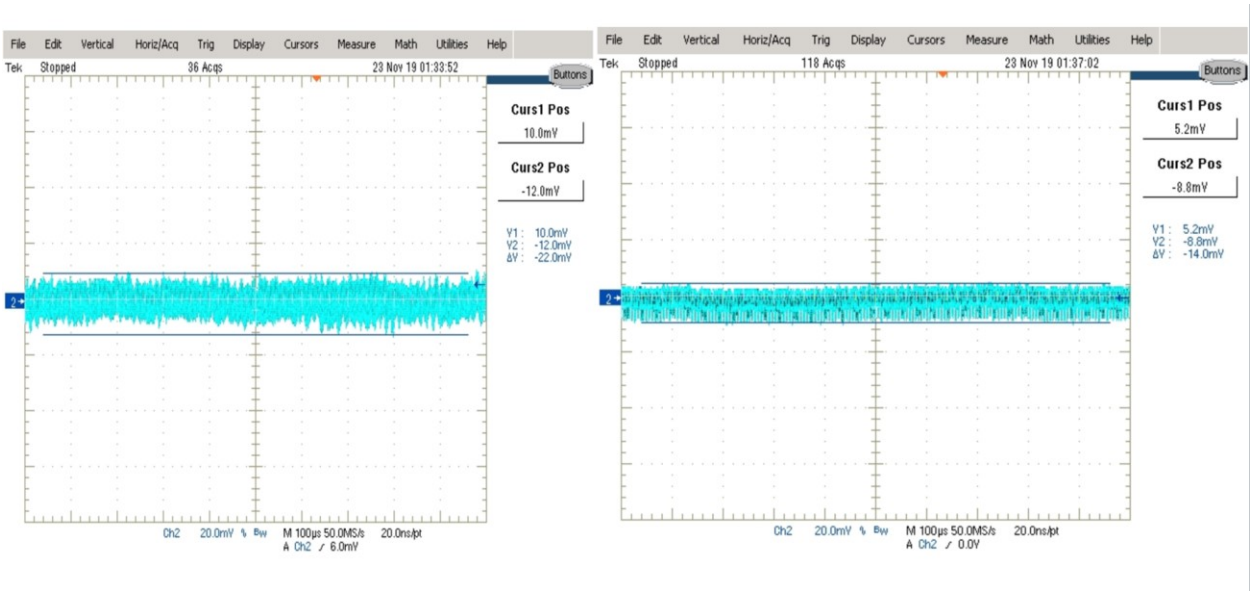


Figure 4-9 Vin =48V, Vout =48V, Iout =0A and 9A

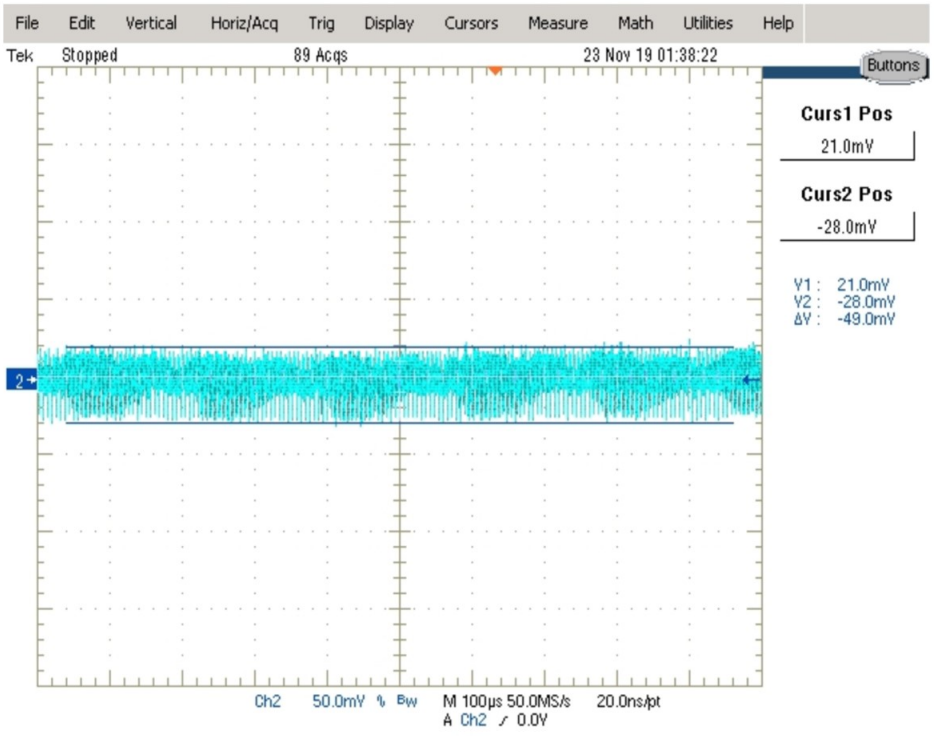


Figure 4-10 Vin =48V, Vout =48V, Iout =18A

4.8 Short Circuit Protection

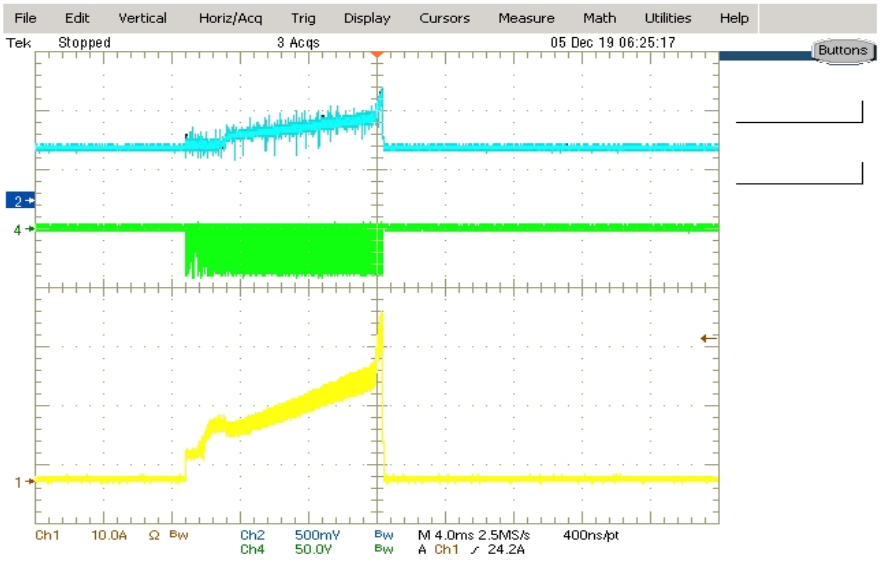


Figure 4-11 Short Circuit Hiccup

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