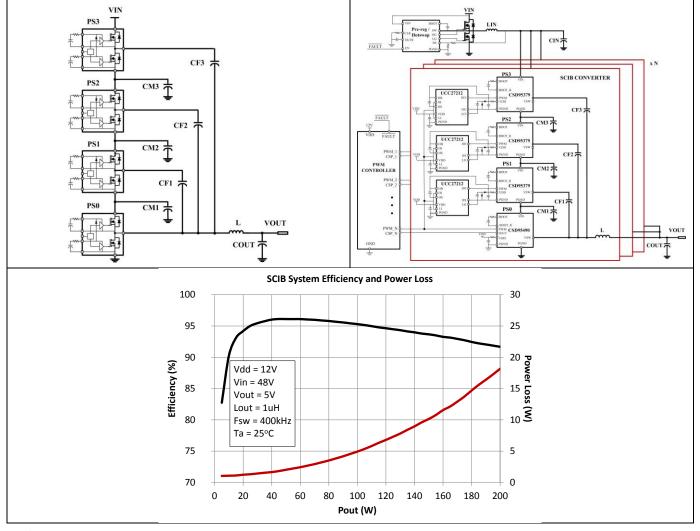
Test Report: PMP22510

Switched Capacitor Integrated Buck (SCIB) Power Converter Reference Design



Description

The SCIB power converter is a highly optimized design for use in a high-power, high-density single output power converter, operating from a wide-range 40-V to 60-V input rail to produce a 8.0-V, 5.0-V, 3.3-V or 1.8-V rail up to 40A of load current each phase. It is suitable for POL DC-DC converter, memory and graphic cards, data center and server power, high-current POL for network communications and other high-voltage input applications. The reference design, PMP22510, integrates the CSD95490Q5MC and CSD95379Q3M NexFET power MOSFET stages, the UCC27212 driver ICs, capacitors and inductors to complete the power stage switching function. This combination produces high-current, high-efficiency and high-speed switching capability in a small 23-mm x 23-mm outline PCB layout. It is also compatible with multiphase buck controllers, such as TPS53667RTAT. In addition, a front-end pre-regulator / hotswap controller, such as LM5069, is used to generate VIN of SCIB with a controlled ramp-up slew rate for startup.



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements (One Phase)

| | PARAMETER | TEST CONDICTIONS | MIN | TYP | MAX | UNITS |
|-------------------------|-----------------------|-----------------------|-----|------|------|-------|
| INPUT CHARACTERISTICS | | | | | | |
| Vin | Voltage range | | 40 | 48 | 60 | V |
| lin,max | Maximum input current | Vin = 40V, lout = 40A | | 5 | | Α |
| | No load input current | Vin = 48V, lout = 0A | | 8 | | mA |
| OUTPUT CHARACTERISTICS | | | | | | |
| Vout | Output voltage | | 1.0 | 5.0 | 8.0 | V |
| lout | Output load current | | 0 | | 40 | Α |
| Vripple | Output voltage ripple | Vin = 48V, lout = 40A | | 10 | | mVpp |
| SYSTEMS CHARACTERISTICS | | | | | | |
| Fsw | Switching frequency | Vin = 48V | 300 | 400 | 1000 | kHz |
| | Peak efficiency | Vin = 48V, lout = 12A | | 96.2 | | % |
| | Full-load efficiency | Vin = 48V, lout = 40A | | 91.7 | | % |
| Та | Operating temperature | | | 25 | | °C |

1.2 Considerations*

1.2.1 Principle of Operation

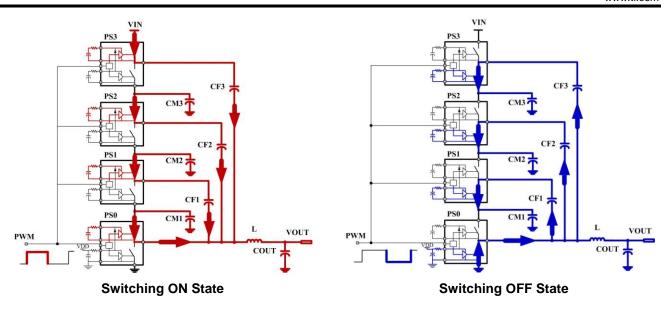
There are two phases of SCIB converter in this design. Each phase is controlled by the multiphase buck controller with one of PWM signals. When PWM signal is high, the low-side FETs of power stages PS0-PS3 are turned OFF and high-side FETs of power stages PS0-PS3 are turned ON, with a dead time in between; when PWM signal is low, the high-side FETs of PS0-PS3 are turned OFF and low-side FETs of PS0-PS3 are turned ON, with a dead time in between.

External resistors are placed in series with bootstrap capacitors and decoupling capacitors of PS1-PS3 to generate ON delay of both high-side FETs and low-side FETs of PS1-PS3. This yields zero voltage switching of PS1-PS3 and adds more protection from shoot through between PS1-PS3 and PS0.

Due to the delay of level shifter, additional RCD delay circuits can be added to separate the PWM signals of PS1-PS3 and PS0.

The switching operation modes with PWM control are shown as below.

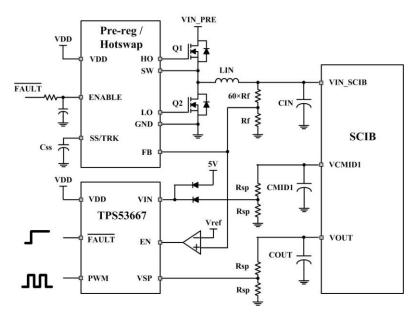




1.2.2 Pre-regulator / Hotswap

A front-end pre-regulator or hotswap is placed between the VIN Bus and the input of SCIB to control the SCIB's VIN ramp-up slew rate. It can use a buck regulator with 100% duty cycle or an alternative hotswap controller, such as LM5069. A controlled VIN ramp-up protects the PS3 from voltage break down during startup and avoids surge current due to capacitor hard charge. In normal operation, the pre-regulator works as a highly efficient low voltage drop regulator. During startup, its Vout ramps up at a predetermined slew rate.

The simplified schematic of SCIB with pre-regulator / hotswap is shown as below.



Simplified Schematic of SCIB with Pre-regulator / Hotswap

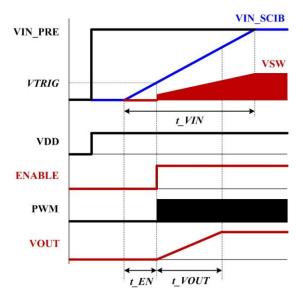


1.2.3 Startup Sequence

When VIN is high, VDD of controller is high; then PWM and V3R3 are active with a delay. VINBUS rampup starts with enable on and is controlled by a front-end buck pre-regulator. Hence, the startup sequence is:

- VIN_PRE of pre-regulator / hotswap and VDD of controller are high;
- When ENABLE of pre-regulator / hotswap is actively triggered, VIN_SCIB begins to ramp up;
- When VIN_SCIB exceeds VIN_UVLO (12V typically), ENABLE of controller is triggered;
- After ENABLE voltage goes high, PWM is generated and VOUT begins to ramp up;
- VSW rises following VIN_SCIB / 4
- VOUT stops to ramp up when reaching VBOOT.

In the feed forward circuit, forward voltage needs to be connected to VCB instead of VIN. The startup sequence of SCIB with TPS53667 controller is shown as below.



Startup Sequence of SCIB with TPS53667 Buck Controller

1.2.4 Minimum OFF Time during Startup

At the beginning of startup, the output voltage is zero; hence the compensator saturates until the output voltage rises to the desired value. The converter continues with ON for a very long period and OFF for a very short period.

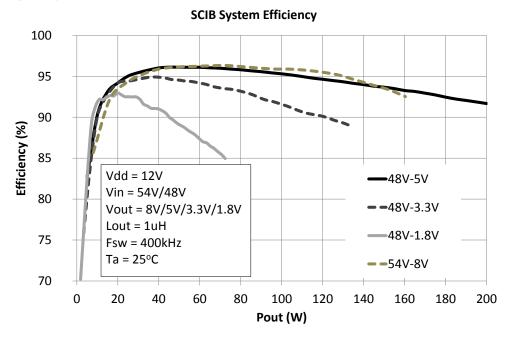
Under no load condition, the minimum OFF time required to start the converter depends on the hard charge energy of the effective capacitor and the loss energy unrelated to the hard charge. The effective capacitor, including flying capacitor and output capacitor, is only charged during OFF (1-D) period. Hence, one needs to ensure that the charge energy of the effective capacitor is larger than the loss energy, including switching loss, gate loss and leaking loss, during a minimum OFF time. A typical minimum OFF time for startup under no load condition is 200ns.

If there is a certain load, the charge energy of the effective capacitor needs to be larger than the sum of loss energy and load energy during a minimum OFF time.



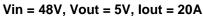
2 Testing and Results

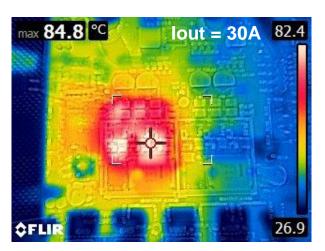
2.1 Efficiency Graphs



2.2 Thermal Images



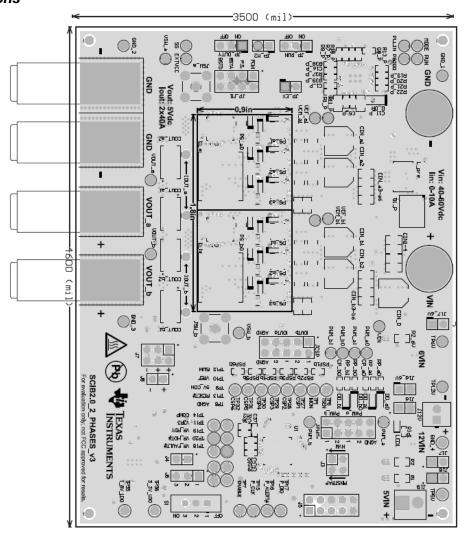


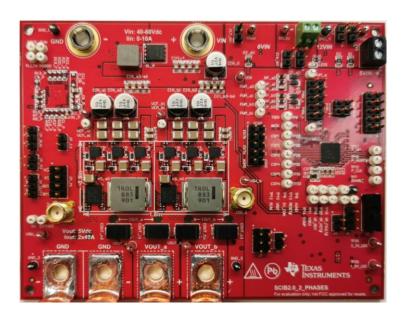


Vin = 48V, Vout = 5V, Iout = 30A



2.3 Dimensions



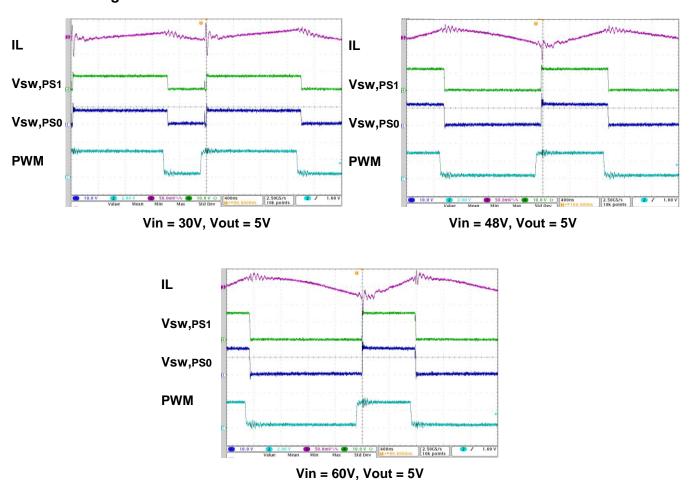






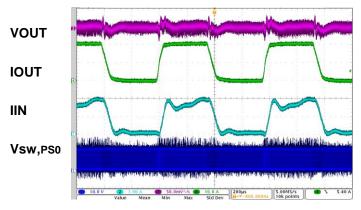
3 Waveforms

3.1 Switching*



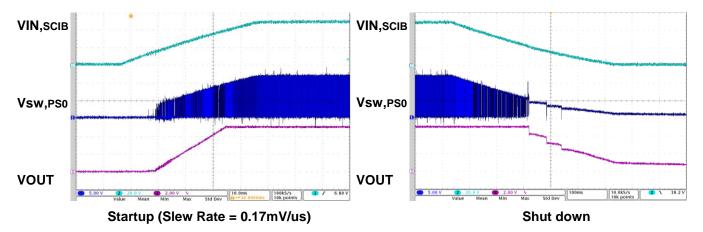


3.2 Load Transients*



Load transient (0.3A/ms, 1.3kHz)

3.3 Start-up Sequence*



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