Test Report: PMP30785
Automotive Multi-Rail Power Supply for Driver Monitoring System Reference Design

Description

This reference design depicts the performance of an automotive power supply for a driving monitoring system for the electronic control unit (ECU).

The reference design includes TI´s power portfolio with following devices:

- LM63625-Q1 – Sync. Buck Controller supplying 3.3 V @ 2.2 A rail
- TPS22918-Q1 – Load Switch for disconnect of SoC, DDR3, Des
- TPS62813-Q1 – Sync. Buck Converter supplying 1.03 V @ 3 A
- TPS62811-Q1 – Sync. Buck Converter supplying 1.8 A @ 0.5 A
- TPS22918-Q1 – Load Switch for disconnect of SoC
- TPS62812-Q1 – Sync. Buck Converter supplying 1.5 V @ 1.2 A
- TPS51200A-Q1 – Termination
- TLV733P-Q1 – LDO supplying 1.2 V @ 0.1 A
- LM2775-Q1 – Switch Cap Boost supplying 5 V @ 43 mA
- TPS1H200A-Q1 – Smart High-Side Switch to connect to CAM- Board

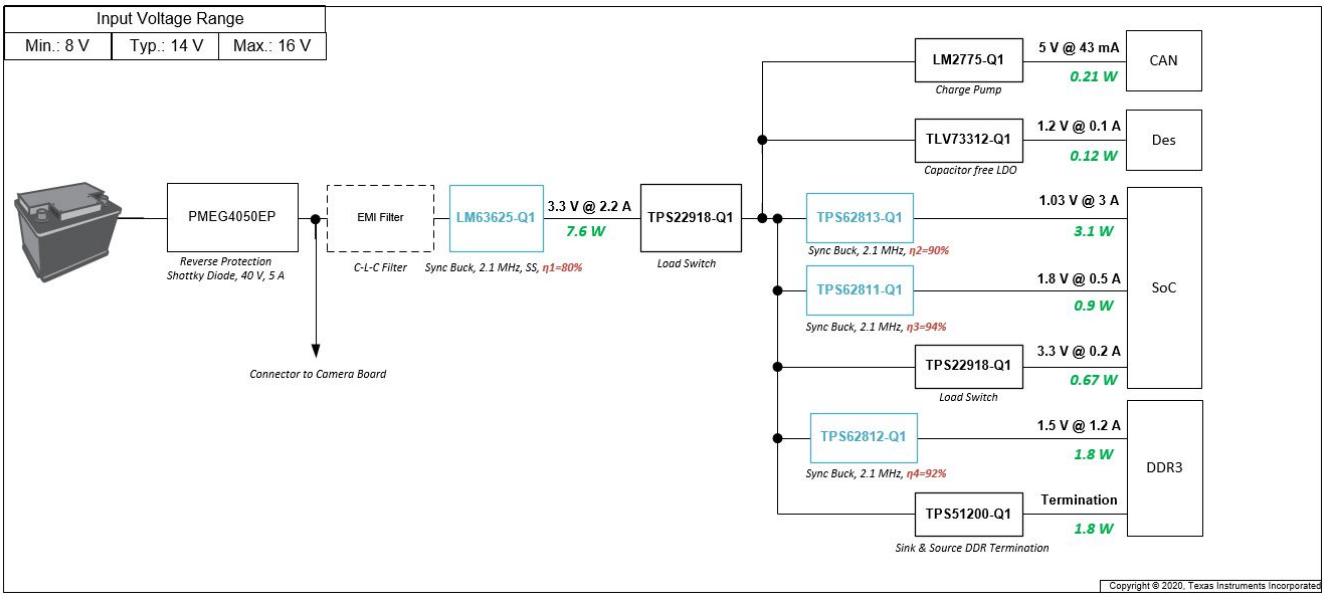

Figure 1: Block diagram PMP30785

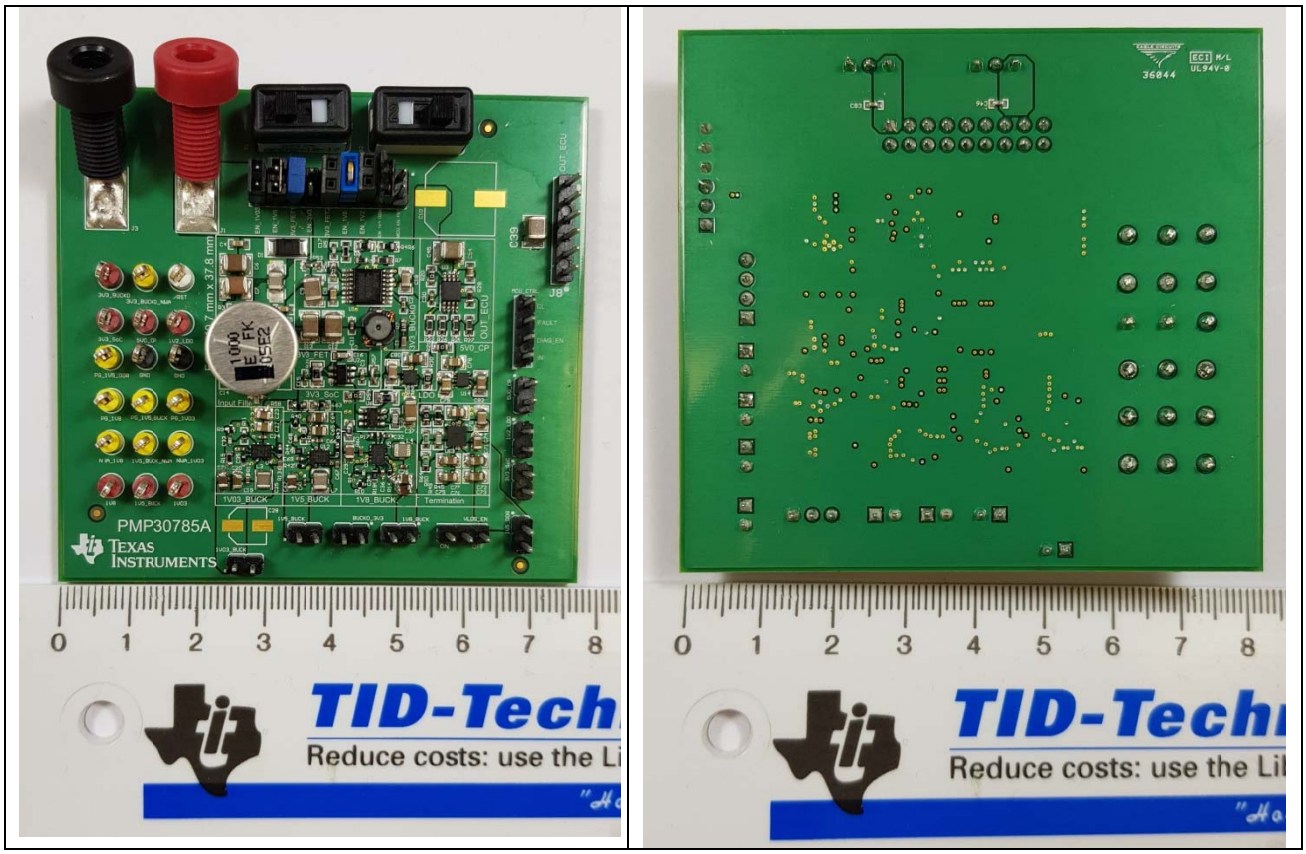

Figure 2: Top and Bottom View of the Board

1 Test Prerequisites

1.1 Block Diagram

1.2 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range:	8 V < Vin < 16 V @ Vin(typ) = 14 V
Output Rails:	
3V3_BUCK0	3.3 V @ 2.2 A
1V8_BUCK	1.8 V @ 0.5 A
1V03_BUCK	1.03 V @ 3.0 A
1V5_BUCK	1.5 V @ 1.2 A

1V2_LDO	1.2 V @ 100 mA
5V0_CP	5.0 V @ 43 mA
3V3_FET	Load Switch on 3V3_BUCK0
3V3_SoC	Load Switch on 3V3_FET
OUT_ECU	Load Switch to CAM- Board
1V5_DDR	Termination

1.3 Required Equipment

- Power Supply: EA-PS-3032-10B
- Ohmic Load
- Frequency Response Analyzer: Venable Model 3120
- Digital Amperemeter
- Oscilloscope LeCroy WaveSurfer104X

1.4 Considerations*

Measurements in Waveforms were performed on the switched mode power supplies namely 3V3_BUCK0, 1V8_BUCK, 1V03_BUCK, and 1V5_BUCK.

---------- *NOTE* ----------

The bode plot analysis shows the 1V8_BUCK, 1V03_BUCK and 1V5_BUCK rails result in an inflated crossover frequency at a phase margin of less than 50 °. For reliable operation it is highly recommended to add an additional 22 uF / 0805 / 6.3 V ceramic capacitor in parallel to the output capacitors of each of these rails.

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2 Testing and Results

2.1 Efficiency Graphs

The efficiency graph depicts the efficiency of each power rail. During each measurement the other rails were disabled, except the pre-regulator 3V3_BUCK0.

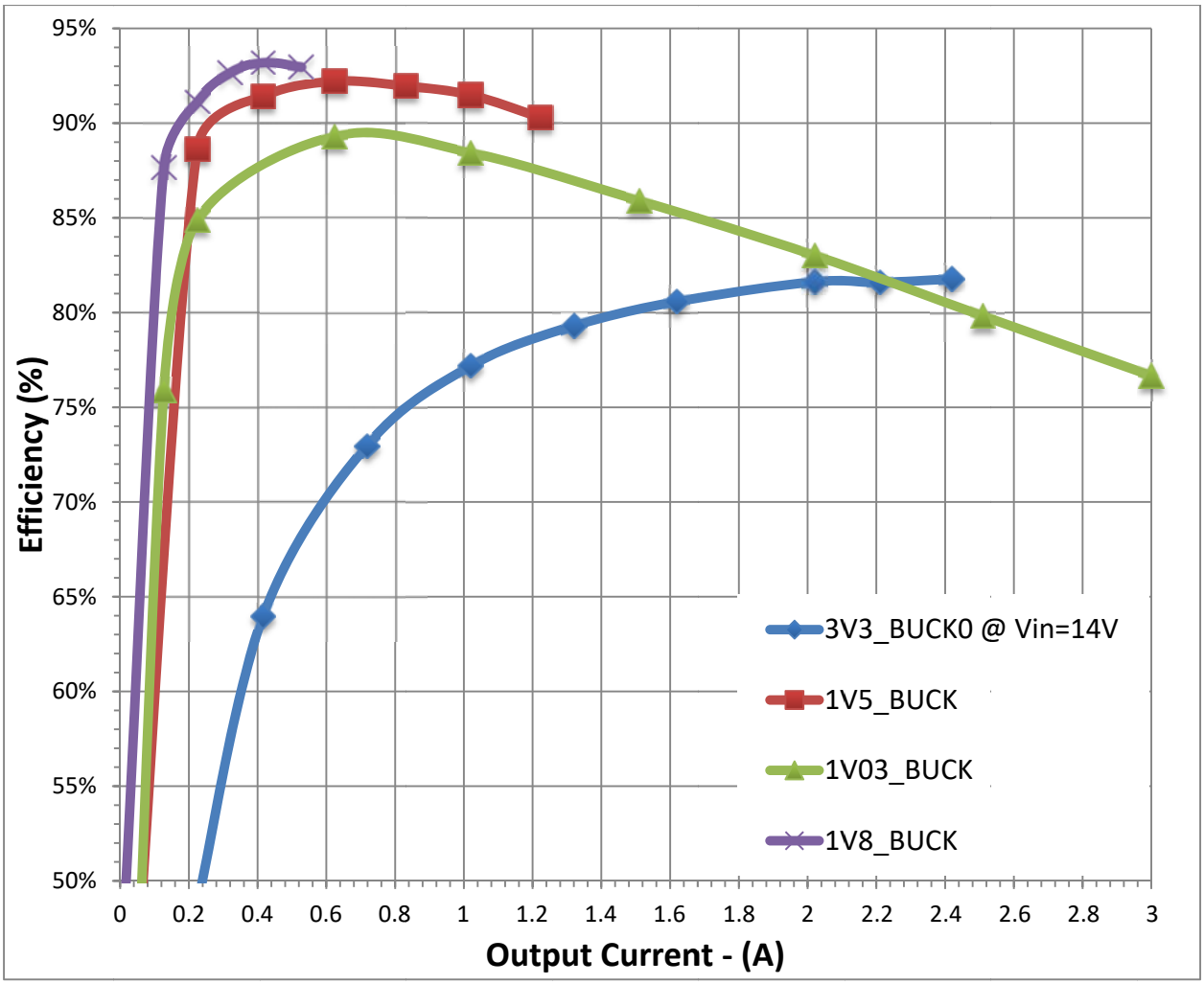


Figure 3: Efficiency Graph

2.2 Efficiency Data

3V3_BUCK0				
Vin (V)	**Iin (A)**	**Vout1 (V)**	**Iout1 (A)**	**η1**
14.1	0.039	3.32	0.001	0.006
14.06	0.0776	3.32	0.127	0.386
14.04	0.109	3.32	0.224	0.486
14.02	0.154	3.32	0.416	0.640
14.02	0.233	3.32	0.718	0.730
14.02	0.312	3.31	1.02	0.772
14.02	0.393	3.31	1.32	0.793
14.01	0.475	3.31	1.62	0.806
14.05	0.583	3.31	2.02	0.816
14.01	0.638	3.3	2.21	0.816
14	0.697	3.3	2.418	0.818

1V03_BUCK				
Vin2 (V)	**Iin2 (A)**	**Vout2 (V)**	**Iout2 (A)**	**η2**
3.319	0.017	1.03	0.015	0.274
3.314	0.052	1.03	0.127	0.759
3.311	0.082	1.029	0.224	0.849
3.295	0.217	1.025	0.623	0.893
3.28	0.359	1.021	1.02	0.884
3.255	0.549	1.016	1.511	0.859
3.225	0.762	1.01	2.02	0.830
3.202	0.987	1.005	2.51	0.798
3.171	1.234	1	3	0.767

1V8_BUCK				
Vin3 (V)	**Iin3 (A)**	**Vout3 (V)**	**Iout3 (A)**	**η3**
3.32	0.0166	1.805	0.015	0.491
3.316	0.0788	1.804	0.127	0.877
3.312	0.1338	1.803	0.224	0.911
3.31	0.188	1.802	0.32	0.927
3.3	0.243	1.801	0.415	0.932
3.3	0.3086	1.8	0.526	0.930

1V5_BUCK				
Vin4 (V)	**Iin4 (A)**	**Vout4 (V)**	**Iout4 (A)**	**η4**
3.319	0.019	1.506	0.015	0.358
3.307	0.115	1.505	0.224	0.886
3.296	0.207	1.5	0.4157	0.914
3.284	0.3086	1.5	0.623	0.922
3.272	0.414	1.499	0.831	0.920
3.26	0.512	1.497	1.02	0.915
3.25	0.623	1.495	1.223	0.903

2.3 Thermal Images

Below picture is showing the thermal performance of the reference design. The thermal image has been taken after 20 minutes of operating at maximum loading conditions.

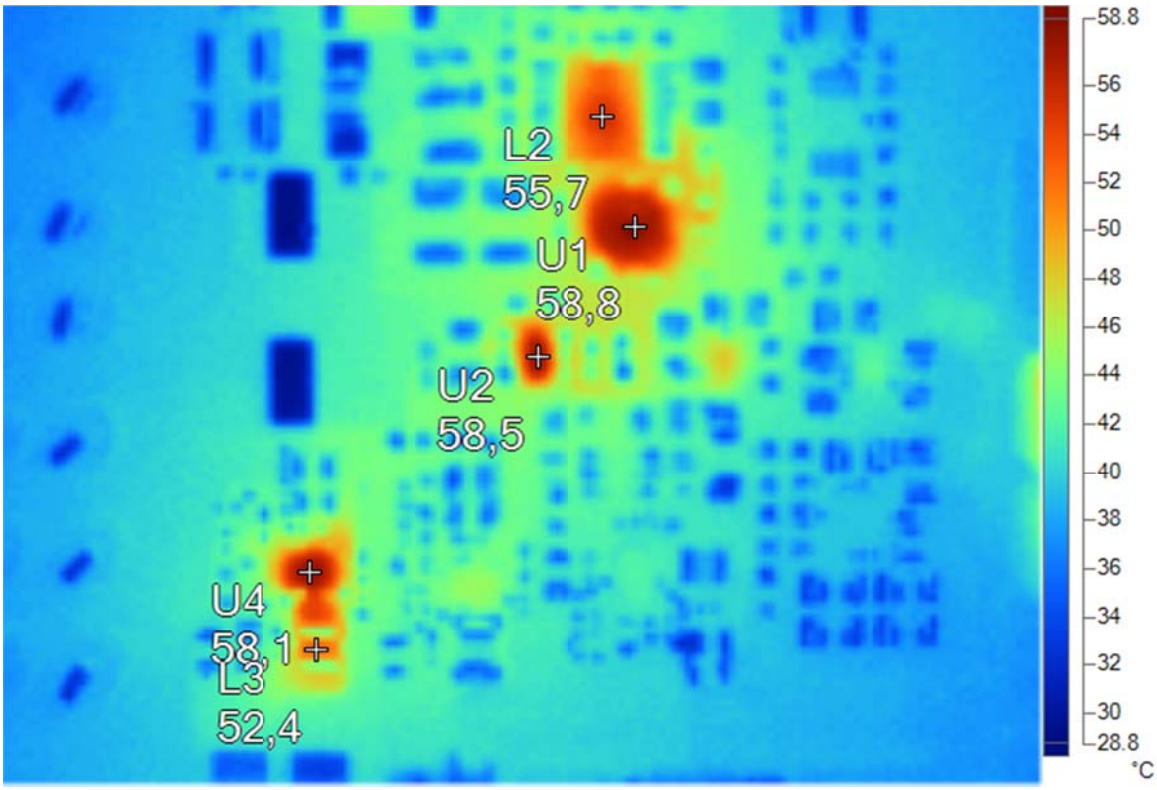


Figure 4: Thermal Image

Image Info | Marker Data | Graph | IR-PhotoNotes™

Label	Emissivity	Background Temp	Min	Avg	Max	St. Dev.	Units
L2	0.96	25.5	55.7	55.7	55.7	0.00	°C
L3	0.96	25.5	52.4	52.4	52.4	0.00	°C
U1	0.96	25.5	58.8	58.8	58.8	0.00	°C
U2	0.96	25.5	58.5	58.5	58.5	0.00	°C
U4	0.96	25.5	58.1	58.1	58.1	0.00	°C

2.4 Dimensions

PCB Area of Components Placement: 40.7 mm x 37.8 mm

3 Waveforms

If not otherwise noted, all measurements were performed at typical input voltage of Vin(typ) = 14 V and under full load conditions. All measurements were performed at room temperature.

3.1 Switching

Figure 5 through Figure 8 depicts the waveforms of the switching nodes of each power rail:

- Figure 5: Switching Waveform of 3V3_BUCK0 at 2.2 AFigure 5: Switching Waveform of 3V3_BUCK0 at
- Figure 6: Switching Waveform of 1V8_BUCK at 500 mA
- Figure 7: Switching Waveform of 1V03_BUCK at 3 A
- Figure 8: Switching Waveform of 1V5_BUCK at 1.2 A

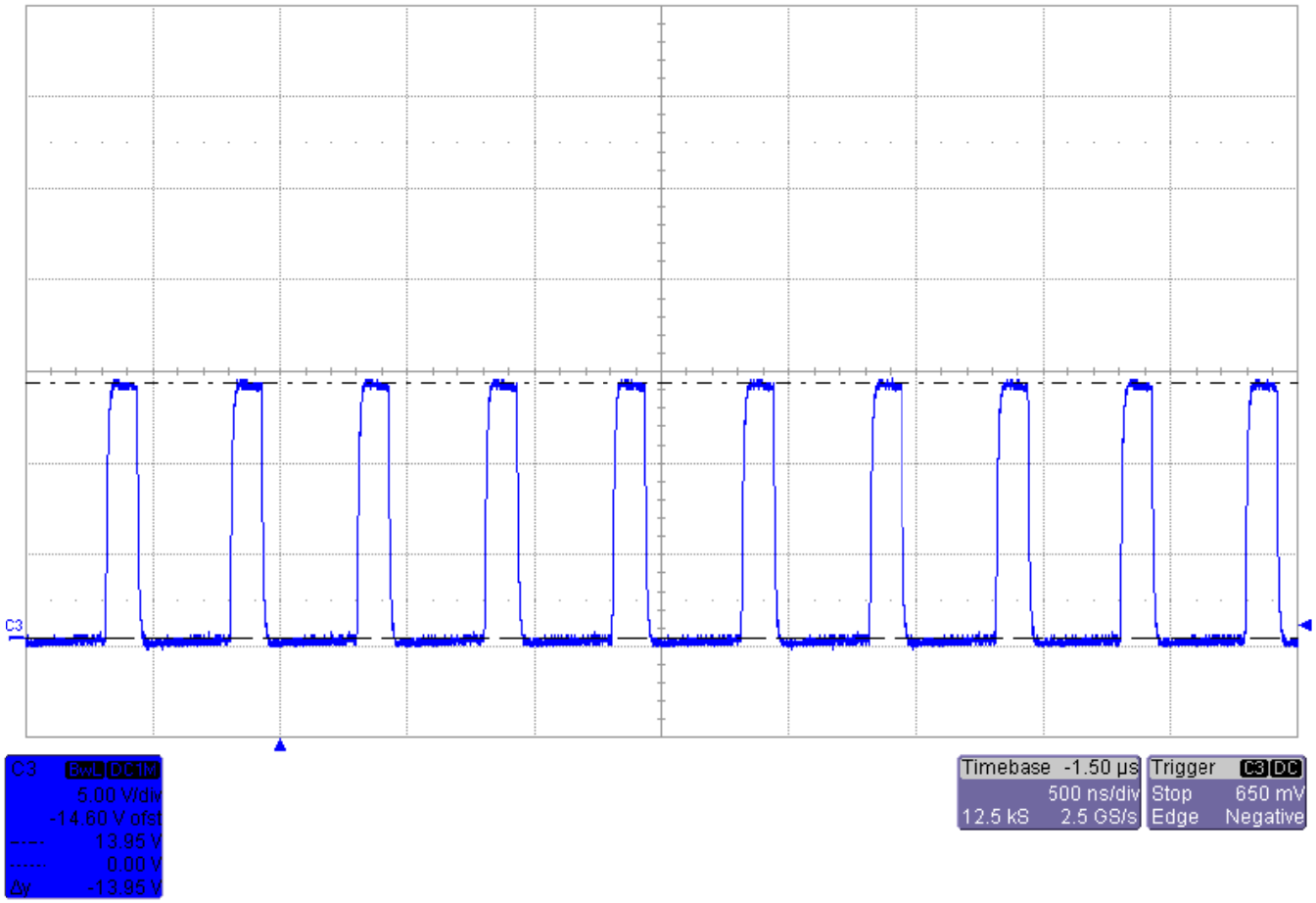


Figure 5: Switching Waveform of 3V3_BUCK0 at 2.2 A

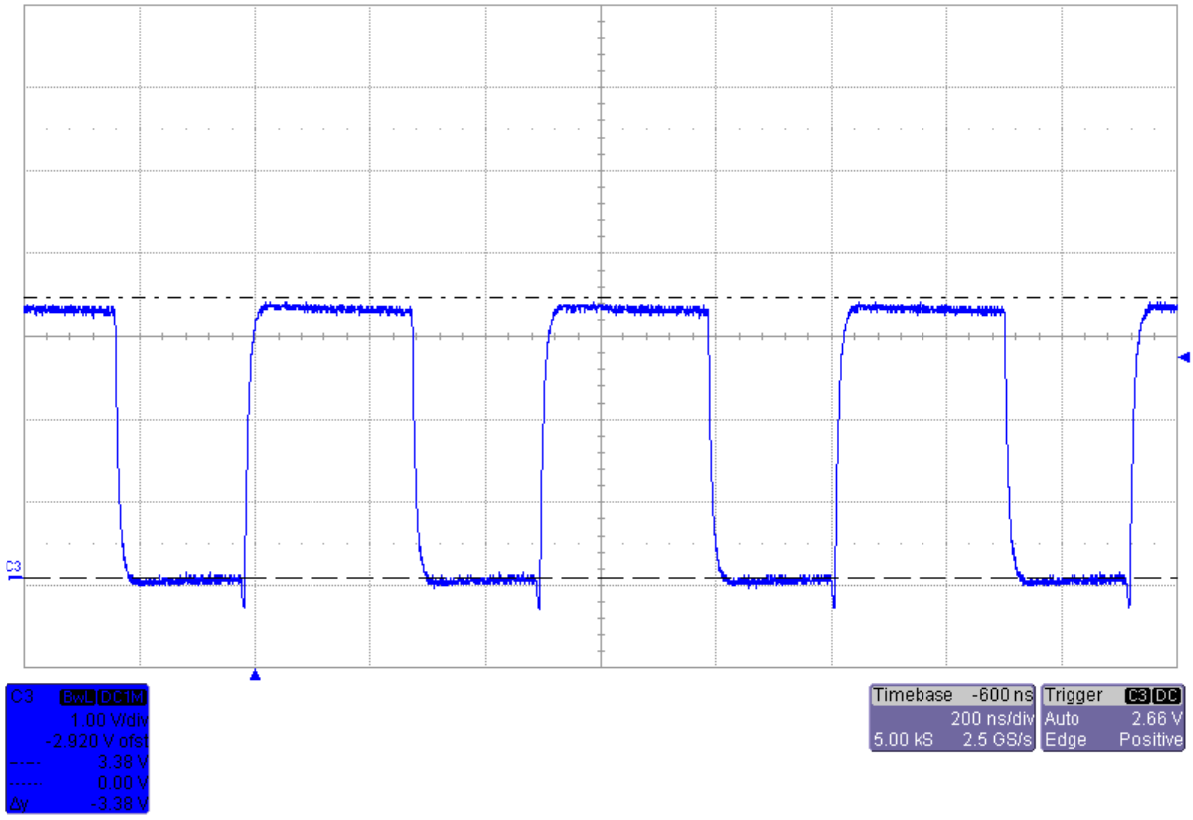


Figure 6: Switching Waveform of 1V8_BUCK at 500 mA

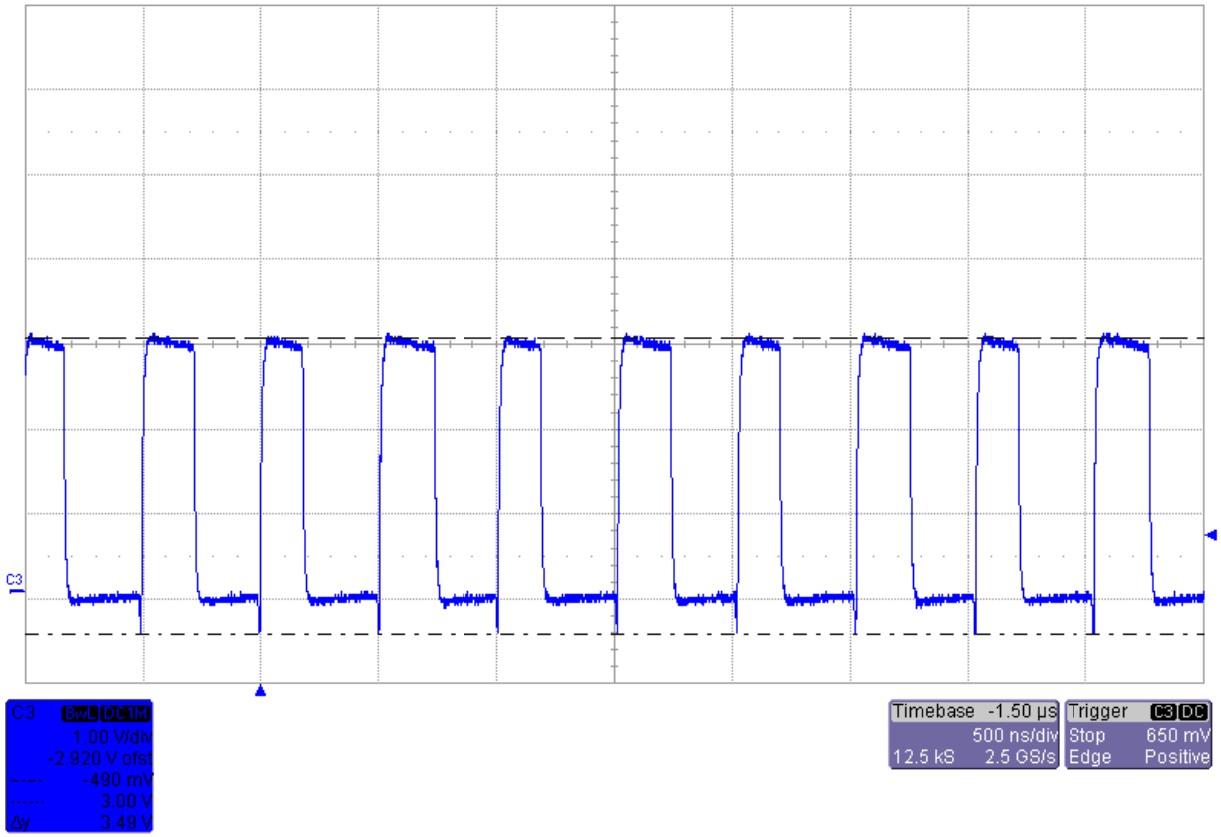


Figure 7: Switching Waveform of 1V03_BUCK at 3 A

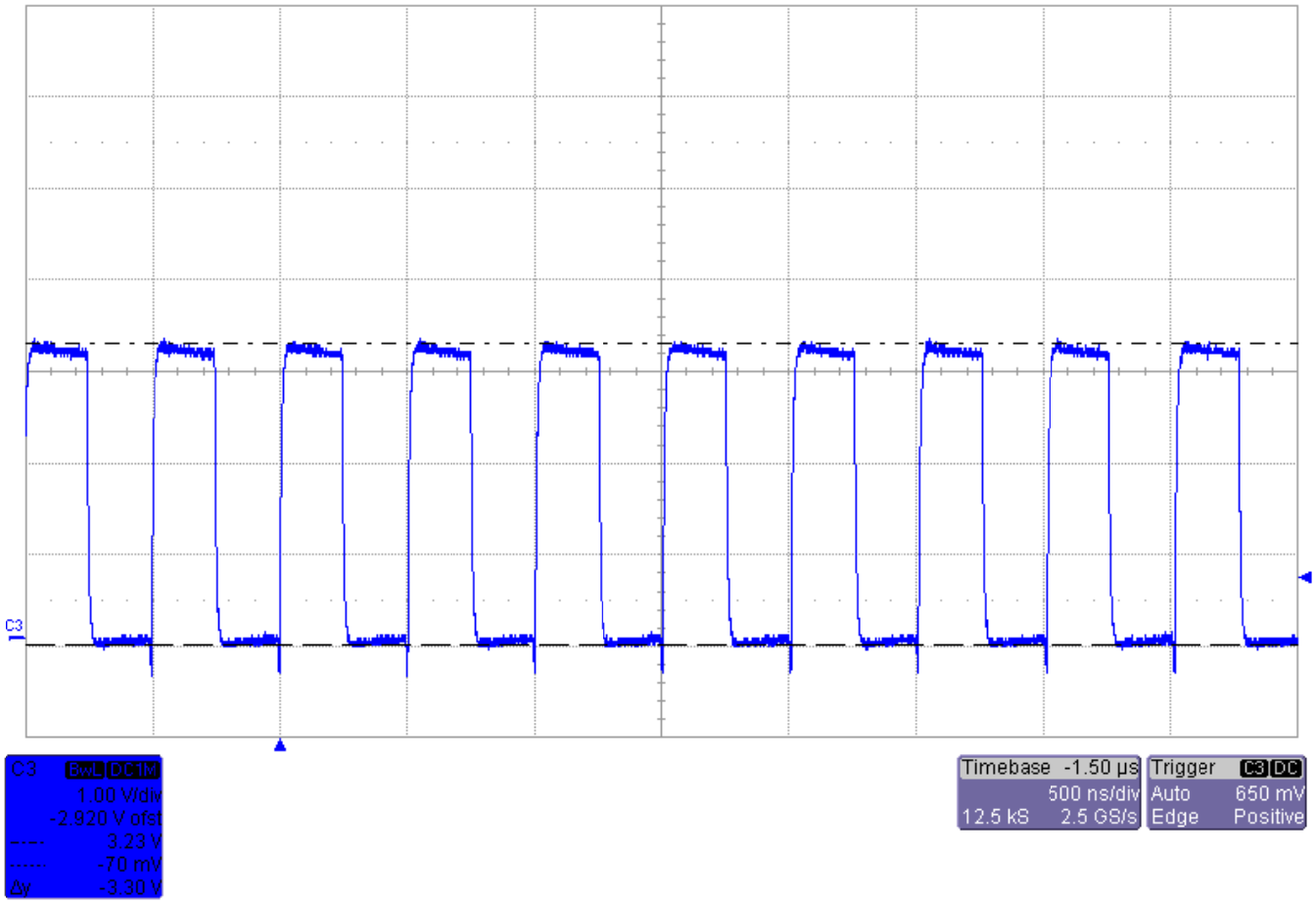


Figure 8: Switching Waveform of 1V5_BUCK at 1.2 A

3.2 Output Voltage Ripple

Figure 9 through Figure 12 shows the output voltage ripple measurements of each power rail:

- Figure 9: Output Voltage Ripple of 3V3_BUCK0 at 2.2 A
- Figure 10: Output Voltage Ripple of 1V8_BUCK at 0.5 A
- Figure 11: Output Voltage Ripple of 1V5_BUCK at 1.2 A
- Figure 12: Output Voltage Ripple of 1V03_BUCK at 3 A

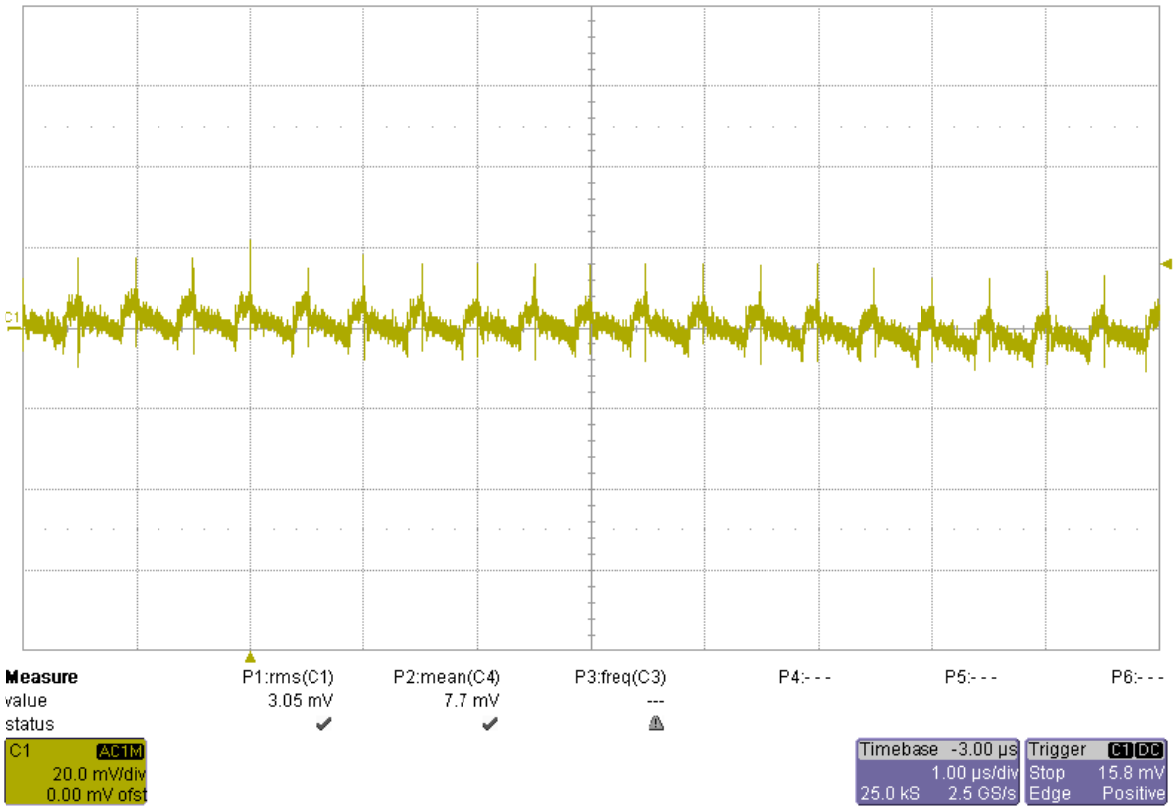


Figure 9: Output Voltage Ripple of 3V3_BUCK0 at 2.2 A

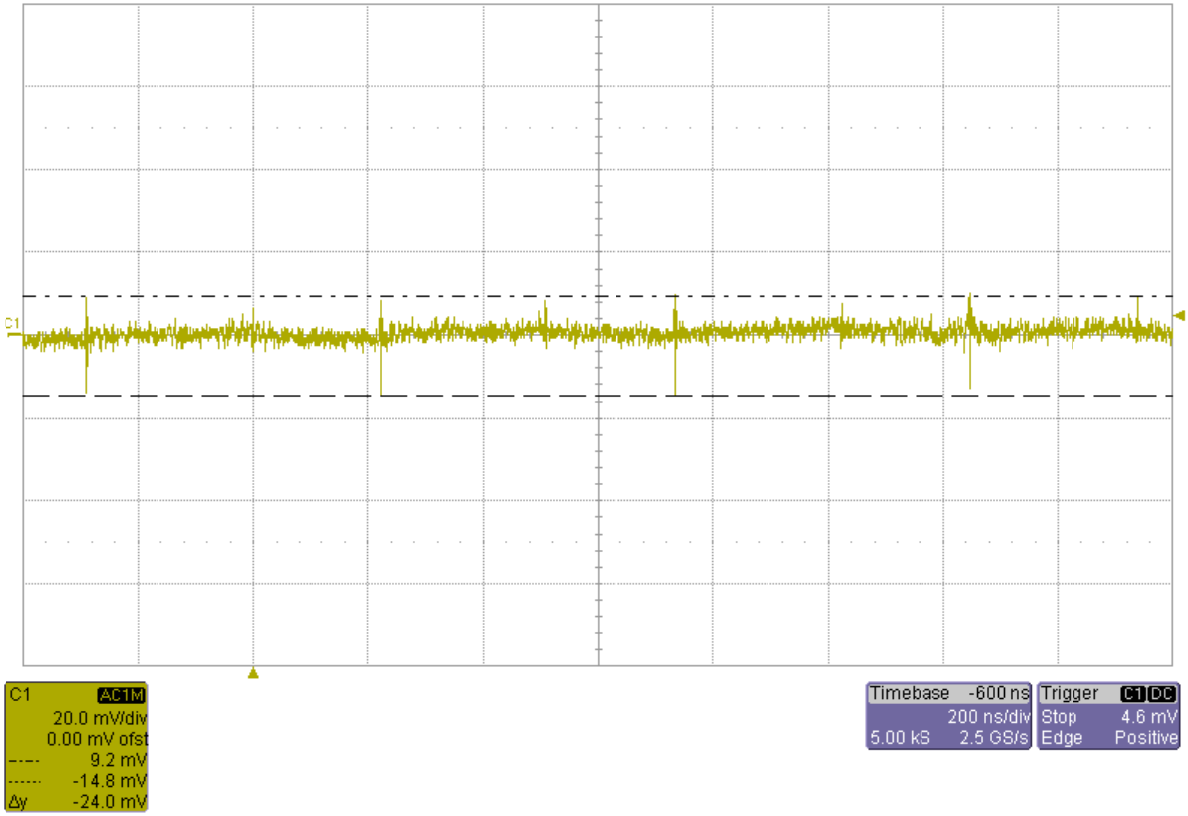


Figure 10: Output Voltage Ripple of 1V8_BUCK at 0.5 A

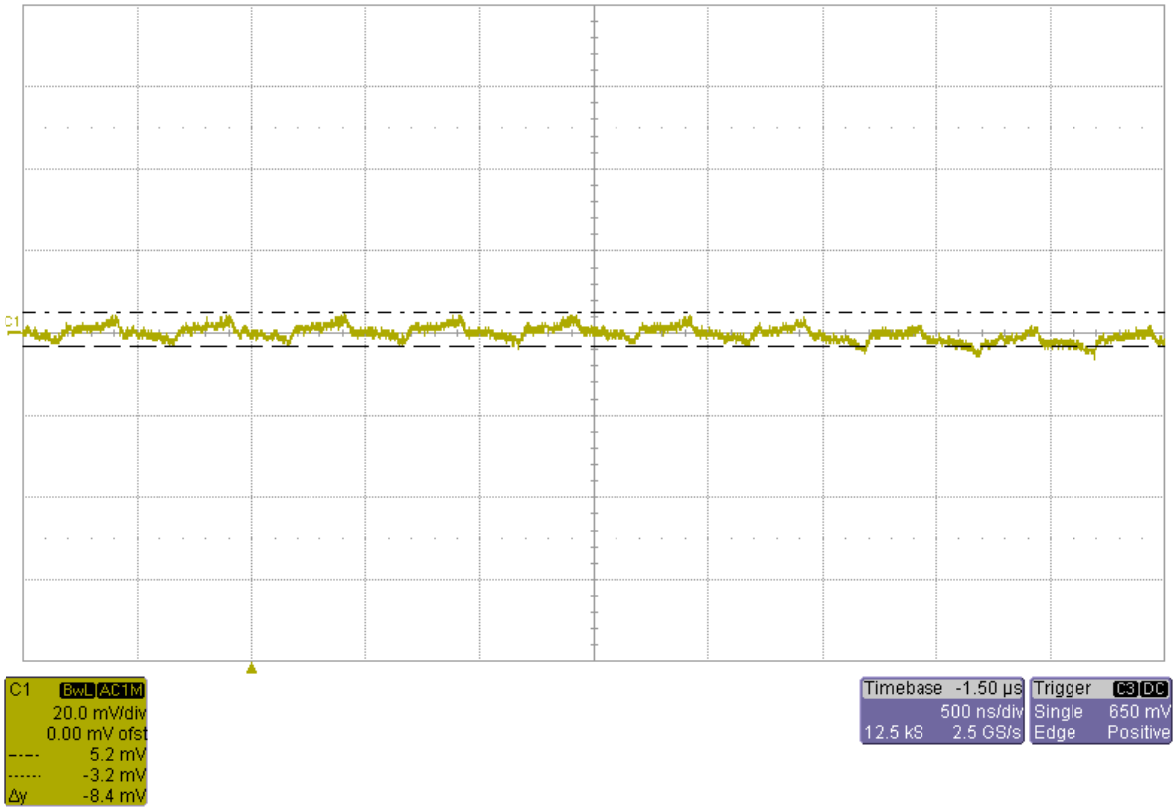


Figure 11: Output Voltage Ripple of 1V5_BUCK at 1.2 A

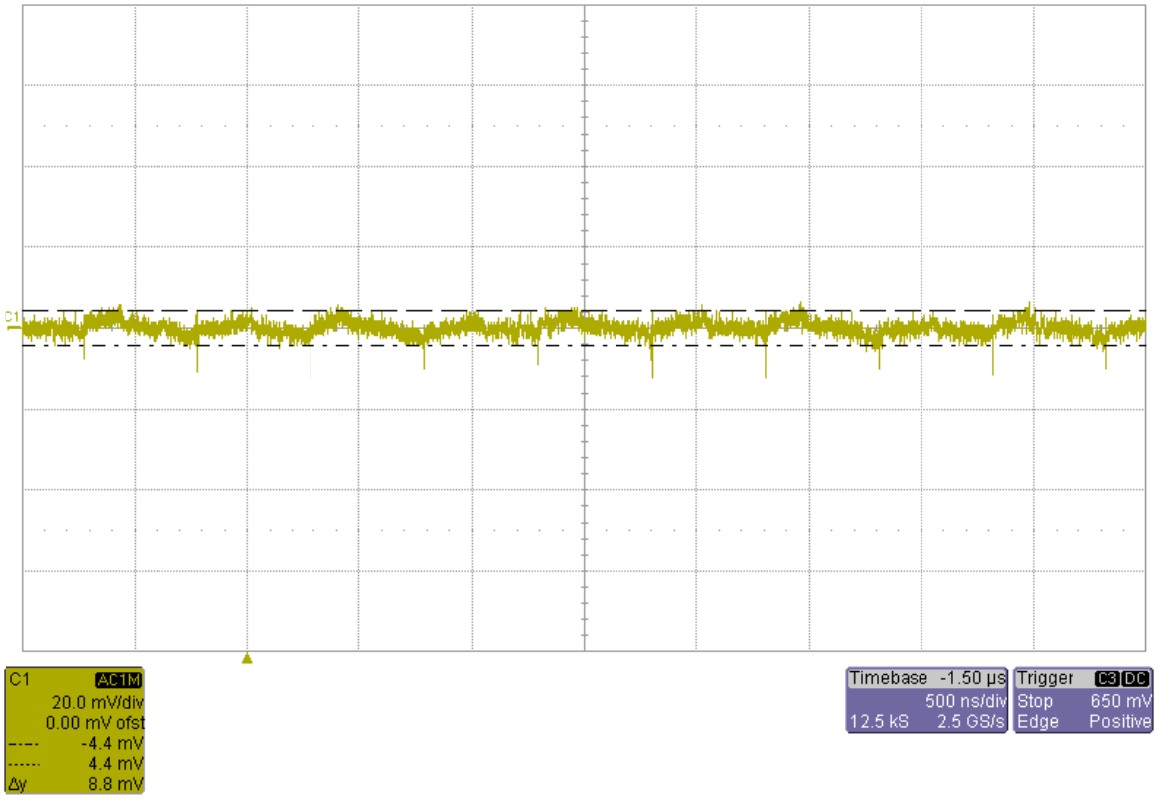


Figure 12: Output Voltage Ripple of 1V03_BUCK at 3 A

3.3 Bode Plot

Figure 13 through Figure 16 depicts the small signal analysis of the power rails at different input voltages:

- Figure 13: Bode Plot Measurement of 3V3_BUCK0 at 2.2 A
- Figure 14: Bode Plot Measurement of 1V8_BUCK at 500 mA
- Figure 15: Bode Plot Measurement of 1V5_BUCK at 1.2 A
- Figure 16: Bode Plot Measurement of 1V03_BUCK at 3 A

3.3.1 3V3_BUCK0

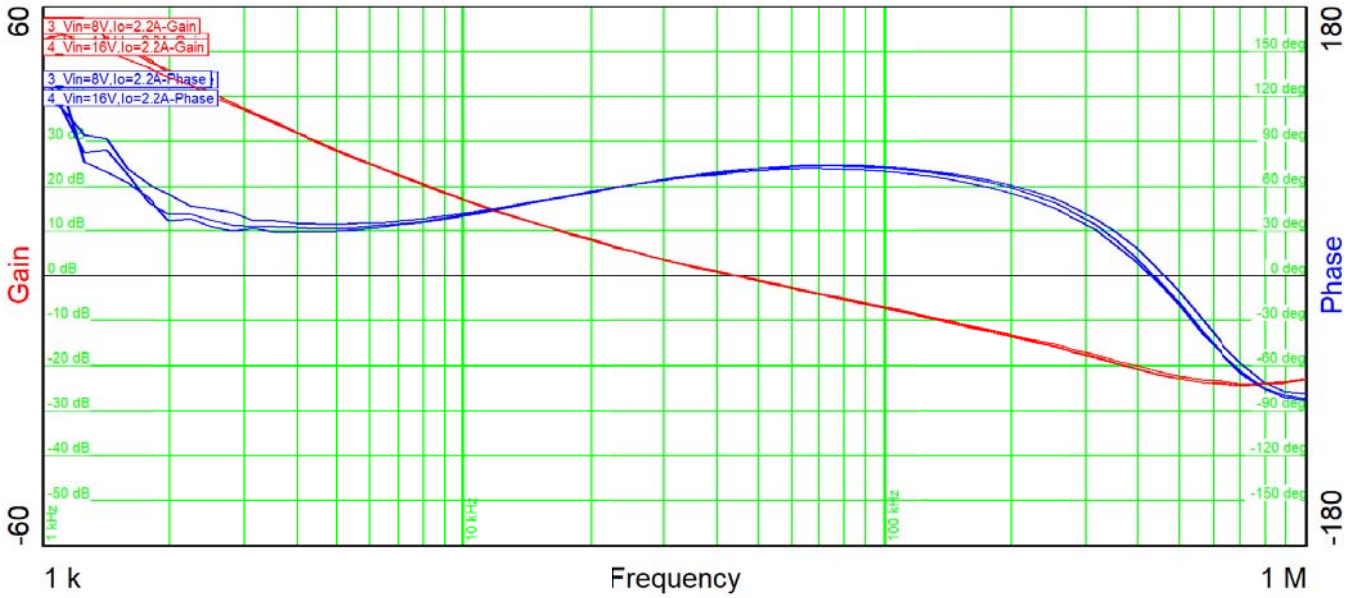


Figure 13: Bode Plot Measurement of 3V3_BUCK0 at 2.2 A

Input Voltage (V)	Crossover Frequency (kHz)	Phase Margin (°)	Slope (dB/decade)	GainCrossover Frequency (kHz)	Gain Margin (°)	Slope (dB/decade)
8	44.7	71	-1	461.1	-21.7	-1
14	44.1	70.3	-1	437.7	-21.8	-1.2
16	43.5	69.2	-1	429	-21.7	-1.2

3.3.2 1V8_BUCK

Note: This measurement is at improved output capacitance (additional 22 uF / 0805 / 6.3 V)

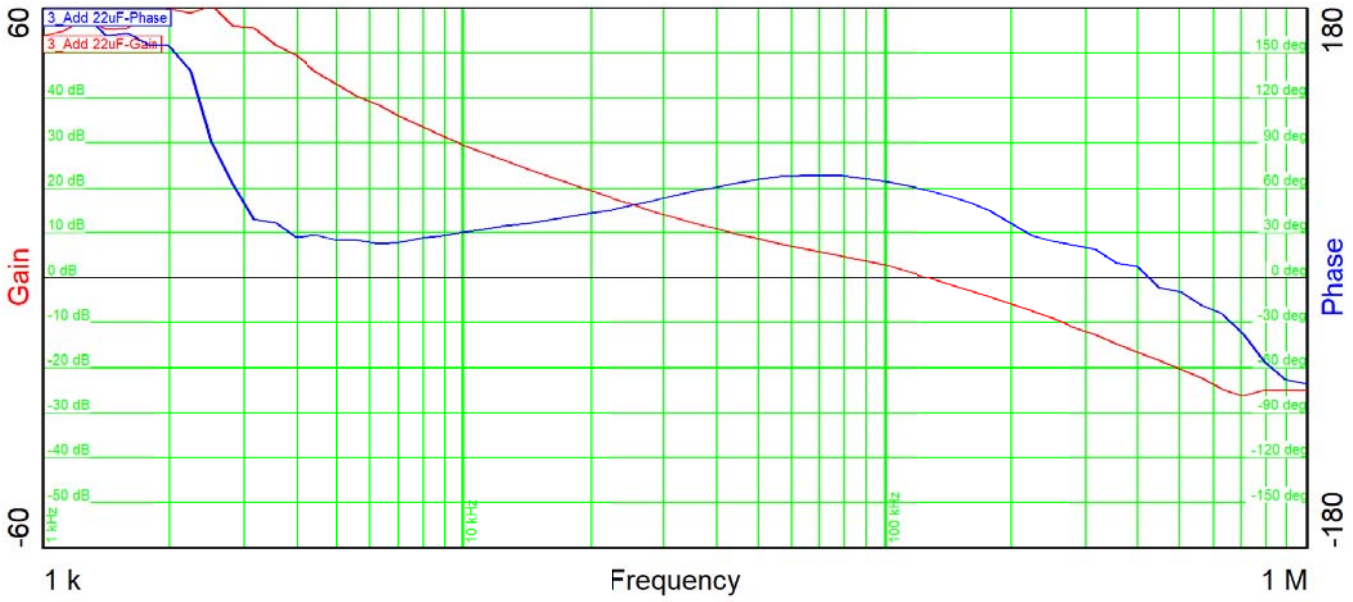


Figure 14: Bode Plot Measurement of 1V8_BUCK at 500 mA

Input Voltage (V)	Crossover Frequency (kHz)	Phase Margin (°)	Slope (dB/decade)	GainCrossover Frequency (kHz)	Gain Margin (°)	Slope (dB/decade)
3.3	127	58.2	-1.5	421.7	-17.5	-1.8

3.3.3 1V5_BUCK

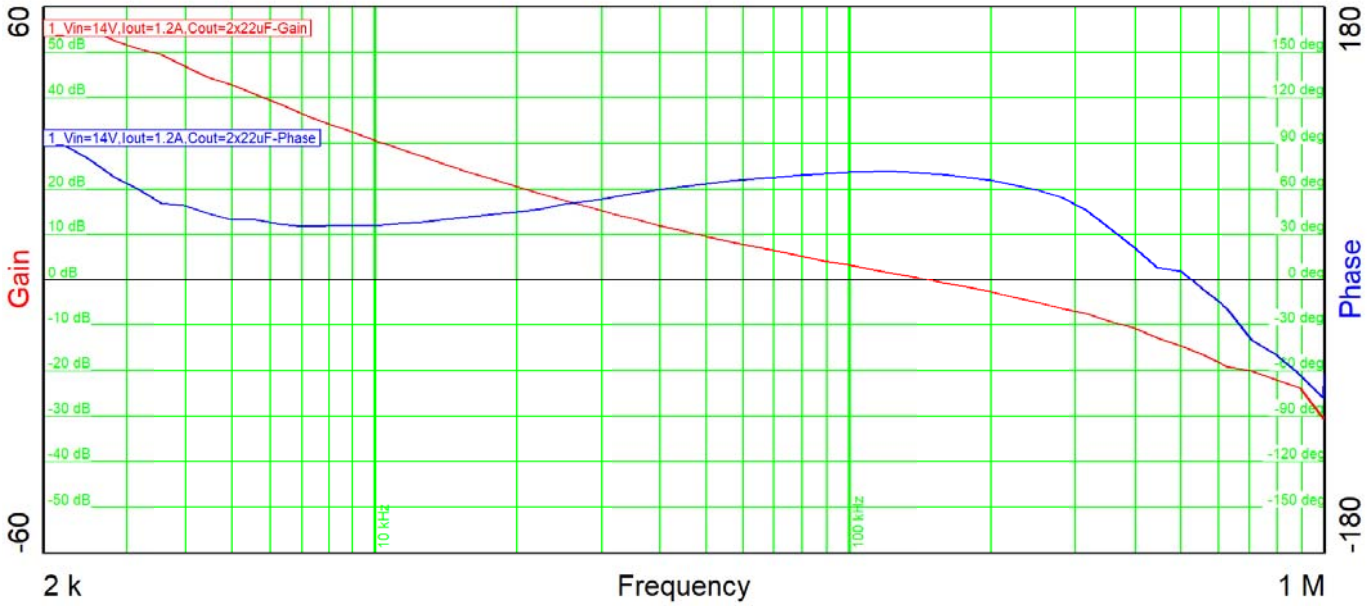


Figure 15: Bode Plot Measurement of 1V5_BUCK at 1.2 A

Input Voltage (V)	Crossover Frequency (kHz)	Phase Margin (°)	Slope (dB/decade)	GainCrossover Frequency (kHz)	Gain Margin (°)	Slope (dB/decade)
3.3	147.4	70.3	-1	527.2	-15.5	-2.2

3.3.4 1V03_BUCK

Note: This measurement is at improved output capacitance (additional 22 uF / 0805 / 6.3 V)

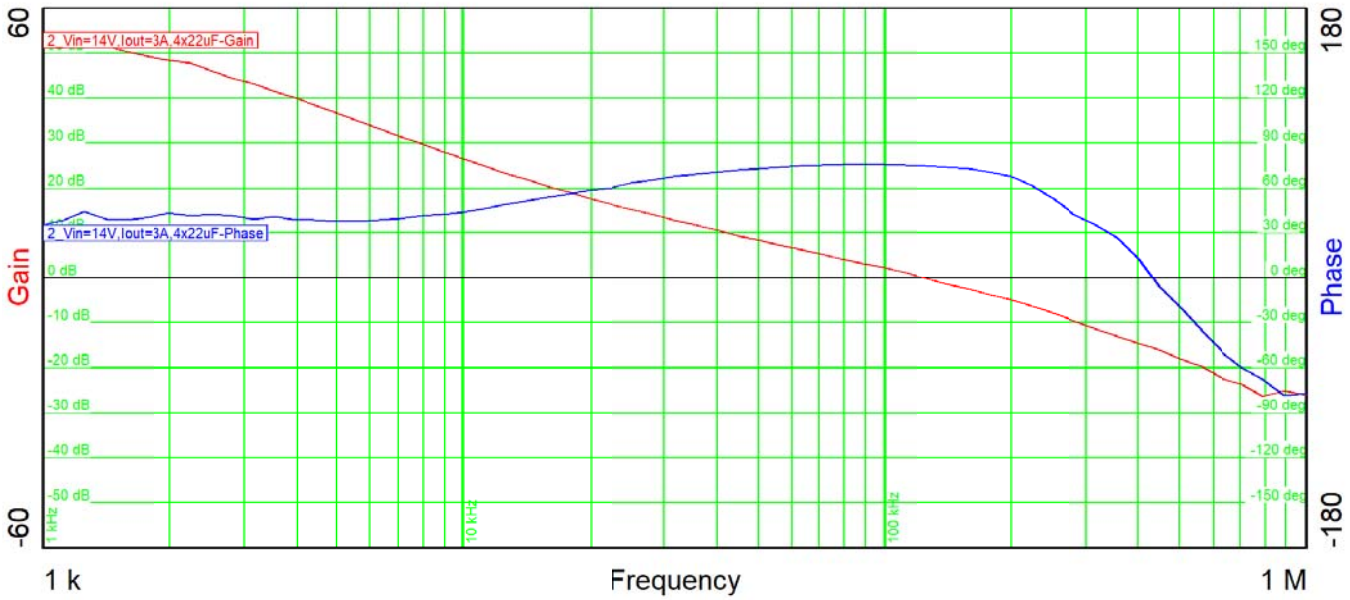


Figure 16: Bode Plot Measurement of 1V03_BUCK at 3 A

Input Voltage (V)	Crossover Frequency (kHz)	Phase Margin (°)	Slope (dB/decade)	GainCrossover Frequency (kHz)	Gain Margin (°)	Slope (dB/decade)
3.3	124	74.7	-1.3	431.2	-15.6	-1.4

3.4 Load Transients

Figure 17 through Figure 20 depicts the load transient response of all power rails:

- Figure 17: Load Step Response of 3V3_BUCK0 at Vin(typ) = 14 V
- Figure 18: Load Step Response of 1V8_BUCK
- Figure 19: Load Step Response of 1V03_BUCK
- Figure 20: Load Step Response of 1V5_BUCK

3.4.1 3V3_BUCK0 Load Step Response

The slew rate of the below load step is at 0.1 A/us at a pulse frequency of 1 kHz and a duty cycle of 50 %.

CH1: Output Voltage (AC coupled, 50 mV/div)
CH4: Output Current (1 A/div)

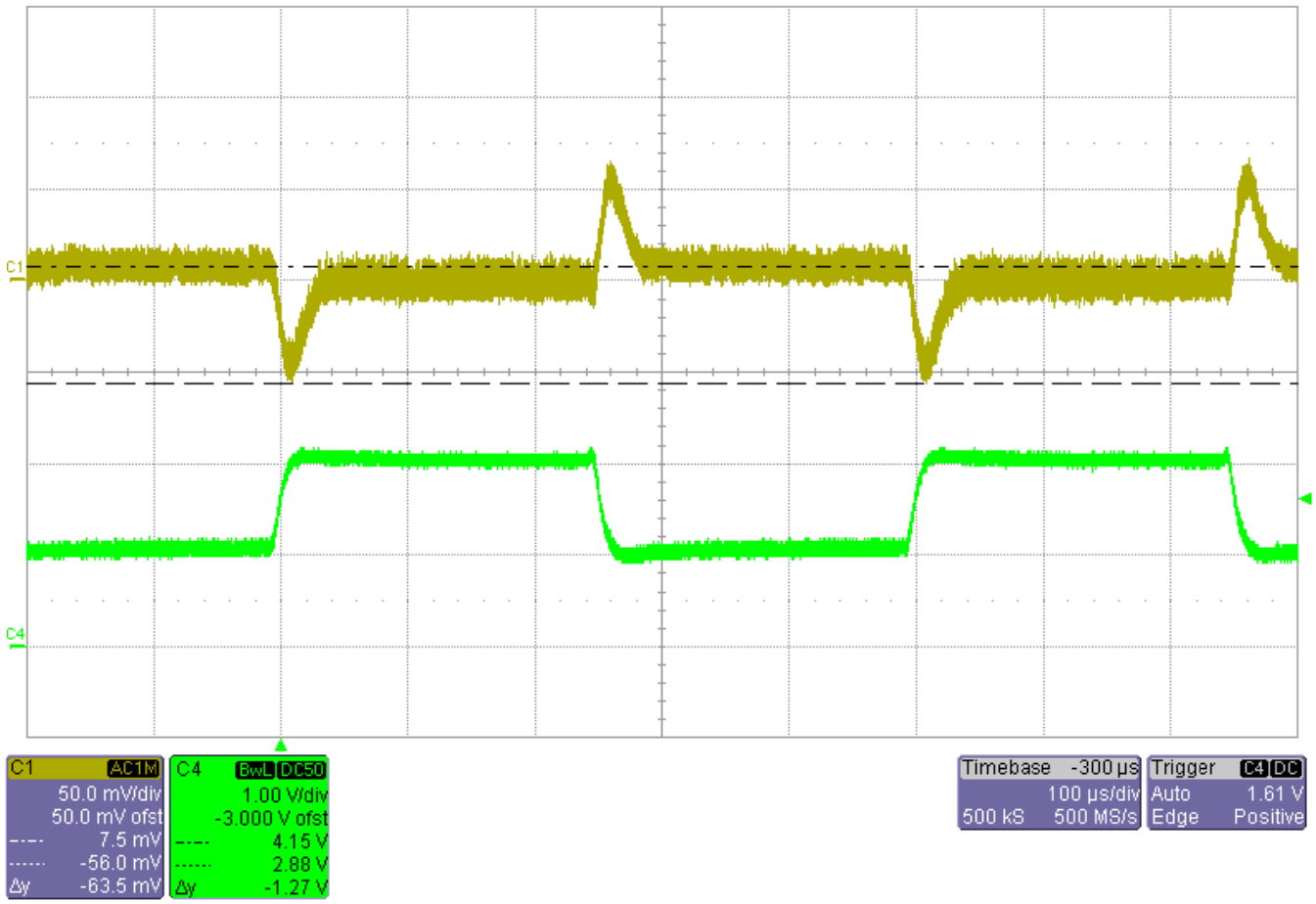


Figure 17: Load Step Response of 3V3_BUCK0 at Vin(typ) = 14 V

At a positive load jump the maximum output deviation of 3V3_BUCK0 is at 53 mV which corresponds to approx.1.6%.
At a negative load jump the maximum output deviation of 3V3_BUCK0 is at 58 mV which corresponds to approx.1.8%.

3.4.2 1V8_BUCK Load Step Response

Note: This measurement is at improved output capacitance (additional 22 uF / 0805 / 6.3 V)

The slew rate of the below load step is at 5 mA/us at a pulse frequency of 1.4 kHz and a duty cycle of 50 %.

CH1: Output Voltage (AC coupled, 20 mV/div)
CH4: Output Current (0.2 A/div)

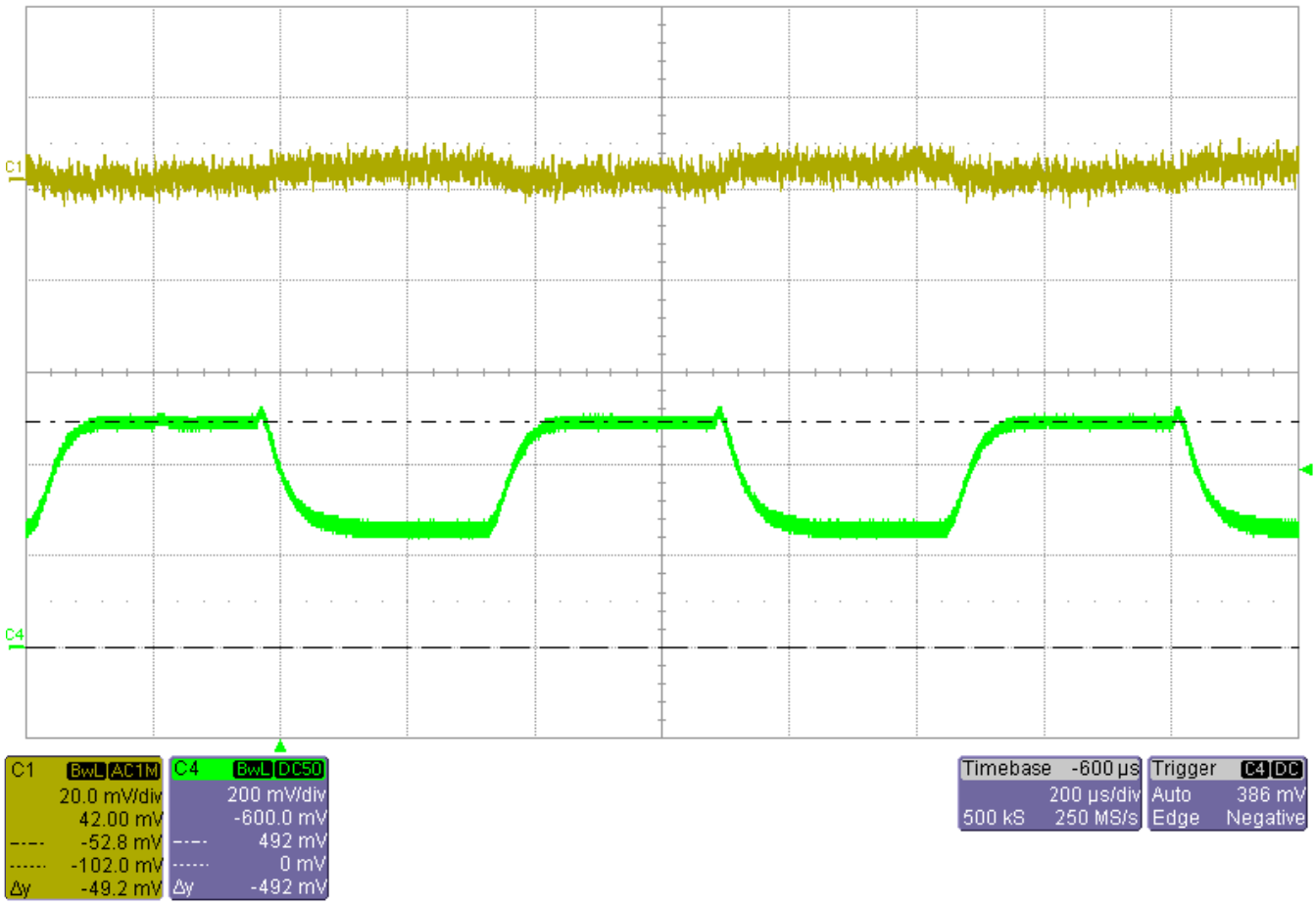


Figure 18: Load Step Response of 1V8_BUCK

At a positive load jump the maximum output deviation of 1V8_BUCK is below 10 mV which corresponds to approx.0.5 %.
At a negative load jump the maximum output deviation of 1V8_BUCK is below 10 mV which corresponds to approx.0.5 %.

3.4.3 1V03_BUCK Load Step Response

Note: This measurement is at improved output capacitance (additional 22 uF / 0805 / 6.3 V)

The slew rate of the below load step is at 40 mA/us at a pulse frequency of 1.25 kHz and a duty cycle of 50 %.

CH1: Output Voltage (AC coupled, 20 mV/div)
CH4: Output Current (1 A/div)

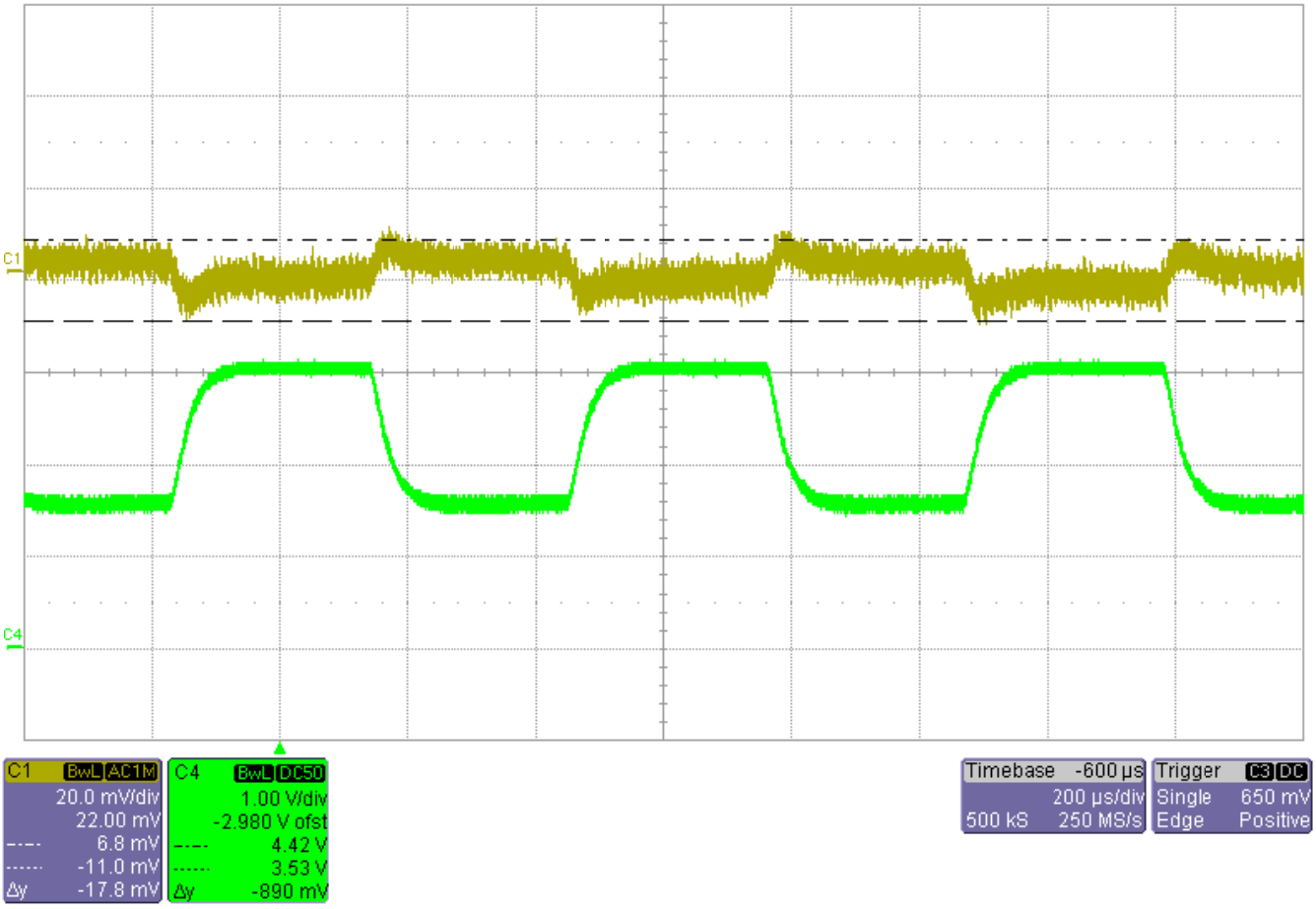


Figure 19: Load Step Response of 1V03_BUCK

At a positive load jump the maximum output deviation of 1V03_BUCK is below 6.8 mV which corresponds to approx.0.7 %.
At a negative load jump the maximum output deviation of 1V03_BUCK is below 11 mV which corresponds to approx.1.1 %.

3.4.4 1V5_BUCK Load Step Response

The slew rate of the below load step is at 40 mA/us at a pulse frequency of 1.25 kHz and a duty cycle of 50 %.

CH1: Output Voltage (AC coupled, 20 mV/div)
CH4: Output Current (500 mA/div)

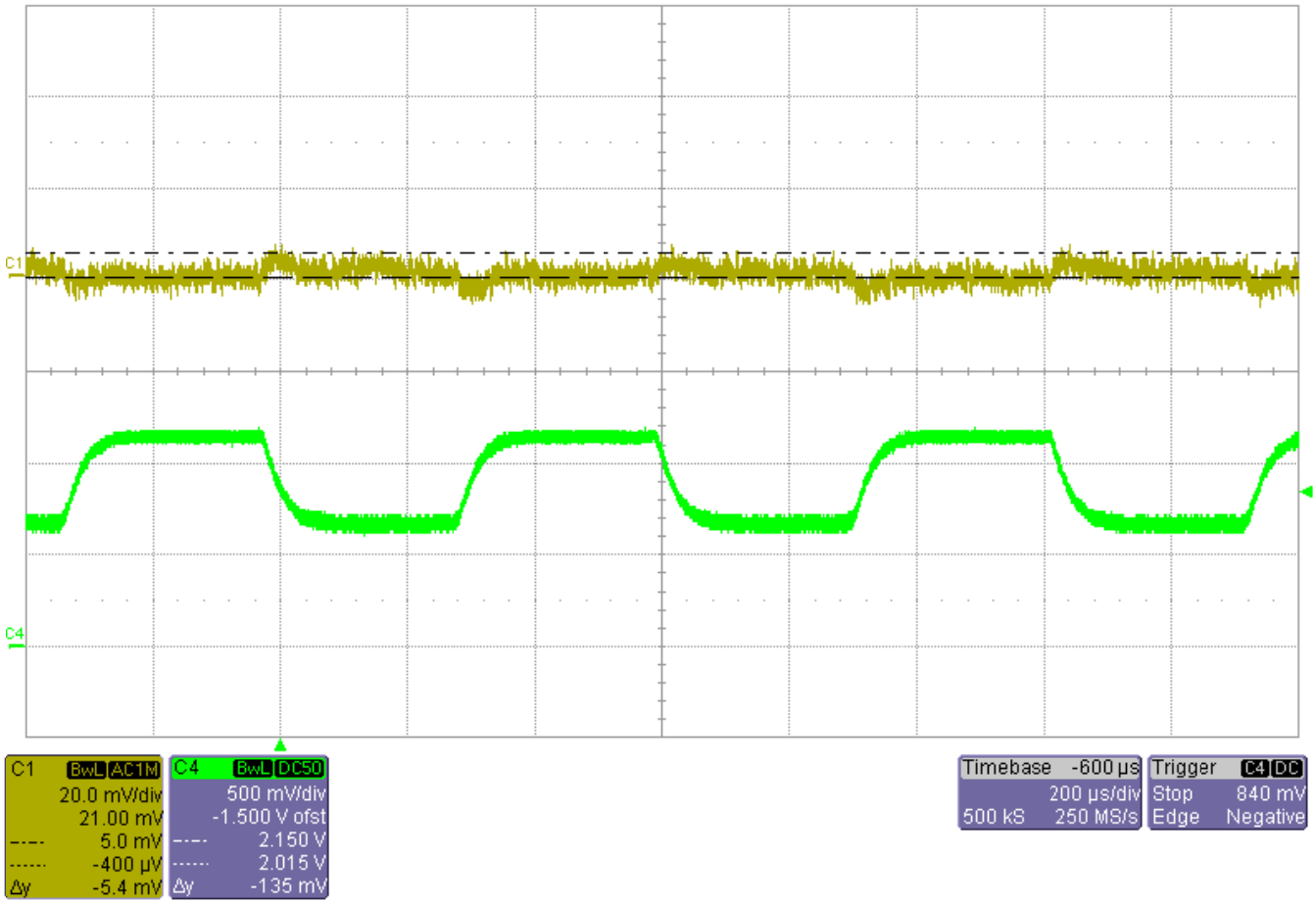


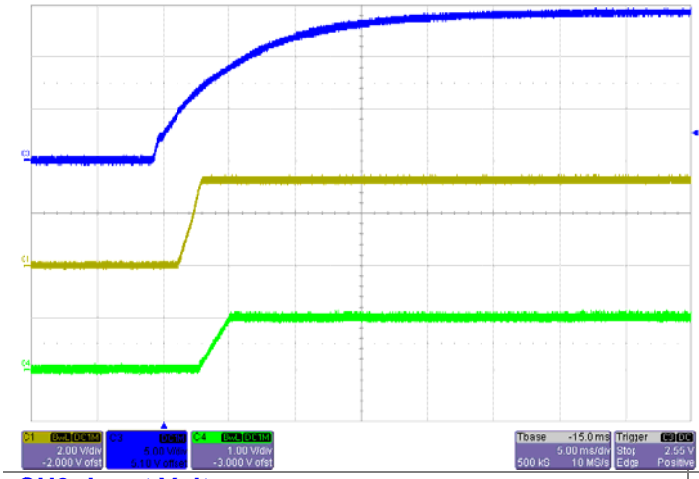
Figure 20: Load Step Response of 1V5_BUCK

At a positive load jump the maximum output deviation of 1V5_BUCK is below 5.4 mV which corresponds to approx.0.4 %.
At a negative load jump the maximum output deviation of 1V03_BUCK is below 5.5 mV which corresponds to approx.0.4 %.

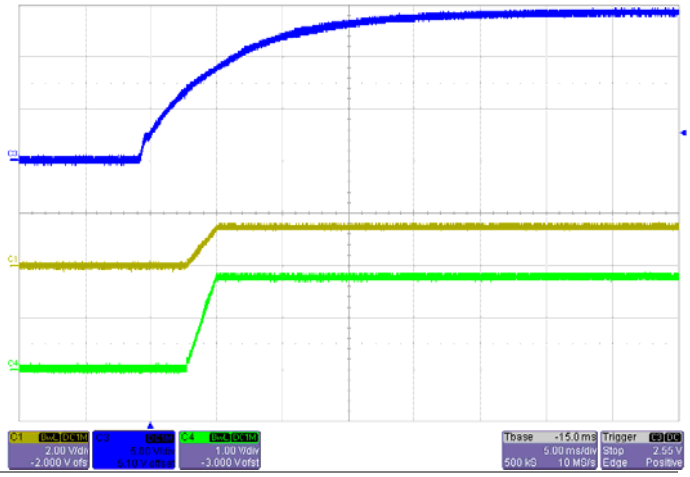
3.5 Start-up Sequence

Following figures show the startup sequence of the power rails.

Whereas,



CH3: Input Voltage
CH1: 3V3_BUCK0
CH4: 1V03_BUCK



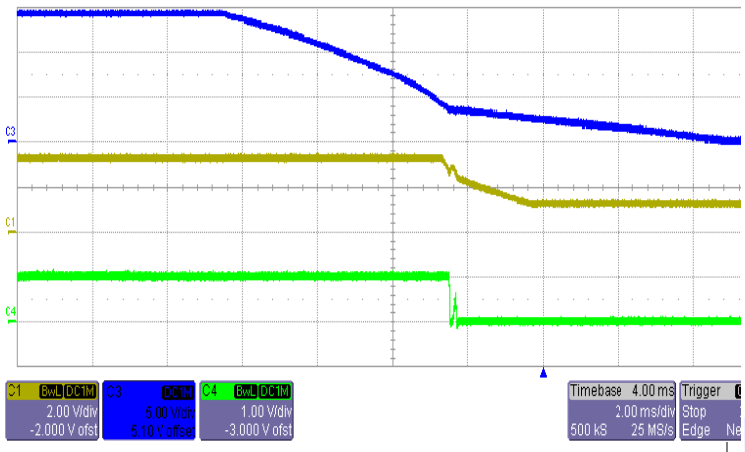
CH3: Input Voltage
CH1: 1V5_BUCK
CH4: 1V8_BUCK

Table 1. Startup Sequence

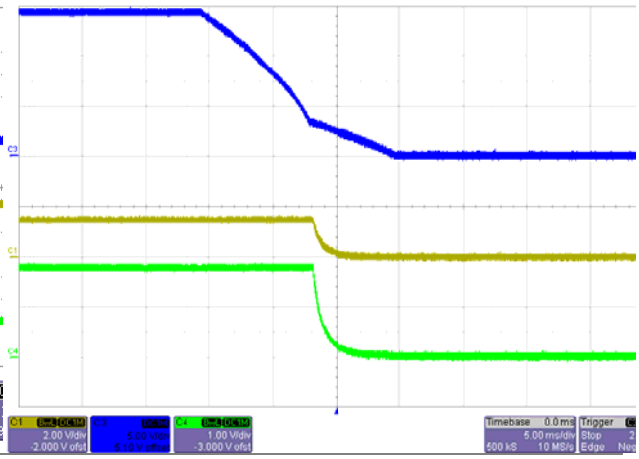
3.6 Shutdown Sequence

Following figures show the shutdown sequence of the power rails.

Whereas,



CH3: Input Voltage
CH1: 3V3_BUCK0
CH4: 1V03_BUCK



CH3: Input Voltage
CH1: 1V5_BUCK
CH4: 1V8_BUCK

Table 2. Shutdown Sequence

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