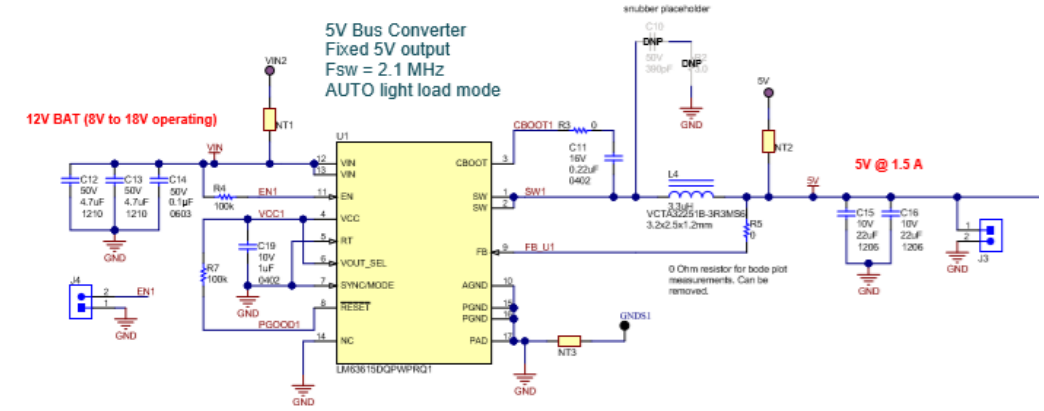
Test Report: PMP22030

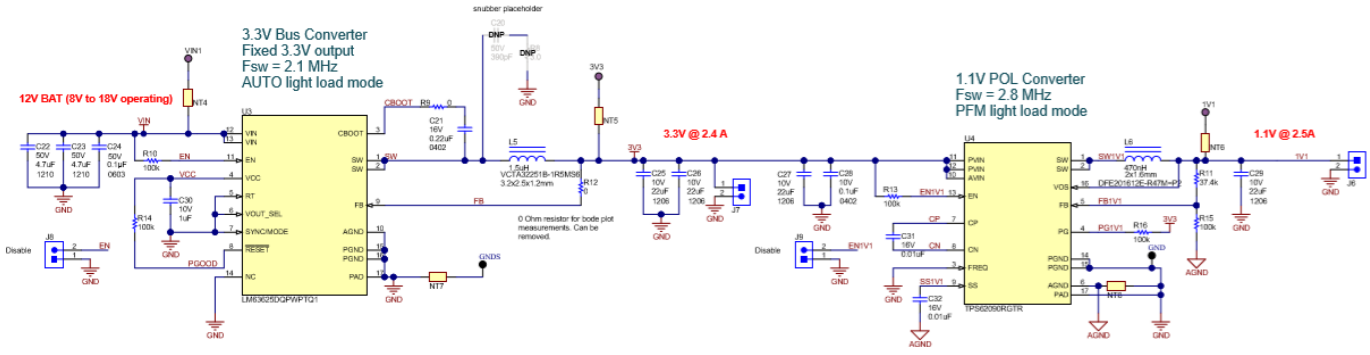
Efficient, Low-Heat, CISPR 25 Class 5-Compliant Power Reference Design for Infotainment Display

Description

The PMP22030 reference design is focused on the power tree for an automotive infotainment display unit. The reference design covers various power supply rails. This document presents results from testing the LM63615-Q1 used to provide 5.0V output from battery input (typical 13.5V), LM63625-Q1 used to provide 3.3V output from battery input (typical 13.5V) and TPS62090-Q1 used to provide 1.1V output from 3.3V input.



Schematic of LM63615-Q1



Schematic of LM63625-Q1 and TPS62090-Q1

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements for 5V output

PARAMETER	SPECIFICATIONS
Input voltage	8V to 18V, 13.5V typical (4 to 36V worst case)
Output voltage	5V
Output current	1.5A
Switching frequency	2.1MHz

Table 2. Voltage and Current Requirements for 3V3 output

PARAMETER	SPECIFICATIONS
Input voltage	8V to 18V, 13.5V typical (4 to 36V worst case)
Output voltage	3.3V
Output current	2.4A
Switching frequency	2.1MHz

Table 3. Voltage and Current Requirements for 1V1 output

PARAMETER	SPECIFICATIONS
Input voltage	3.3V
Output voltage	1.1V
Output current	2.5A
Switching frequency	2.8MHz

1.2 Considerations

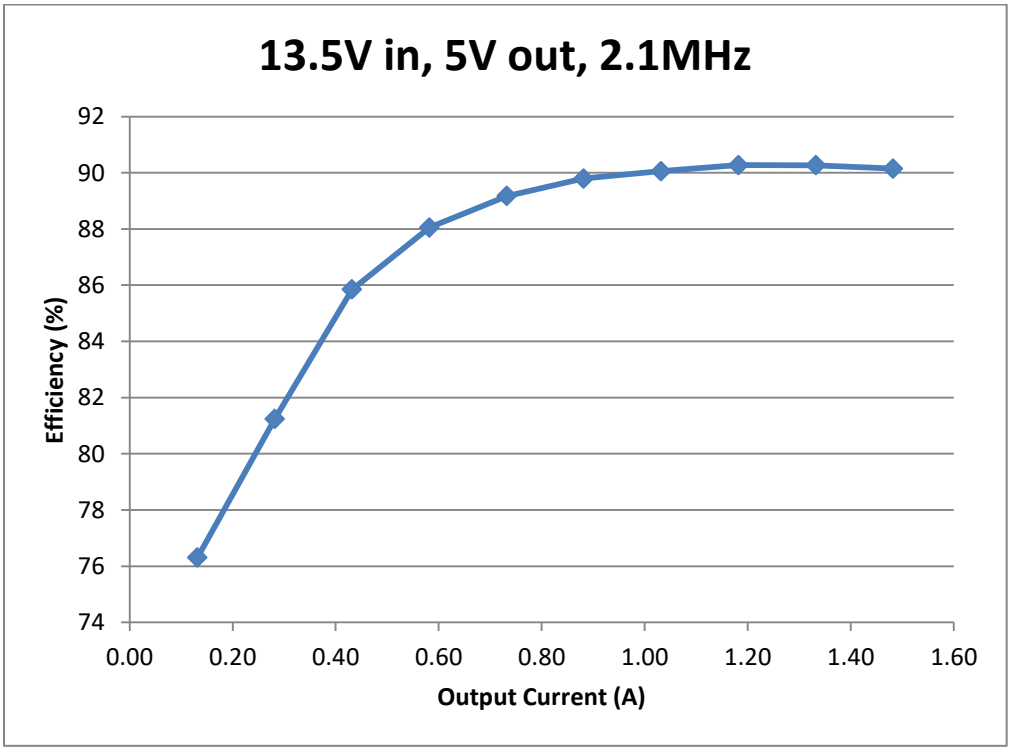
Unless stated otherwise, tests were performed at 13.5V input. The input supply was connected to the input of the EMI filter (instead of being directly connected to the input of the converter).

2 Testing and Results

2.1 Efficiency Graphs

2.1.1 5V output rail

Efficiency was taken with the converter operating with 13.5V input, 5V output using an automated efficiency measurement station. The input was connected directly at the input of the converter. All other parts of the board were disabled. Peak efficiency is above 90%. Light load efficiency remains high due to AUTO light load mode.

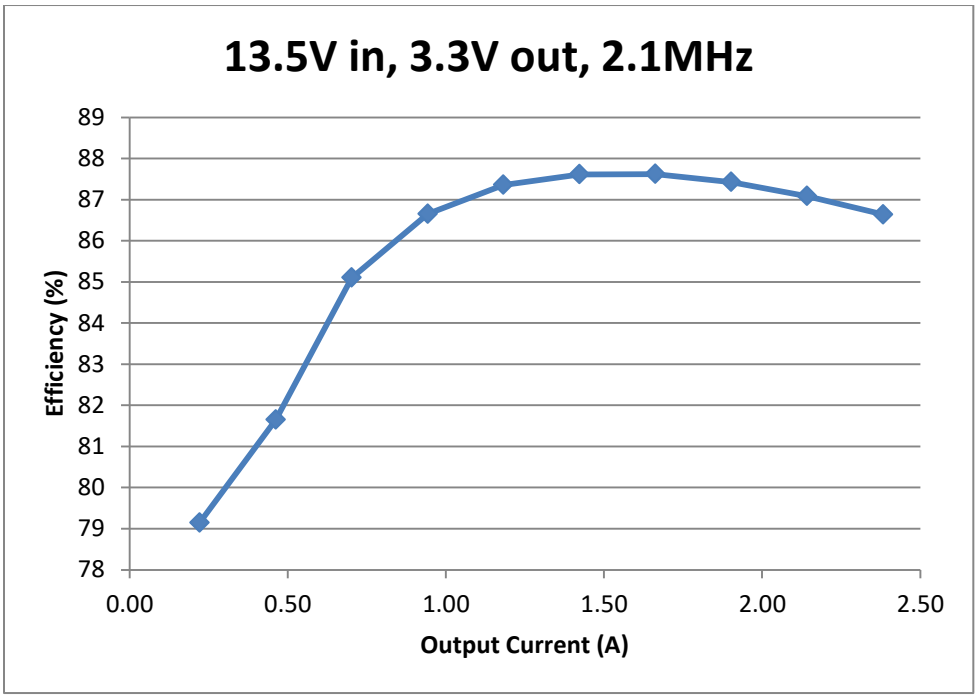


Efficiency Data

VIN	IVIN	ILOAD	VOUT	EFFI%
13.53754	0.063788	0.13	5.000467	76.31252
13.50521	0.128417	0.28	4.99667	81.23623
13.47515	0.186641	0.43	4.997967	85.84891
13.44191	0.24593	0.58	4.999238	88.05455
13.41703	0.30615	0.73	5.000552	89.17562
13.39089	0.366658	0.88	5.001928	89.79615
13.36667	0.428836	1.03	5.00331	90.05561
13.29226	0.493066	1.18	5.004844	90.27205
13.28744	0.556176	1.33	5.006302	90.26951
13.28884	0.619688	1.48	5.007766	90.15091

2.1.2 3V3 output rail

Efficiency was taken with the converter operating with 13.5V input, 3.3V output using an automated efficiency measurement station. The input was connected directly at the input of the converter. All other parts of the board were disabled. Peak efficiency is above 87%. Light load efficiency remains high due to AUTO light load mode.

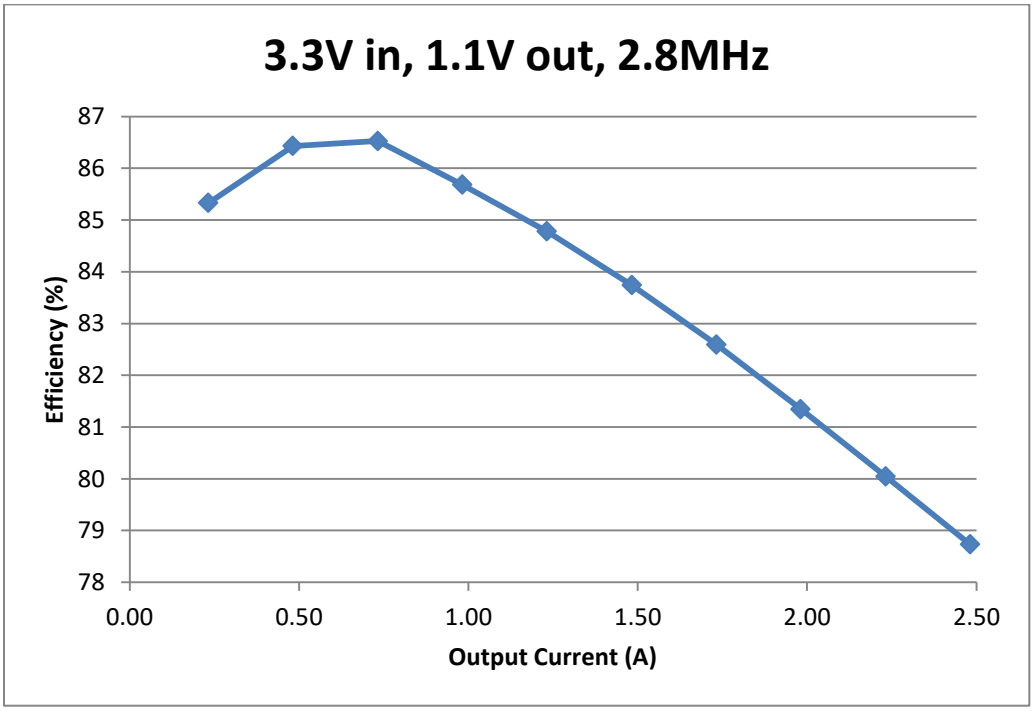


Efficiency Data

VIN	IVIN	ILOAD	VOUT	EFFI%
13.55968	0.068119	0.22	3.309276	79.14174
13.5488	0.138122	0.46	3.305639	81.6529
13.53915	0.201475	0.70	3.306194	85.10186
13.52942	0.265938	0.94	3.306756	86.65412
13.51951	0.33097	1.18	3.307303	87.3572
13.5094	0.397555	1.42	3.30794	87.61505
13.49928	0.465014	1.66	3.308504	87.62386
13.48889	0.533813	1.90	3.309122	87.42675
13.47826	0.604002	2.14	3.309742	87.08658
13.46737	0.676058	2.38	3.310595	86.63716

2.1.3 1V1 output rail

Efficiency was taken with the converter operating with 3.3V input, 1.1V output using an automated efficiency measurement station. The input was connected directly at the input of the converter. All other parts of the board were disabled. Peak efficiency is above 86%. Light load efficiency remains high due to pulse frequency modulation (PFM).



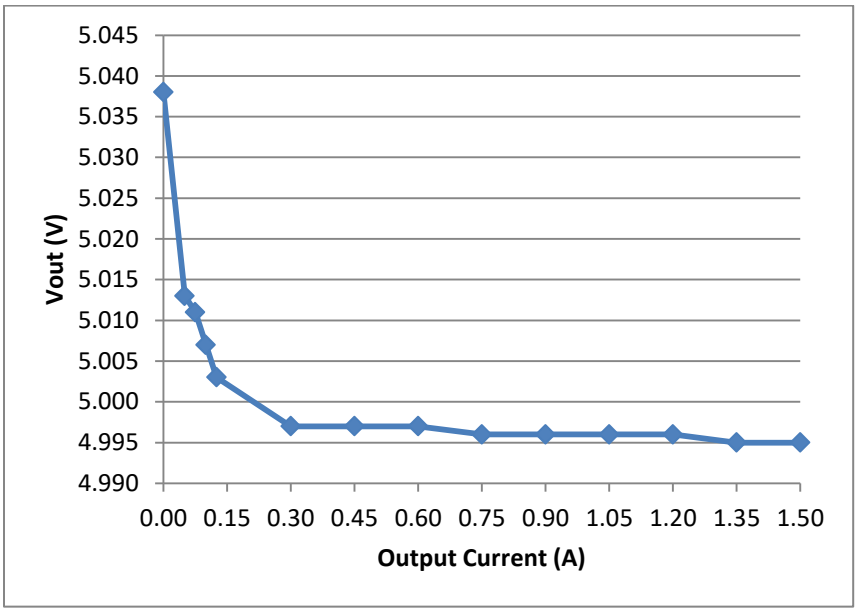
Efficiency Data

VIN	IVIN	ILOAD	VOUT	EFFI%
3.379732	0.088861	0.23	1.101253	85.33105
3.363421	0.182589	0.48	1.101198	86.43064
3.346686	0.278582	0.73	1.101153	86.5253
3.329153	0.379074	0.98	1.101107	85.6837
3.311036	0.483386	1.23	1.101051	84.77915
3.292099	0.592201	1.48	1.100975	83.73952
3.272295	0.705609	1.73	1.100869	82.59464
3.251515	0.824708	1.98	1.100743	81.34415
3.229538	0.950615	2.23	1.100582	80.04318
3.206626	1.081778	2.48	1.100425	78.73236

2.2 Load Regulation

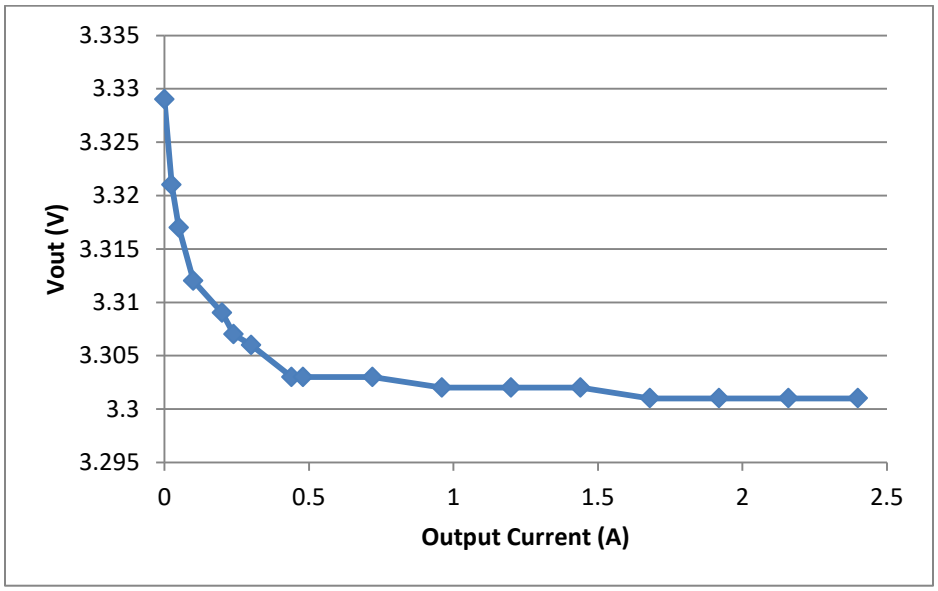
2.2.1 5V output rail

Load regulation test was carried out with the converter operating at 13.5V input, 5V output. The output was measured at the output capacitor C16.The load regulation is less than 1% over the given load range. The average output voltage rises at light load due to PFM.



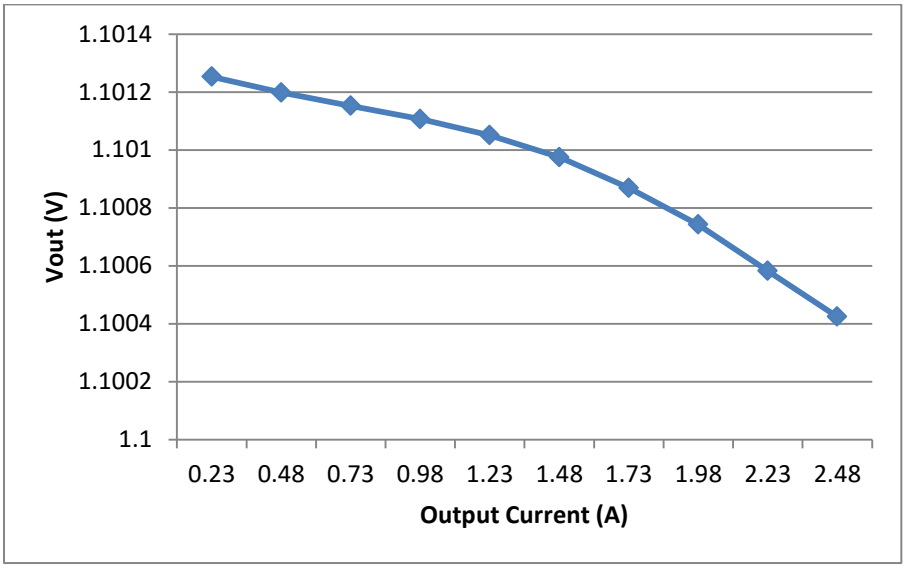
2.2.2 3V3 output rail

Load regulation test was carried out with the converter operating at 13.5V input, 3.3V output. The output was measured at the output capacitor C26.The load regulation is less than 1% over the given load range. The average output voltage rises at light load due to PFM.



2.2.3 1V1 output rail

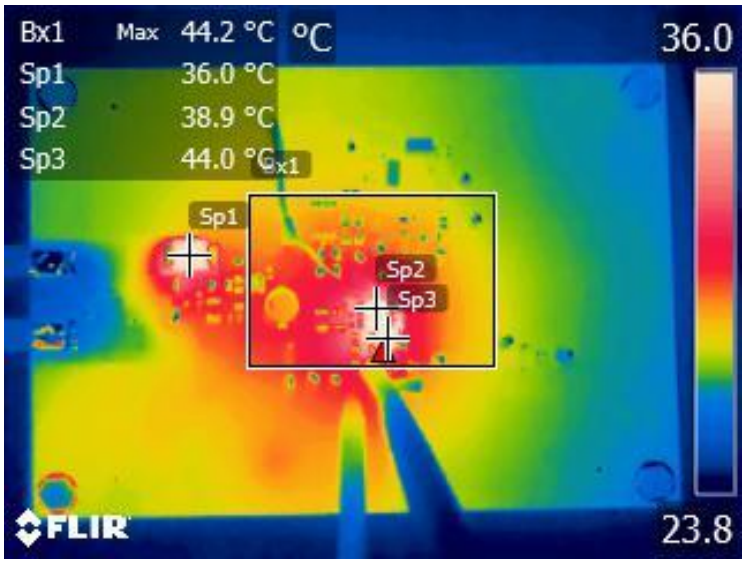
Load regulation data was extracted from the efficiency measurement data. The load regulation is less than 0.11% over the given load range. The average output voltage rises at light load due to PFM.



2.3 Thermal Images

2.3.1 5V output rail

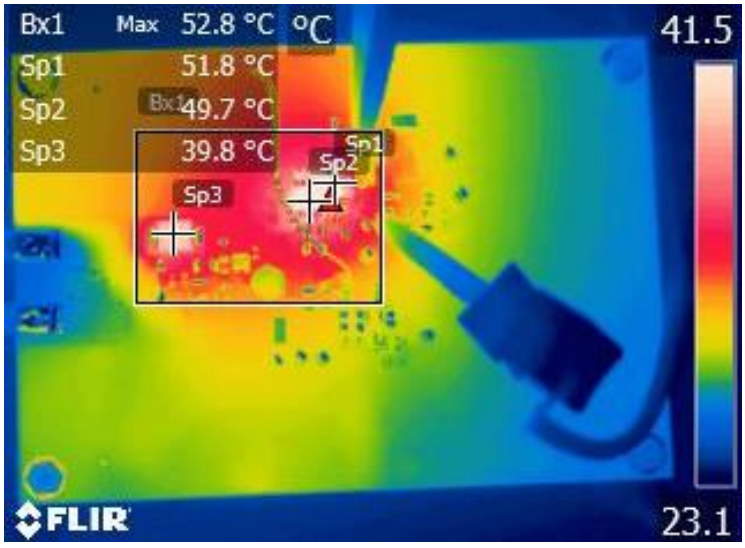
Thermal image was taken with a 1.5A load applied. The converter was operated for approximately 10 minutes before thermal image was taken to ensure thermal steady state was reached.



Label	Component	Temperature
Sp1	D1 (reverse polarity protection diode)	36.0 ºC
Sp2	U1 (LM63615)	38.9 ºC
Sp3	L4(Inductor)	44.0 ºC

2.3.2 3V3 output rail

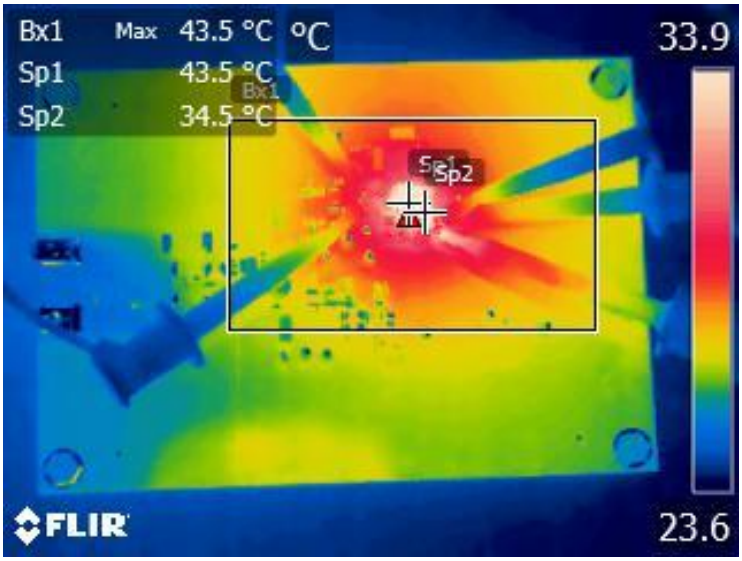
Thermal image was taken with a 2.4A load applied. The converter was operated for approximately 10 minutes before thermal image was taken to ensure thermal steady state was reached.



Label	Component	Temperature
Sp1	L5(Inductor)	51.8 ºC
Sp2	U3 (LM63625)	49.7 ºC
Sp3	D1 (reverse polarity protection diode)	39.8 ºC

2.3.3 1V1 output rail

Thermal image was taken with a 2.5A load applied. A 3.3V input was applied directly at the input of the converter. The converter was operated for approximately 10 minutes before thermal image was taken to ensure thermal steady state was reached.



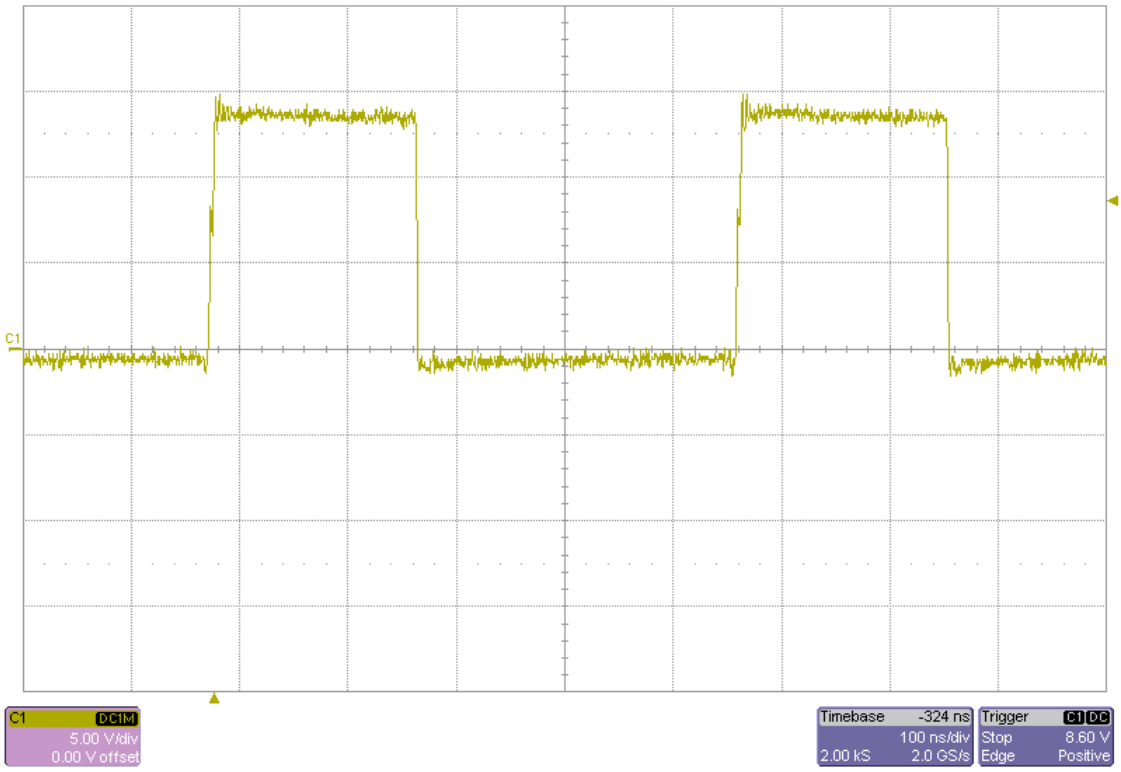
Label	Component	Temperature
Sp1	U4 (TPS62090)	43.5 ºC
Sp2	L6 (Inductor)	34.5 ºC

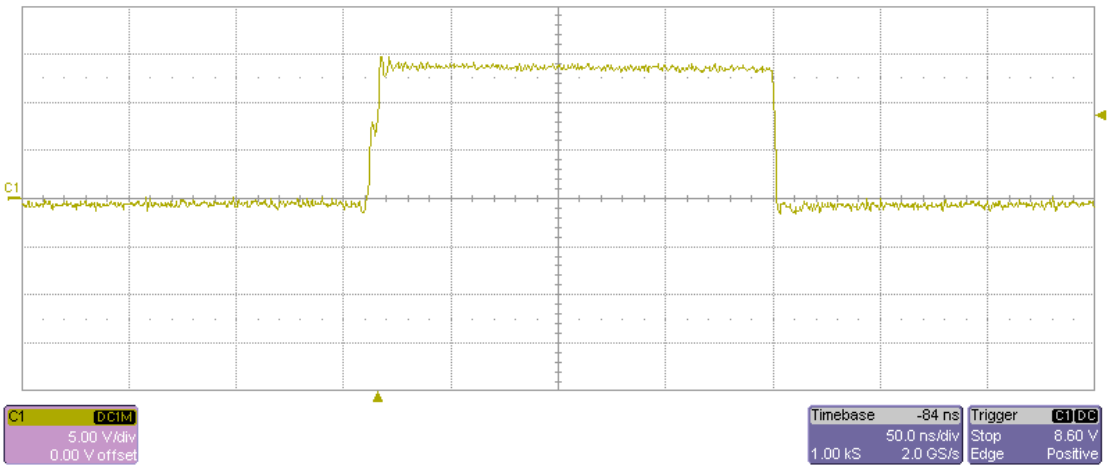
3 Waveforms

3.1 Switching

3.1.1 5V output rail

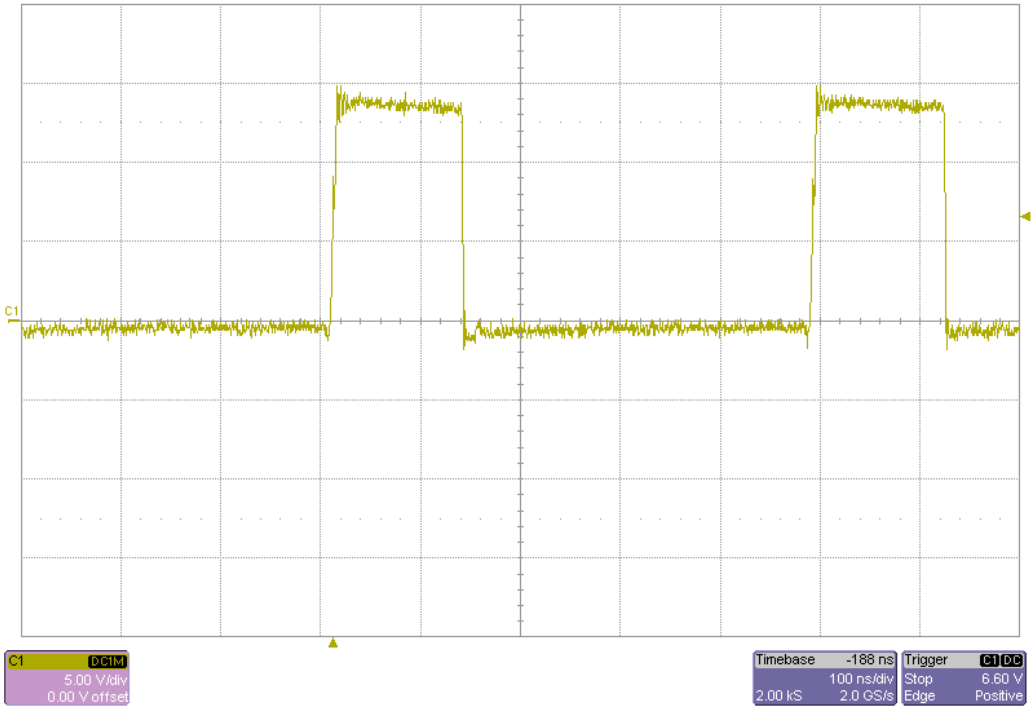
Switch node voltage measurement taken at 1.5A load current.

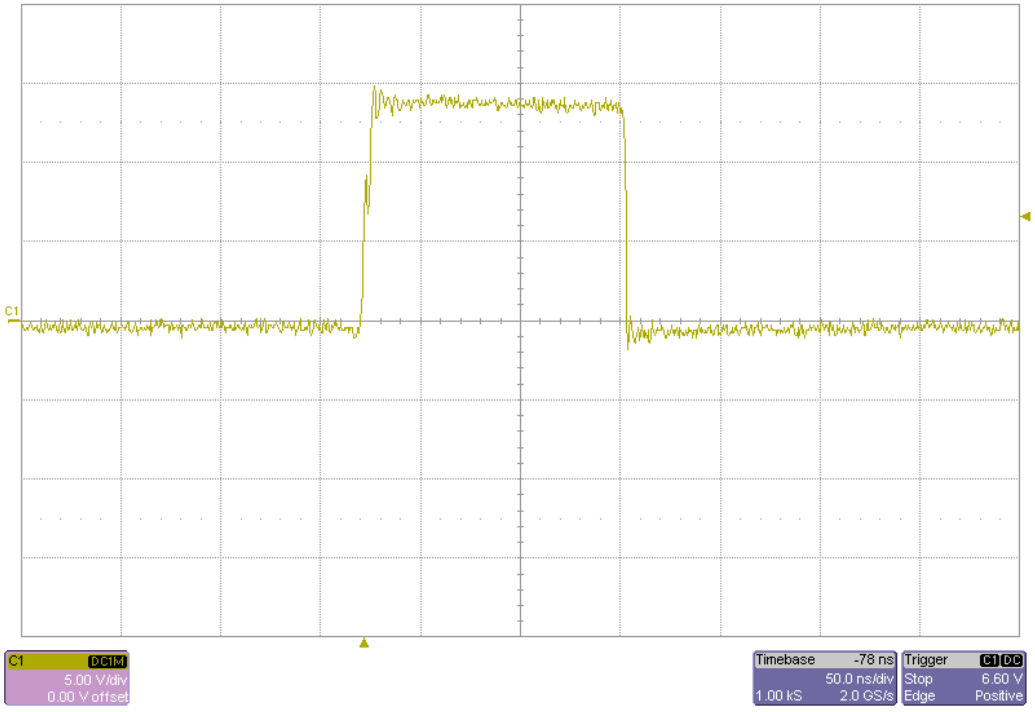




3.1.2 3V3 output rail

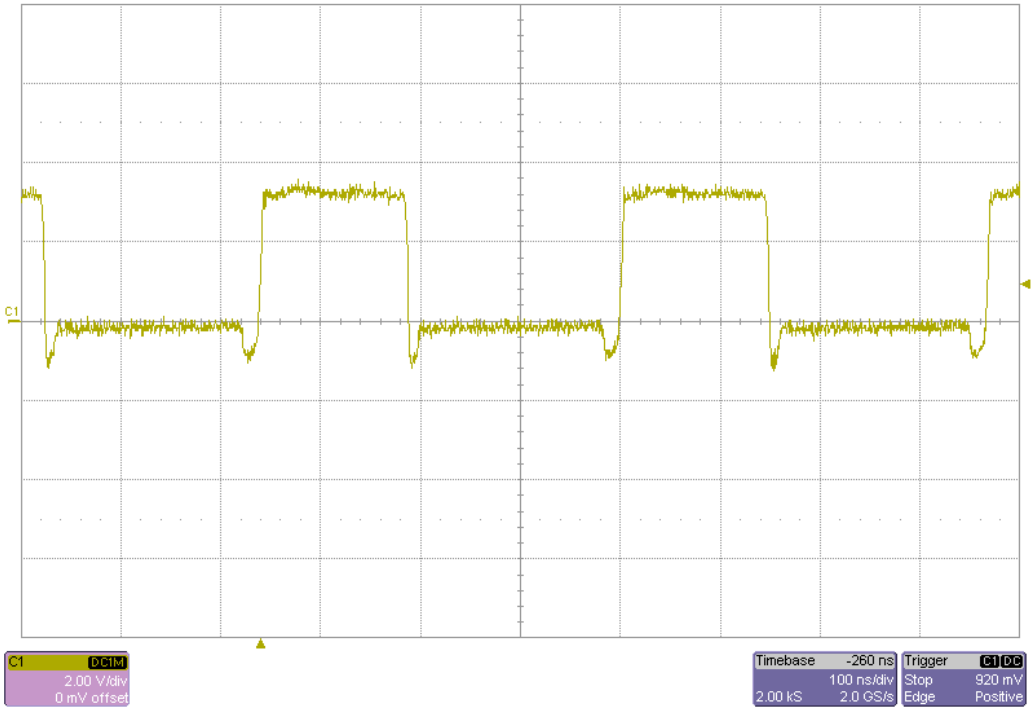
Switch node voltage measurement taken at 2.4A load current.

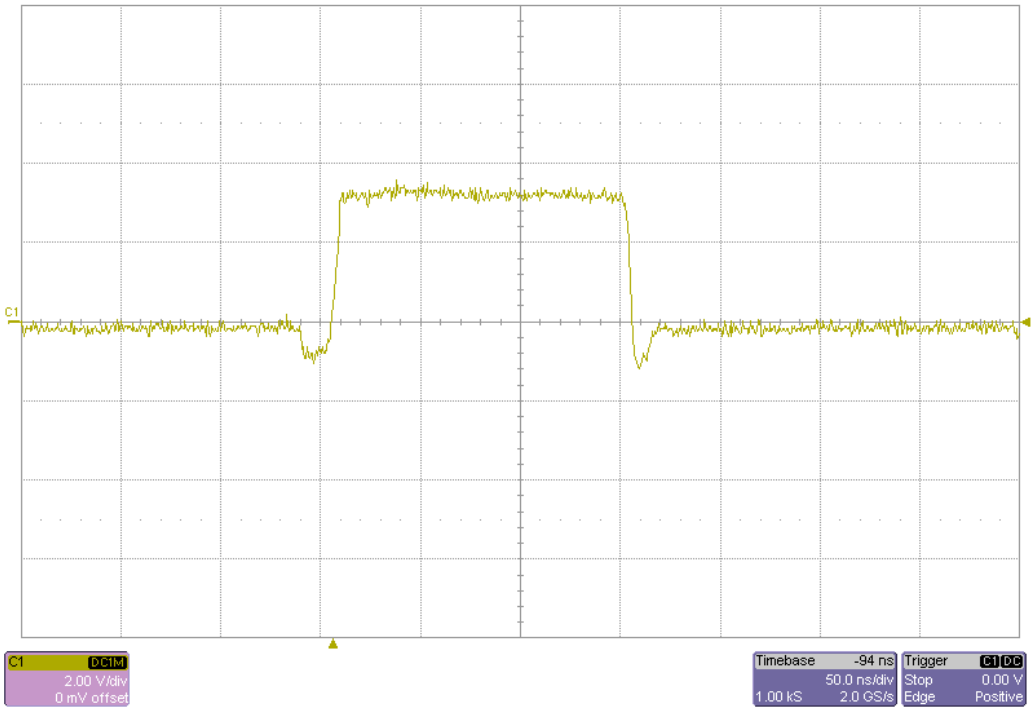




3.1.3 1V1 output rail

Switch node voltage measurement taken at 2.5A load current. A 3.3V input was applied directly at the input of the converter.



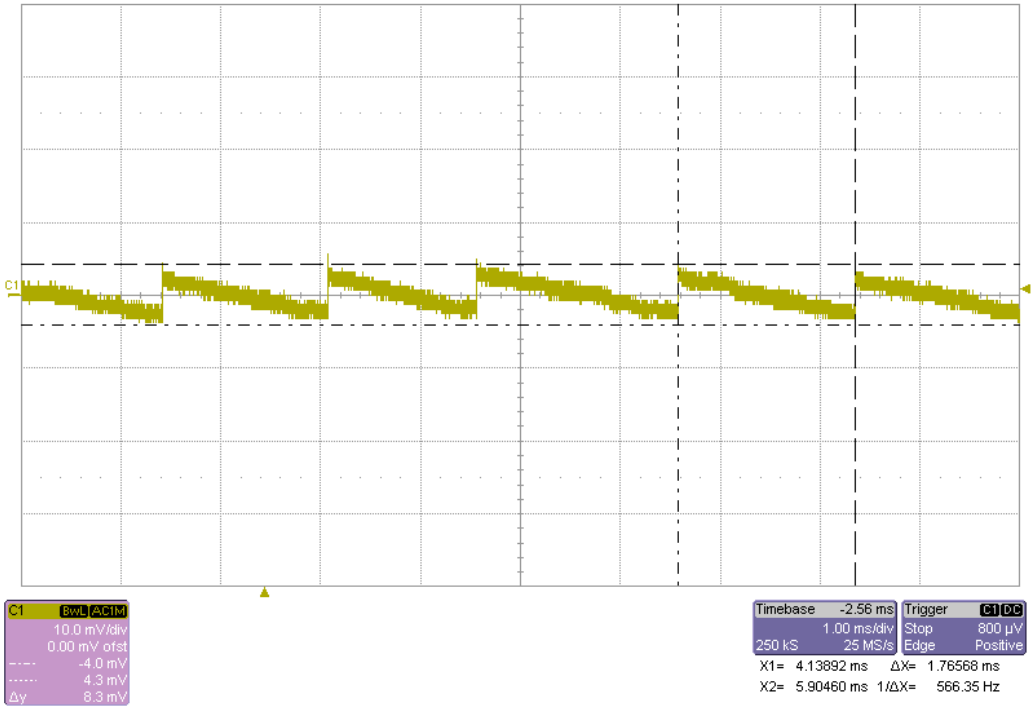


3.2 Output Voltage Ripple

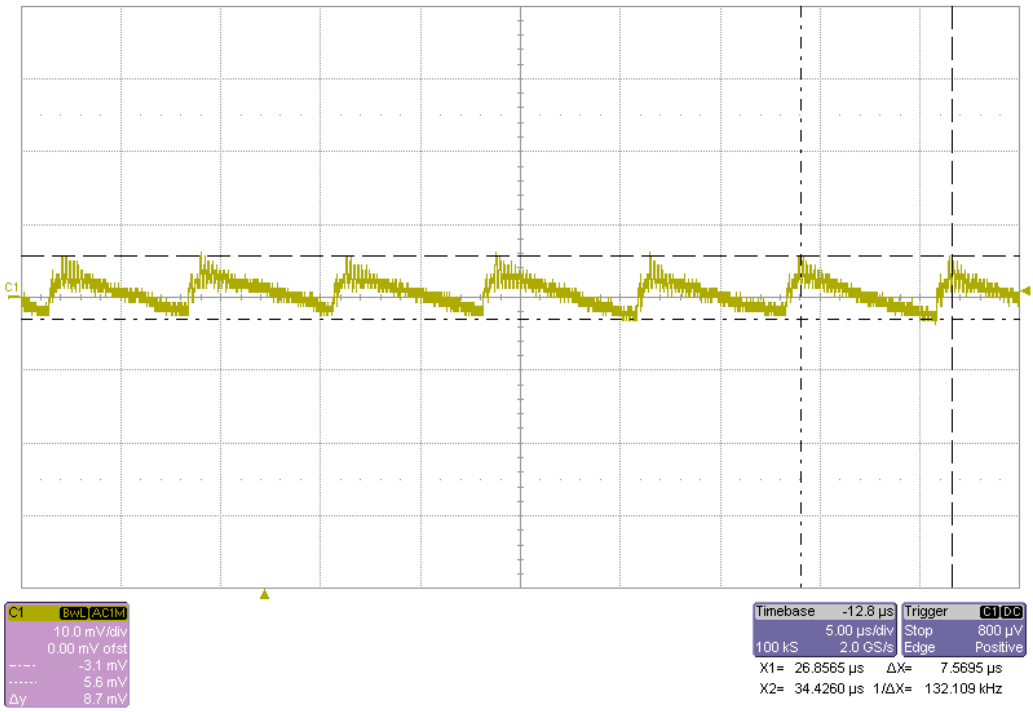
3.2.1 5V output rail

Output voltage was measured at various load current levels. The scope images show the ac coupled measurement. Note the changing time scale for different load levels. Output ripple is less than 25mV for all cases. Scope bandwidth is limited to 20 MHz.

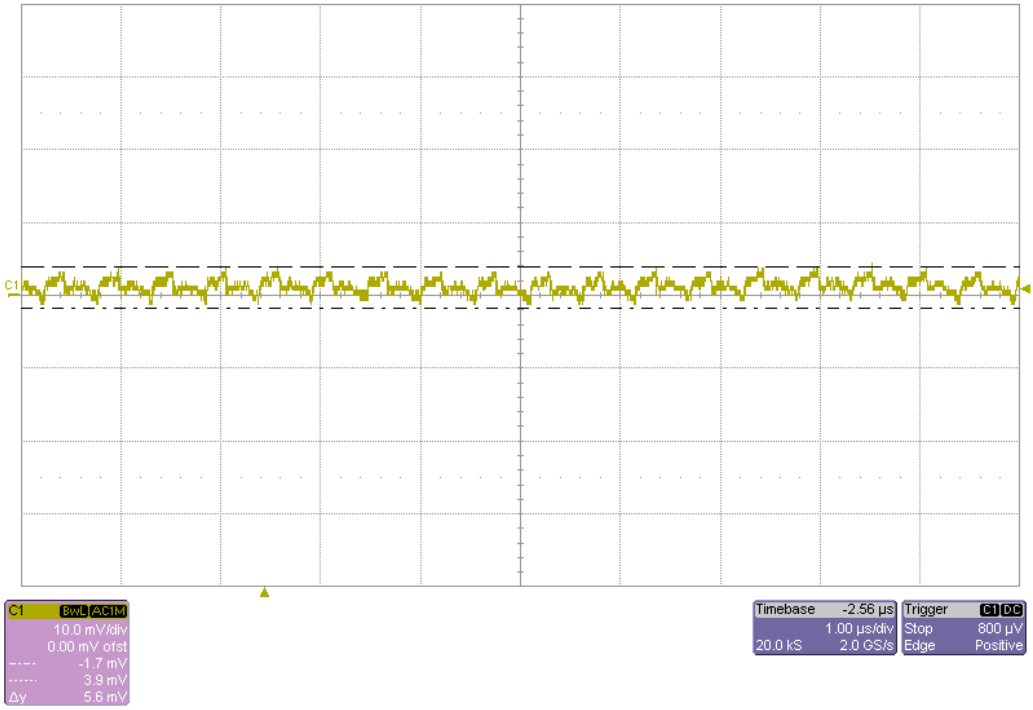
0A Load



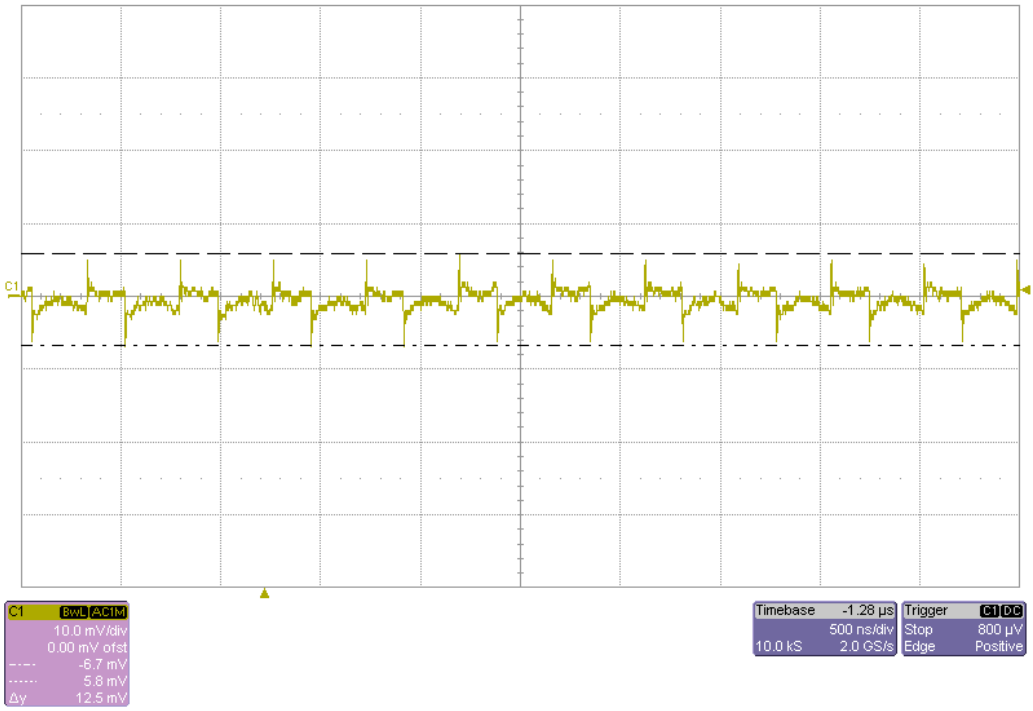
15mA Load



150mA Load



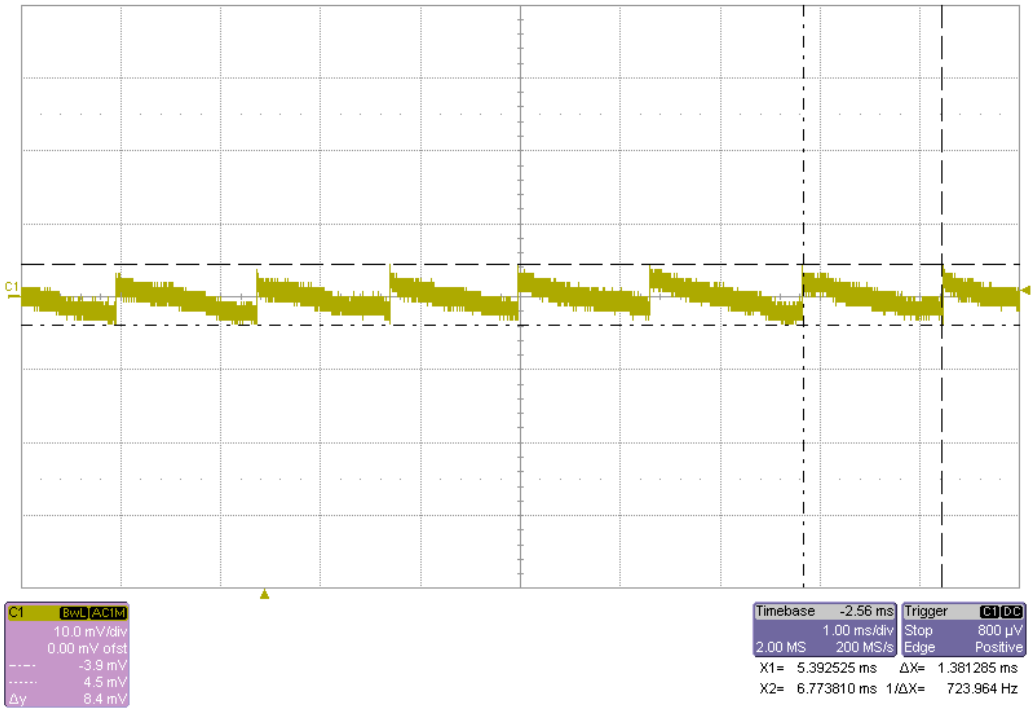
1.5A Load



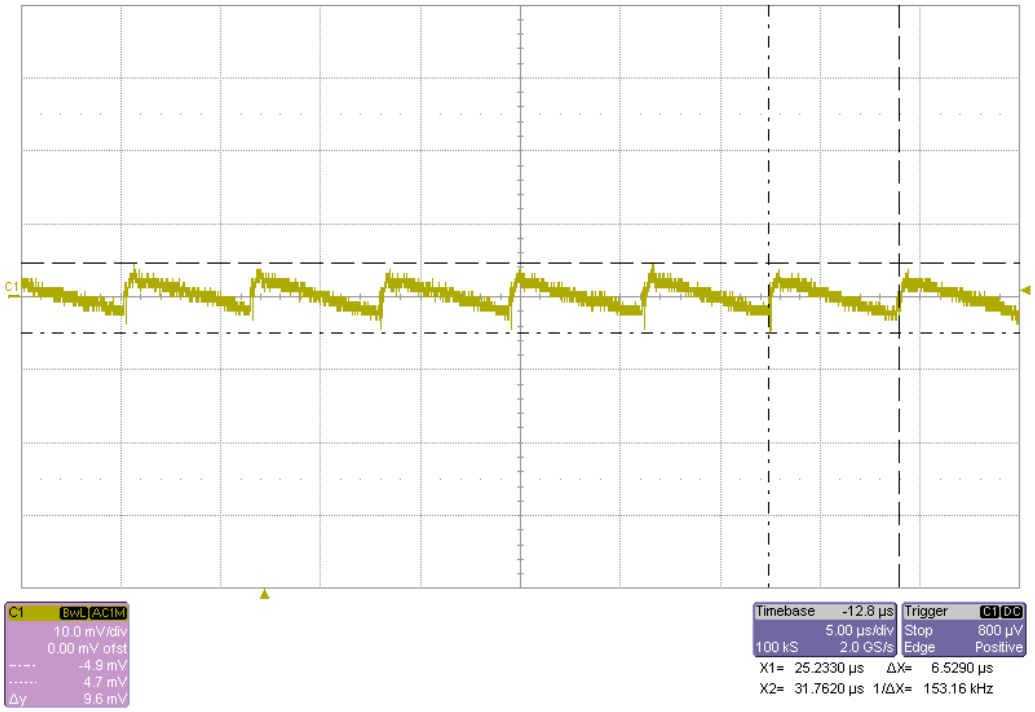
3.2.2 3V3 output rail

Output voltage was measured at various load current levels. The scope images show the ac coupled measurement. Note the changing time scale for different load levels. Output ripple is less than 30mV for all cases. Scope bandwidth is limited to 20 MHz.

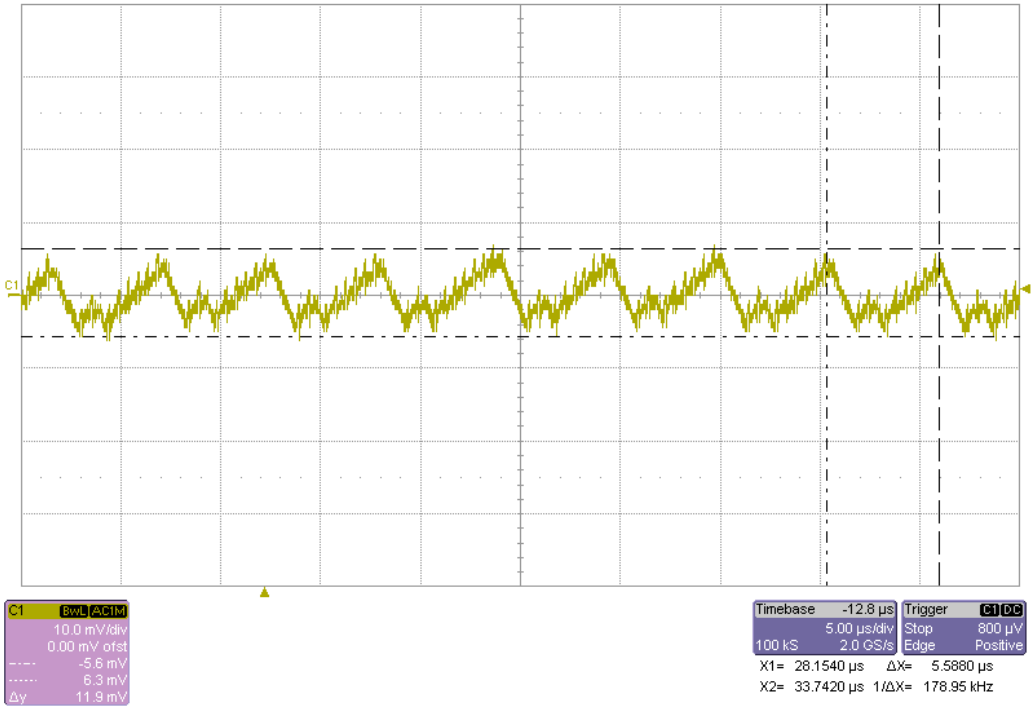
0A Load



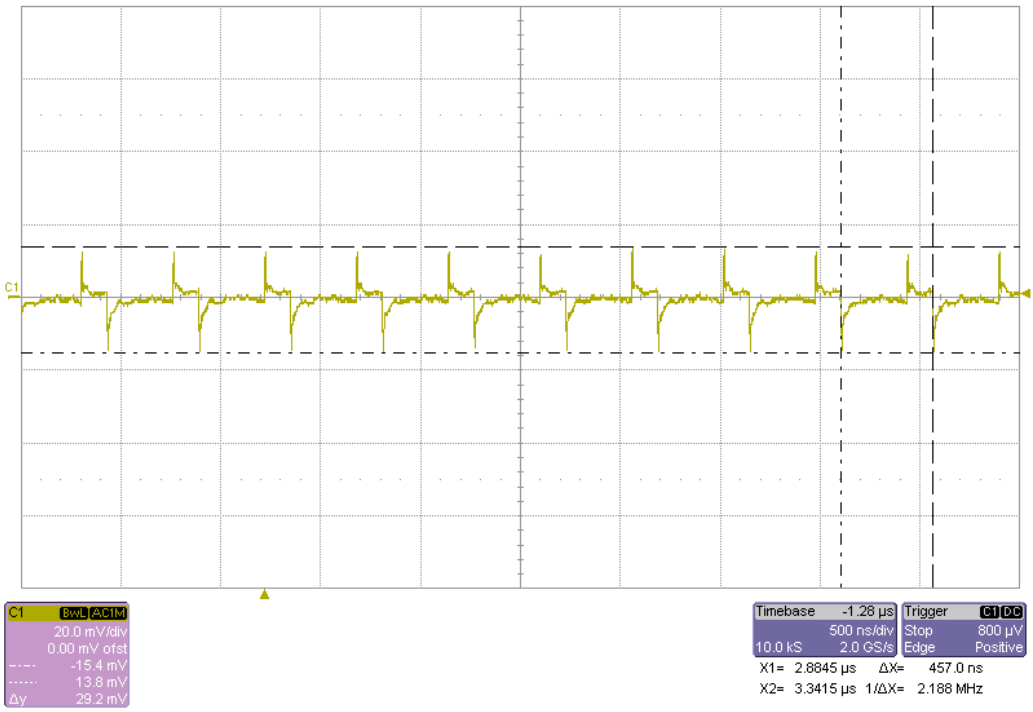
24mA Load



240mA Load



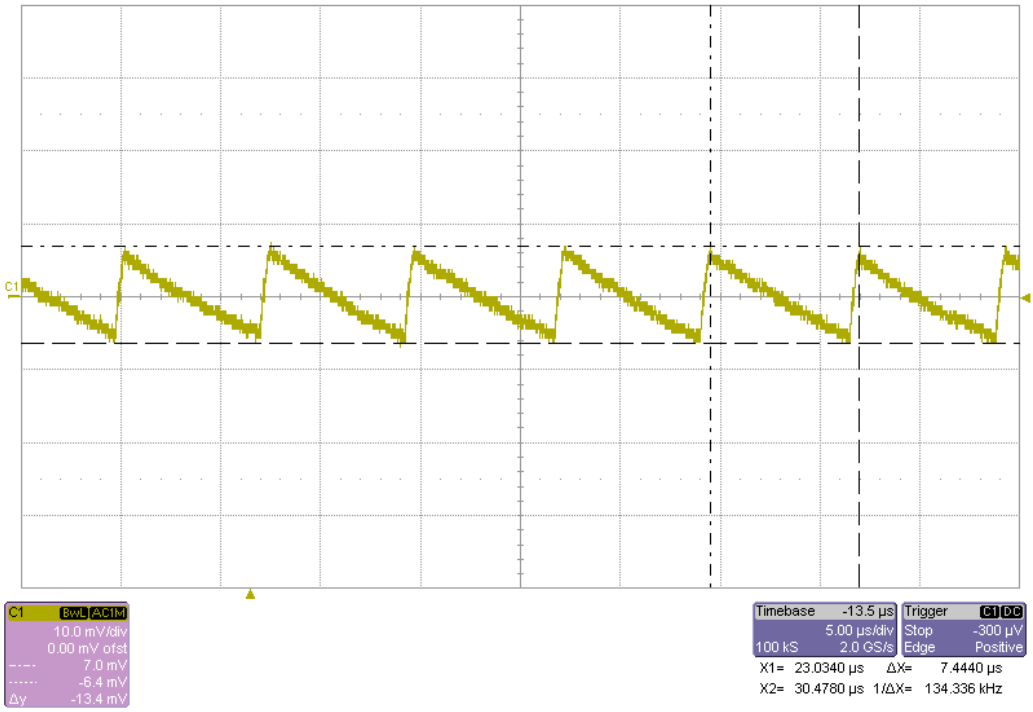
2.4A Load



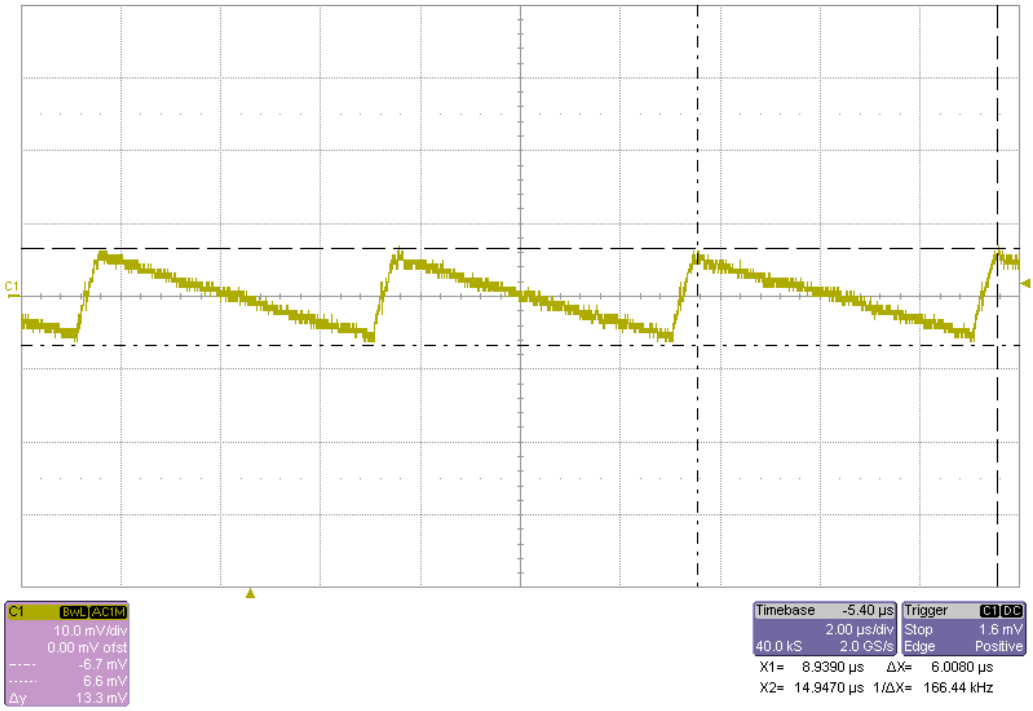
3.2.3 1V1 output rail

Output voltage was measured at various load current levels. A 3.3V input was applied directly at the input of the converter .The scope images show the ac coupled measurement. Note the changing time scale for different load levels. Output ripple is less than 25mV for all cases. Scope bandwidth is limited to 20 MHz.

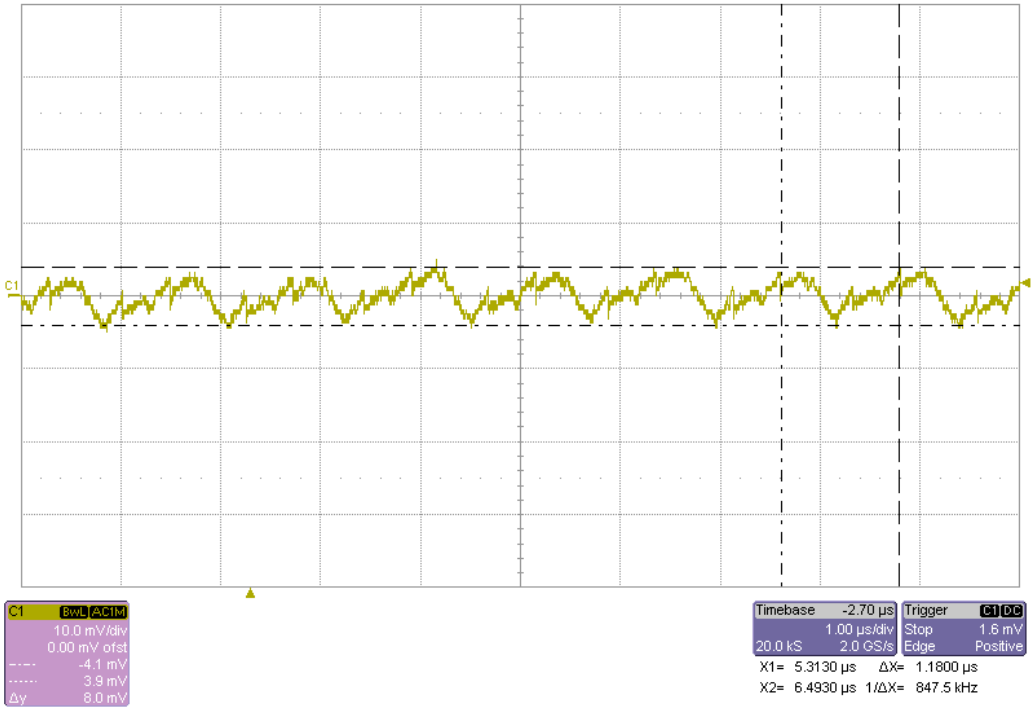
0A Load



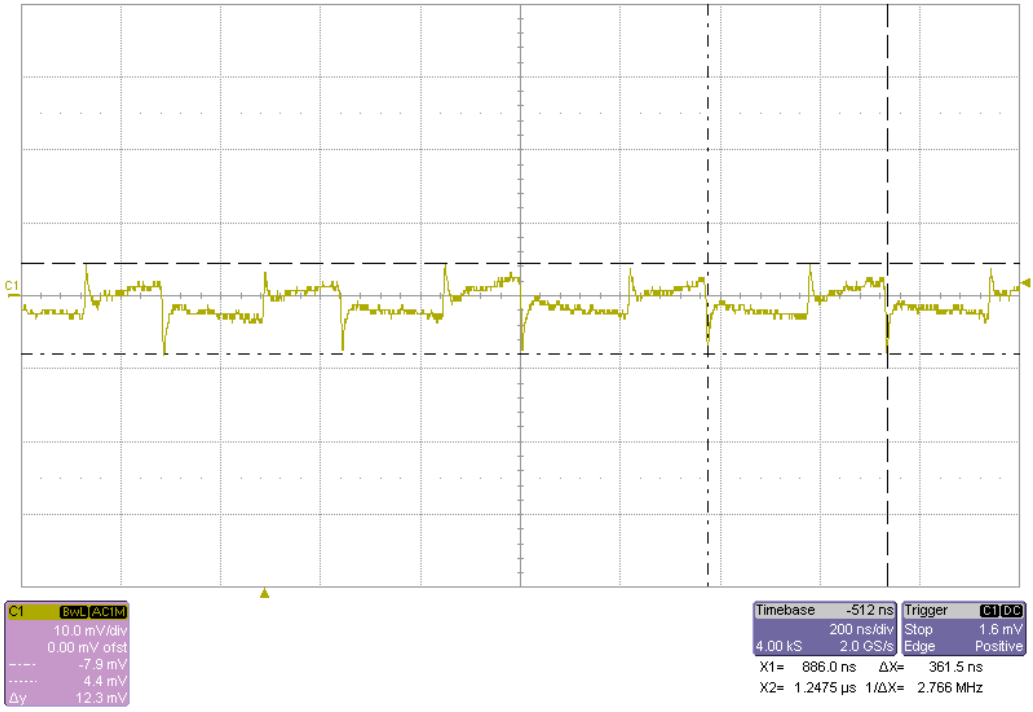
25mA Load



250mA Load



2.5A Load

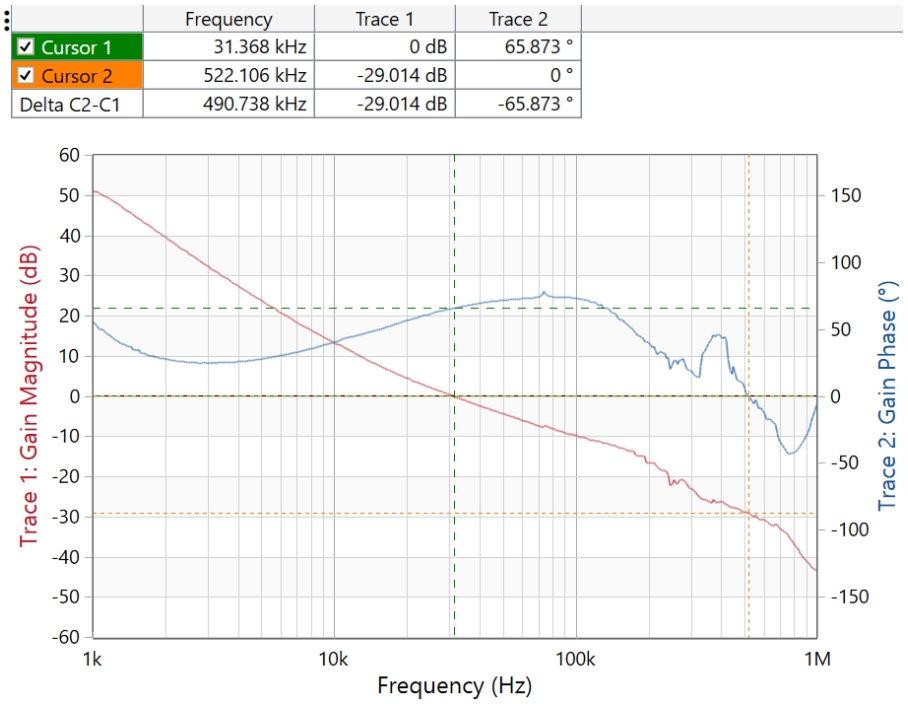


3.3 Bode Plot

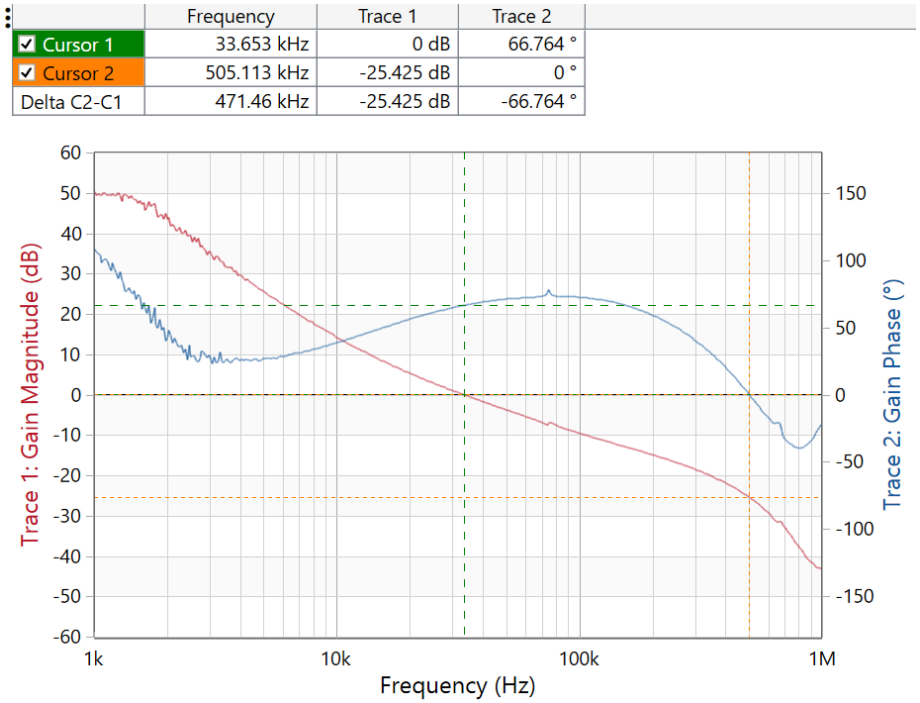
3.3.1 5V output rail

Bode plot measurements taken using an electronic load. The converter exhibits robust stability with phase margin over 65 deg. and gain margin over 25dB in all cases.

0.5A Load



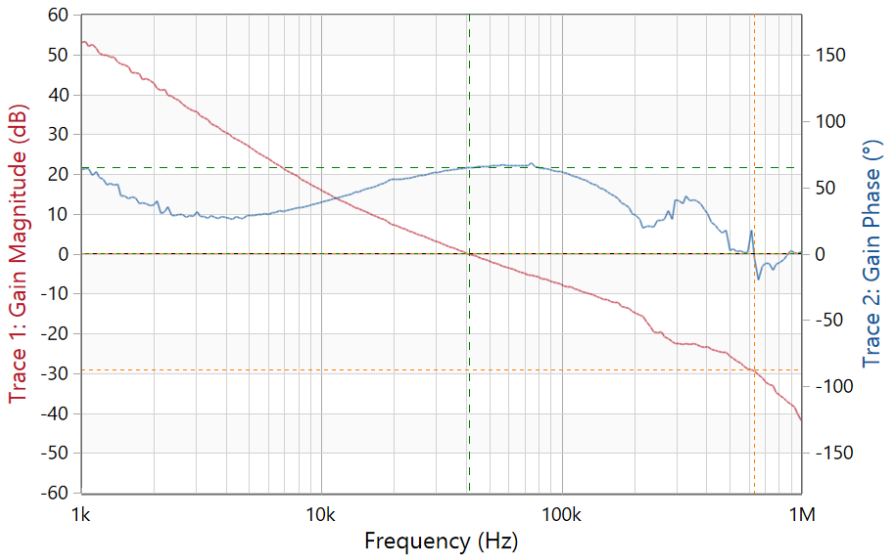
1.5A Load



3.3.2 3V3 output rail

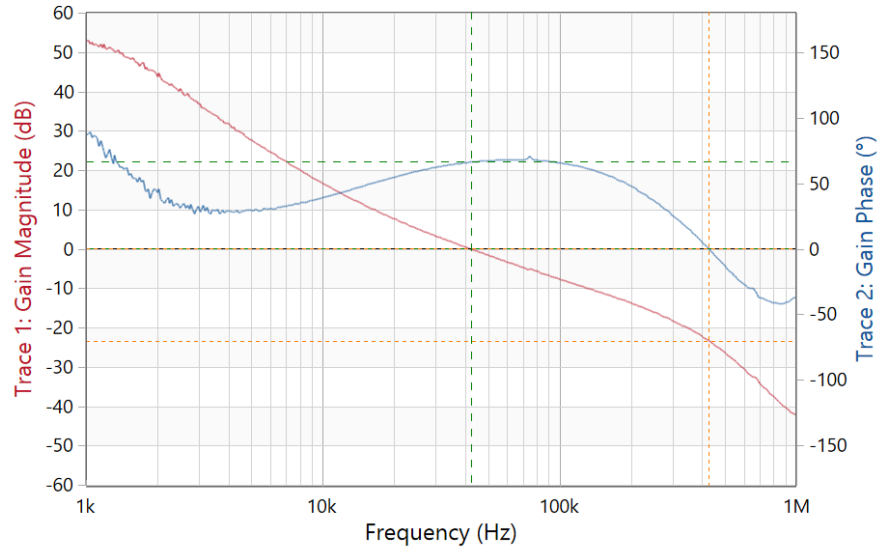
0.5A Load

	Frequency	Trace 1	Trace 2
Cursor 1	41.298 kHz	0 dB	65.113 °
Cursor 2	634.84 kHz	-29.177 dB	0 °
Delta C2-C1	593.542 kHz	-29.177 dB	-65.113 °



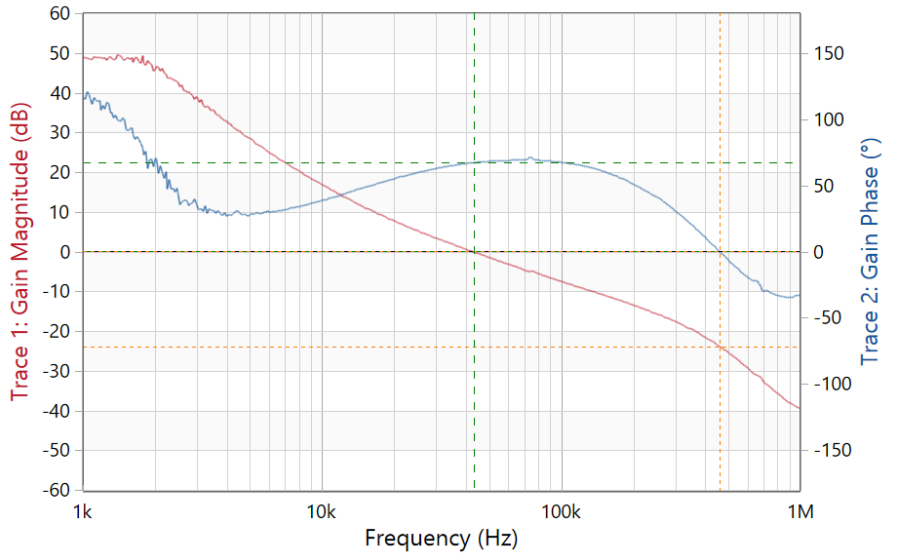
1A Load

	Frequency	Trace 1	Trace 2
Cursor 1	42.408 kHz	0 dB	66.427 °
Cursor 2	429.897 kHz	-23.325 dB	0 °
Delta C2-C1	387.489 kHz	-23.325 dB	-66.427 °



2.4A Load

	Frequency	Trace 1	Trace 2
Cursor 1	43.129 kHz	0 dB	67.446 °
Cursor 2	462.526 kHz	-23.808 dB	0 °
Delta C2-C1	419.398 kHz	-23.808 dB	-67.446 °

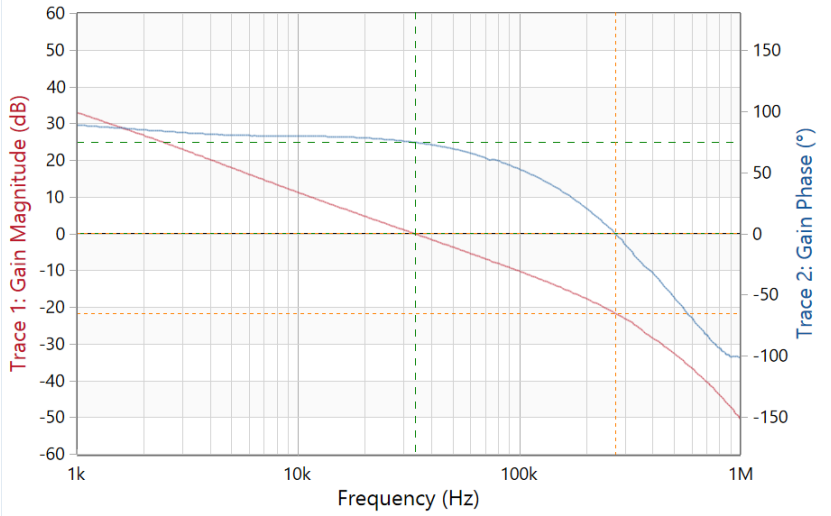


3.3.3 1V1 output rail

Bode plot measurements taken using an electronic load. A 3.3V input was applied directly at the input of the converter. The converter exhibits robust stability with phase margin over 70 deg. and gain margin over 20dB in all cases.

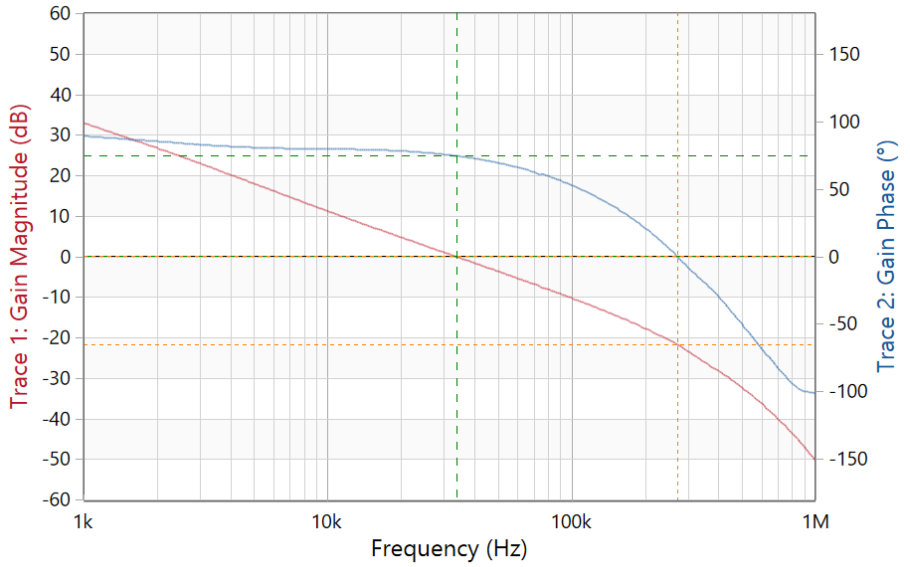
0.5A Load

	Frequency	Trace 1	Trace 2
Cursor 1	33.797 kHz	0 dB	74.665 °
Cursor 2	273.207 kHz	-21.607 dB	0 °
Delta C2-C1	239.41 kHz	-21.607 dB	-74.665 °



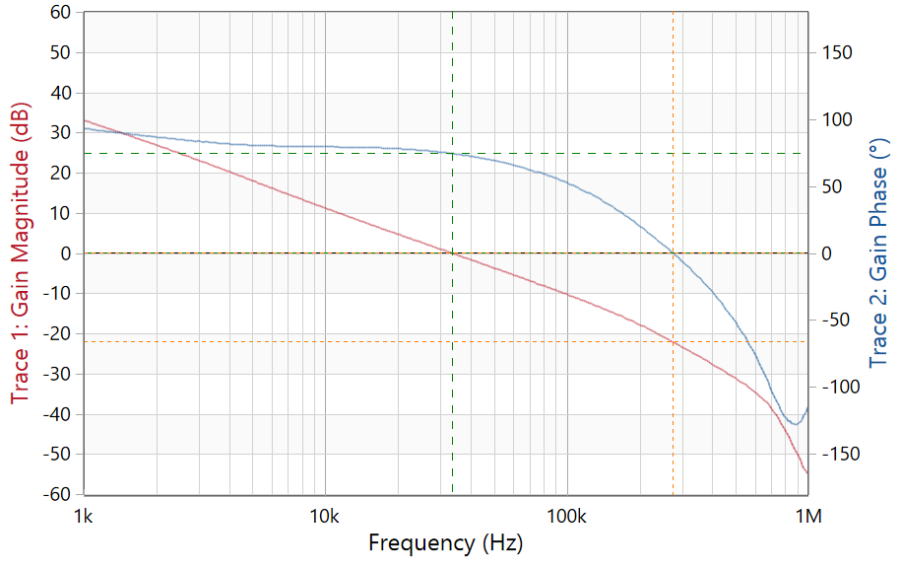
1A Load

	Frequency	Trace 1	Trace 2
Cursor 1	33.816 kHz	0 dB	74.666 °
Cursor 2	272.911 kHz	-21.732 dB	0 °
Delta C2-C1	239.096 kHz	-21.732 dB	-74.666 °



2.5A Load

	Frequency	Trace 1	Trace 2
Cursor 1	33.728 kHz	0 dB	74.545 °
Cursor 2	276.875 kHz	-22.065 dB	0 °
Delta C2-C1	243.148 kHz	-22.065 dB	-74.545 °

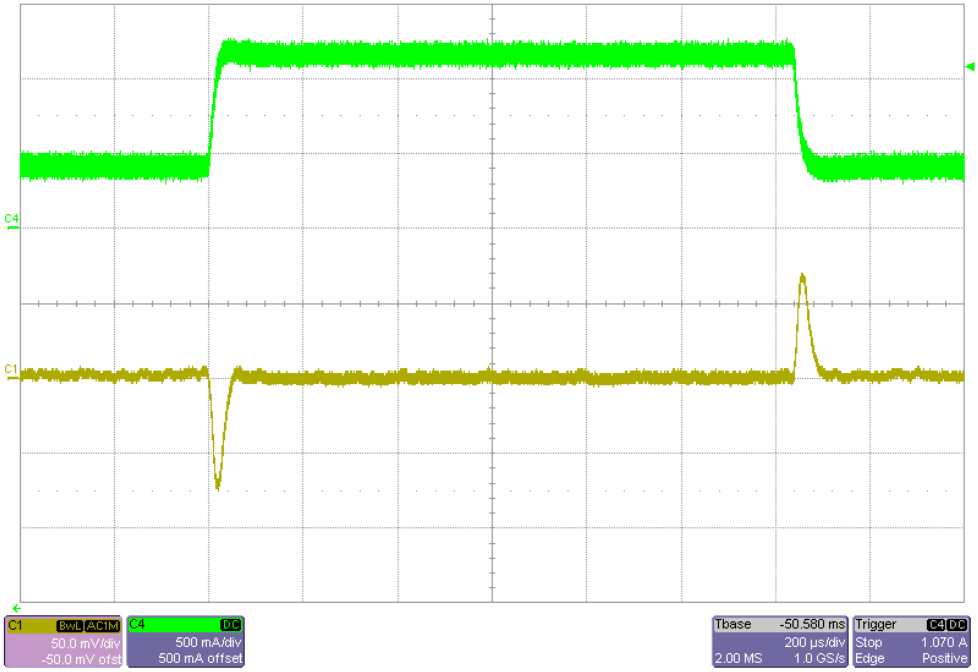


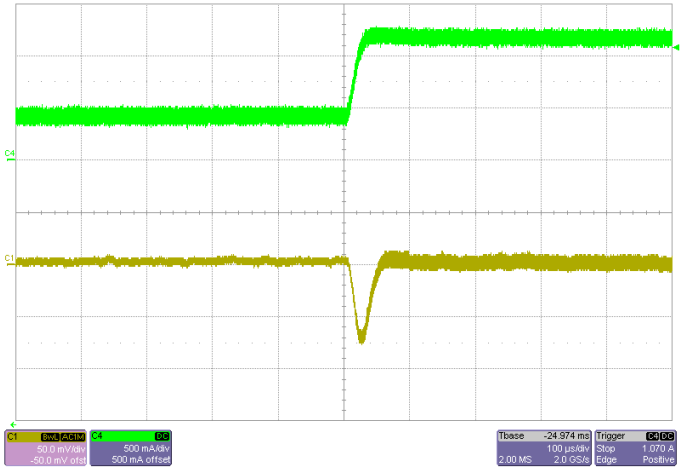
3.4 Load Transients

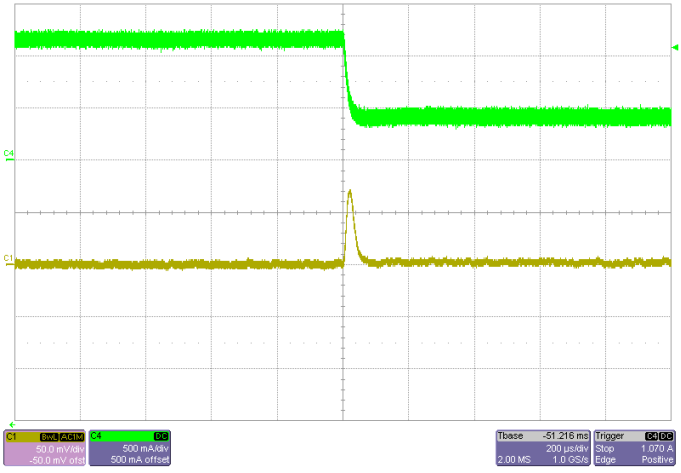
3.4.1 5V output rail

Load step response results show that the output voltage stays within +/-5% under largest load step (100%). Less than +/-2% deviation is observed for 25%-75% load steps. An electronic load was used for applying the load steps. Yellow waveform is VOUT (ac coupled), Green waveform is IOUT.
Load step slew rate: 2.5A/µs, scope bandwidth: 20 MHz

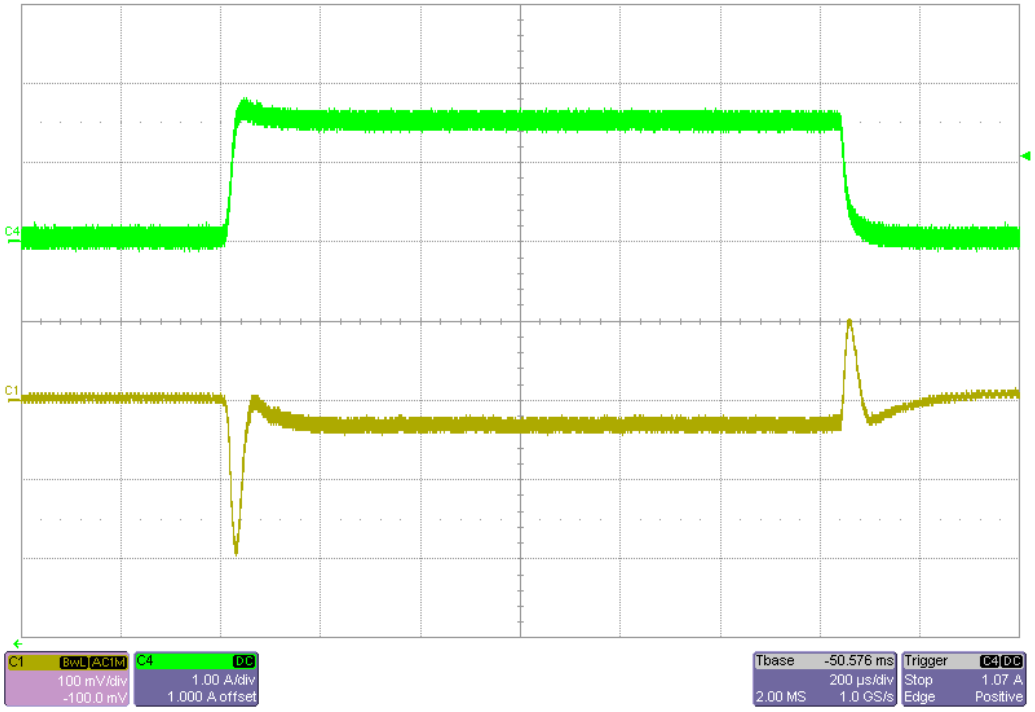
25% to 75%

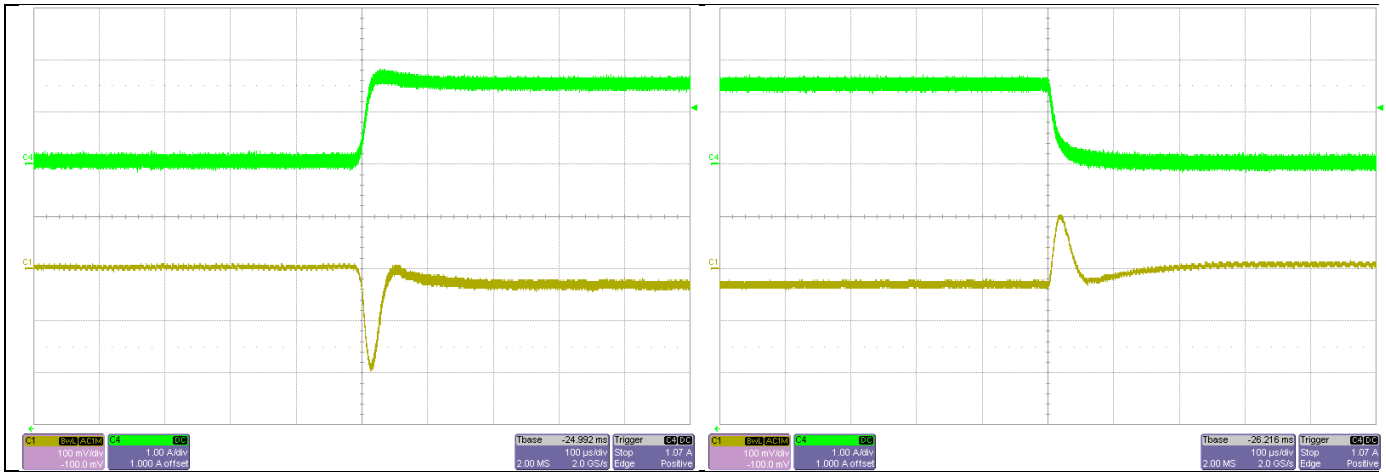






0 to 100%

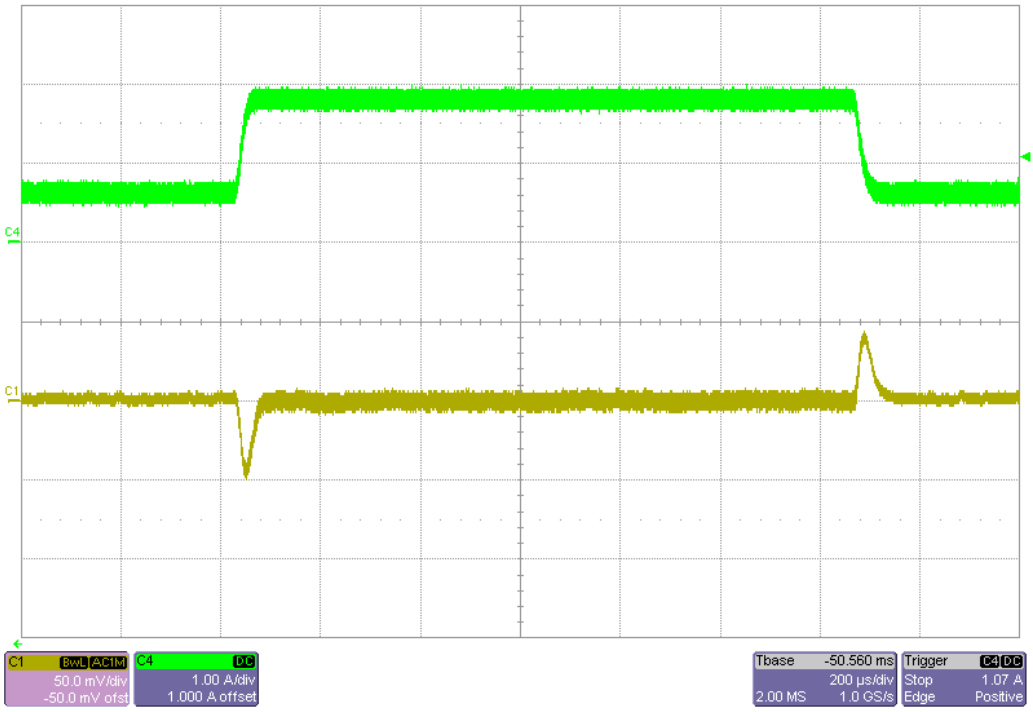


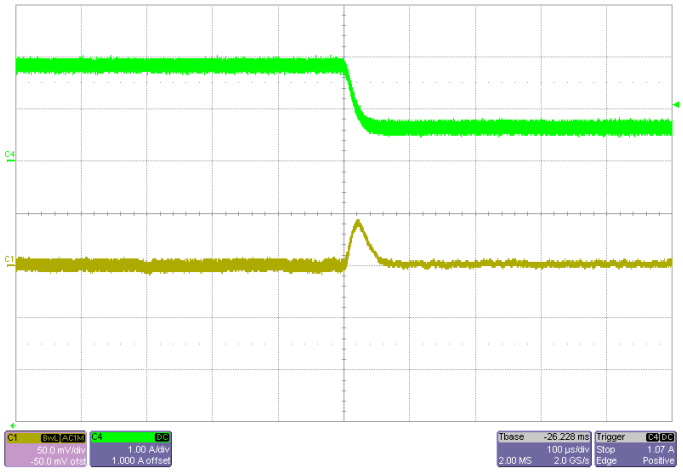


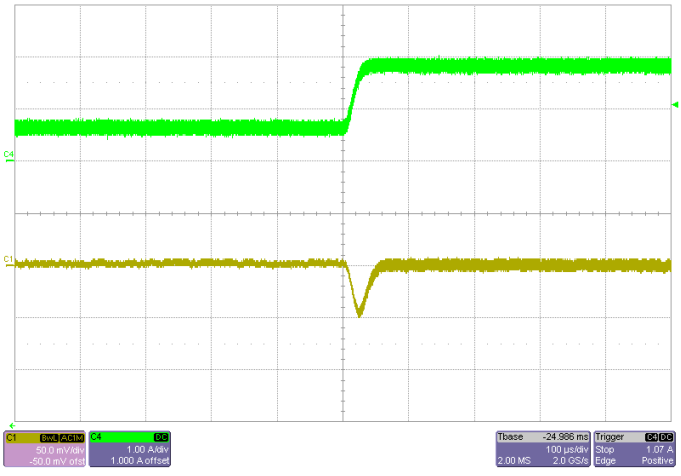
3.4.2 3V3 output rail

Load step response results show that the output voltage stays within +/-5% under largest load step (100%). Less than +/-2% deviation is observed for 25%-75% load steps. An electronic load was used for applying the load steps. Yellow waveform is VOUT (ac coupled), Green waveform is IOUT.
Load step slew rate: 2.5A/µs, scope bandwidth: 20 MHz

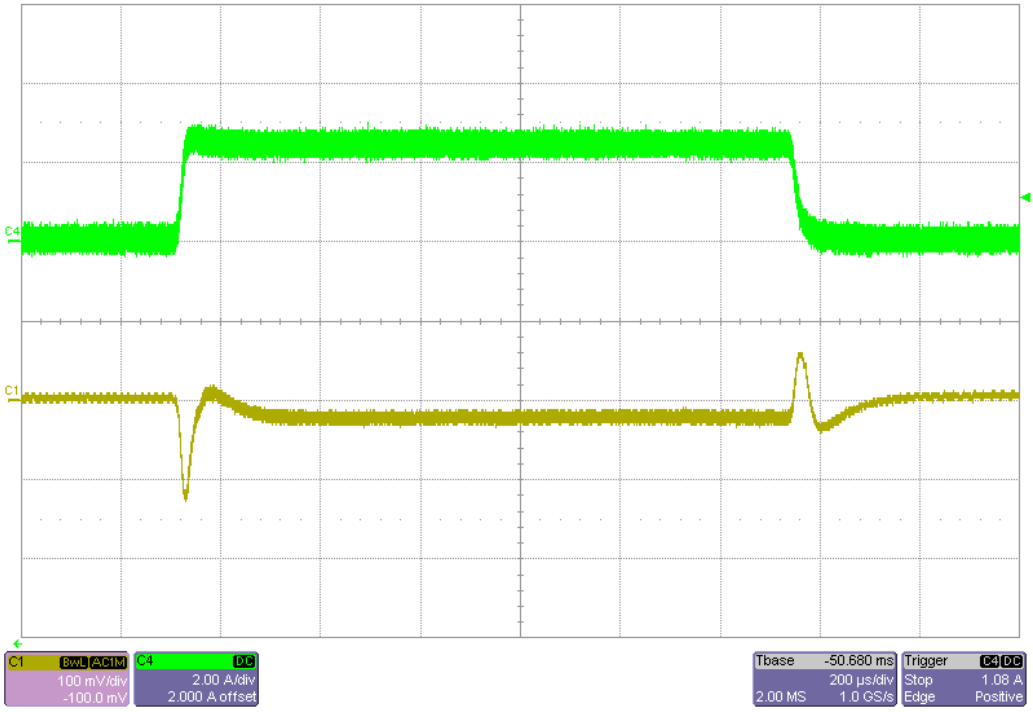
25% to 75%

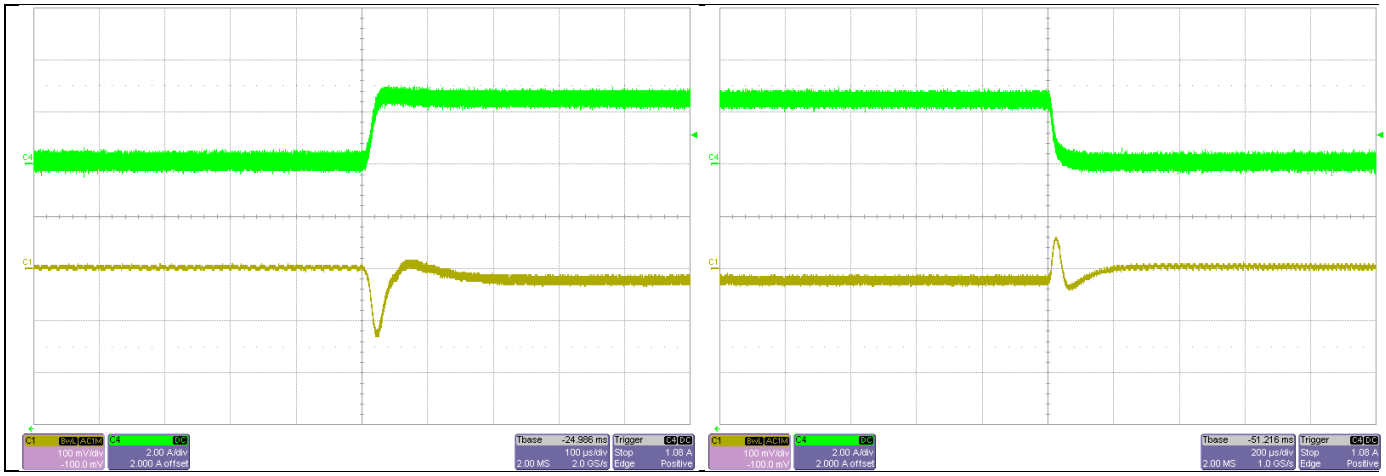






0% to 100%

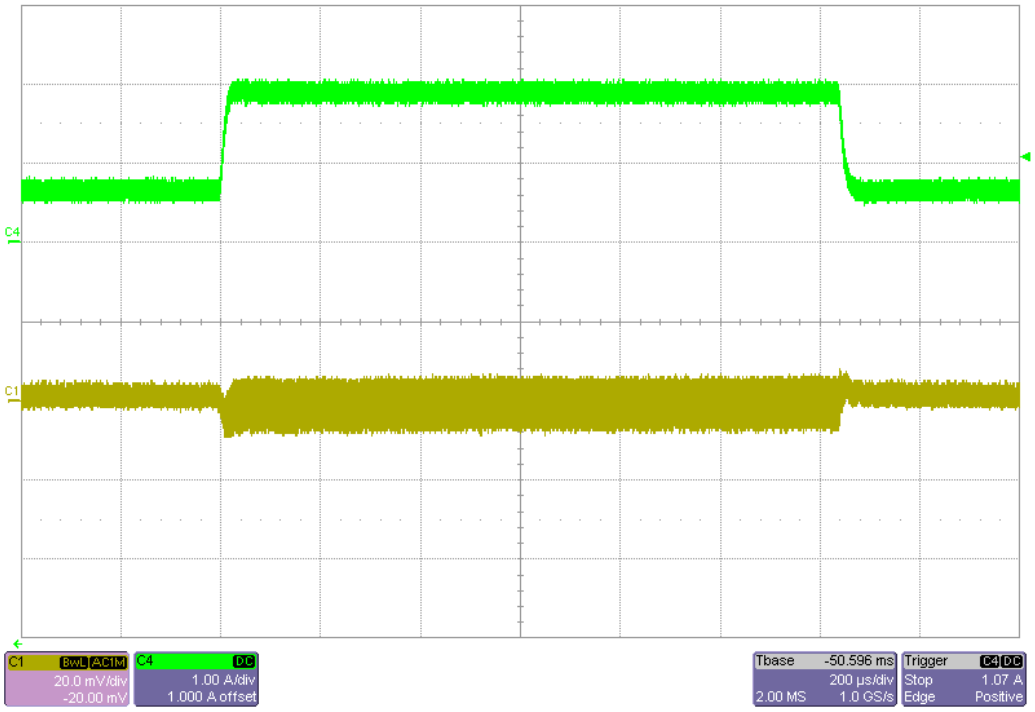


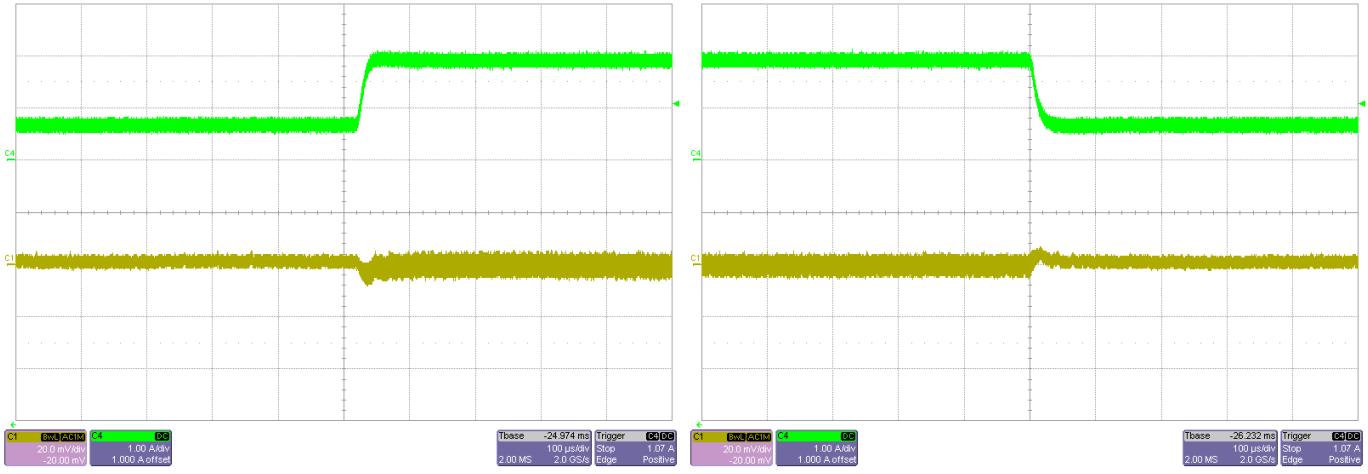


3.4.3 1V1 output rail

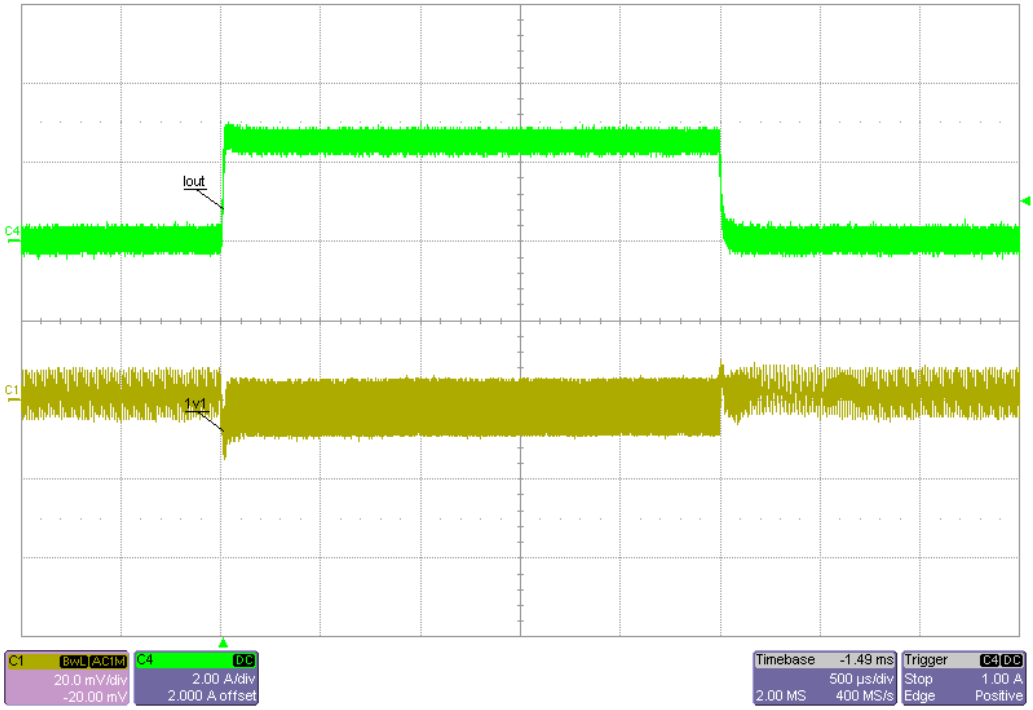
Load step response results show that the output voltage stays within +/-2% under largest load step (100%). Less than +/-1.5% deviation is observed for 25%-75% load steps. An electronic load was used for applying the load steps. Yellow waveform is VOUT (ac coupled), Green waveform is IOUT.
Load step slew rate: 2.5A/µs, scope bandwidth: 20 MHz

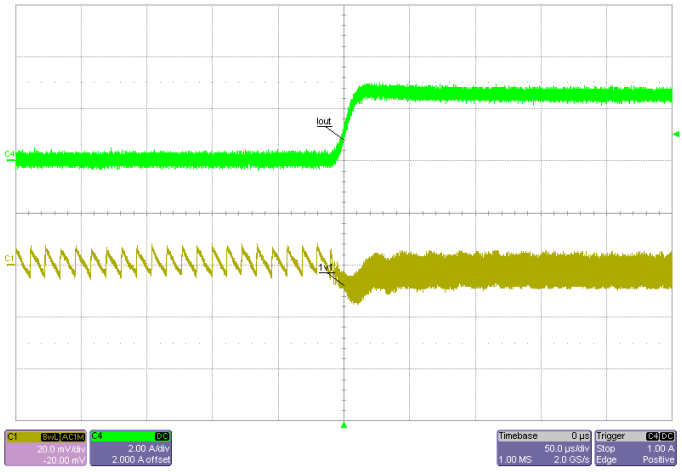
25% to 75%

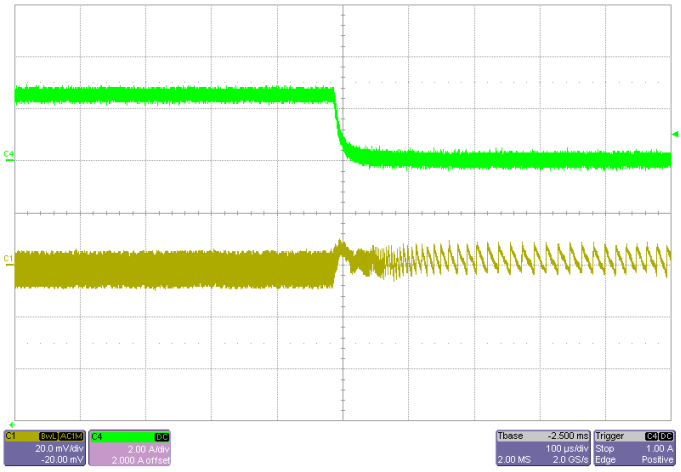




0% to 100%







3.5 Start-up Sequence

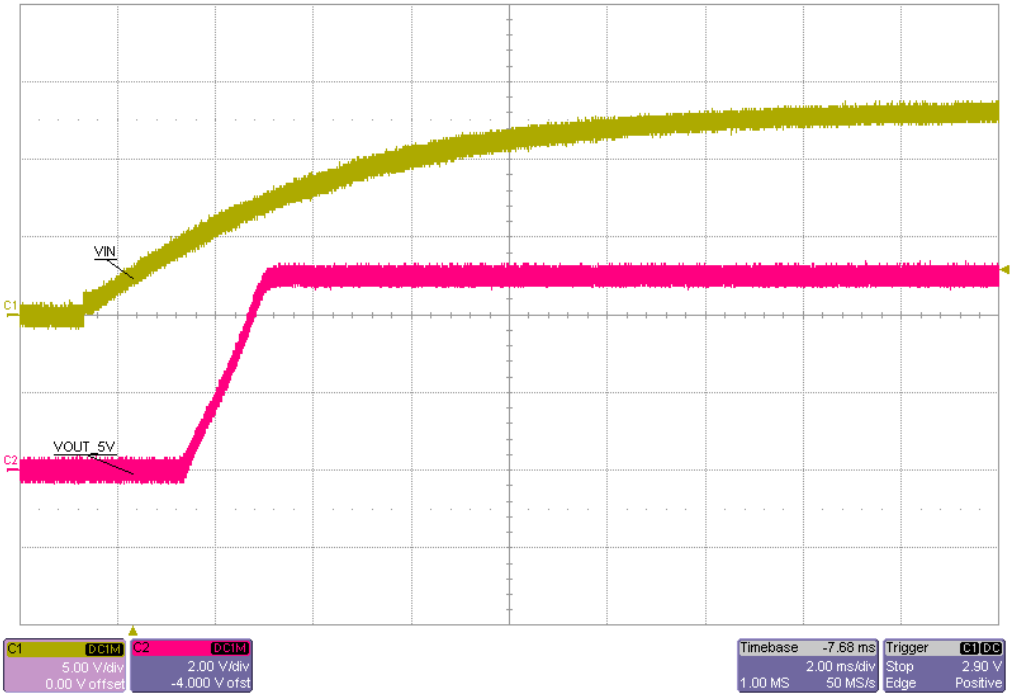
3.5.1 5V output rail

Enable is connected to Vin

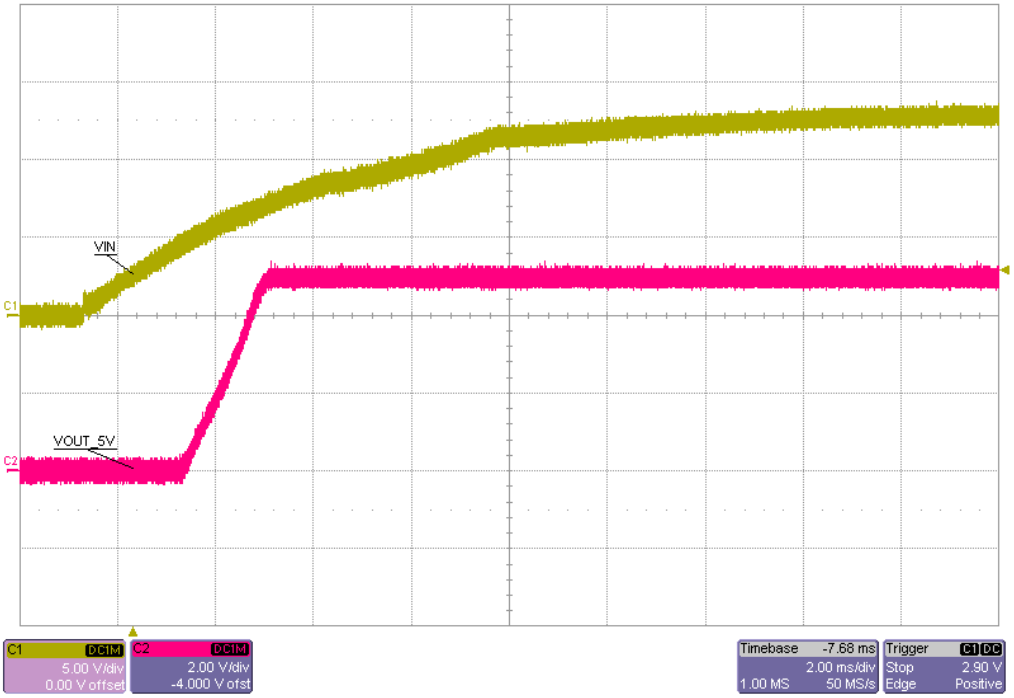
Yellow: Vin 13.5V; Red: Vout 5V;

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



1.5A Load

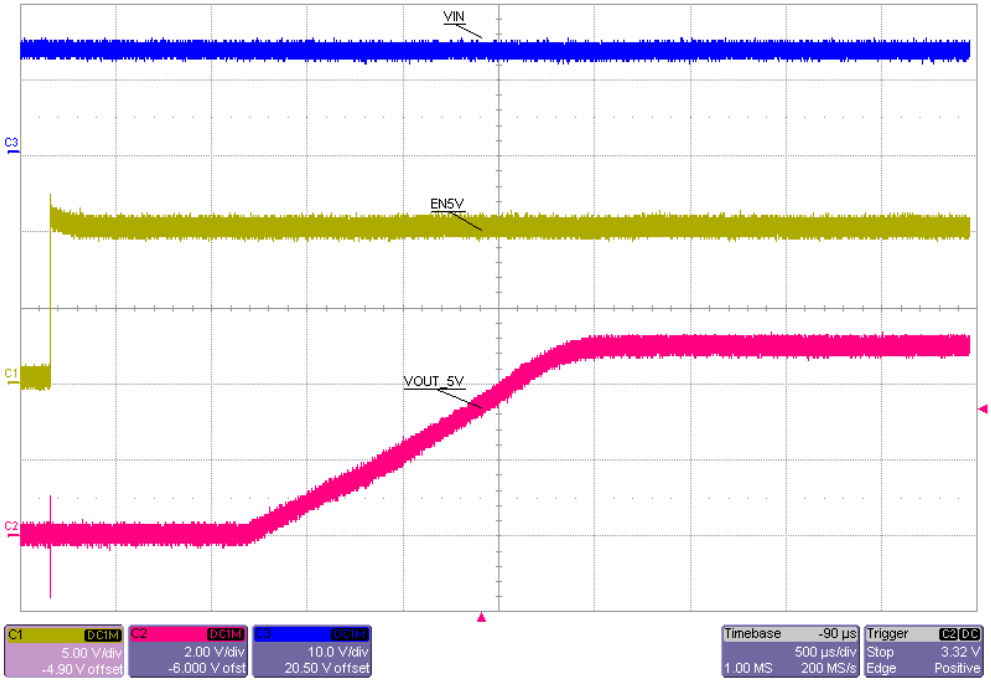


Vin is high and enable is ramped within 10µs

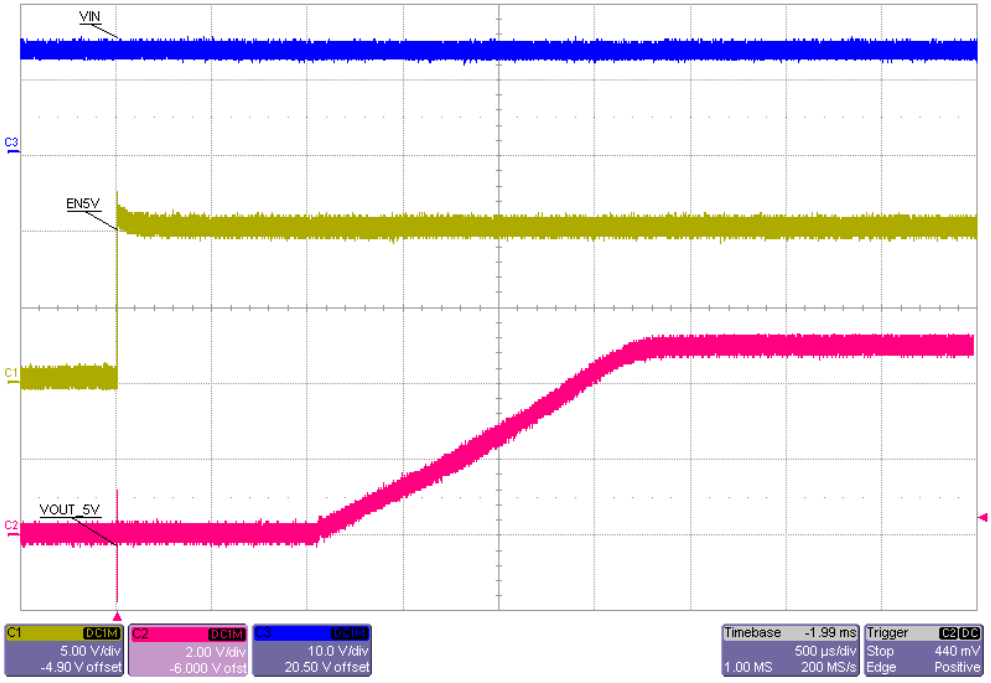
Blue: Vin 13.5V; Red: Vout 5V; Yellow: Enable

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



1.5A Load



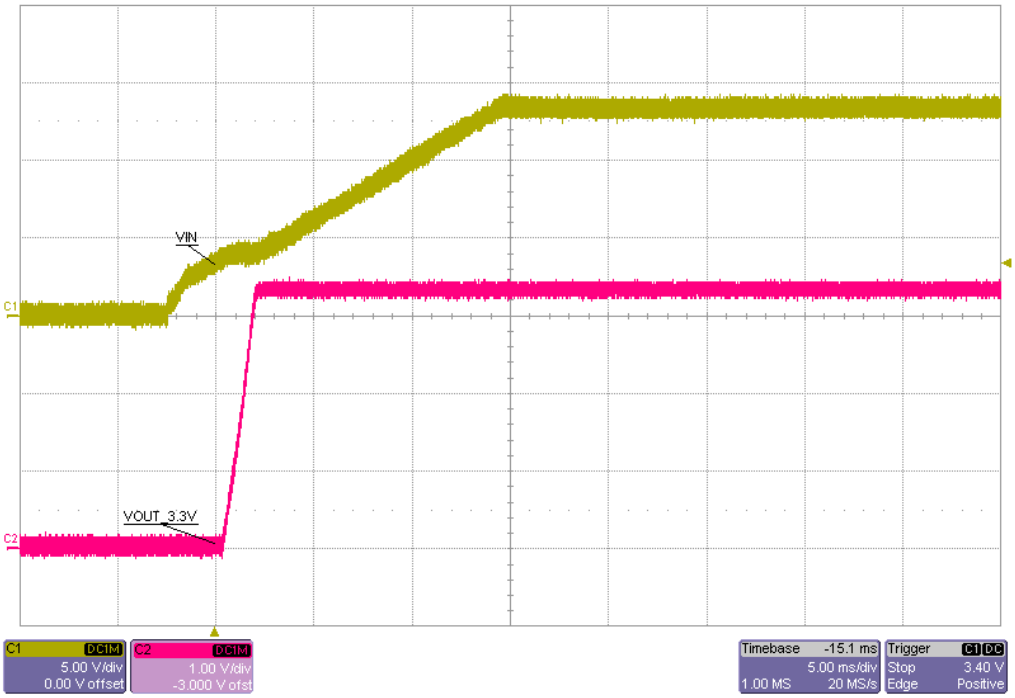
3.5.2 3V3 output rail

Enable is connected to Vin

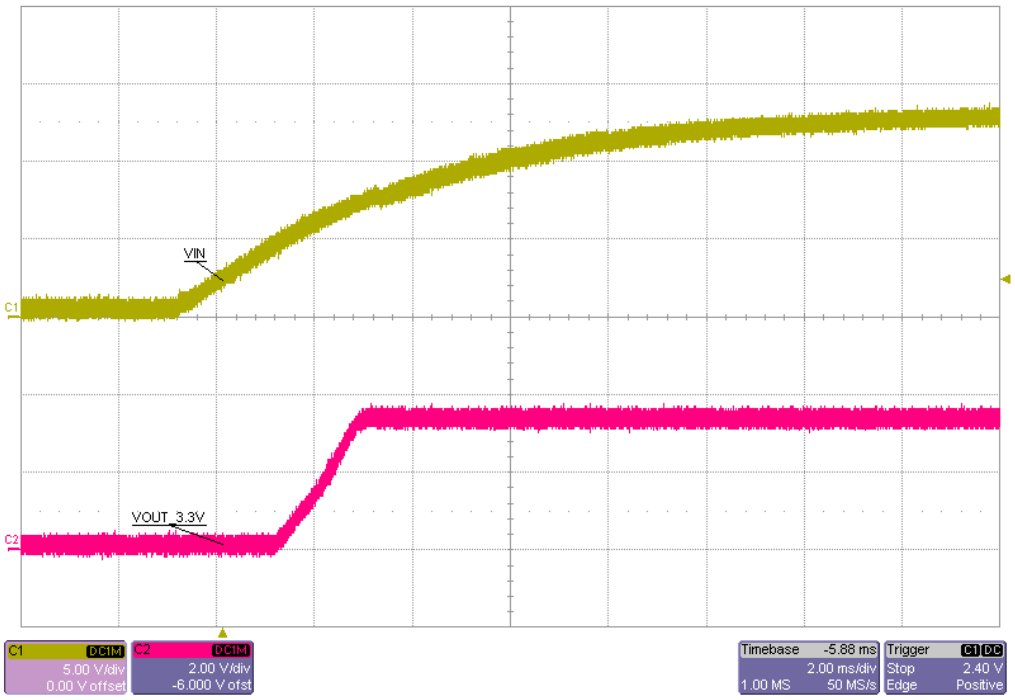
Yellow: Vin 13.5V; Red: Vout 3.3V;

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



2.4A Load

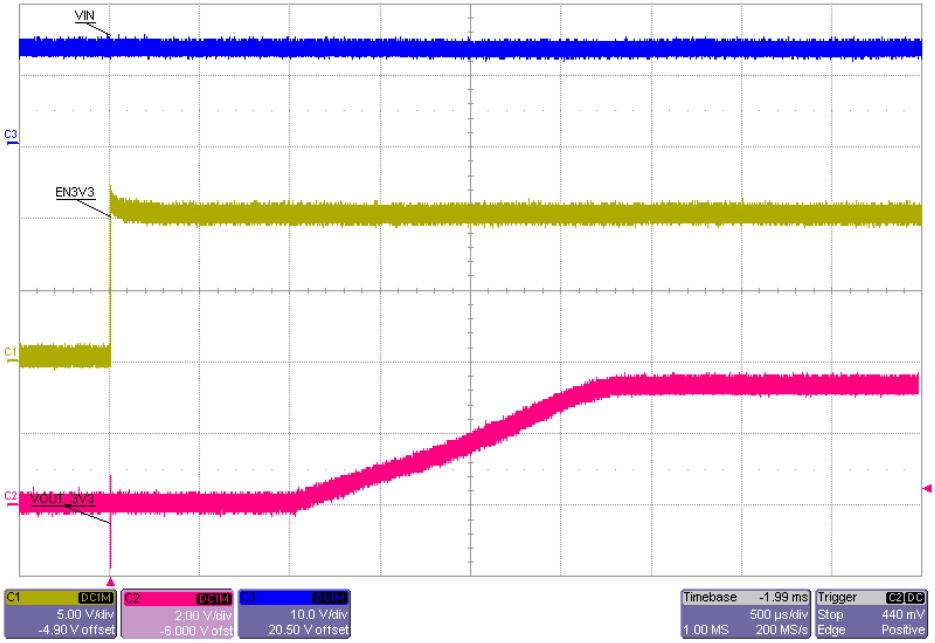


Vin is high and enable is ramped within 10µs

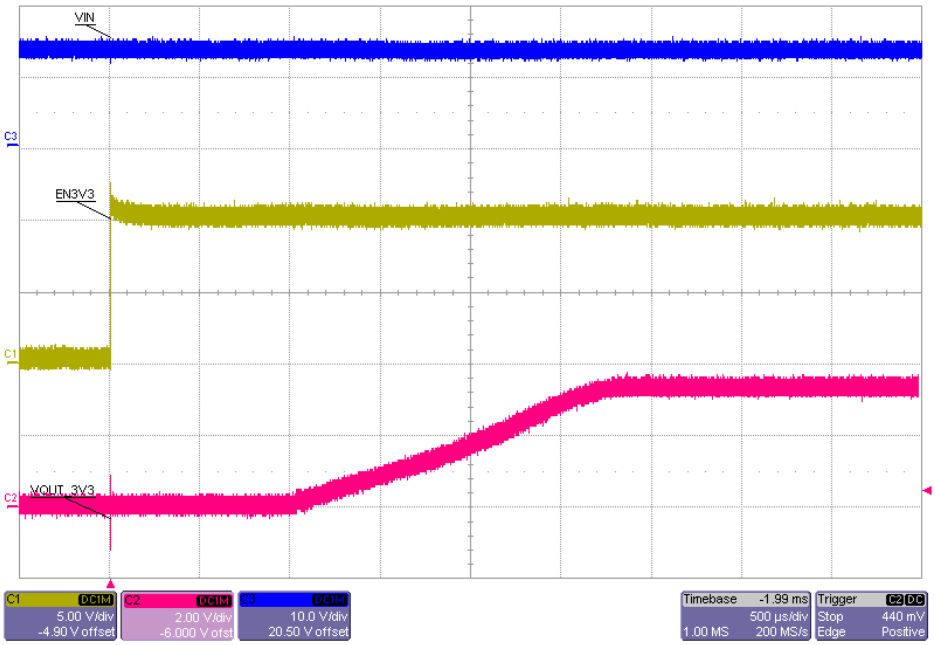
Blue: Vin 13.5V; Red: Vout 3.3V; Yellow: Enable

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



2.4A Load



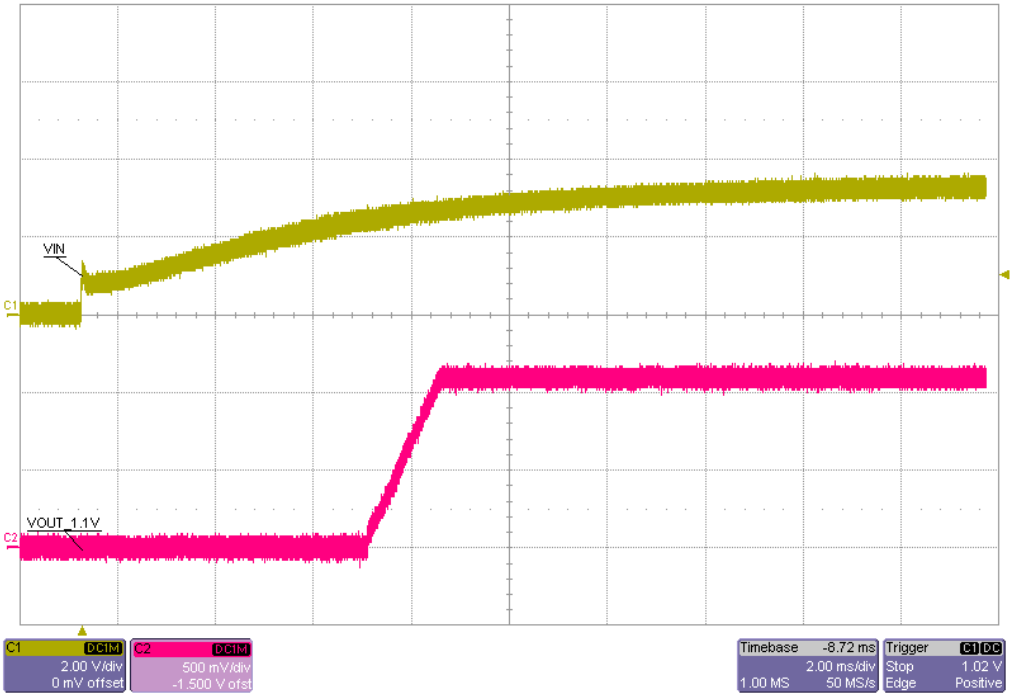
3.5.3 1V1 output rail

Enable is connected to Vin

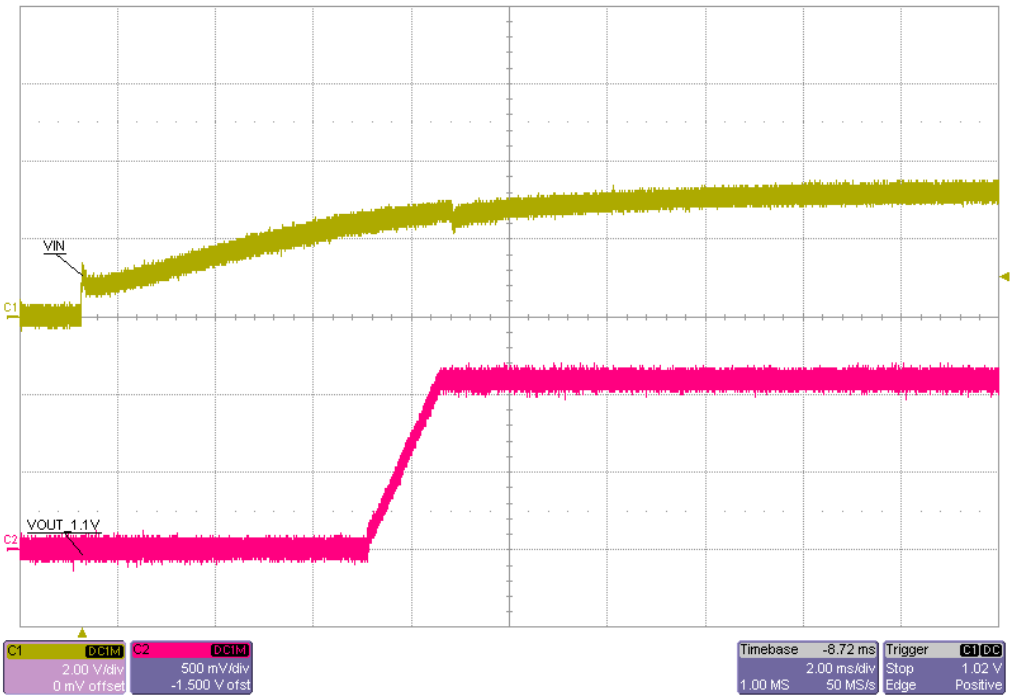
Yellow: Vin 3.3V; Red: Vout 1.1V;

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



2.5A Load

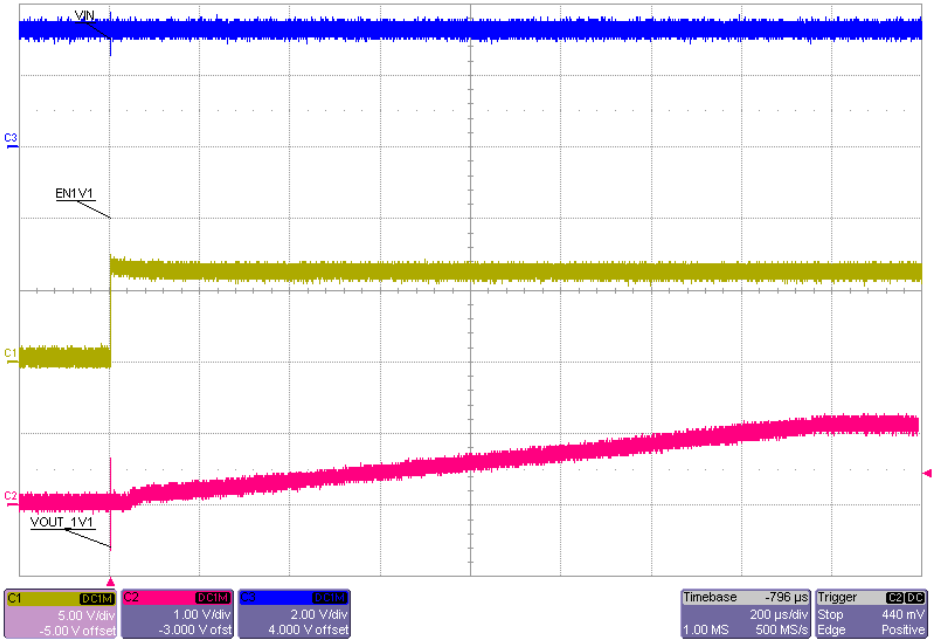


Vin is high and enable is ramped within 10µs

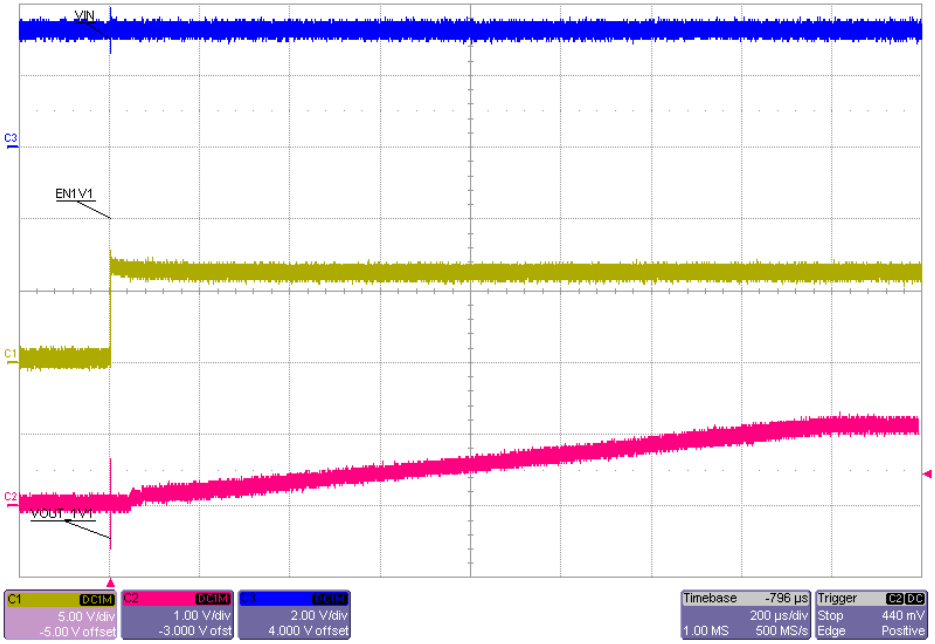
Blue: Vin 3.3V; Red: Vout 1.1V; Yellow: Enable

Smooth, monotonic startup observed on the output. No overshoot occurs at the end of soft start.

0A Load



2.5A Load



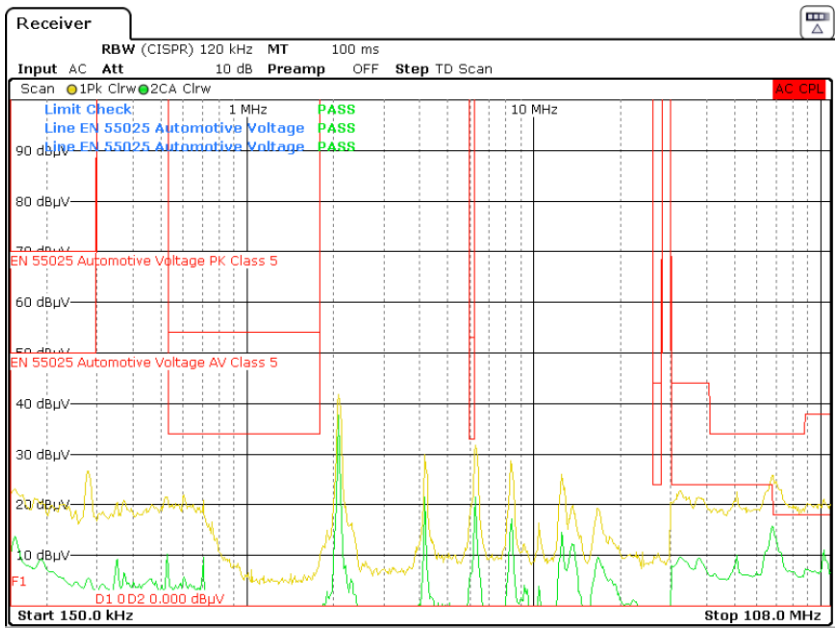
3.6 Conducted Emission (Standard: EN55025 (CISPR 25))

Tests were carried out with a) only 5V rail loaded; b) only 3V3 rail loaded; c) all the rails (5V, 3V3 and 1V1) loaded. Results show that the design was able to pass the conducted emission CISPR 25 Class 5 standard in all the cases. The yellow trace is the peak measurement, and the green trace is the average measurement.

3.6.1 13.5 VDC input/ 5 VDC out - Full Load

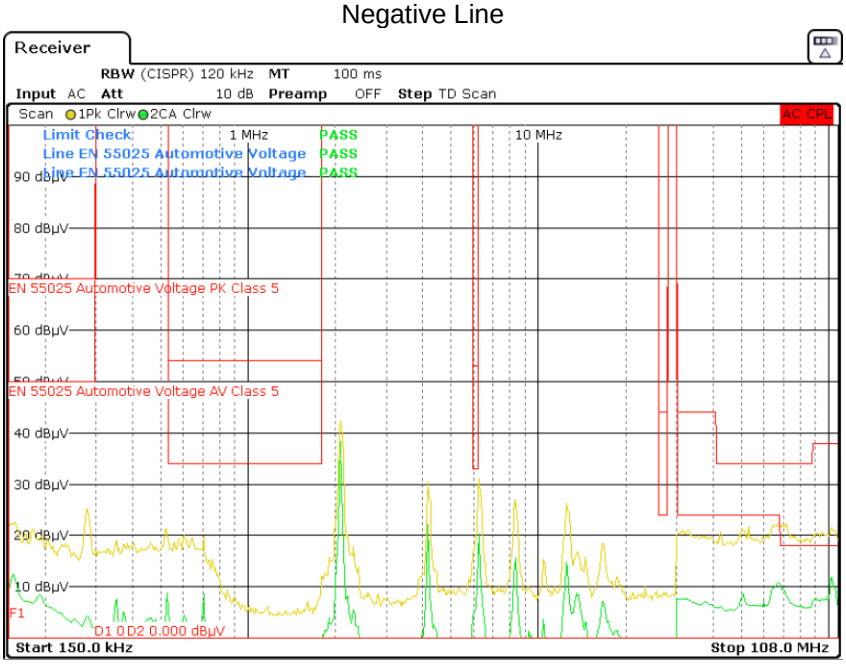
Test was carried out at 13.5V input and 5V output under full load. All other parts of the board were disabled.

Positive Line



Date: 3.JUN.2019 09:34:44

Negative Line

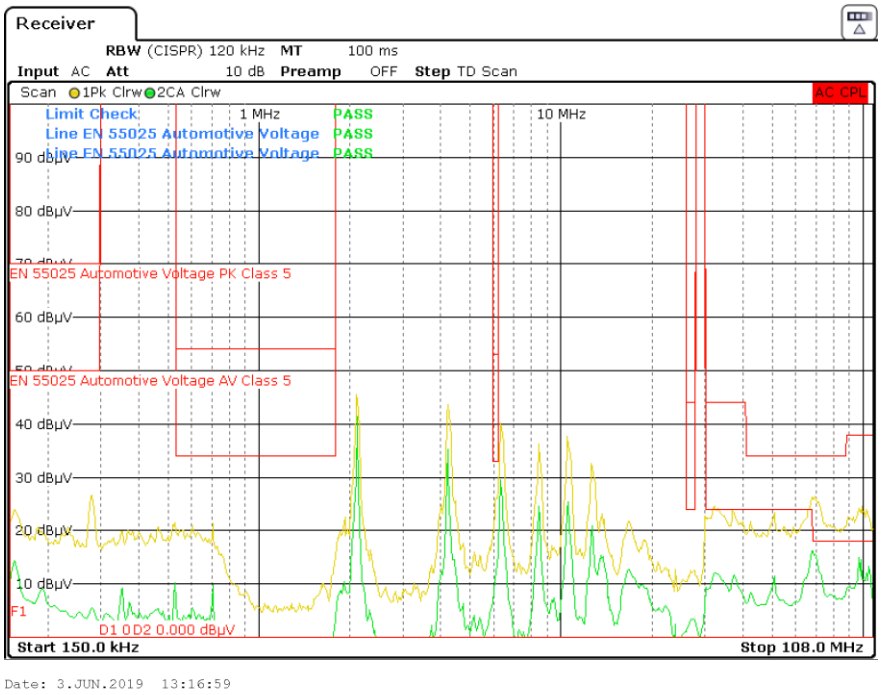


Date: 3.JUN.2019 09:25:06

3.6.2 13.5 VDC in/ 3.3 VDC out - Full Load

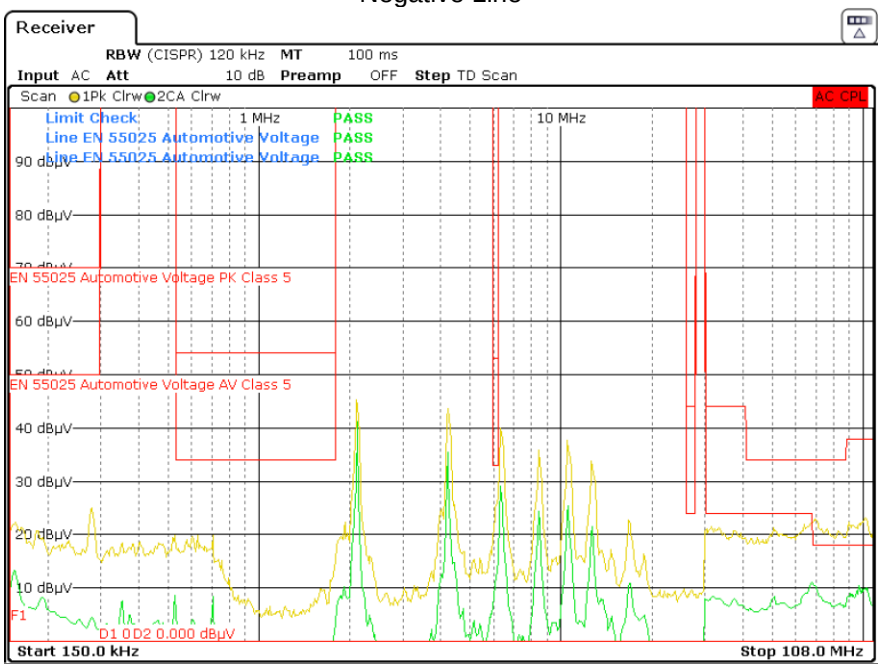
Test was carried out at 13.5V input and 3.3V output under full load. All other parts of the board were disabled.

Positive Line



Date: 3.JUN.2019 13:16:59

Negative Line

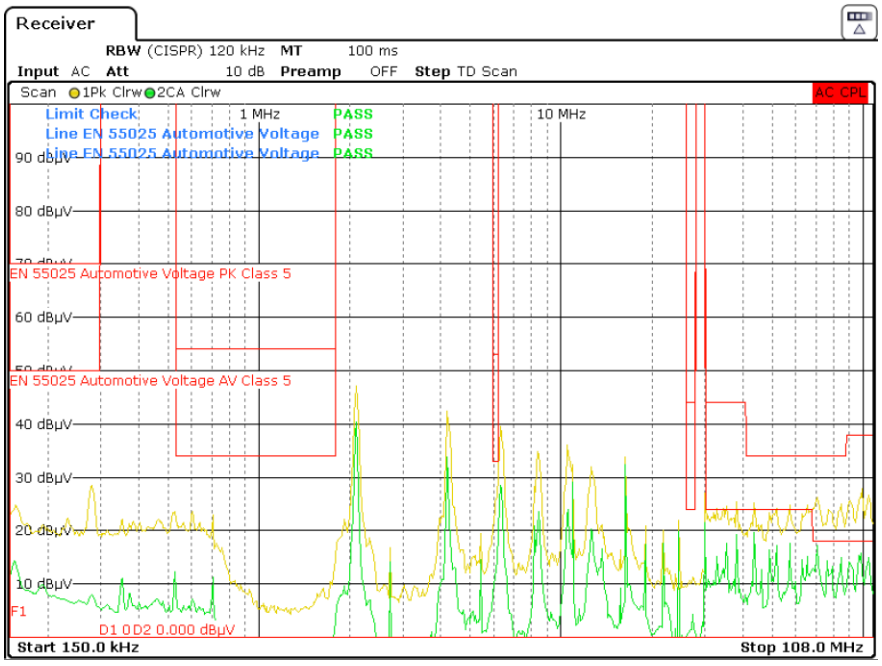


Date: 3.JUN.2019 13:09:47

3.6.3 13.5 VDC input/ 5 VDC, 3.3 VDC, 1.1 VDC out - Full Load

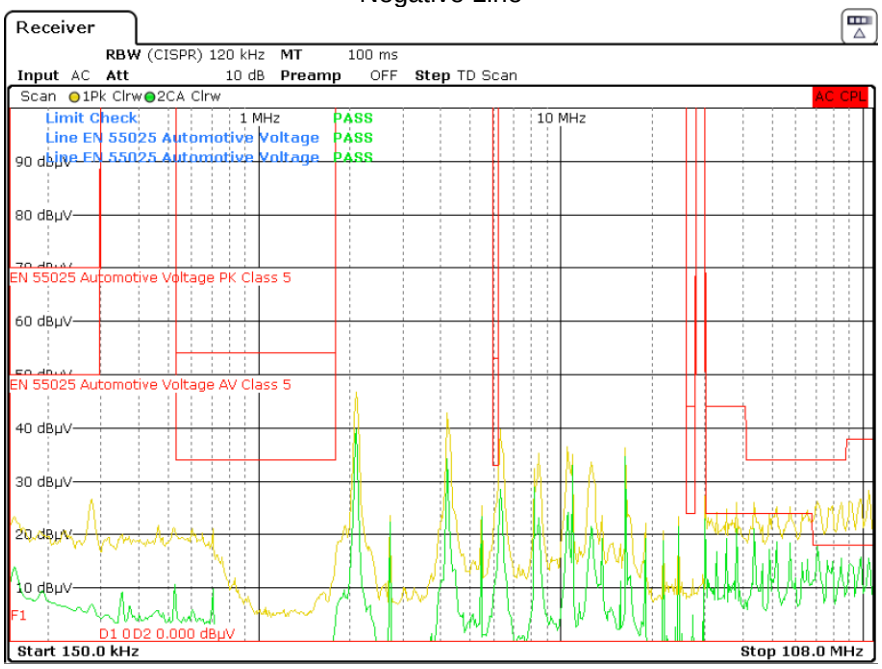
Test was carried out at 13.5V input with all the rails (5V, 3.3V and 1.1V) fully loaded.

Positive Line



Date: 3.JUN.2019 14:41:26

Negative Line



Date: 3.JUN.2019 14:07:23

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