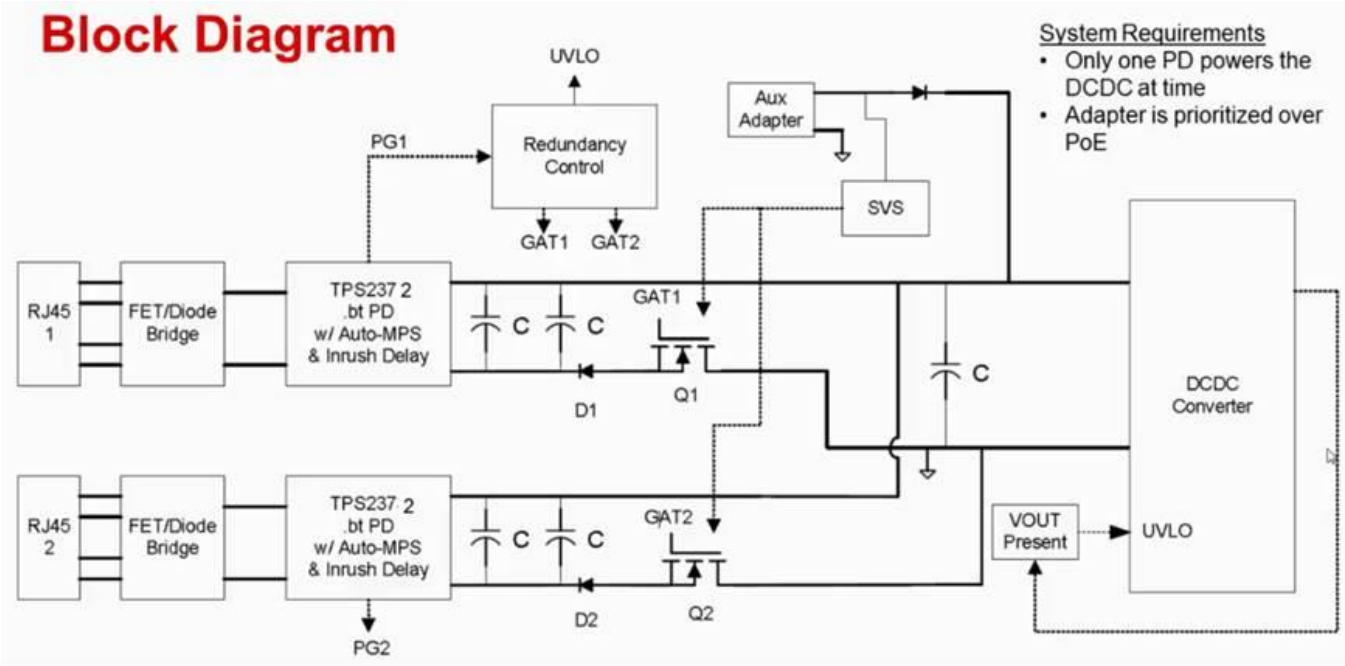
*Test Report: PMP20859*

# *Dual-Input Redundant PoE PD with Smooth Transition Reference Design*

TEXAS INSTRUMENTS

**Description**

PMP20859 implements an IEEE802.3bt (draft) Power over Ethernet (PoE) Powered Device (PD) with dual redundant inputs and smooth transition between these inputs and an auxiliary input. The design consists of a 5V/6A synchronous flyback converter and allows for up to three power supplies (two PoE Power Source Equipment (PSE) supplies and one ac/dc wall adapter auxiliary supply) to be used in order to decrease the probability of power and data loss in your system. Two IEEE802.3bt (draft) TPS2372-3 PD controllers are utilized for high power PoE up to 40W. In addition, a TPS3808 delay supervisor and additional circuitry enable the PD to achieve a smooth transition between PoE to auxiliary and PoE to PoE power supply connections (in the event the main power supply is removed or fails) without an interruption in output voltage or disconnecting from the PSE.



# Test Prerequisites

## *1.1 Voltage and Current Requirements*

**Table 1. Voltage and Current Requirements**

| PARAMETER | SPECIFICATIONS |
|---|---|
| PoE Input Voltage | 42.5-57V (48V nominal) |
| Adapter (AUX) Input Voltage | 48V+/-10% |
| Vout | 5V |
| Iout | 6A |
| Nominal Switching Frequency | 250kHz |

## *1.2 Required Equipment*

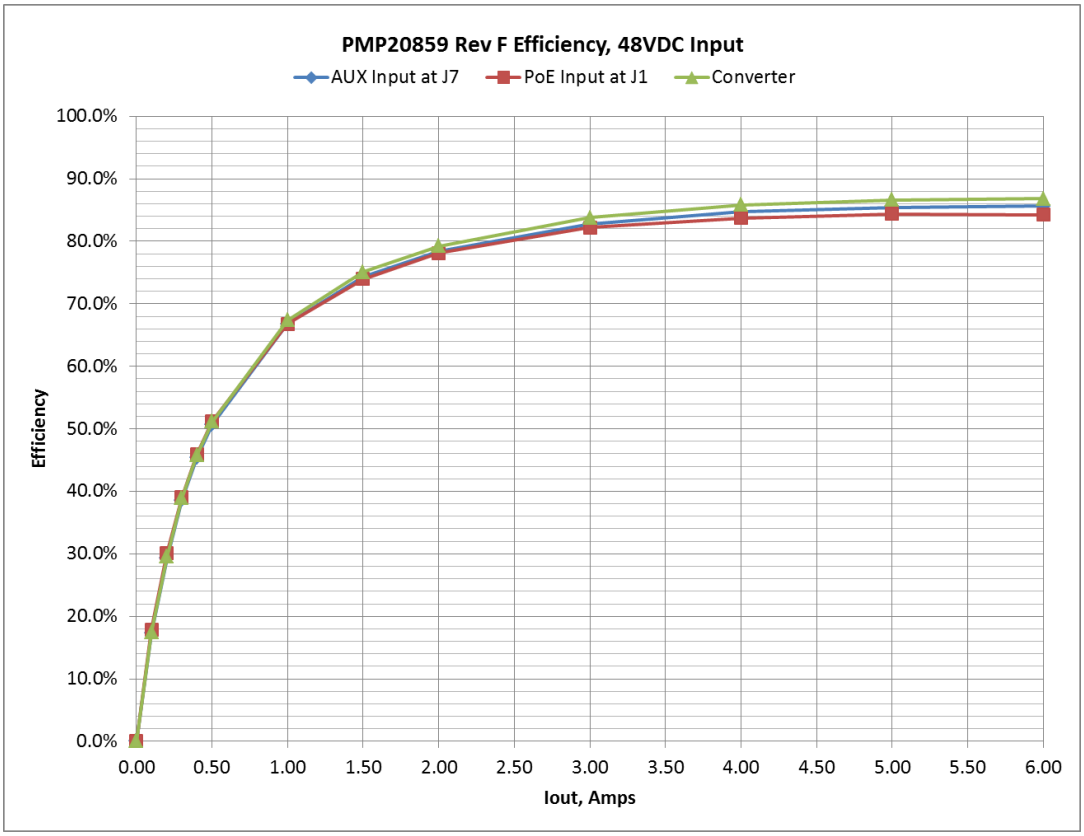
- Two IEEE802.3.bt (draft) Type 3 PSE's
- AC/DC isolated wall adapter, 48V +/-10%, 1A minimum
- CAT5e ethernet cables (<100m)
- 5V/6A load

## *1.3 Considerations*

All testing performed with a 48V input and 6A load unless otherwise noted.

# 2 Testing and Results

## 2.1 Efficiency Graph

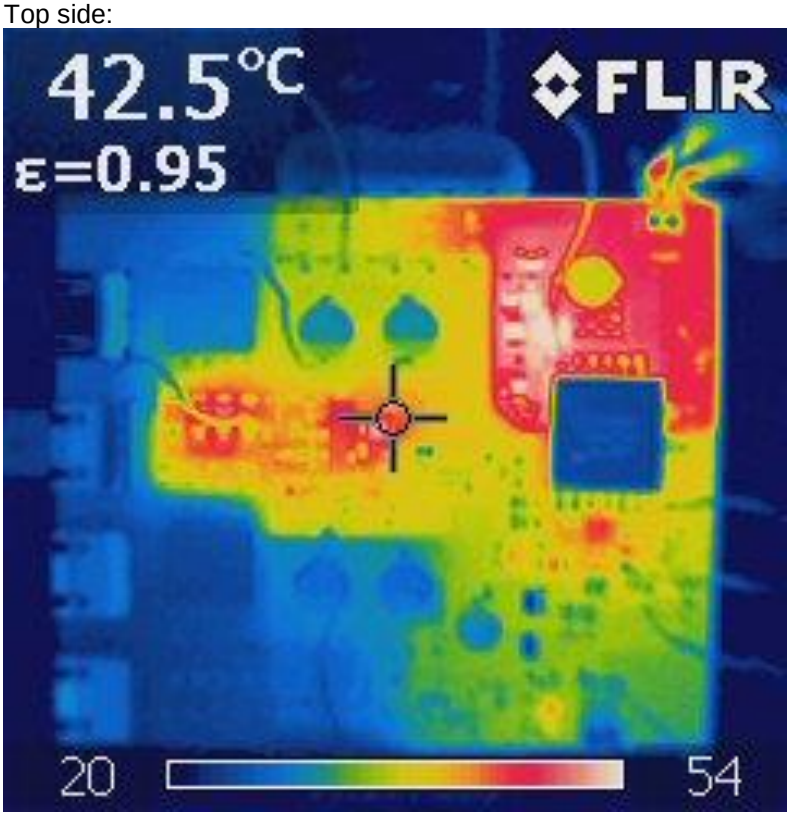



## 2.2 Efficiency Data

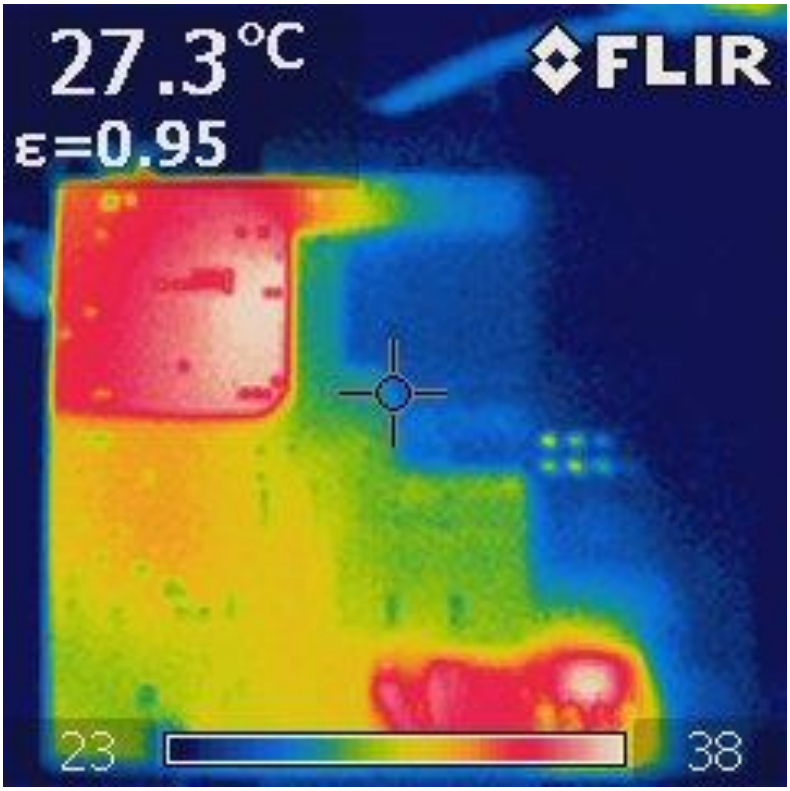
| J8 Amps Iout | J8 Volts Vout | AUX J7 Amps Iin | AUX J7 Volts Vin | AUX J7 Eff | CONV Volts Vin | CONV Eff | PoE J1 Amps Iin | PoE J1 Volts Vin | PoE J1 Eff |
|---|---|---|---|---|---|---|---|---|---|
| 0.00 | 5.064 | 0.050 | 48.00 | 0.0% | 47.61 | 0.0% | 0.048 | 48.00 | 0.0% |
| 0.10 | 5.064 | 0.061 | 48.00 | 17.3% | 47.60 | 17.4% | 0.059 | 48.00 | 17.9% |
| 0.20 | 5.064 | 0.072 | 48.00 | 29.3% | 47.59 | 29.6% | 0.070 | 48.00 | 30.1% |
| 0.30 | 5.064 | 0.082 | 48.01 | 38.6% | 47.60 | 38.9% | 0.081 | 48.01 | 39.1% |
| 0.40 | 5.064 | 0.093 | 48.01 | 45.4% | 47.59 | 45.8% | 0.092 | 48.01 | 45.9% |
| 0.50 | 5.064 | 0.104 | 48.01 | 50.7% | 47.58 | 51.2% | 0.103 | 48.01 | 51.2% |
| 1.00 | 5.064 | 0.158 | 48.01 | 66.8% | 47.55 | 67.4% | 0.158 | 48.01 | 66.8% |
| 1.50 | 5.064 | 0.213 | 48.00 | 74.3% | 47.51 | 75.1% | 0.214 | 48.00 | 73.9% |
| 2.00 | 5.064 | 0.269 | 48.01 | 78.4% | 47.50 | 79.3% | 0.270 | 48.01 | 78.1% |
| 3.00 | 5.063 | 0.382 | 48.01 | 82.8% | 47.46 | 83.8% | 0.385 | 48.01 | 82.2% |
| 4.00 | 5.063 | 0.498 | 48.00 | 84.7% | 47.39 | 85.8% | 0.504 | 48.00 | 83.7% |
| 5.00 | 5.063 | 0.617 | 48.01 | 85.5% | 47.37 | 86.6% | 0.625 | 48.01 | 84.4% |
| 6.00 | 5.063 | 0.739 | 48.01 | 85.6% | 47.33 | 86.9% | 0.751 | 48.01 | 84.3% |

### 2.3 Thermal Images

Top side:



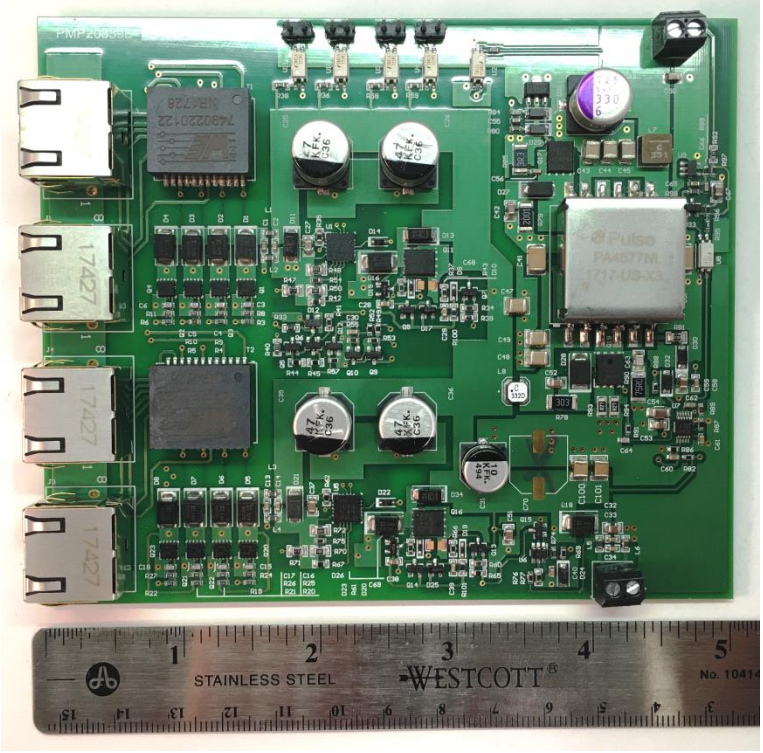

Bottom side:



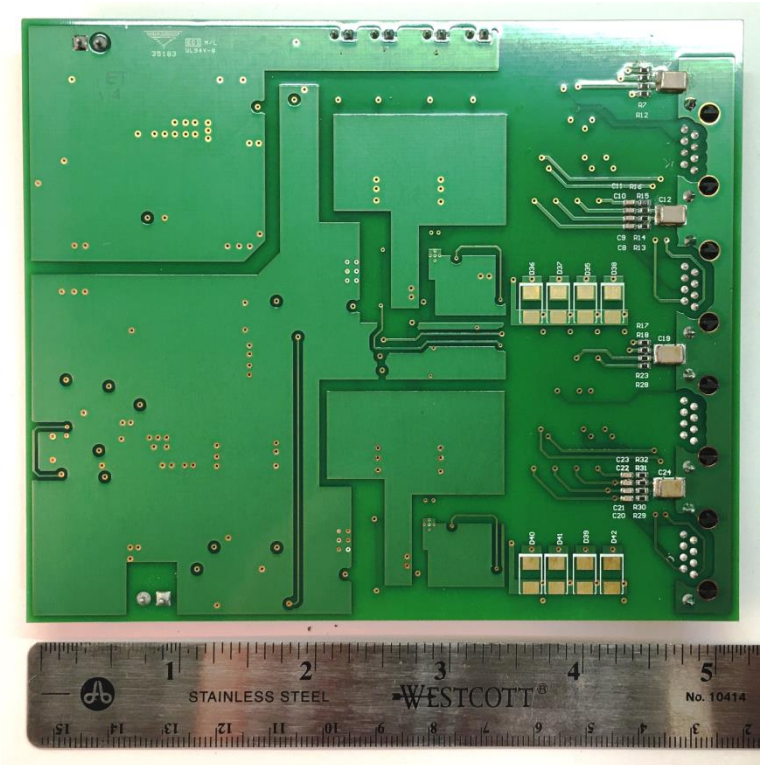
## 2.4 Photo

The board measures 117mm x 127mm.

Top:



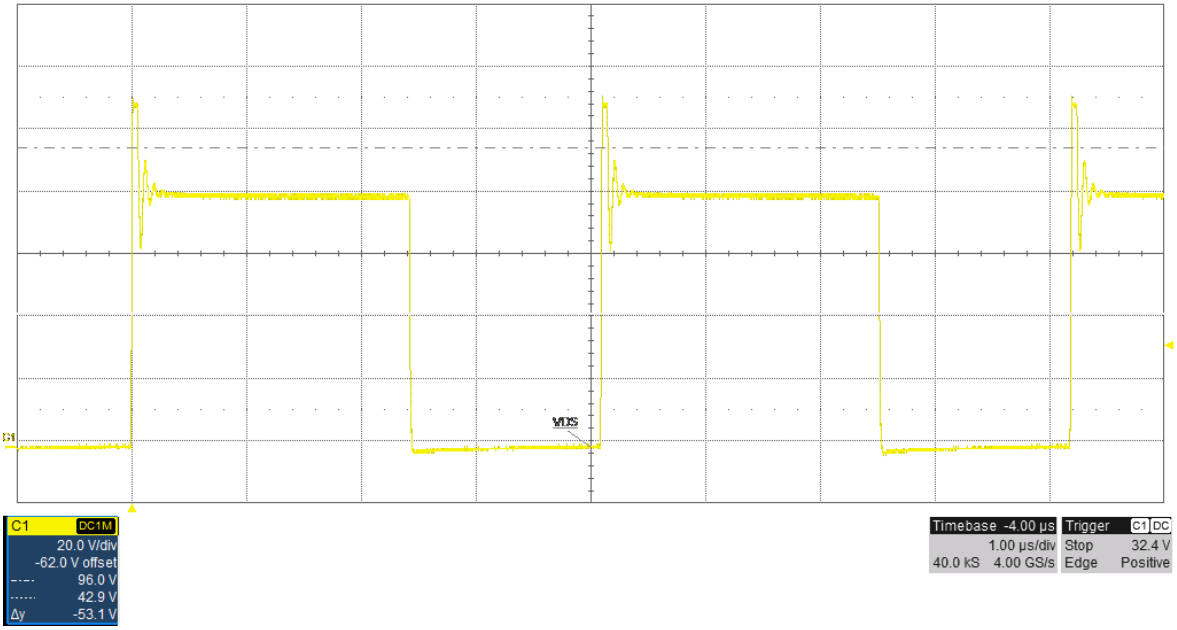

Bottom:



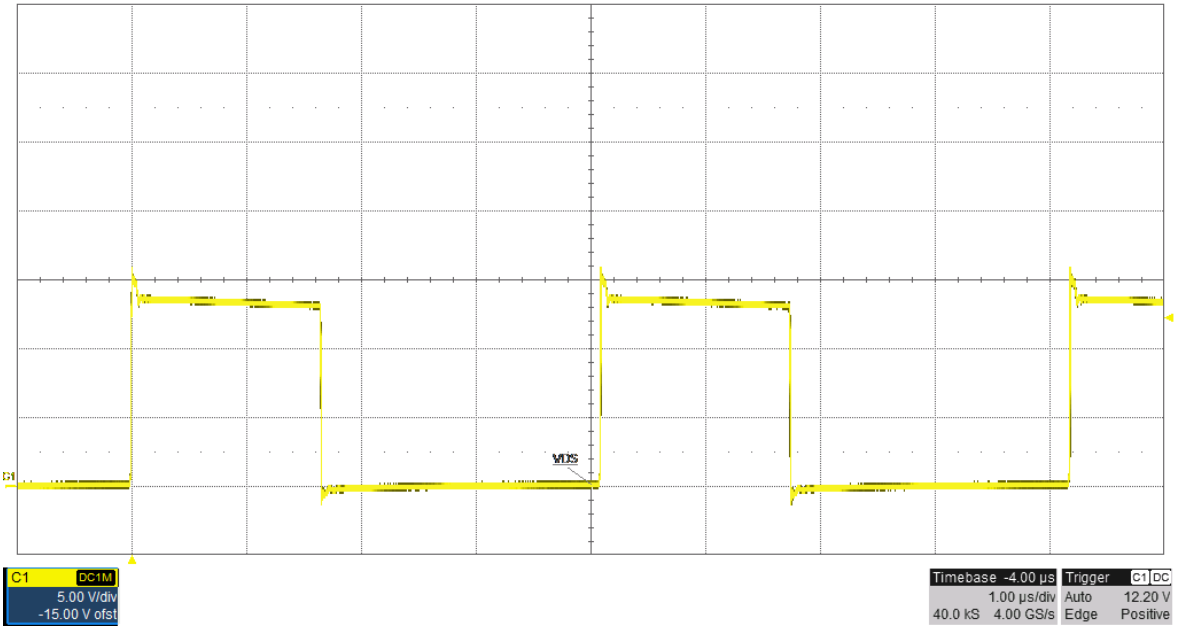
# 3 Waveforms

## 3.1 Switching

Primary FET (Q19) Drain to PWRGND:

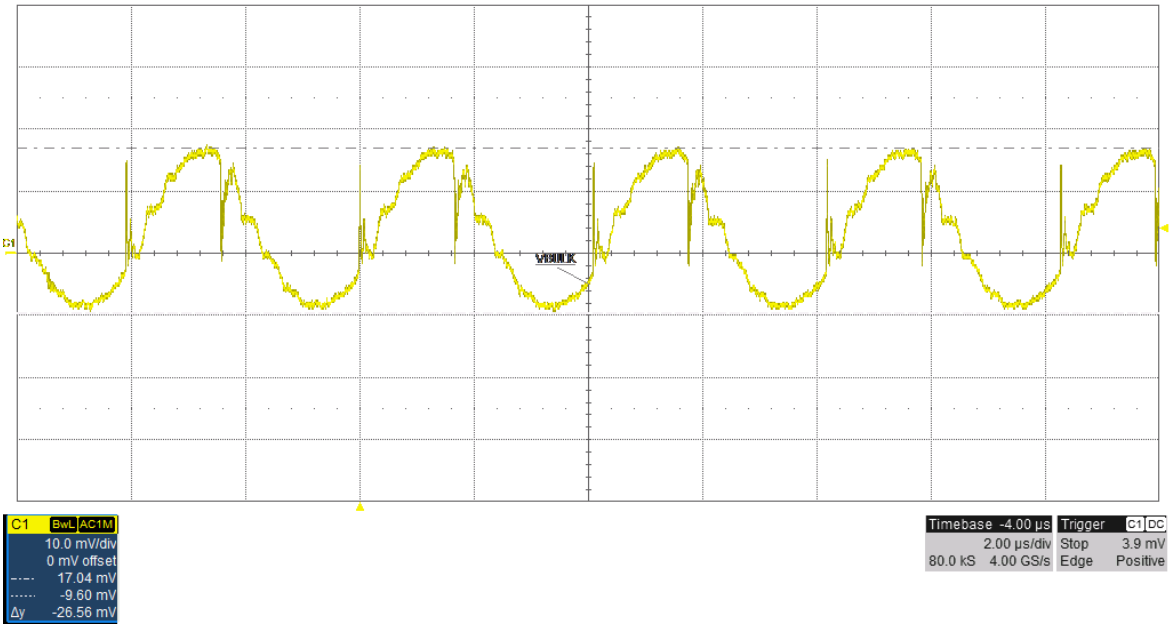



Secondary FET (Q17) Drain to GND:

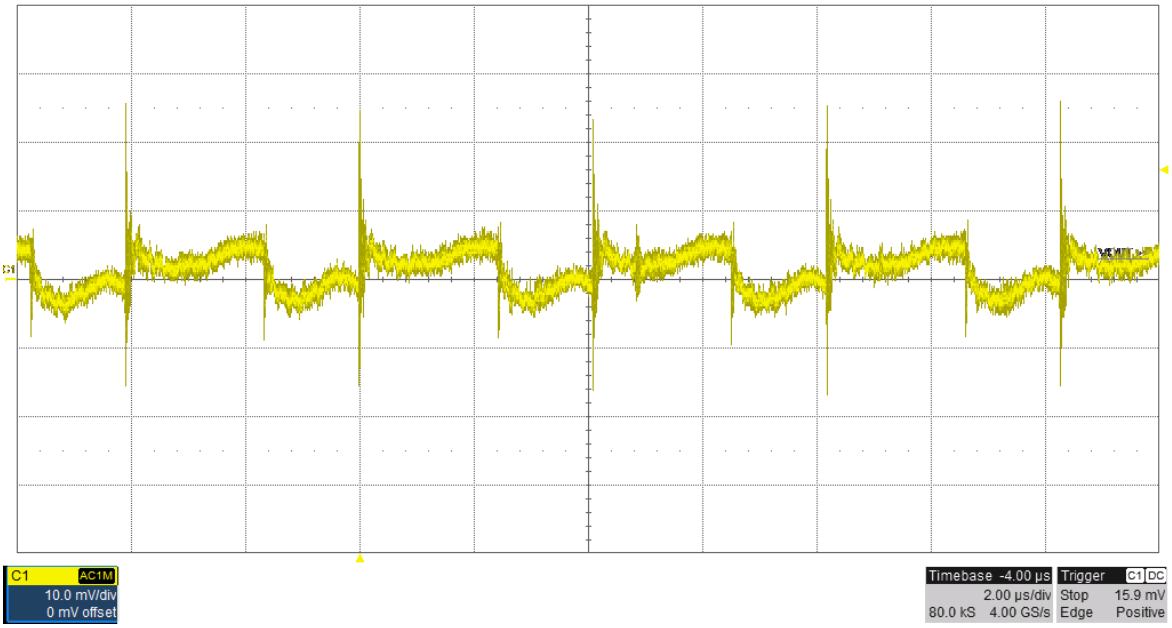


## 3.2 Voltage Ripple

Input Voltage Ripple:

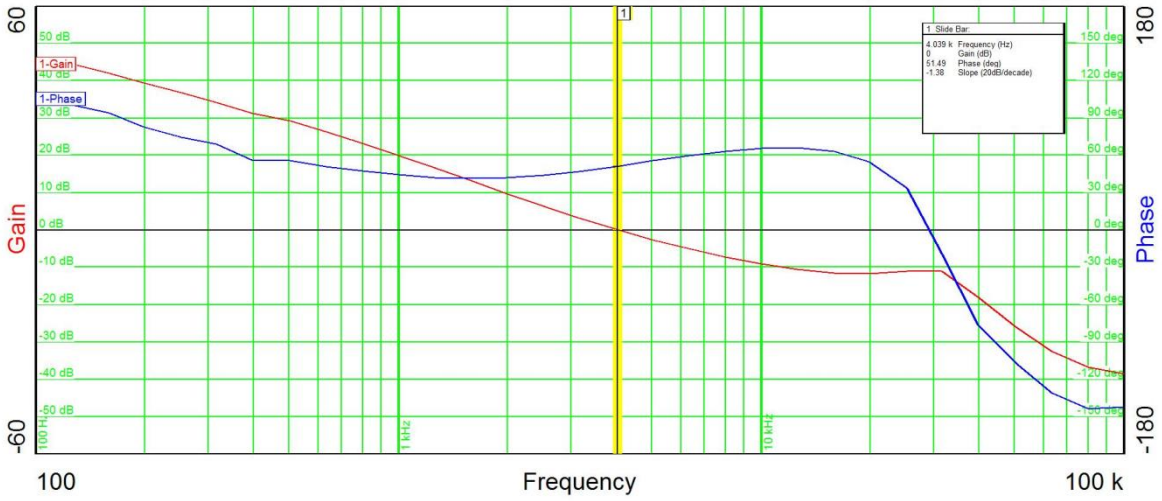



Output Voltage Ripple:



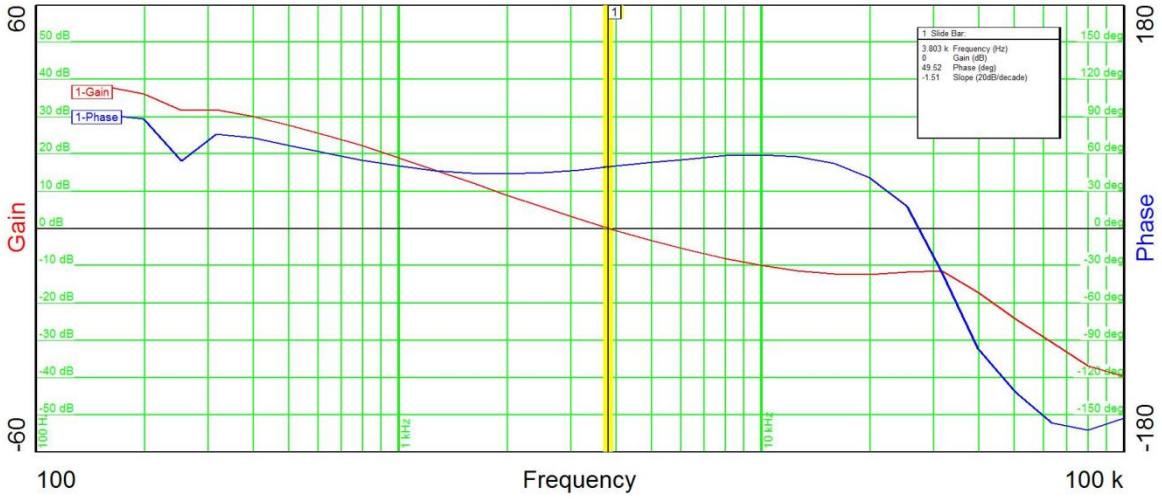
### 3.3 Bode Plot

0A Load:




Bandwidth = 4 kHz Phase Margin = 51.5 degrees Gain Margin = 11 dB

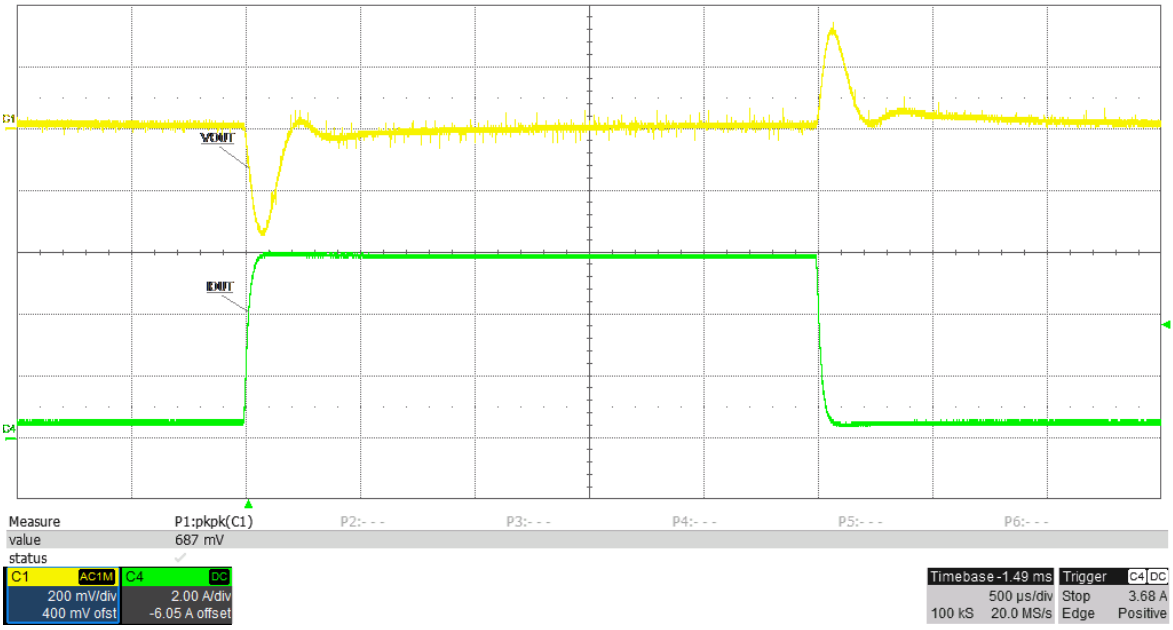
6A Load:



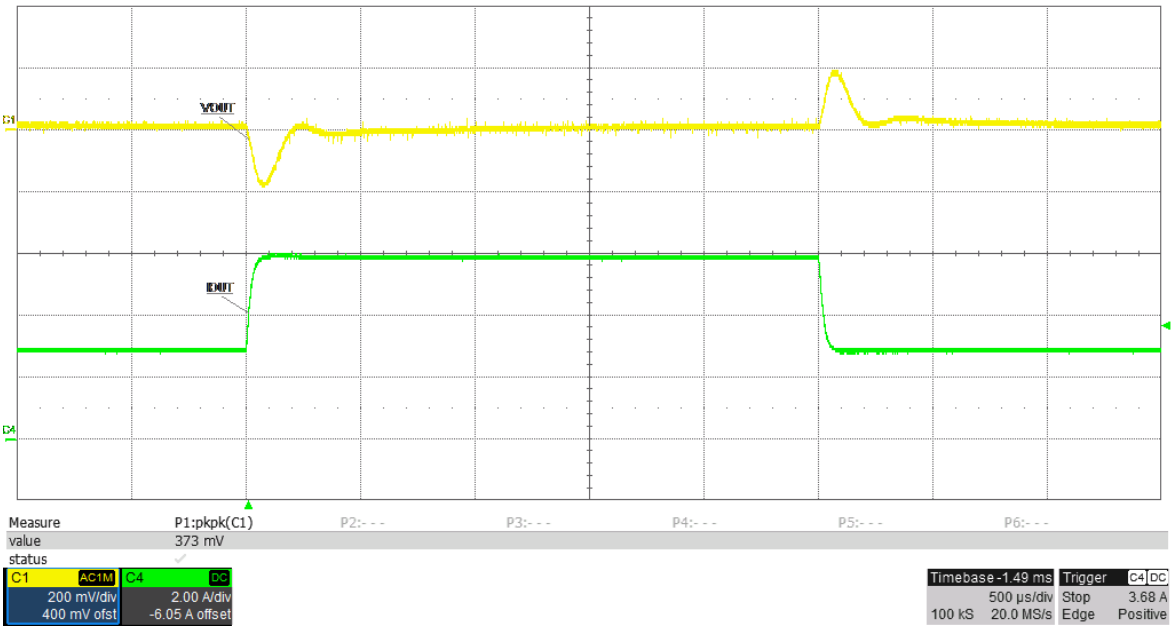

Bandwidth = 3.8 kHz Phase Margin = 49.5 degrees Gain Margin = 12 dB

## 3.4 Load Transients

600mA to 6A Load Step:

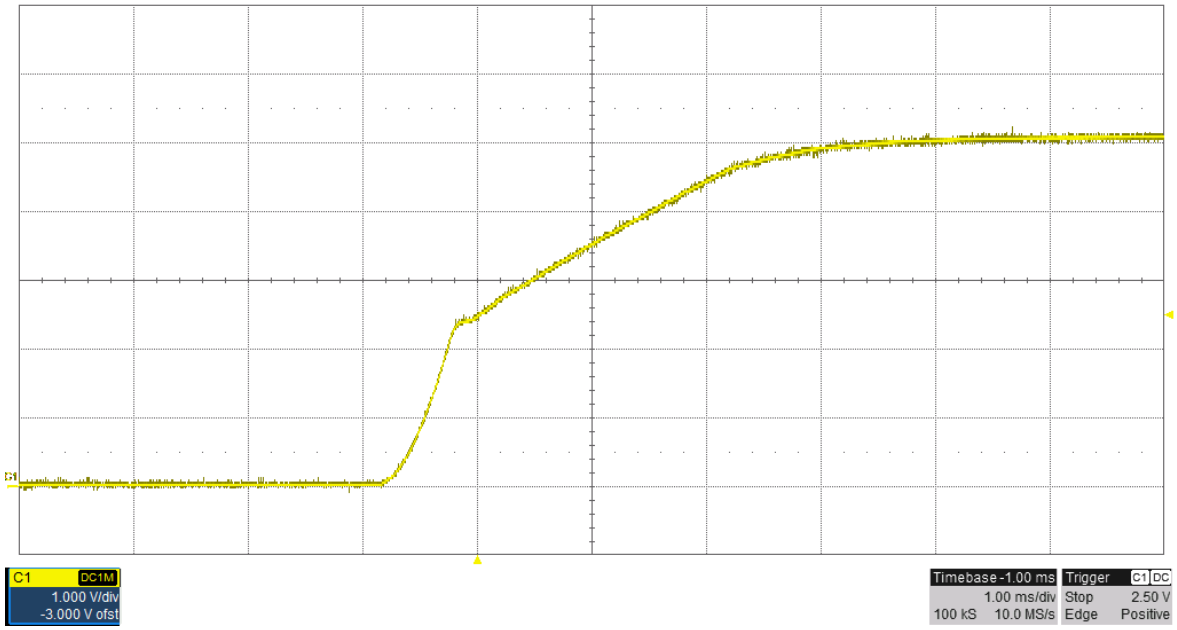



3A to 6A Load Step:

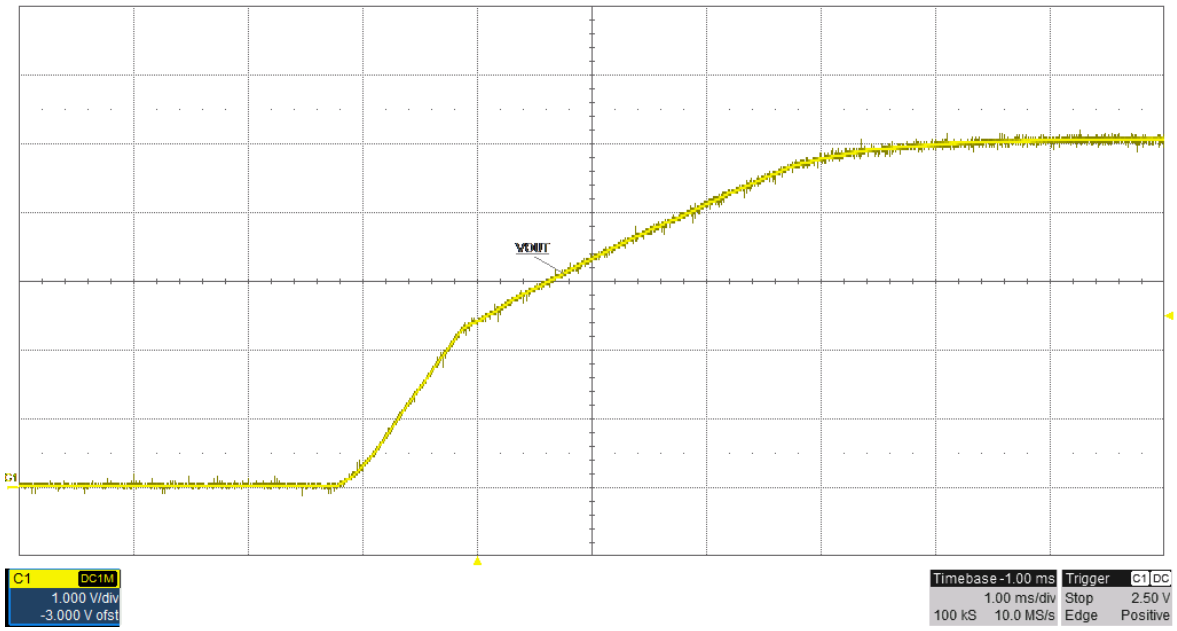


## 3.5 Start-up Sequence

0A Load:




6A Load:

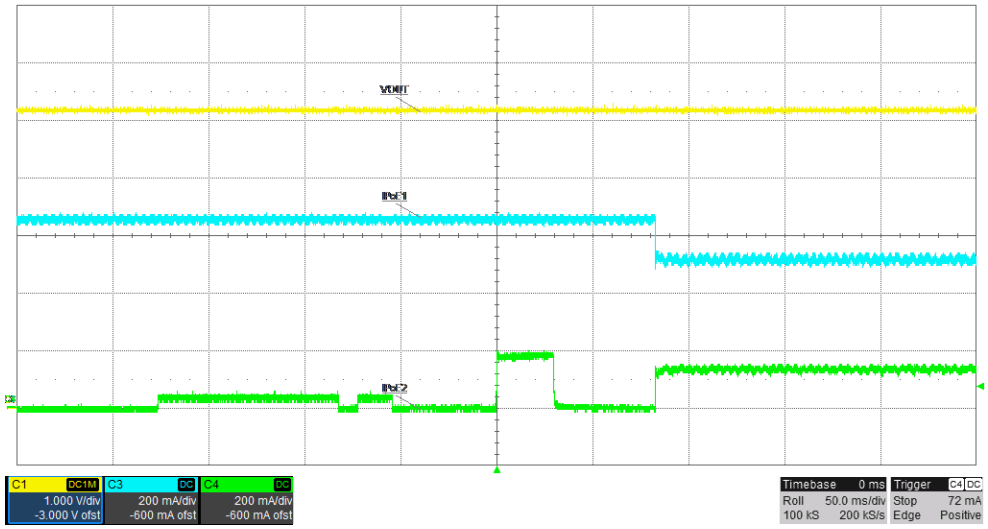


# 4 Smooth Transition

## *4.1 Transitions Between Two PoE Inputs*

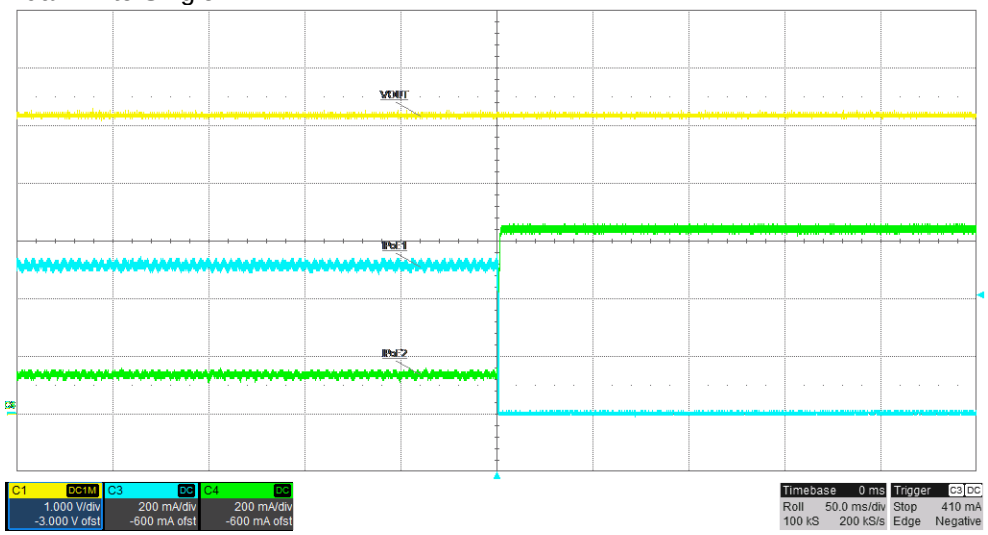
| Initial State | Change | Expected Result |
|---|---|---|
| Single PD connected | Add second PD | Both PD's connected to PSE, one PD enters standby and one PD provides power. Output voltage remains within transient limits |
| Dual PD's connected | Remove one PD | PD still connected provides power. Output voltage remains within transient limits |

Single PD to Dual PD:




Note: If the CAT5e cables have similar lengths/resistance and both PD circuits have similar losses, the PD circuits may share the input current. This is not typical.

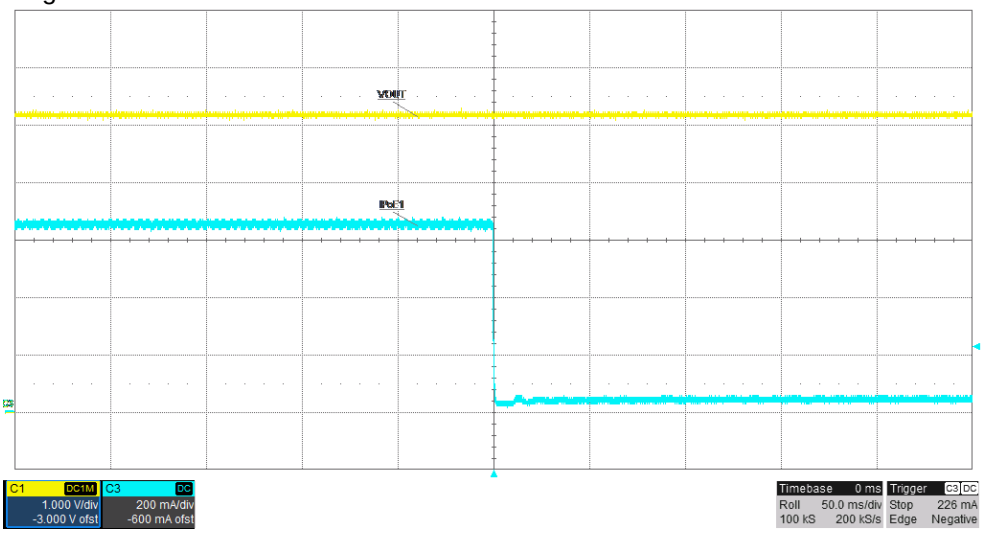
Dual PD to Single PD:



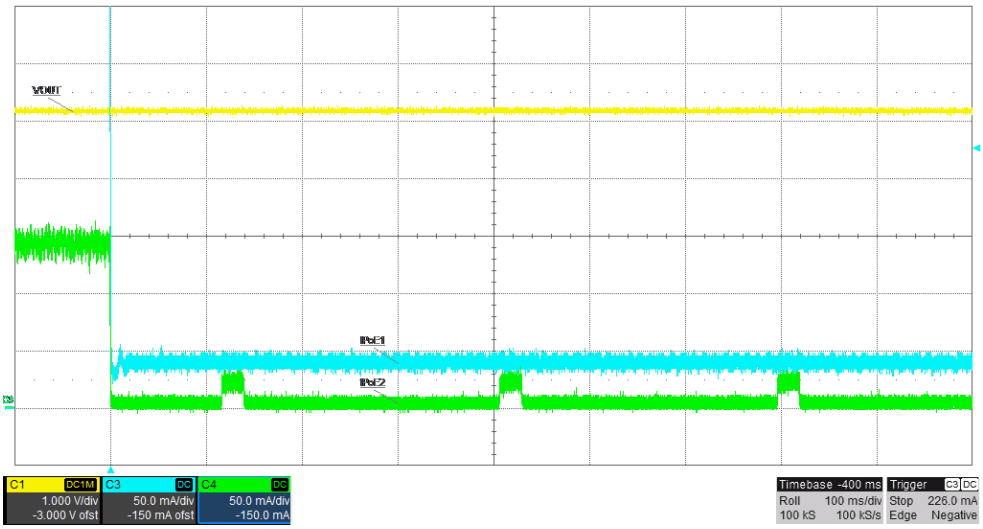
## 4.2 Transitions Between PoE Inputs and AUX

| Initial State | Change | Expected Result |
|---|---|---|
| Single PD connected | Add AUX | AUX provides power and PD enters standby. Output voltage remains within transient limits. |
| Dual PDs connected | Add AUX | AUX provides power and PD's enter standby. Output voltage remains within transient limits. |

Single PD to AUX:



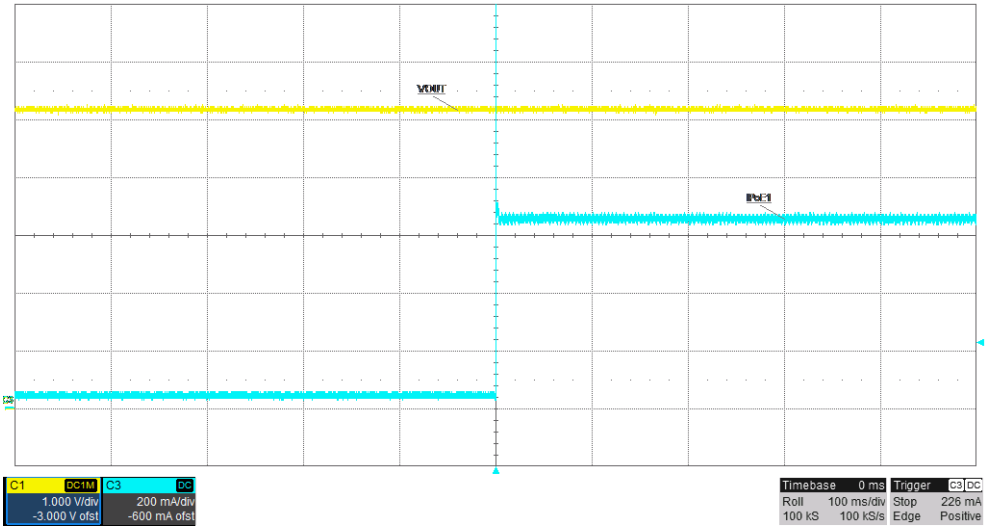

Dual PD to AUX:



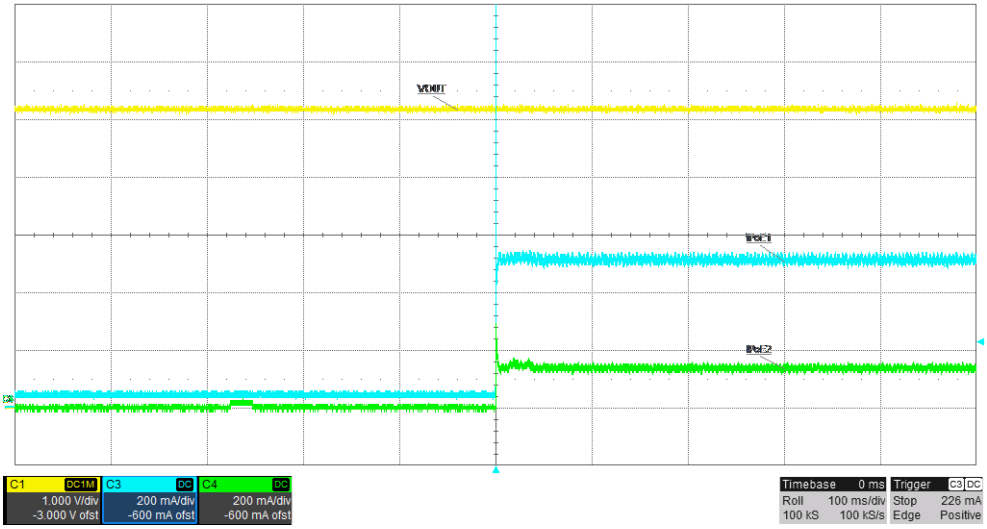
### 4.3 Transitions From AUX to PD

| Initial State | Change | Expected Result |
|---|---|---|
| Single PD and AUX connected | Remove AUX | PD continues to provide power. Output voltage remains within transient limits. |
| Dual PD's and AUX connected | Remove AUX | One PD continues to provide power and the second enters standby. Output voltage remains within transient limits. |

Single PD and AUX, Remove AUX:




Dual PD and AUX, Remove AUX:

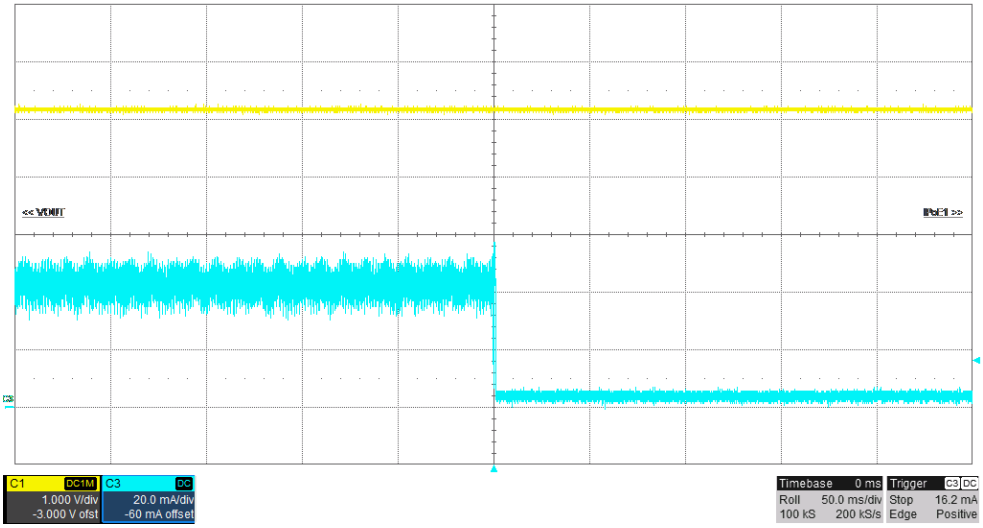



Note: If the CAT5e cables have similar lengths/resistance and both PD circuits have similar losses, the PD circuits may share the input current. This is not typical.

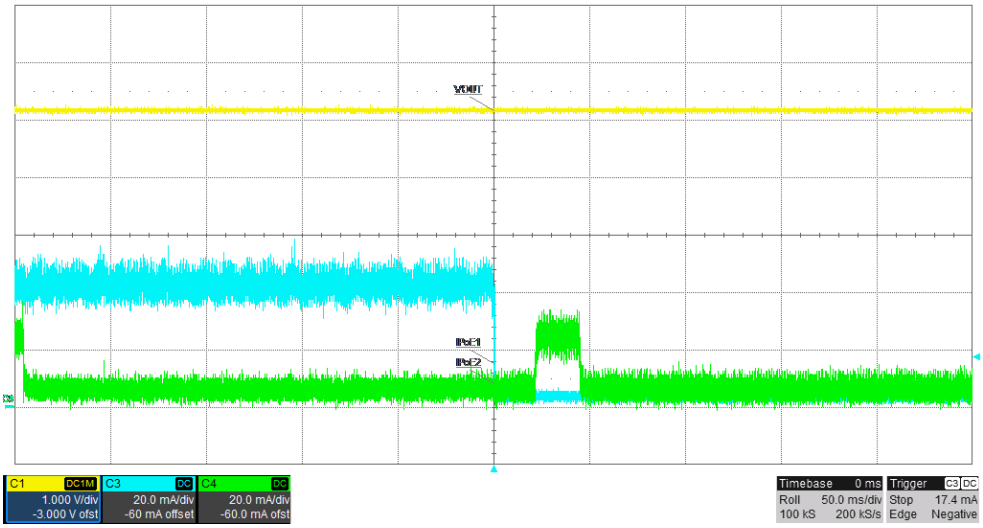
### 4.4 Transitions Between AUX and Single/Dual PD Inputs

| Initial State | Change | Expected Result |
|---|---|---|
| Single PD and AUX connected | Remove PD | AUX continues to provide power. Output voltage remains within transient limits. |
| Dual PD's and AUX connected | Remove one PD | AUX continues to provide power and remaining PD enters standby. Output voltage remains within transient limits. |
| Single PD and AUX connected | Add second PD | AUX continues to provide power and PD's enter standby. Output voltage remains within transient limits. |

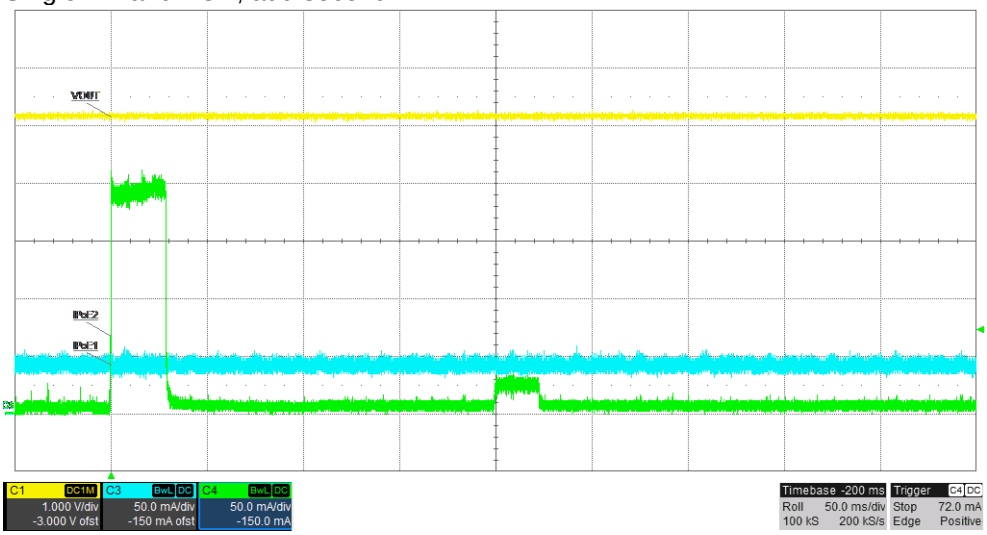
Single PD and AUX, Remove PD:




Dual PD's and AUX, Remove one PD:



Single PD and AUX, add second PD:



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