Test Report: PMP15044

PMP15044 Test Results

System Description

Effectively limiting the input current within a required range is particularly difficult in the super-capacitor (CAP) charge-up circuit. For a boost converter with a large output capacitor, if the initial voltage on the output capacitor is zero, then the inductor current loses control during startup and rises to a high value. Therefore, the input current also rises to a high value. It is easy to exceed the maximum output current capability of the input-power supply. In some applications, such as a USB-supplied system, the input voltage is pulled low or even dropped to zero when the supplied current exceeds the maximum limit. Therefore, users need a solution that can effectively limit the input current in the super-CAP charge-up circuit application.

This test report on the PMP15044 device focuses on the previously listed requirements. Figure 1 shows the block diagram of the PMP15044 device. This solution uses the natural-input current-limit characteristic of the flyback topology. During start-up, even though the initial output voltage of the super CAP is zero, the primary winding current is always limited by the peak-switch current limit of the TPS61087 device. Considering the duty cycle during soft-start, the input current is lower than the peak-switch current-limit value of the TPS61087 device.

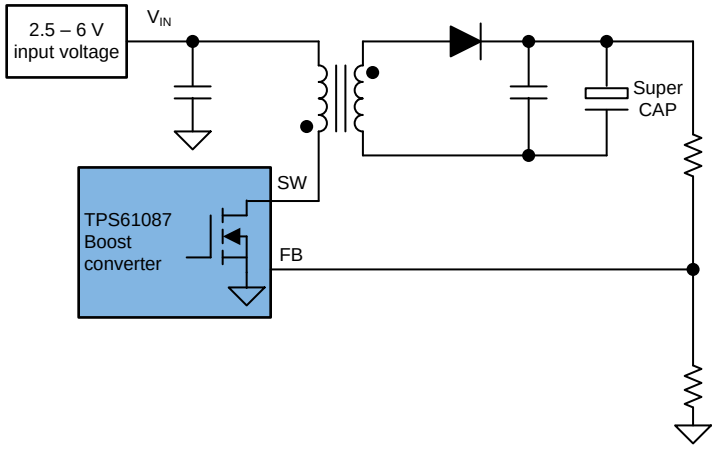

Figure 1. PMP15044 Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1 lists the performance specifications of the PMP15044 device. Regardless of how large the capacitive load at the output side, the input current can be effectively limited below 3 A, even during start-up.

Table 1. PMP15044 Specification

PARAMETER	SPECIFICATION
Input-voltage range	2.5 to 6 V
Maximum input current at any condition	3 A
Output voltage	13.5 V
Load	EL CAP / Super CAP

1.2 Required Equipment

- 2.5- to 6.5-V output DC source
- 10-A rating current probe
- Voltage probe
- Oscilloscope

2 Design Theory

2.1 Design Theory

Figure 2 shows the schematic of the PMP15044 schematic, with a 4700-µF capacitor load at the output side. The device is of flyback topology, but the primary winding and secondary winding share the same ground, so the configuration is simple. This flyback inductor does not need reinforced insulation, basic insulation is enough. Therefore, this is a low-cost solution for the super-CAP charge-up circuit application.

The boost converter, TPS61087, always works at the current-limit mode during start-up, before the output voltage reaches the target value. After the output capacitor is fully charged, the TPS61087 device works in the skip mode.

Larger inductance means a larger inductor size. In this design, the TPS61087 device works at the DCM and CCM boundary when the output voltage reaches the target value. The target output voltage is 13.5 V in this test report. Based on the maximum allowable primary-FET voltage stress and leave, around a 20% voltage margin, a NP/NS = 1:4 turns-ratio flyback inductor can be chosen. Then, based on the 4-A current-limit value and 1:4 turns ratio, 0.6-µH primary inductance can be chosen, to let the TPS61087 device work in the DCM and CCM boundary, at a VIN = 3.3 V and VOUT = 13.5 V condition.

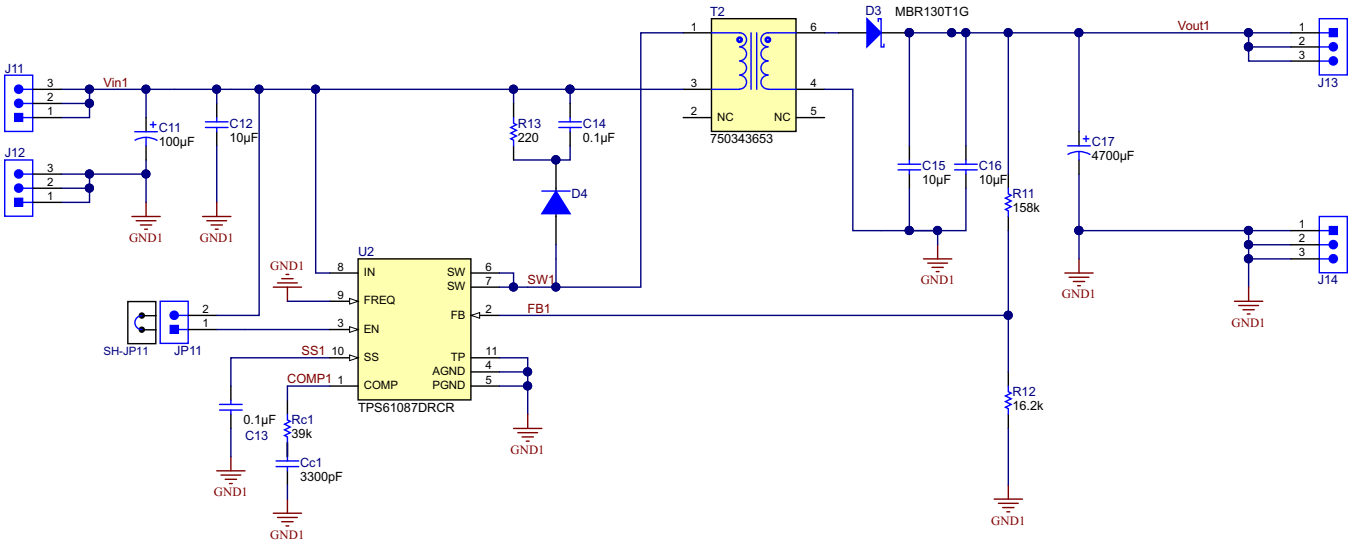

Figure 2. PMP15044 Schematic

2.2 PMP15044 Board Image

Figure 3 shows the board image of the PMP15044 device.

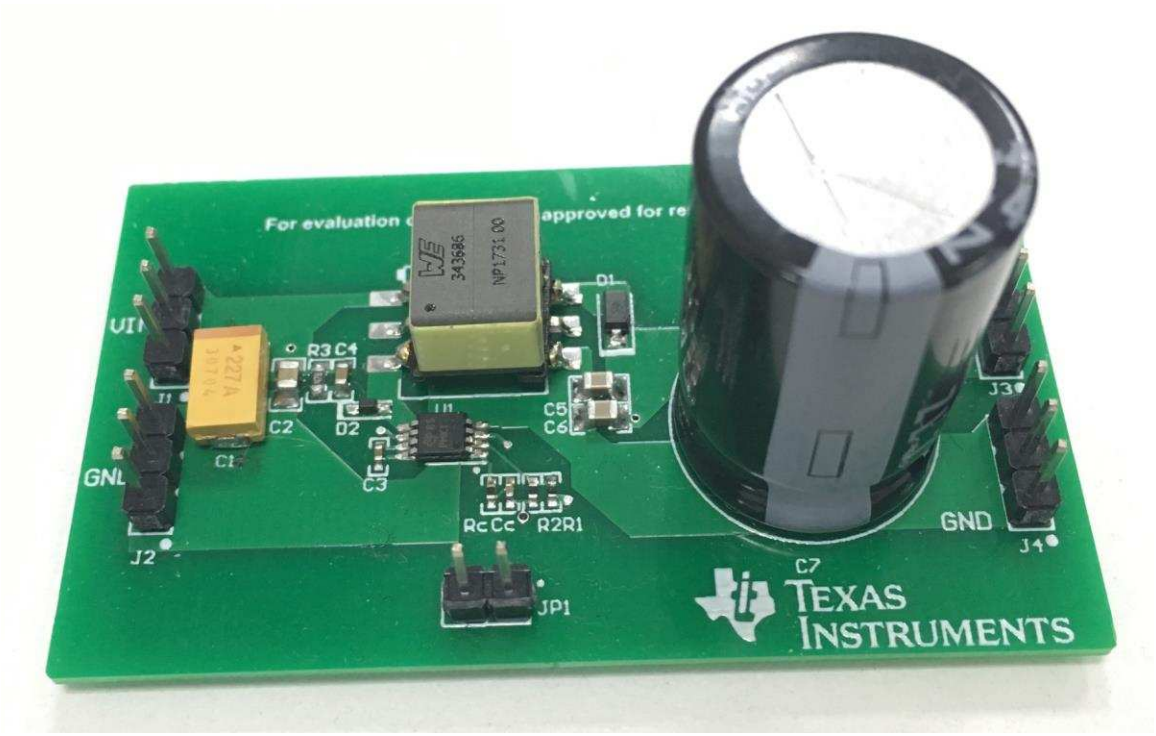

Figure 3. PMP15044 Board Image

3 Test Waveforms

3.1 Start-Up Waveforms

Figure 4 and Figure 5 show the start-up waveforms of VIN and VO, with a 4.7-mF output capacitor and 70-mF output capacitor, respectively. Users can see that regardless of the value of the output capacitance, the maximum input current is limited well below 3 A, which is around 1.3 A in the real test.

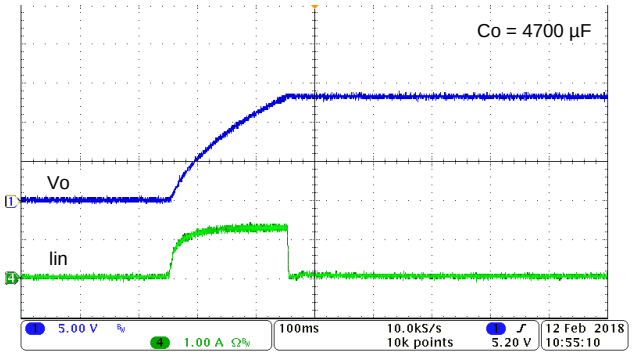

Figure 4. Start-Up Waveforms With 4700-µF Output Capacitor

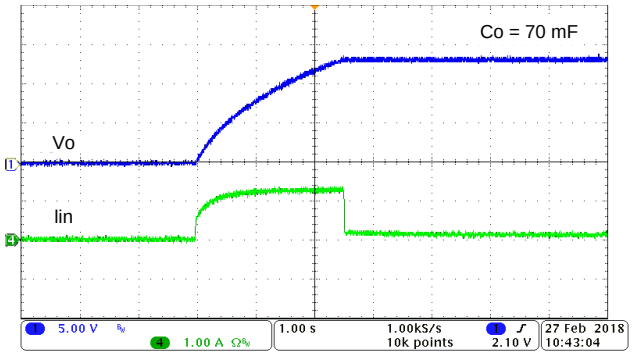

Figure 5. Start-Up Waveforms With 70-mF Output Capacitor

3.2 Switching Waveforms

Figure 6 through Figure 9 show the switching waveform and the primary-current waveform during start-up. Users can see that the TPS61087 device works in the current-limit mode during start-up.

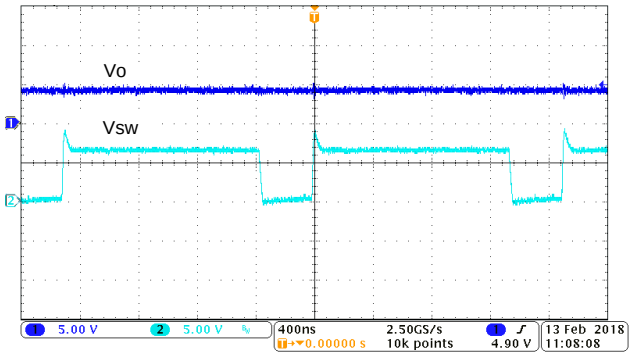

Figure 6. Switching Waveform During Start-Up (VO = 4 V)

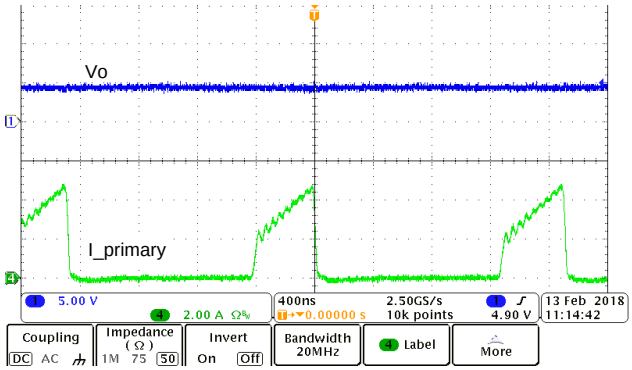

Figure 7. Primary-Current Waveform During Start-Up (VO = 4 V)

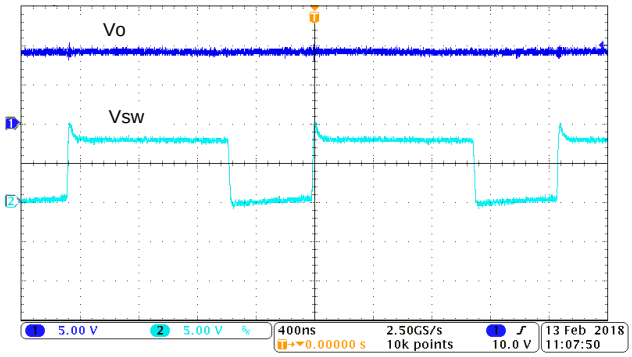

Figure 8. Switching Waveform During Start-Up (VO = 9 V)

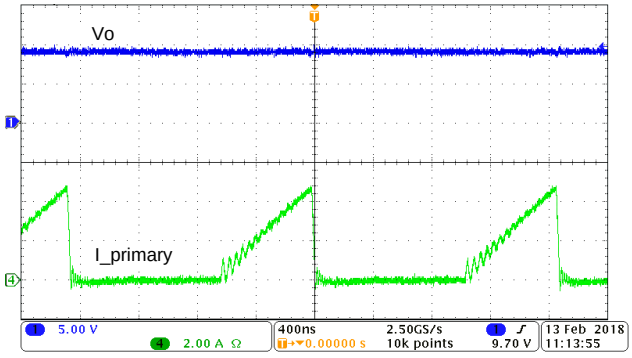

Figure 9. Primary-Current Waveform During Start-Up (VO = 9 V)

3.3 Steady-State Waveforms

Figure 10 shows the output voltage and the primary-current waveform in the steady state after start-up. When the output voltage reaches the target value, the primary current becomes very small.

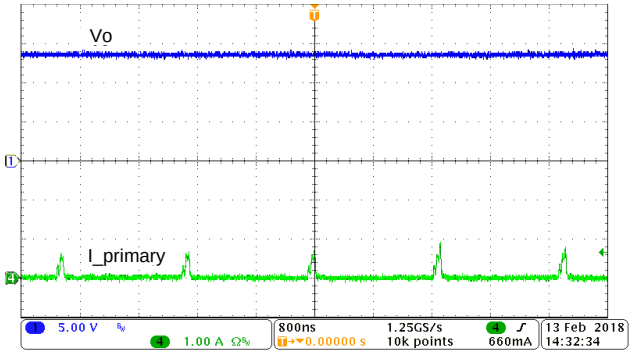

Figure 10. Primary-Current Waveform After Start-Up (VO = 13.5 V)

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