REV B1 SCHEMATIC CHANGES

UPDATE THE SOC SYMBOL TO v1.2

UPDATE Q4,Q5,Q6,Q7,Q9,Q10 TO BSZ068N06NSATMA1 (AVAILABILITY)

UPDATE R18 TO 6.04K FOR BSZ068N06NSATMA1

UPDATE PMIC PART NUMBER TO O919A14CTRGZRQ1

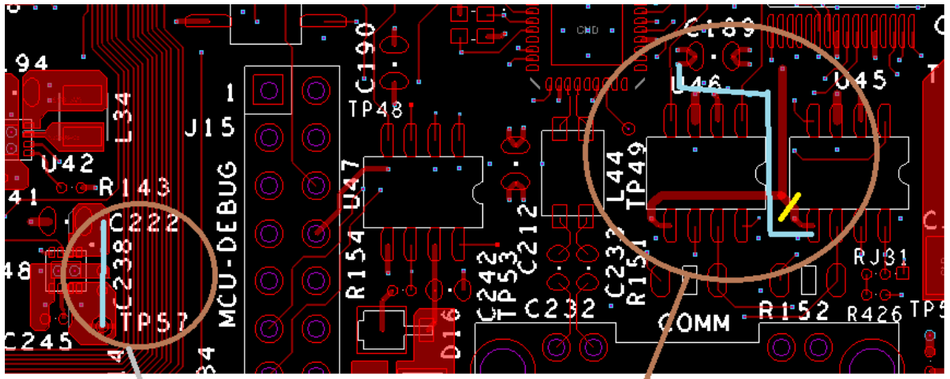
UPDATE THE AUTOMATION HEADER NOTES

REV B2 SCHEMATIC CHANGES

SHEET 20: WIRE CAN XCVR I/O SUPPLY TO VIO_3V3 INSTEAD OF VSYS_3V3. CONNECTING TO VSYS_3V3 CAUSES LEAKAGE BACK THROUGH THE VDA_USB_3V3 RAIL.

SHEET 25: WIRE ACROSS VSYS_5V0 TO VSW_5V0. NEED TO DRIVE USB LDO INPUT SUPPLY EARLIER TO PREVENT LEAKAGE THROUGH THE VDA_USB_3V3 RAIL.

REV B2 REWORK DETAILS:



REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	10/18/2016	JAC
B	BETA	07/19/2017	JAC
B1	BETA	09/06/2017	JAC
B2	BETA	10/21/2017	JAC

REVISION STATUS OF SHEETS

REV												
SH												
REV	A	B1	B1	B1	B2	B1						
SH	21	22	23	24	25	26						
REV	B	A	B	A	A	B	B	A	B	B2		
SH	11	12	13	14	15	16	17	18	19	20		
REV	B2	B	B1	B1	B1	B1	B1	A	B	B	NEXT ASSY	USED ON
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION	

DWN	J.A.C.	DATE 10/18/2016
CHK	T.W.K.	DATE 10/18/2016
ENGR	J.A.C.	DATE 10/18/2016
ENGR-MGR	J.A.C.	DATE 10/18/2016
QA	C.M.D.	DATE 10/18/2016
MFG	J.A.C.	DATE 10/18/2016
RLSE	J.A.C.	DATE 10/18/2016

TEXAS INSTRUMENTS INCORPORATED

Title: DRA71x LCARD CPU Board		
Page Contents: TITLE PAGE		
Size: C	DOC NO: 518392	REV: B2
Date: Thursday, November 09, 2017	Sheet 1 of 26	

INDEX	BALL	SIGNAL	GPIO	RAIL	IPU/IPD	SCHEMATIC NET	XPU/XPD	REF	TP OPEN GPIO
1	L3	GPMC_A11	GP2_01	VDDSHV10	IPD	SIL_RSTB_CHIP0	PD-10K	R320	1.8V GPIO
2	G1	GPMC_A12	GP2_02	VDDSHV10	IPD	SIL_RSTB_CHIP1	PD-10K	R126	REV-B
3	H3	GPMC_A13	GP2_03	VDDSHV10	IPD	NEO_RESETN			
4	H4	GPMC_A14	GP2_04	VDDSHV10	IPD	APL_RSTn	PU-2.2K	R191	
5	K6	GPMC_A15	GP2_05	VDDSHV10	IPD	nSTANDBY			
6	K5	GPMC_A16	GP2_06	VDDSHV10	IPD	nMUTE			
7	G2	GPMC_A17	GP2_07	VDDSHV10	IPD	DET_USB2_VBUS			
8	F2	GPMC_A18	GP2_08	VDDSHV10	IPD	DET_USB1_VBUS			
9	C20	MCASP2_AXR7	GP1_05	VDDSHV3	IPD	EXP_GPIO_OUT_57			
10	D20	MCASP2_AXR6	GP2_29	VDDSHV3	IPD	EXP_GPIO_OUT_74			
11	H24	XREF_CLK2	GP6_19	VDDSHV3	IPD	NEO_TIMEPULSE	PU-2.2K	R68	REV-B
12	H25	XREF_CLK3	GP6_20	VDDSHV3	IPD	H_XREF_CLK3			REV-B
13	V5	MMC1_SDWP	GP6_28	VDDSHV8	IPD	GNSS_TIME_STAMP			REV-B
14	P5	RMII_MHZ_50_CLK	GP5_17	VDDSHV9	IPD	H_GPIO5_17			REV-B
15	N5	UART3_RXD	GP5_18	VDDSHV9	IPD	VBIAS_SNS_SEL	PD-10K	R384	
16	N2	RGMII0_RXC	GP5_26	VDDSHV9	IPD	H_MMC1_SELn	PD-10K	R425	REV-B
17	P2	RGMII0_RXCTL	GP5_27	VDDSHV9	IPD	H_MCU_DCAN1_STB	PD-10K	R382	REV-B
18	N1	RGMII0_RXD3	GP5_28	VDDSHV9	IPD	H_MCU_GPIO_1			
19	P1	RGMII0_RXD2	GP5_29	VDDSHV9	IPD	H_MCU_GPIO_2			
20	N3	RGMII0_RXD1	GP5_30	VDDSHV9	IPD	H_MCU_GPIO_3			
21	N4	RGMII0_RXD0	GP5_31	VDDSHV9	IPD	H_MCU_GPIO_4			
22	F3	GPMC_CS0	GP2_19	VDDSHV10	IPU	SIL_INTB_CHIP0	PU-10K	R313	
23	G4	GPMC_CS2	GP2_20	VDDSHV10	IPU	SIL_INTB_CHIP1	PU-10K	R122	
24	L4	GPMC_CLK	GP2_22	VDDSHV10	IPU	ENET_INTSn	PU-10K	R342	
25	H5	GPMC_ADVN_ALE	GP2_23	VDDSHV10	IPU	ENET_EN	PU-10K	R358	
26	G5	GPMC_OEN_REN	GP2_24	VDDSHV10	IPU	ENET_WAKE	PU-10K	R360	
27	G6	GPMC_WEN	GP2_25	VDDSHV10	IPU	ENET_INH	PU-10K	R365	
28	H2	GPMC_BEN0	GP2_26	VDDSHV10	IPU	nFAULT	PU-2.2K-LED	R242	
29	H6	GPMC_BEN1	GP2_27	VDDSHV10	IPU	nWARN	PU-2.2K-LED	R239	
30	F6	GPMC_WAIT0	GP2_28	VDDSHV10	IPU	VBIAS_ERR	PU-10K	R135	
31	H21	GPIO6_14	GP6_14	VDDSHV3	IPU	USB1_VBUS_OCN	PU-100K	R3	
32	K22	GPIO6_15	GP6_15	VDDSHV3	IPU	USB1_STATUS	PU-100K	R2	
33	K23	GPIO6_16	GP6_16	VDDSHV3	IPU	MMC_PWR_ON	PU-10K	R412	REV-B
34	E24	SPI1_CS2	GP7_12	VDDSHV3	IPU	EXP_GPIO_INTR_43			
35	E25	SPI1_CS3	GP7_13	VDDSHV3	IPU	EXP_GPIO_OUT_78			
36	N23	UART2_RXD	GP7_26	VDDSHV4	IPU	HDMI_CEC_A	IPU-10K		
37	N25	UART2_TXD	GP7_27	VDDSHV4	IPU	HDMI_HPD			
38	U5	MMC1_SDCD	GP6_27	VDDSHV8	IPU	H_MMC1_SDCD	PU-10K	R410	REV-B
39	L5	MDIO_MCLK	GP5_15	VDDSHV9	IPU	CAMERA_PDB	PU-10K\10uF	R334	
40	L6	MDIO_D	GP5_16	VDDSHV9	IPU	CAMERA_LOCK			
41	AA4	MMC3_DAT6	GP1_24	VDDSHV8	IPU	BT_EN	PD-2.2K	R223	
42	AB1	MMC3_DAT7	GP1_25	VDDSHV8	IPU	WL_EN	PD-2.2K	R224	
43	Y2	MMC3_CLK	GP6_29	VDDSHV8	IPU	WLAN_IRQ			
44	Y1	MMC3_CMD	GP6_30	VDDSHV8	IPU	IRQ_GNSS			
45	AC10	WAKEUP0	GP1_00	VDDA33V_USB1	NA	VOUT3_INTB	PU-10K	R237	
46	AB10	WAKEUP3	GP1_03	VDDA33V_USB1	NA	H_PMIC_INTn	PU-10K(np)	R236	
47	AD3	USB1_DRVVBUS	GP6_12	VDDA33V_USB2	IPD	H_USB1_DRVVBUS	PD-10K	R11	
48	AA6	USB2_DRVVBUS	GP6_12	VDDA33V_USB2	IPD	H_USB1_DRVVBUS	PD-10K	R13	

	I2C1	I2C2	I2C4
CPU ID EEPROM	0x50		
CPU TAS6424QDKQRQ1	0x6A		
CPU DS90UB921-Q1			0x0C
CPU DS90UB934-Q1			0x30
CPU O919A13CTRGZRQ1	0x58,0x59,0x5A		
APPLE AUTHENTICATION	0x10,0x11		
CPU HDMI EEDID		0x50	

	I2C4	I2C Display
Display DS90UB924-Q1	0x2C	0x2C
Display PCF8575	Slave Device Alias ID(tbd)	0x27
Display TLC59108IPW	Slave Device Alias ID(tbd)	0x40
Display TLC59108IPW ALL CALL	Slave Device Alias ID(tbd)	0x48
Display EEPROM	Slave Device Alias ID(tbd)	0x57
Display Touch Controller	Slave Device Alias ID(tbd)	0x14
RF430CL330H	Slave Device Alias ID(tbd)	0x28

REV-B	Population	RJ-Option	Div	Device	Coupling	Sync PU/PD	SOC PIN	IPU/IPD
H_EHRPWM2A	CLK1X_A		1x	LM5175-Q1	AC	PD-110K	Y5	PU
H_EHRPWM2B	CLK2X_B		2x	LM5141-Q1	DC(VDIV)	DIV-10K/10K	Y6	PU
H_EHRPWM3A/3B	CLK8X_B_10V5	CLK8X_A_10V5	8x	LMR23625CF-Q1	AC(VDIV)	DIV-10K/3.32K	Y3/AA1	PU
H_EHRPWM3B/3A	CLK8X_B_PMIC	CLK8X_A_PMIC	8x	O917A1xxTRGZRQ1	DC	PD-49.9	AA1/Y3	PU
H_EHRPWM3A/3B	CLK8X_A	CLK8X_B	8x	LM53603	AC	PD-10K	Y3/AA1	
H_EHRPWM3A/3B	CLK8X_A	CLK8X_B	8x	TPA6404	AC/DC		Y3/AA1	

TEXAS INSTRUMENTS INCORPORATED

Title: DRA71x LCARD CPU Board		
Page Contents: NOTES		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 2 of 26	

DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

U27A

HDMI
VDDA_HDMI

hdmi1_data2x / hdmi1_data2y — AE14 / AD15 — H_HDMI_DX2 21 / H_HDMI_DY2 21
hdmi1_data1x / hdmi1_data1y — AE12 / AD13 — H_HDMI_DX1 21 / H_HDMI_DY1 21
hdmi1_data0x / hdmi1_data0y — AE11 / AD12 — H_HDMI_DX0 21 / H_HDMI_DY0 21
hdmi1_clockx / hdmi1_clocky — AE9 / AD10 — H_HDMI_CLKX 21 / H_HDMI_CLKY 21

GPMC/GPIO
VDDSHV10

GPIO
VDDSHV3

gpio6_14/mcasp1_axr8/dcan2_tx/uart10_rxd/i2c3_sda/timer1/gpio6_14 — H21 — USB1_VBUS_OCN 16
gpio6_15/mcasp1_axr9/dcan2_rx/uart10_txd/i2c3_scl/timer2/gpio6_15 — K22 — USB1_STATUS 16
gpio6_16/mcasp1_axr10/clkout1/timer3/gpio6_16 — K23 — MMC_PWR_ON 26

GPMC/MMC2
VDDSHV11

R99 0

SYSTEM

GPMC/GPIO
VDDSHV10

MEMORY-Nonvolatile

CLOCKING
VDDA_OSC

Y12 xi_osc0 — 10pF C292 — 19.2MHz/10pF Y3 — C276 10pF — xo_osc0 AB12 — vssa_osc0 AA12

xi_osc1 AC11
xo_osc1 AA11
vssa_osc1 AB11

MMC1
VDDSHV8

R68 REV-B 100

MMC3/GPIO
VDDSHV7

CONTROL
VDDSHV3

nmin_dsp — L24 — H_NMIN_DSP
porz — F19 — H_PORz 17,24
resetn — K24
rstoutn — E20 — H_RSTOUTn 9,24,26

VDDA33V_USB

Wakeup0/dcan1_rx/gpio1_0/sys_nirq2 — AC10 — VOUT3_INTB 14
Wakeup3/sys_nirq1/gpio1_3/dcan2_rx — AB10 — H_PMIC_INTn 24

Video Inputs

I2C
VDDSHV3

i2c1_scl — G22 — H_I2C1_SCL 9,11,13,19,24
i2c1_sda — G23 — H_I2C1_SDA 9,11,13,19,24
i2c2_scl/hdmi1_ddc_sda — G21 R266 0 — H_HDMI_DSDA 21
i2c2_sda/hdmi1_ddc_scl — F23 R265 0 — H_HDMI_DSCL 21
PULLUPS AT HDMI

VIN2
VDDSHV1

Debug
VDDSHV3

emu0/gpio8_30 — C21
emu1/gpio8_31 — C22
emu2 — E14 R292 22 — H_EMU0 18
emu3 — F14 — H_EMU1 18
emu4 — F13 — H_EMU2 18
H_EMU3 18
H_EMU4 18
EMU2 IS DEFAULT TRACE CLOCK.

rtck/gpio8_29 — K25 R70 22 — H_JTAG_RTCK 18
tclk — K21 — H_JTAG_TCK 18
tdi/gpio8_27 — L23 — H_JTAG_TDI 18
tdo/gpio8_28 — J20 R264 22 — H_JTAG_TDO 18
tms — L21 — H_JTAG_TMS 18
trstn — L22 — H_JTAG_TRSTn 18

CSI
VDDA_CSI

Si Test

rsv_iforce — K20
rsv_vsense — G20
rsv_atestv — L19
rsv_vpp — F20 — TP32

X777AJGCBD

DRA71x

VDA_USB_3V3
VIO_3V3
R237 10K
R236 NP
R71 2.2K
R262 10K
R402 REV-B
R263 100
C375 1000pF
PM_RESETn 26
EMU_RSTn 18
H_PORz 17,24
H_RSTOUTn 9,24,26
TP36
R104 2.2K
VOUT3_INTB 14
H_PMIC_INTn 24
VIO_3V3
R234 3.32K
R233 3.32K

J25 R72 0 — H_XREF_CLK0 19
J24 R74 0 — H_XREF_CLK1 19
H24 R79 0 — NEO_TIMEPULSE 13 REV-B
H25 R75 0 — H_XREF_CLK3 11 REV-B

VOUT3B_D16 14 — M1 — gpmc_a0/vin1a_d16/vout3_d16/vin1b_d0/i2c4_scl/uart5_rxd/gpio7_3/gpmc_a26/gpmc_a16
VOUT3B_D17 14 — M2 — gpmc_a1/vin1a_d17/vout3_d17/vin1b_d1/i2c4_sda/uart5_txd/gpio7_4
VOUT3B_D18 14 — L2 — gpmc_a2/vin1a_d18/vout3_d18/vin1b_d2/uart7_rxd/uart5_ctsn/gpio7_5
VOUT3B_D19 14 — L1 — gpmc_a3/qspi1_cs2/vin1a_d19/vout3_d19/vin1b_d3/uart7_txd/uart5_rtsn/gpio7_6
VOUT3B_D20 14 — K3 — gpmc_a4/qspi1_cs3/vin1a_d20/vout3_d20/vin1b_d4/i2c5_scl/uart6_rxd/gpio1_26
VOUT3B_D21 14 — K2 — gpmc_a5/vin1a_d21/vout3_d21/vin1b_d5/i2c5_sda/uart6_txd/gpio1_27
VOUT3B_D22 14 — J1 — gpmc_a6/vin1a_d22/vout3_d22/vin1b_d6/uart8_rxd/uart6_ctsn/gpio1_28
VOUT3B_D23 14 — K1 — gpmc_a7/vin1a_d23/vout3_d23/vin1b_d7/uart8_txd/uart6_rtsn/gpio1_29
VOUT3B_HSYNC 14 — K4 — gpmc_a8/vin1a_hsync0/vout3_hsync/vin1b_hsync1/timer12/spi4_sclk/gpio1_30
VOUT3B_VSYNC 14 — H1 — gpmc_a9/vin1a_vsync0/vout3_vsync/vin1b_vsync1/timer1/spi4_d1/gpio1_31
VOUT3B_DE 14 — J2 — gpmc_a10/vin1a_de0/vout3_de/vin1b_clk1/timer10/spi4_d0/gpio2_0
SIL_RSTB_CHIP0 10 — L3 — gpmc_a11/vin1a_fld0/vout3_fld/vin1b_de1/timer9/spi4_cs0/gpio2_1
SIL_RSTB_CHIP1 10 — G1 — gpmc_a12/gpmc_a0/vin1b_fld1/timer8/spi4_cs1/dma_evt1/gpio2_2
NEO_RESETN 13 — H3 — gpmc_a13/qspi1_rtclk/timer7/spi4_cs2/dma_evt2/gpio2_3
APL_RSTn 19 — H4 — gpmc_a14/qspi1_d3(I)/timer6/spi4_cs3/gpio2_4
nSTANDBY 11 — K6 — gpmc_a15/qspi1_d2(I)/timer5/gpio2_5
nMUTE 11 — K5 — gpmc_a16/qspi1_d0(I/O)/gpio2_6
DET_USB2_VBUS 16 — G2 — gpmc_a17/qspi1_d1(I)/gpio2_7
DET_USB1_VBUS 16 — F2 — gpmc_a18/qspi1_sclk/gpio2_8

MMC2_DAT4 9 — A4 — gpmc_a19/mmc2_dat4/gpmc_a13/vin2b_d0/vin1b_d0/gpio2_9
MMC2_DAT5 9 — E7 — gpmc_a20/mmc2_dat5/gpmc_a14/vin1b_d1/vin1b_d1/gpio2_10
MMC2_DAT6 9 — D6 — gpmc_a21/mmc2_dat6/gpmc_a15/vin1b_d2/vin1b_d2/gpio2_11
MMC2_DAT7 9 — C5 — gpmc_a22/mmc2_dat7/gpmc_a16/vin2b_d3/vin1b_d3/gpio2_12
MMC2_CLK 9 R99 0 — B5 — gpmc_a23/mmc2_clk/gpmc_a17/vin2b_d4/vin1b_d4/gpio2_13
MMC2_DAT0 9 — D7 — gpmc_a24/mmc2_dat0/gpmc_a18/vin2b_d5/vin1b_d5/gpio2_14
MMC2_DAT1 9 — C6 — gpmc_a25/mmc2_dat1/gpmc_a19/vin2b_d6/vin1b_d6/gpio2_15
MMC2_DAT2 9 — A5 — gpmc_a26/mmc2_dat2/gpmc_a20/vin2b_d7/vin1b_d7/gpio2_16
MMC2_DAT3 9 — B6 — gpmc_a27/mmc2_dat3/gpmc_a21/vin2b_hsync1/vin1b_hsync1/gpio2_17
MMC2_CMD 9 — A6 — gpmc_cs1/mmc2_cmd/gpmc_a22/vin2b_vsync1/vin1b_vsync1/gpio2_18

VOUT3B_D0 9,14,26 — F1 — gpmc_ad0/vin1a_d0/vout3_d0/gpio1_6/sysboot0
VOUT3B_D1 9,14,26 — E2 — gpmc_ad1/vin1a_d1/vout3_d1/gpio1_7/sysboot1
VOUT3B_D2 9,14,26 — E1 — gpmc_ad2/vin1a_d2/vout3_d2/gpio1_8/sysboot2
VOUT3B_D3 9,14,26 — C1 — gpmc_ad3/vin1a_d3/vout3_d3/gpio1_9/sysboot3
VOUT3B_D4 9,14,26 — D1 — gpmc_ad4/vin1a_d4/vout3_d4/gpio1_10/sysboot4
VOUT3B_D5 9,14,26 — D2 — gpmc_ad5/vin1a_d5/vout3_d5/gpio1_11/sysboot5
VOUT3B_D6 9,14 — B1 — gpmc_ad6/vin1a_d6/vout3_d6/gpio1_12/sysboot6
VOUT3B_D7 9,14 — B2 — gpmc_ad7/vin1a_d7/vout3_d7/gpio1_13/sysboot7
VOUT3B_D8 9,14 — C2 — gpmc_ad8/vin1a_d8/vout3_d8/gpio7_18/sysboot8
VOUT3B_D9 9,14 — D3 — gpmc_ad9/vin1a_d9/vout3_d9/gpio7_19/sysboot9
VOUT3B_D10 9,14 — A2 — gpmc_ad10/vin1a_d10/vout3_d10/gpio7_28/sysboot10
VOUT3B_D11 9,14 — B3 — gpmc_ad11/vin1a_d11/vout3_d11/gpio7_29/sysboot11
VOUT3B_D12 9,14 — C3 — gpmc_ad12/vin1a_d12/vout3_d12/gpio1_18/sysboot12
VOUT3B_D13 9,14 — C4 — gpmc_ad13/vin1a_d13/vout3_d13/gpio1_19/sysboot13
VOUT3B_D14 9,14 — A3 — gpmc_ad14/vin1a_d14/vout3_d14/gpio1_20/sysboot14
VOUT3B_D15 9,14 — B4 — gpmc_ad15/vin1a_d15/vout3_d15/gpio1_21/sysboot15

ENET_EN 17 — H5 — gpmc_advn_ale/gpmc_cs6/clkout2/gpmc_wait1/gpmc_a2/gpmc_a23/timer3/i2c3_sda/dma_evt2/gpio2_23/gpmc_a19
nFAULT 11 — H2 — gpmc_ben0/gpmc_cs4/vin2b_de1/vin1b_de1/timer2/dma_evt3/gpio2_26/gpmc_a21
nWARN 11 — H6 — gpmc_ben1/gpmc_cs5/vin2b_clk1/vin1b_clk1/gpmc_a3/vin2b_fld1/vin1b_fld1/timer1/dma_evt4/gpio2_27/gpmc_a22
ENET_WAKE 17 — G5 — gpmc_oen_ren/gpio2_24
ENET_INH 17 — G6 — gpmc_wen/gpio2_25
VBIAS_ERR 25 — F6 — gpmc_wait0/gpio2_28/gpmc_a25/gpmc_a15
SIL_INTB_CHIP0 10 — F3 — gpmc_cs0/gpio2_19
SIL_INTB_CHIP1 10 — G4 — gpmc_cs2/qspi1_cs0/gpio2_20/gpmc_a23/gpmc_a13
VOUT3B_CLK 14 R73 0 — G3 — gpmc_cs3/qspi1_cs1/vin1a_clk0/vout3_clk/gpmc_a1/gpio2_21/gpmc_a24/gpmc_a14
ENET_INTSn 17 — L4 — gpmc_clk/gpmc_cs7/clkout1/gpmc_wait1/vin2b_clk1/vin1b_clk1/timer4/i2c3_scl/dma_evt1/gpio2_22/gpmc_a20

H_MMC1_CLK 13,26 — V4 — mmc1_clk/gpio6_21
H_MMC1_CMD 13,26 — V3 — mmc1_cmd/gpio6_22
H_MMC1_D0 13,26 — V2 — mmc1_d0/gpio6_23
H_MMC1_D1 13,26 — W1 — mmc1_d1/gpio6_24
H_MMC1_D2 13,26 — V1 — mmc1_d2/gpio6_25
H_MMC1_D3 13,26 — U5 — mmc1_d3/gpio6_26
H_MMC1_SDCD REV-B 26 — V5 — mmc1_sdcd/uart6_rxd/i2c4_sda/gpio6_27
H_MMC1_SDWP REV-B 26 — mmc1_sdwp/uart6_txd/i2c4_scl/gpio6_28

WLAN_IRQ 13 — Y2 — mmc3_clk/usb3_ulpi_d5/vin2b_d7/vin1a_d7/ehrpwm2_tripzone_input/pr2_mii1_txd3/xx/gpio6_29
IRQ_GNSS 13 — Y1 — mmc3_cmd/spi3_sclk/usb3_ulpi_d4/vin2b_d6/vin1a_d6/eCAP2_in_PWM2_out/pr2_mii1_txd2/xx/gpio6_30
H_UART5_RXD 13 — Y4 — mmc3_dat0/spi3_d1/uart5_rxd/usb3_ulpi_d3/vin2b_d5/vin1a_d5/eQEP3A_in/pr2_mii1_txd1/xx/gpio6_31
H_UART5_TXD WILINK 1.8VIO 13 — AA2 — mmc3_dat1/spi3_d0/uart5_txd/usb3_ulpi_d2/vin2b_d4/vin1a_d4/eQEP3B_in/pr2_mii1_txd0/xx/gpio7_0
H_UART5_CTSN 13 — AA3 — mmc3_dat2/spi3_cs0/uart5_ctsn/usb3_ulpi_d1/vin2b_d3/vin1a_d3/eQEP3_index/pr2_mii_mrt_clk/xx/gpio7_1
H_UART5_RTSN 13 — W2 — mmc3_dat3/spi3_cs1/uart5_rtsn/usb3_ulpi_d0/vin2b_d2/vin1a_d2/eQEP3_strobe/pr2_mii1_rxdv/xx/gpio7_2
H_EHRPWM3A 22 — Y3 — mmc3_dat4/spi4_sclk/uart10_rxd/usb3_ulpi_nxt/vin2b_d1/vin1a_d1/ehrpwm3A/pr2_mii1_rxd3/xx/gpio1_22
H_EHRPWM3B REV-B 22 — AA1 — mmc3_dat5/spi4_d1/uart10_txd/usb3_ulpi_dir/vin2b_d0/vin1a_d0/ehrpwm3B/pr2_mii1_rxd2/xx/gpio1_23
BT_EN 13 — AA4 — mmc3_dat6/spi4_d0/uart10_ctsn/usb3_ulpi_stp/vin2b_de1/vin1a_hsync0/ehrpwm3_tripzone_input/pr2_mii1_rxd1/xx/gpio1_24
WL_EN 13 — AB1 — mmc3_dat7/spi4_cs0/uart10_rtsn/usb3_ulpi_clk/vin2b_clk1/vin1a_vsync0/eCAP3_in_PWM3_out/pr2_mii1_rxd0/xx/gpio1_25
H_EHRPWM2A 22 — V5 — gpio6_10/mdio_mclk/i2c3_sda/usb3_ulpi_d7/vin2b_hsync1/vin1a_clk/ehrpwm2a/pr2_mii_mt1_clk/xx/gpio6_10
H_EHRPWM2B 22 — Y6 — gpio6_11/mdio_d/i2c3_scl/us3_ulpi_d6/vin2b_vsync1/vin1a_de0/ehrpwm2b/pr2_mii1_txen/xx/gpio6_11

EMAC[1]_RXD0 17 — D13 — vin2a_d23/vin2b_d0/rgmii1_rxd0/vout2_d0/mii1_txen/pr1_mii1_crs/xx/gpio4_31
EMAC[1]_RXD1 17 — C13 — vin2a_d22/vin2b_d1/rgmii1_rxd1/vout2_d1/mii1_crs/pr1_mii1_col/xx/gpio4_30
EMAC[1]_RXD2 17 — E13 — vin2a_d21/vin2b_d2/rgmii1_rxd2/vout2_d2/mii1_col/pr1_mii1_rxlink/xx/gpio4_29
EMAC[1]_RXD3 17 — B13 — vin2a_d20/vin2b_d3/rgmii1_rxd3/vout2_d3/mii1_rxer/eCAP3_in_PWM3_out/pr1_mii1_rxer/xx/gpio4_28
EMAC[1]_RXCTL 17 — F11 — vin2a_d19/vin2b_d4/rgmii1_rxctl/vout2_d4/mii1_txer/ehrpwm3_tripzone_input/pr1_mii1_rxd0/xx/gpio4_27
EMAC[1]_RXC 17 — E11 — vin2a_d18/vin2b_d5/rgmii1_rxc/vout2_d5/mii1_txd3/ehrpwm3B/pr1_mii1_rxd1/xx/gpio4_26
EMAC[1]_TXD0 17 — A13 — vin2a_d17/vin2b_d6/rgmii1_txd0/vout2_d6/mii1_txd2/ehrpwm3A/pr1_mii1_rxd2/xx/gpio4_25
EMAC[1]_TXD1 17 — A12 — vin2a_d16/vin2b_d7/rgmii1_txd1/vout2_d7/mii1_txd1/eQEP3_strobe/pr1_mii1_rxd3/xx/gpio4_24
EMAC[1]_TXD2 17 — B12 — vin2a_d15/rgmii1_txd2/vout2_d8/mii1_txd0/eQEP3_index/pr1_mii1_rxdv/xx/gpio4_16
EMAC[1]_TXD3 17 — C11 — vin2a_d14/rgmii1_txd3/vout2_d9/mii1_txclk/eQEP3B_in/pr1_mii_mr1_clk/xx/gpio4_15
EMAC[1]_TXCTL 17 — D11 — vin2a_d13/rgmii1_txctl/vout2_d10/mii1_rxdv/kbd_row8/eQEP3A_in/pr1_mii1_txd0/xx/gpio4_14
EMAC[1]_TXC 17 R101 0 — B11 — vin2a_d12/rgmii1_txc/vout2_d11/mii1_rxclk/kbd_col8/eCAP2_in_PWM2_out/pr1_mii1_txd1/xx/gpio4_13
MDIO_MDIO 17 — C10 — vin2a_d11/mdio_d/vout2_d12/kbd_row7/ehrpwm2_tripzone_input/pr1_mdio_data/xx/gpio4_12/gpmc_a23
MDIO_MDCLK 17 — D10 — vin2a_d10/mdio_mclk/vout2_d13/kbd_col7/ehrpwm2B/pr1_mdio_mdclk/xx/gpio4_11/gpmc_a24
CAM_D9 18 — E10 — vin2a_d9/vout2_d14/emu19/mii1_rxd0/kbd_col6/ehrpwm2A/pr1_mii1_txd2/xx/gpio4_10/gpmc_a25
CAM_D8 18 — B10 — vin2a_d8/vout2_d15/emu18/mii1_rxd3/kbd_col5/eQEP2_strobe/pr1_mii1_txd3/xx/gpio4_9/gpmc_a26
CAM_D7 15,18 — A10 — vin2a_d7/vout2_d16/emu17/mii1_rxd2/kbd_col4/eQEP2_index/pr1_mii1_txen/xx/gpio4_8
CAM_D6 15,18 — F10 — vin2a_d6/vout2_d17/emu16/mii1_rxd1/kbd_col3/eQEP2B_in/pr1_mii_mt1_clk/xx/gpio4_7
CAM_D5 15,18 — A11 — vin2a_d5/vout2_d18/emu15/uart10_rtsn/kbd_col2/eQEP2A_in/pr1_edio_sof/xx/gpio4_6
CAM_D4 15,18 — A8 — vin2a_d4/vout2_d19/emu14/uart10_ctsn/kbd_col1/ehrpwm1_synco/pr1_edc_sync0_out/xx/gpio4_5
CAM_D3 15,18 — A9 — vin2a_d3/vout2_d20/emu13/uart10_txd/kbd_col0/ehrpwm1_synci/pr1_edc_latch0_in/xx/gpio4_4
CAM_D2 15,18 — A7 — vin2a_d2/vout2_d21/emu12/uart10_rxd/kbd_row6/eCAP1_in_PWM1_out/pr1_ecap0_ecap_capin_apwm_o/xx/gpio4_3
CAM_D1 15,18 — B9 — vin2a_d1/vout2_d22/emu11/uart9_rtsn/spi4_cs0/kbd_row5/ehrpwm1_tripzone_input/pr1_uart0_txd/xx/gpio4_2
CAM_D0 15,18 — C8 — vin2a_d0/vout2_d23/emu10/uart9_ctsn/spi4_d0/kbd_row4/ehrpwm1B/pr1_uart0_rxd/xx/gpio4_1

CAM_PCLK 15,18 — EMU5 — D8 — vin2a_clk0/vout2_fld/emu5/kbd_row0/eQEP1A_in/xx/gpio3_28/gpmc_a27/gpmc_a17
CAM_VSYNC 15,18 — EMU9 — B8 — vin2a_vsync0/vin2b_vsync1/vout2_vsync/emu9/uart9_txd/spi4_d1/kbd_row3/ehrpwm1A/pr1_uart0_rts_n/xx/gpio4_0
CAM_HSYNC 15,18 — EMU8 — E8 — vin2a_hsync0/vin2b_hsync1/vout2_hsync/emu8/uart9_rxd/spi4_sclk/kbd_row2/eQEP1_strobe/pr1_uart0_cts_n/xx/gpio3_31/gpmc_a27
CAM_FLD0 18 — EMU7 — C7 — vin2a_fld0/vin2b_clk1/vout2_clk/emu7/eQEP1_index/xx/gpio3_30/gpmc_a27/gpmc_a18
CAM_DE0 18 — EMU6 — B7 — vin2a_de0/vin2a_fld0/vin2b_fld1/vin2b_de1/vout2_de/emu6/kbd_row1/eQEP1B_in/xx/gpio3_29

H_CSI2_DX0 19 — AC1 — csi2_0_dx0
H_CSI2_DY0 19 — AB2 — csi2_0_dy0
H_CSI2_DX1 19 — AD1 — csi2_0_dx1
H_CSI2_DY1 19 — AC2 — csi2_0_dy1
H_CSI2_DX2 19 — AE2 — csi2_0_dx2
H_CSI2_DY2 19 — AD2 — csi2_0_dy2

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA71x LCARD CPU Board		
Page Contents:	DRA71x MEM VIP CAM DIS SYS		
Size: C	DOC NO: 518392	REV: B1	
Date: Thursday, November 09, 2017	Sheet 3 of 26		

U27E

DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

CONNECTIVITY

PCIe

VDDA_PCIE

AD7 pcie_rxp0
AE6 pcie_rxn0
AD9 pcie_txp0
AE8 pcie_txn0
AC8 ljcb_clkp
AB9 ljcb_clkn

USB

VDDA33V_USB

AC6 usb1_dp
AB7 usb1_dn
AD3 usb1_drvvbus/timer16/gpio6_12
AB6 usb2_dp
AC5 usb2_dn
AA6 usb2_drvvbus/timer15/gpio6_13

VDDA_USB

AD6 usb_rxp0/pcie_rxp1
AE5 usb_rxn0/pcie_rxn1
AD4 usb_txp0/pcie_txp1
AE3 usb_txn0/pcie_txn1

ETHERNET

VDDSHV9

T4 rgmii0_txc/uart3_ctsn/rmii1_rxd1/mii0_rxd3/vin2a_d3/vin1b_d3/usb3_ulpi_clk/spi3_d0/spi4_cs2/pr1_mii0_rxd3/xx/gpio5_20
T5 rgmii0_txctl/uart3_rtsn/rmii1_rxd0/mii0_rxd2/vin2a_d4/vin1b_d4/usb3_ulpi_stp/spi3_cs0/spi4_cs3/pr1_mii0_rxd2/xx/gpio5_21
R1 rgmii0_txd0/rmii0_rxd0/mii0_rxd0/vin2a_d10/usb3_ulpi_d1/spi4_cs0/uart4_rtsn/pr1_mii0_rxd0/xx/gpio5_25
R2 rgmii0_txd1/rmii0_rxd1/mii0_rxd1/vin2a_vsync0/vin1b_vsync1/usb3_ulpi_d0/spi4_d0/uart4_ctsn/pr1_mii0_rxd1/xx/gpio5_24
P3 rgmii0_txd2/rmii0_rxer/mii0_rxer/vin2a_hsync0/vin1b_hsync1/usb3_ulpi_nxt/spi4_d1/uart4_txd/pr1_mii0_rxer/xx/gpio5_23
P4 rgmii0_txd3/rmii0_crs/mii0_crs/vin2a_de0/vin1b_de1/usb3_ulpi_dir/spi4_sclk/uart4_rxd/pr1_mii0_crs/xx/gpio5_22

N2 rgmii0_rxc/rmii1_txen/mii0_txclk/vin2a_d5/vin1b_d5/usb3_ulpi_d2/pr1_mii_mt0_clk/xx/gpio5_26
P2 rgmii0_rxctl/rmii1_txd1/mii0_txd3/vin2a_d6/vin1b_d6/usb3_ulpi_d3/pr1_mii0_txd3/xx/gpio5_27
N4 rgmii0_rxd0/rmii0_txd0/mii0_txd0/vin2a_fld0/vin1b_fld1/usb3_ulpi_d7/pr1_mii0_txd0/xx/gpio5_31
N3 rgmii0_rxd1/rmii0_txd1/mii0_txd1/vin2a_d9/usb3_ulpi_d6/pr1_mii0_txd1/xx/gpio5_30
P1 rgmii0_rxd2/rmii0_txen/mii0_txen/vin2a_d8/usb3_ulpi_d5/pr1_mii0_txen/xx/gpio5_29
N1 rgmii0_rxd3/rmii1_txd0/mii0_txd2/vin2a_d7/vin1b_d7/usb3_ulpi_d4/pr1_mii0_txd2/xx/gpio5_28

P5 RMII_MHZ_50_CLK/vin2a_d11/xx/gpio5_17

L6 mdio_d/uart3_ctsn/mii0_txer/vin2a_d0/vin1b_d0/pr1_mii0_rxlink/xx/gpio5_16
L5 mdio_mclk/uart3_rtsn/mii0_col/vin2a_clk0/vin1b_clk1/pr1_mii0_col/xx/gpio5_15

MLBP

VDDS_MLB

U2 mlbp_clk_p
U1 mlbp_clk_n
T2 mlbp_d_p
T1 mlbp_d_n
T3 mlbp_sig_p
U4 mlbp_sig_n

UART

VDDSHV4

M25 uart1_txd/mmc4_sdwp/gpio7_23
L25 uart1_rxd/mmc4_sdcd/gpio7_22
M24 uart1_rtsn/uart9_txd/mmc4_cmd/gpio7_25
L20 uart1_ctsn/uart9_rxd/mmc4_clk/gpio7_24

N25 uart2_txd/uart3_rtsn/uart3_sd/mmc4_dat1/uart2_txd/uart1_dsrn/gpio7_27
N23 uart2_rxd/uart3_ctsn/uart3_rctx/mmc4_dat0/uart2_rxd/uart1_dcdn/gpio7_26
N24 uart2_rtsn/uart3_txd/uart3_irtx/mmc4_dat3/uart10_txd/uart1_rin/gpio1_17
N22 uart2_ctsn/uart3_irrx/mmc4_dat2/uart10_rxd/uart1_dtrn/gpio1_16

N6 uart3_txd/rmii1_rxer/mii0_rxclk/vin2a_d2/vin1b_d2/spi3_d1/spi4_cs1/pr1_mii_mr0_clk/xx/gpio5_19
N5 uart3_rxd/rmii1_crs/mii0_rxdv/vin2a_d1/vin1b_d1/spi3_sclk/pr1_mii0_rxdv/xx/gpio5_18

VDDSHV9

MCASP

VDDSHV3

mcasp1_aclkr/mcasp7_axr2/i2c4_sda/gpio5_0
mcasp1_aclkx/vin1a_fld0/i2c3_sda/pr2_mdio_mdclk/xx/gpio7_31
mcasp1_fsx/vin1a_de0/i2c3_scl/pr2_mdio_data/gpio7_30
mcasp1_fsr/mcasp7_axr3/i2c4_scl/gpio5_1
mcasp1_axr0/uart6_rxd/vin1a_vsync0/i2c5_sda/pr2_mii0_rxer/xx/gpio5_2
mcasp1_axr1/uart6_txd/vin1a_hsync0/i2c5_scl/pr2_mii_mt0_clk/xx/gpio5_3
mcasp1_axr2/mcasp6_axr2/uart6_ctsn/gpio5_4
mcasp1_axr3/mcasp6_axr3/uart6_rtsn/gpio5_5
mcasp1_axr4/mcasp4_axr2/gpio5_6
mcasp1_axr5/mcasp4_axr3/gpio5_7
mcasp1_axr6/mcasp5_axr2/gpio5_8
mcasp1_axr7/mcasp5_axr3/timer4/gpio5_9
mcasp1_axr8/mcasp6_axr0/spi3_sclk/vin1a_d15/timer5/pr2_mii0_txen/xx/gpio5_10
mcasp1_axr9/mcasp6_axr1/spi3_d1/vin1a_d14/timer6/pr2_mii0_txd3/xx/gpio5_11
mcasp1_axr10/mcasp6_aclkx/mcasp6_aclkr/spi3_d0/vin1a_d13/timer7/pr2_mii0_txd2/xx/gpio5_12
mcasp1_axr11/mcasp6_fsx/mcasp6_fsr/spi3_cs0/vin1a_d12/timer8/pr2_mii0_txd1/xx/gpio4_17
mcasp1_axr12/mcasp7_axr0/spi3_cs1/vin1a_d11/timer9/pr2_mii0_txd0/xx/gpio4_18
mcasp1_axr13/mcasp7_axr1/vin1a_d10/timer10/pr2_mii_mr0_clk/xx/gpio6_4
mcasp1_axr14/mcasp7_aclkx/mcasp7_aclkr/vin1a_d9/timer11/pr2_mii0_rxdv/xx/gpio6_5
mcasp1_axr15/mcasp7_fsx/mcasp7_fsr/vin1a_d8/timer12/pr2_mii0_rxd3/xx/gpio6_6

D16 H_MCASP1_ACLKR_I2C4_SDA 19
C16 R103 0 H_MCASP1_ACLKX 19
C17 H_MCASP1_FSX 19
D17 H_MCASP1_FSR_I2C4_SCL 19
D14 H_I2C5_SDA 19
B14 H_I2C5_SCL 19
C14 H_MCASP1_AXR2 19
B15 H_MCASP1_AXR3 19
A15 H_MCASP1_AXR4 19
A14 H_MCASP1_AXR5 19
A17 H_MCASP1_AXR6 19
A16 H_MCASP1_AXR7 19
A18 H_MCASP1_AXR8 19
B17 H_MCASP1_AXR1 19
B16 R100 0 H_MCASP6_ACLKX_ACLKR 19
B18 H_MCASP6_FSX_FSR 19
A19 H_MCASP1_AXR12 19
E17 H_MCASP7_AXR1 19
E16 R102 0 H_MCASP7_ACLKX_ACLKR 19
F16 H_MCASP7_FSX_FSR 19

mcasp2_aclkx/vin1a_d7/pr2_mii0_rxd2/xx
mcasp2_fsx/vin1a_d6/pr2_mii0_rxd1/xx
mcasp2_axr0
mcasp2_axr1
mcasp2_axr2/mcasp3_axr2/vin1a_d5/pr2_mii0_rxd0/xx/gpio6_8
mcasp2_axr3/mcasp3_axr3/vin1a_d4/pr2_mii0_rxdnk/xx/gpio6_9
mcasp2_axr4/mcasp8_axr0/gpio1_4
mcasp2_axr5/mcasp8_axr1/gpio6_7
mcasp2_axr6/mcasp8_aclkx/mcasp8_aclkr/gpio2_29
mcasp2_axr7/mcasp8_fsx/mcasp8_fsr/gpio1_5

VDDSHV3

E19 R267 0 H_MCASP2_ACLKX 10
D19 H_MCASP2_FSX 10
A20 H_MCASP2_AXR0 10
B19 H_MCASP2_AXR1 10
A21 H_MCASP3_AXR2 10
B21 H_MCASP3_AXR3 10
B20 H_MCASP2_AXR4 10
C19 H_MCASP2_AXR5 10
D20 EXP_GPIO_OUT_57 19
C20 EXP_GPIO_OUT_74 19

mcasp3_aclkx/mcasp3_aclkr/mcasp2_axr12/uart7_rxd/vin1a_d3/pr2_mii0_crs/xx/gpio5_13
mcasp3_fsx/mcasp3_fsr/mcasp2_axr13/uart7_txd/vin1a_d2/pr2_mii0_col/xx/gpio5_14
mcasp3_axr0/mcasp2_axr14/uart7_ctsn/uart5_rxd/vin1a_d1/pr2_mii1_rxer/xx
mcasp3_axr1/mcasp2_axr15/uart7_rtsn/uart5_txd/vin1a_d0/vin5a_fld0/pr2_mii1_rxlink/xx

VDDSHV3

A22 R98 0 H_MCASP3_ACLKX 10
A23 H_MCASP3_FSX 10
B22 H_MCASP3_AXR0 10
B23 H_MCASP3_AXR1 10

mcasp4_aclkx/mcasp4_aclkr/spi3_sclk/uart8_rxd/i2c4_sda
mcasp4_fsx/mcasp4_fsr/spi3_d1/uart8_txd/i2c4_scl
mcasp4_axr0/spi3_d0/uart8_ctsn/uart4_rxd/i2c6_scl
mcasp4_axr1/spi3_cs0/uart8_rtsn/uart4_txd/xx/i2c6_sda

VDDSHV3

C23 R97 0 H_MCASP4_ACLKX 11
B25 H_MCASP4_FSX 11
A24 H_MCASP4_AXR0 11
D23 H_MCASP4_AXR1 11

mcasp5_aclkx/mcasp5_aclkr/spi4_sclk/uart9_rxd/i2c5_sda/mlb_clk/xx
mcasp5_fsx/mcasp5_fsr/spi4_d1/uart9_txd/i2c5_scl/xx
mcasp5_axr0/spi4_d0/uart9_ctsn/uart3_rxd/mlb_sig/pr2_mdio_mdclk/xx
mcasp5_axr1/spi4_cs0/uart9_rtsn/uart3_txd/mlb_dat/pr2_mdio_data/xx

VDDSHV7

AC3 R429 0 H_MCASP5_ACLKX 13
U6 H_MCASP5_FSX 13
AA5 H_MCASP5_AXR0 13
AC4 H_MCASP5_AXR1 13

SPI

VDDSHV3

spi1_cs0/gpio7_10
spi1_cs1/spi2_cs1/gpio7_11
spi1_cs2/uart4_rxd/mmc3_sdcd/spi2_cs2/dcan2_tx/mdio_mclk/hdmi1_hpd/gpio7_12
spi1_cs3/uart4_txd/mmc3_sdwp/spi2_cs3/dcan2_rx/mdio_d/hdmi1_cec/gpio7_13
spi1_d0/gpio7_9
spi1_d1/gpio7_8
spi1_sclk/gpio7_7

B24 H_SPI1_CS0 10
C25 H_SPI1_CS1 10
E24 EXP_GPIO_INTR_43 19
E25 EXP_GPIO_INTR_77 19
D25 H_SPI1_D0 10
D24 H_SPI1_D1 10
C24 R81 100 H_SPI1_SCLK 10

spi2_cs0/uart3_rtsn/uart5_txd/gpio7_17
spi2_d0/uart3_ctsn/uart5_rxd/gpio7_16
spi2_d1/uart3_txd/gpio7_15
spi2_sclk/uart3_rxd/gpio7_14

F24 H_SPI2_CS0 19
G24 H_SPI2_D0 19
F25 H_SPI2_D1 19
G25 R77 0 H_SPI2_SCLK 19

DCAN

VDDSHV3

dcan1_tx/uart8_rxd/mmc2_sdcd/hdmi1_hpd/gpio1_14
dcan1_rx/uart8_txd/mmc2_sdwp/hdmi1_cec/gpio1_15

H22 H_DCAN1_TX 20
H23 H_DCAN1_RX 20

MCU

X777AJGCBD

R81 FROM 0 OHM TO 100 OHMS TO REDUCE REFLECTION AT THE DRIVER. SOC RCVR IS CLOCKING ON SCLK FEEDBACK AT THE PIN.

16 H_USB1_DP
16 H_USB1_DN
16 H_USB1_DRVVBUS
16 H_USB2_DP
16 H_USB2_DN
16 H_USB2_DRVVBUS
16 H_USB3_RXP
16 H_USB3_RXN
16 H_USB3_TXP
16 H_USB3_TXN

19 H_SPI4_CS2
19 H_SPI4_CS3
19 H_SPI4_CS0
19 H_SPI4_D0
19 H_SPI4_D1
19 H_SPI4_SCLK
R183 0

REV=B 26 H_MMC1_SELn
REV=B 20 H_MCU_DCAN1_STB
20 H_MCU_GPIO_4
20 H_MCU_GPIO_3
20 H_MCU_GPIO_2
20 H_MCU_GPIO_1

26 H_GPIO5_17

15 CAMERA_LOCK
15 CAMERA_PDB

MCU 20 H_UART1_TXD
20 H_UART1_RXD
NEO 13 H_UART9_TXD
13 H_UART9_RXD

21 HDMI_CEC_A
21 HDMI_HPD
18 H_UART3_TXD_BOOT
18 H_UART3_RXD_BOOT

19 H_SPI4_CS1
25 VBIAS_SNS_SEL

EXPANSION

TUNER

TUNER

CLASS D AMP

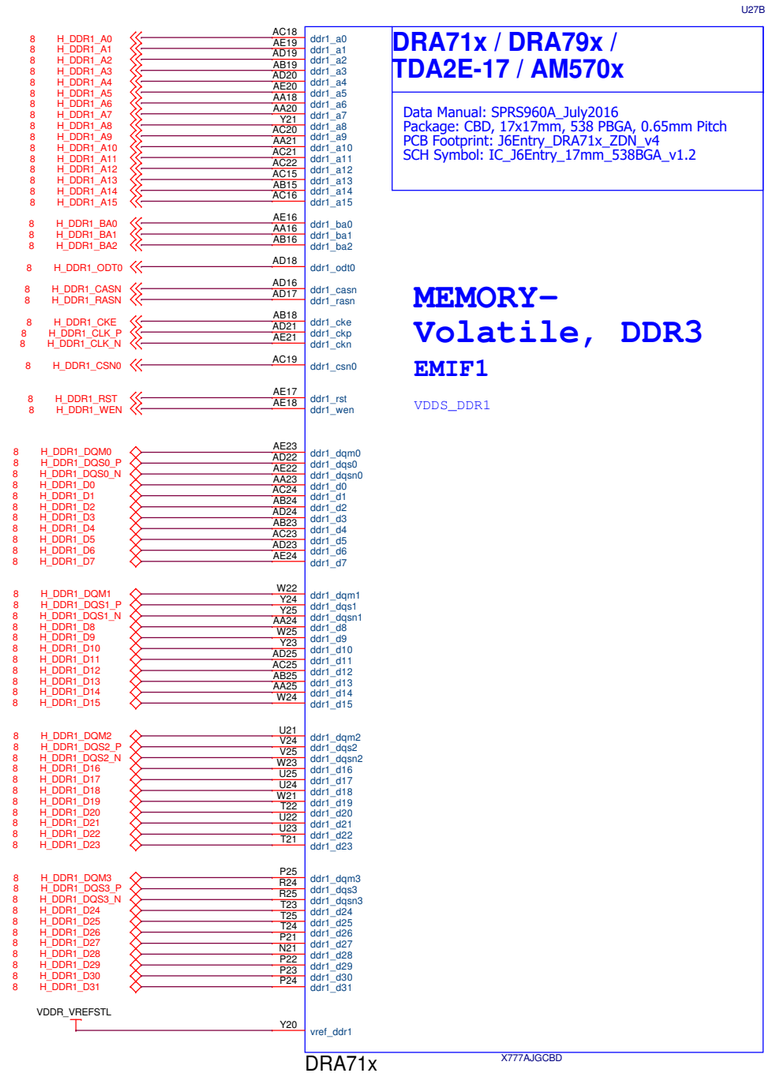
WILINK

TUNER

EXPANSION

MCU

TEXAS INSTRUMENTS INCORPORATED	
Title: DRA71x LCARD CPU Board	
Page Contents: DRA71x CNTVY	
Size: C	DOC NO: 518392 REV: B1
Date: Thursday, November 09, 2017	Sheet 4 of 26



TEXAS INSTRUMENTS INCORPORATED

Title: DRA71x LCARD CPU Board		
Page Contents: DRA71x DDR		
Size: C	DOC NO: 518392	REV: B1
Date: Thursday, November 09, 2017	Sheet 5 of 26	

DRA71x / DRA79x / TDA2E-17 / AM570x

Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER

ANALOG SUPPLIES

INTERNAL LDOs

VDA_PLL_1V8

C406 1uF 10V X7S 0402
C331 0.1uF 16V 0402

E5 80dB @ 27MHz 0805 2A
C372 1uF 10V X7S 0402
C359 0.1uF 16V 0402
VDA_COREGMACVID_FIL1V8

E4 80dB @ 27MHz 0805 2A
C343 1uF 10V X7S 0402
C340 0.1uF 16V 0402
VDA_DDRDBGGPUPER_FIL1V8

E7 80dB @ 27MHz 0805 2A
C407 1uF 10V X7S 0402
C349 0.1uF 16V 0402
VDA_MPU_ABE_FIL1V8

E1 80dB @ 27MHz 0805 2A
C286 1uF 10V X7S 0402
C309 0.1uF 16V 0402
VDA_OSC_FIL1V8

E6 80dB @ 27MHz 0805 2A
C408 1uF 10V X7S 0402
C364 0.47uF 10V X7S 0402
VDA_VIDEO_FIL1V8

VDA_PHY_1V8

E3 80dB @ 27MHz 0805 2A
C324 1uF 10V X7S 0402
C333 0.1uF 16V 0402
VDA_CSI_FIL1V8

C308 0.1uF 16V 0402

E2 80dB @ 27MHz 0805 2A
C301 1uF 10V X7S 0402
C310 0.1uF 16V 0402
VDA_PCIE_FIL1V8

C302 1uF 10V X7S 0402
C306 0.1uF 16V 0402

DRA71x

R20	vdda_ddr
L9	vdda_core_gmac
K10	vdda_dsp_iva_1
L10	vdda_dsp_iva_2
N10	vdda_debug
N9	vdda_gpu
M10	vdda_per
K16	vdda_mpu_abe_1
L16	vdda_mpu_abe_2
W13	vdda_osc_1
Y13	vdda_osc_2
K14	vdda_video_1
L14	vdda_video_2
T6	vdda_csi
W15	vdda_hdmi_1
Y15	vdda_hdmi_2
W11	vdda_pcie_1
Y11	vdda_pcie_2
W8	vdda_usb_1
Y8	vdda_usb_2
Y9	vdda_usb_3
AA10	vdda33v_usb_1
Y10	vdda33v_usb_2

VDA_USB_3V3

C285 0.1uF 0402 16V
C284 1uF 10V X7S 0402
C281 10uF 10V X7R 0805

U27C

X777AJGCBD

cap_vbbldo_dsp	F8	VCAP_VBBLDO_DSP
cap_vbbldo_gpu	T7	VCAP_VBBLDO_GPU
		VCAP_VBBLDO_IVA
		VCAP_VBBLDO_MPU
cap_vbbldo_iva	G14	
cap_vbbldo_mpu	F17	
cap_vddram_core1	U20	VCAP_VDDRAM_CORE1
		VCAP_VDDRAM_CORE3
		VCAP_VDDRAM_CORE4
cap_vddram_core3	K7	
cap_vddram_core4	G19	
cap_vddram_dsp	L7	VCAP_VDDRAM_DSP
cap_vddram_gpu	V7	VCAP_VDDRAM_GPU
		VCAP_VDDRAM_IVA
		VCAP_VDDRAM_MPU
cap_vddram_iva	G12	
cap_vddram_mpu	G18	

C394 1uF 10V X7S 0402
C395 1uF 10V X7S 0402
C329 1uF 10V X7S 0402
C388 1uF 10V X7S 0402

C412 1uF 10V X7S 0402
C358 1uF 10V X7S 0402
C322 1uF 10V X7S 0402

C374 1uF 10V X7S 0402
C426 1uF 10V X7S 0402
C320 1uF 10V X7S 0402
C334 1uF 10V X7S 0402

TEXAS INSTRUMENTS INCORPORATED

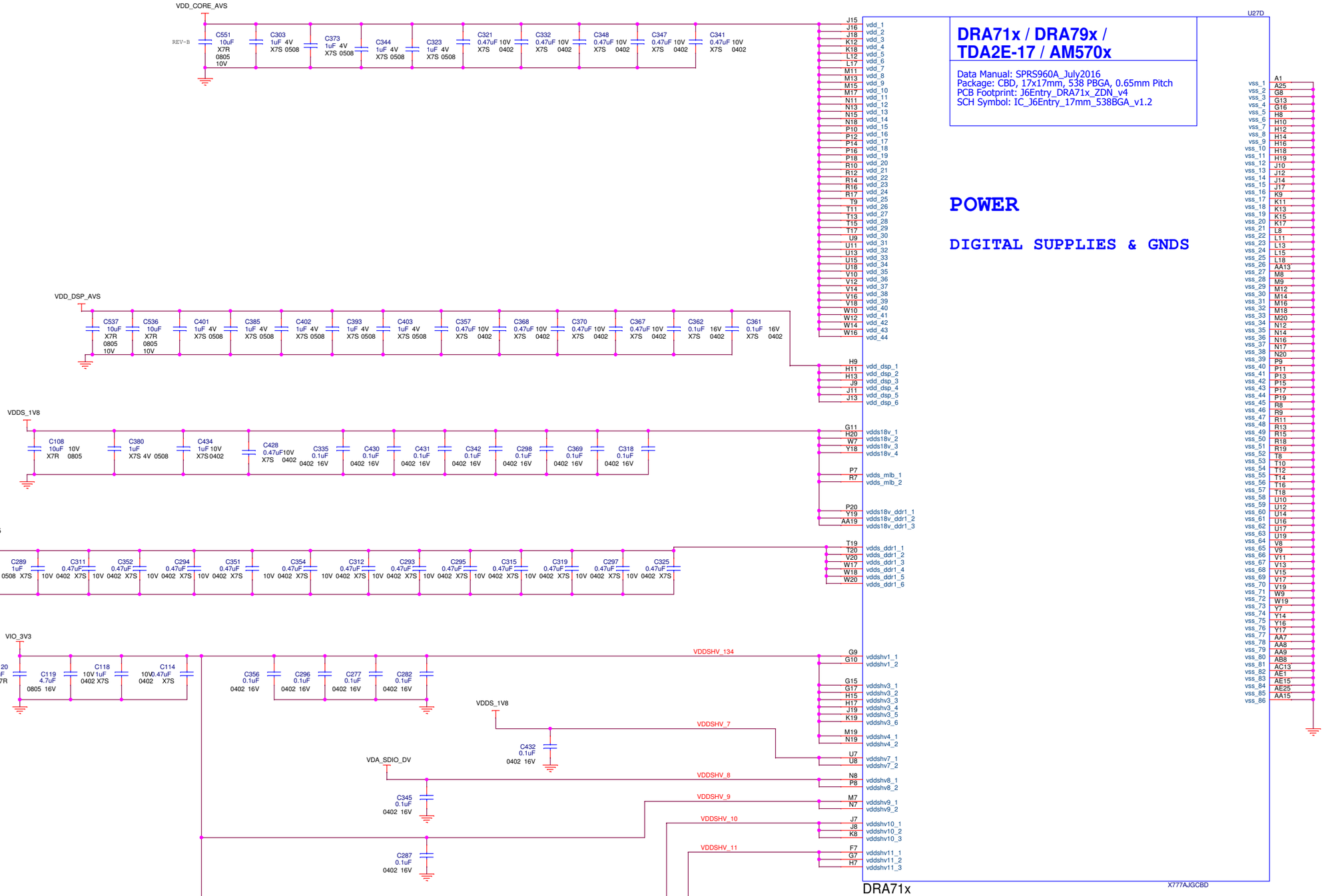
Title:	DRA71x LCARD CPU Board		
Page Contents:	DRA71x ANA PWR		
Size: C	DOC NO: 518392		REV: B1
Date: Thursday, November 09, 2017	Sheet 6	of	26

DRA71x / DRA79x / TDA2E-17 / AM570x

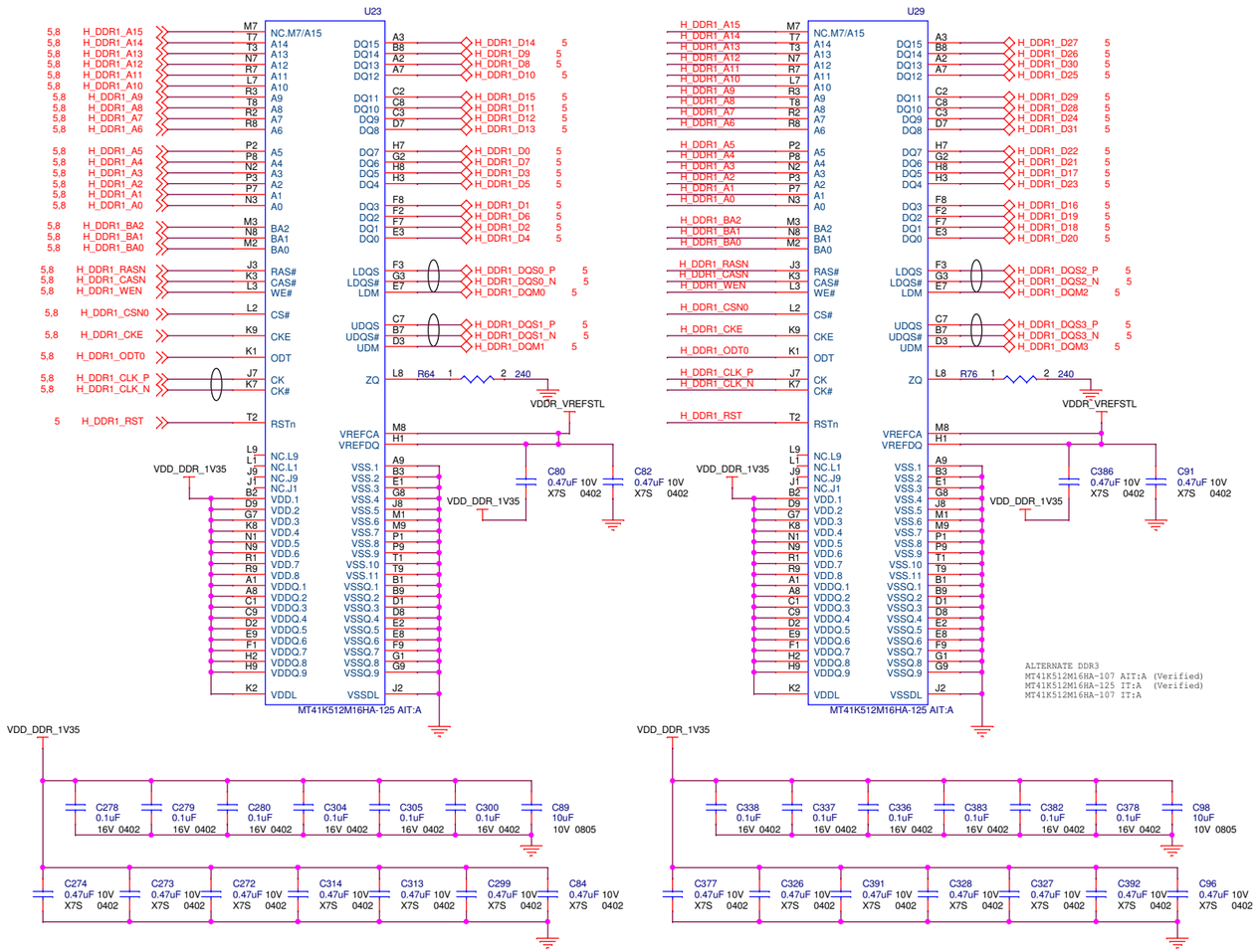
Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

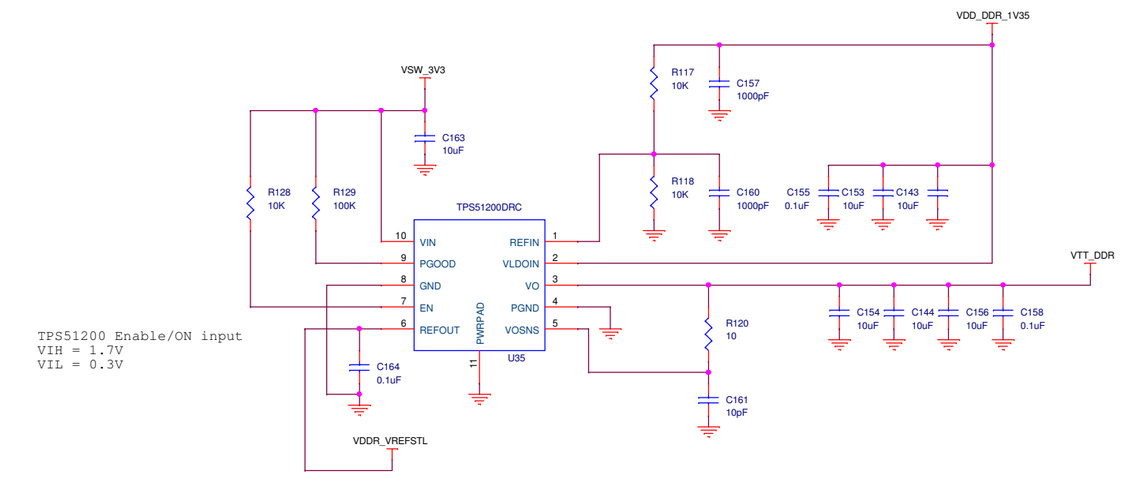
POWER

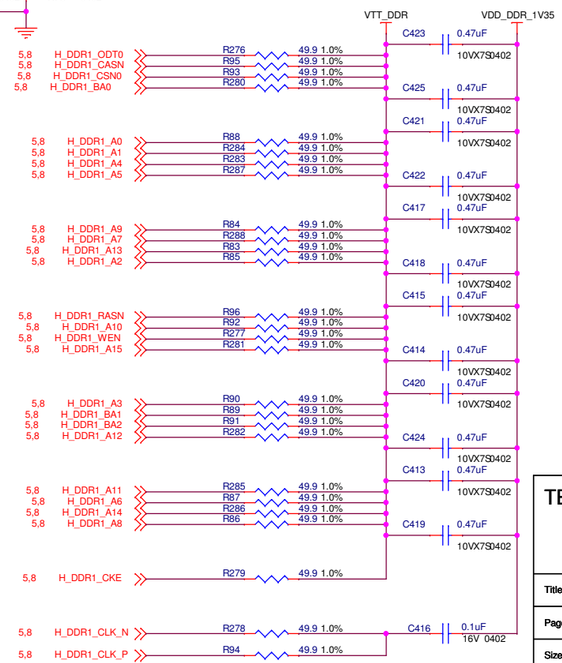
DIGITAL SUPPLIES & GNDS



TEXAS INSTRUMENTS INCORPORATED		
Title: DRA71x LCARD CPU Board		
Page Contents: DRA71x DIG PWR		
Size: C	DOC NO: 518392	REV: B1
Date: Thursday, November 09, 2017	Sheet 7 of 26	

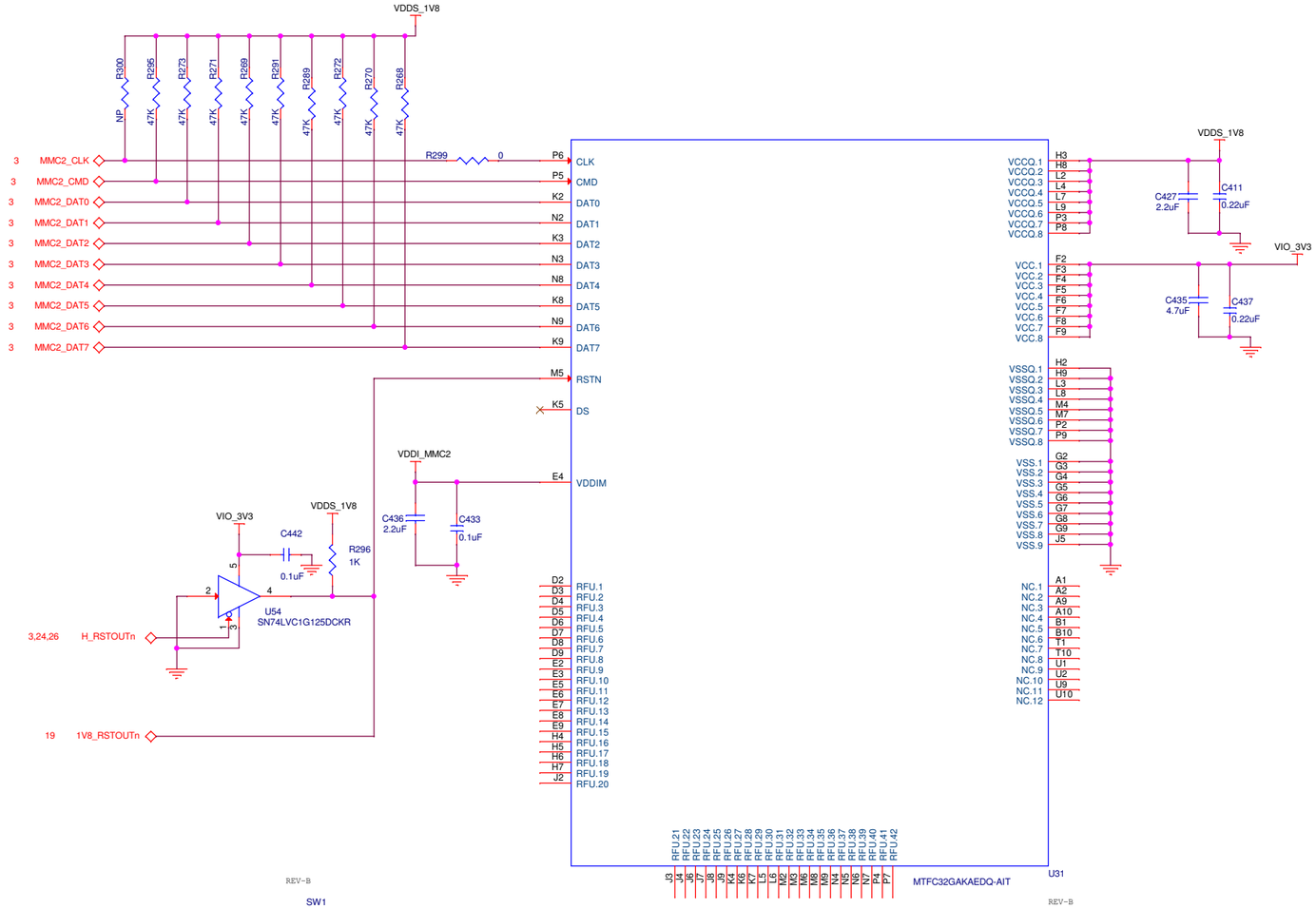


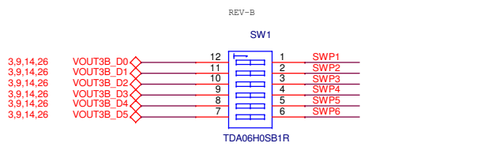


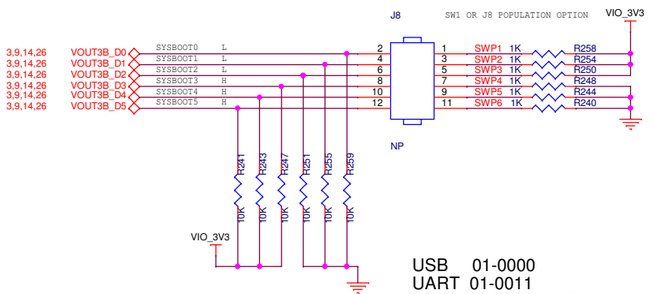


TEXAS INSTRUMENTS INCORPORATED

Title:	DRA71x LCARD CPU Board		
Page Contents:	DDR3 MEMORY BANK 1		
Size: C	DOC NO: 518392		REV: A
Date: Thursday, November 09, 2017	Sheet 8	of	26



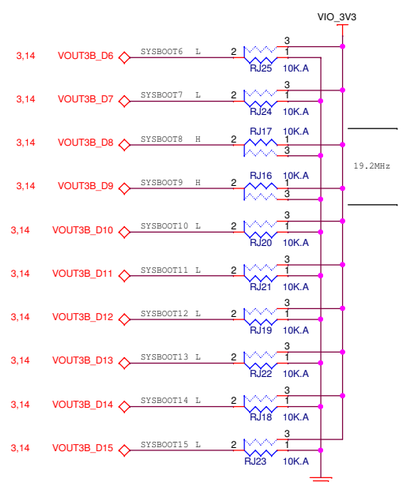


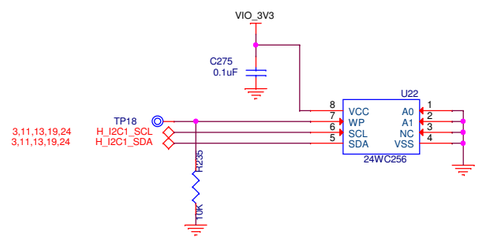


USB 01-0000
UART 01-0011
eMMC 10-0000 (USB)
DEFAULT eMMC 11-1000
eMMC 11-1011 (BOOT PART)
SD 11-0000

JUMPER/SWITCH
X INSTALLED/ON
O NOT INSTALLED/OFF

USB XO-XOOO
UART XO-XOXX
eMMC OX-XOOO
eMMC OO-OOOO
eMMC OO-00XX
SD OO-X000





TEXAS INSTRUMENTS INCORPORATED

Title: DRA71x LCARD CPU Board		
Page Contents: MEM eMMC/SD CARD		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 9 of 26	

REV-B

U36 Si4791x/2x

U34 Si4790x

J18 FAKRA II BLACK

J16 FAKRA II WHITE

J12 NP-HDR3

J11 NP-HDR3

X2 36.864MHz

U56 74LVC125APWR

U55 74LVC125APWR

D17 D14 D13 D12 D18 D15 CM1213A-01SO

VIO_3V3 VTUN_3V3 VTUN_1V8

HUB_AOUT0 HUB_AOUT1 HUB_AOUT2 HUB_AOUT3 HUB0_CLKO

H_MCASP3_AXR0 H_MCASP3_AXR1 H_MCASP3_ACLKX H_MCASP3_FSX

H_MCASP2_AXR0 H_MCASP2_ACLKX H_MCASP2_AXR1 H_MCASP2_FSX

H_MCASP3_AXR2 H_MCASP3_AXR3 H_MCASP2_AXR4 H_MCASP2_AXR5

ISFSP_CHIP_01 ISFSN_CHIP_01

H_SPI1_CS0 H_SPI1_SCLK H_SPI1_D0 H_SPI1_D1

H_SPI1_CS1 H_SPI1_SCLK H_SPI1_D0 H_SPI1_D1

SIL_INTB_CHIP0 SIL_RSTB_CHIP0

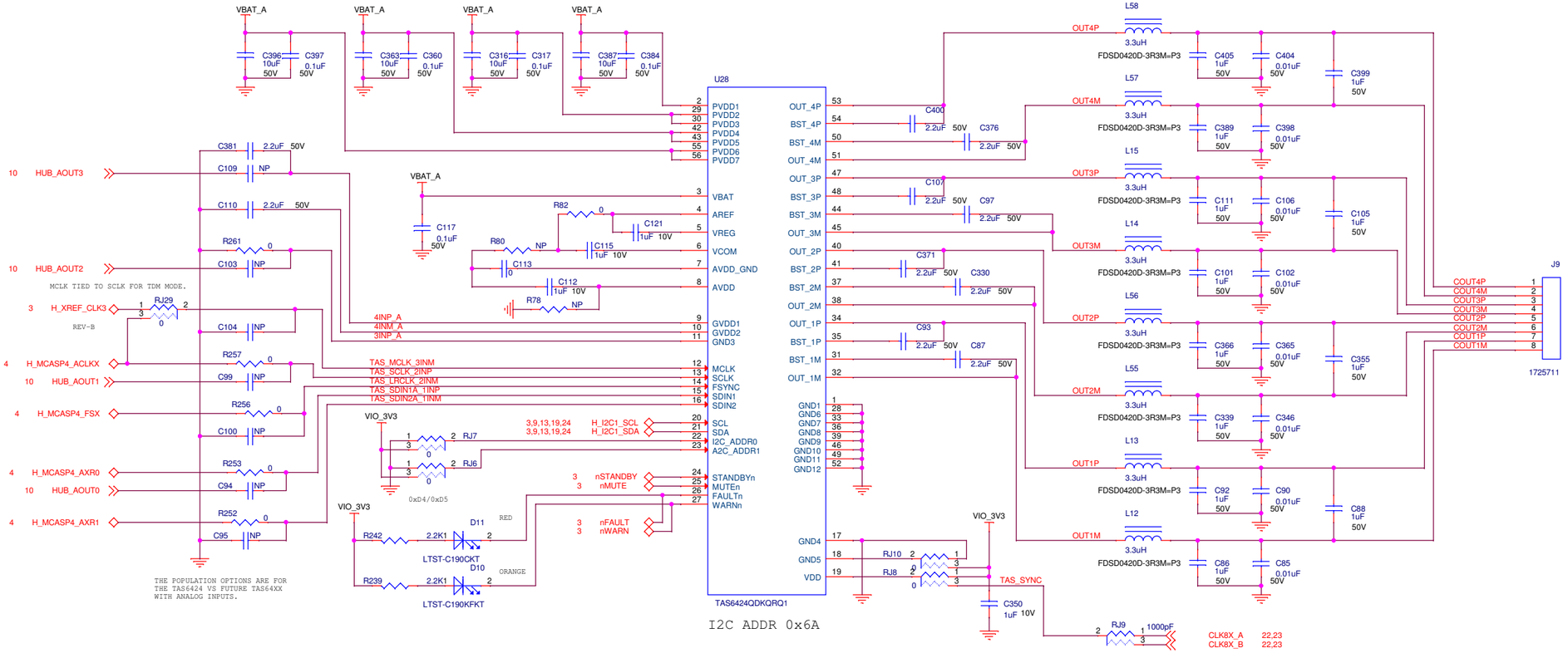
SIL_INTB_CHIP1 SIL_RSTB_CHIP1

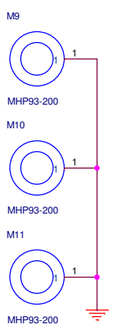
ICLINK_01_0 ICLINK_01_1 ICLINK_01_2 ICLINK_01_3

ZIFCLKOUT1 ZIFFSOUT1

HUB0_AIN2_P HUB0_AIN2_N HUB0_AIN3_P HUB0_AIN3_N HUB0_AIN4_P HUB0_AIN4_N HUB0_AIN5_P HUB0_AIN5_N HUB0_AIN6_P HUB0_AIN6_N

TEXAS INSTRUMENTS INCORPORATED	
Title:	DRA71x LCARD CPU Board
Page Contents:	TUNER 1 SI47912/902
Size: C	DOC NO: 518392 REV: B
Date: Thursday, November 09, 2017	Sheet 10 of 26

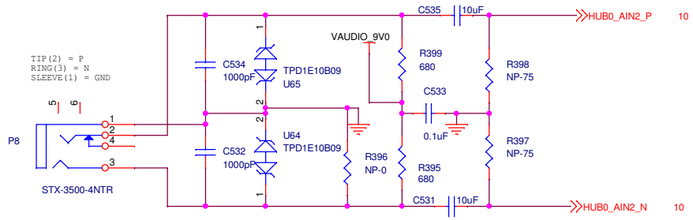


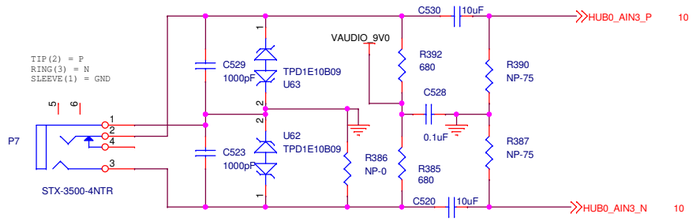


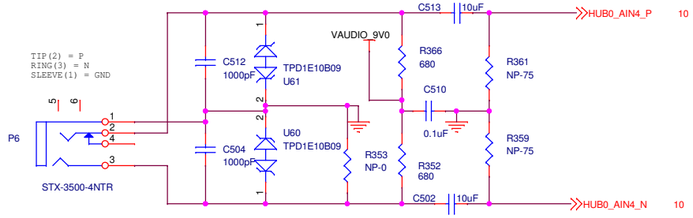
REF	PIN NUM	TAS6424 PIN	TAS6424 POP	TPA6404 PIN	TPA6404 POP
R82	4	AREF	0-OHM	AVSS	NP
C121	5	VREG	1uF	AVDD	1uF
R80			NP		0-OHM
C115	6	VCOM	1uF	GVDD_34	2.2uF
C113	7		0-OHM	GVDD_12	2.2uF
C112	8	AVDD	1uf	GND	0-OHM
R78			NP		0-OHM
RJ10	18	GND5	P1-2 0-OHM	DVDD	P2-3 0-OHM
RJ11	19	VD	P1-2 0-OHM	SYNC	P2-3 0-OHM
C381	9	GVDD1	2.2uF	IN_4P	NP
C109			NP		1uF
C110	10	GVDD2	2.2uF	IN_4M	1uF
R261	11	GND3	0-OHM	IN_3P	NP
C103			NP		1uF
RJ29	12	MCLK	0-OHM	IN_3M	NP
C104			NP		1uF
R257	13	SCLK	0-OHM	IN_2P	NP
C99			NP		1uF
R256	14	FSYNC	0-OHM	IN_2M	NP
C100			NP		1uF
R253	15	SDIN1	0-OHM	IN_1P	NP
C94			NP		1uF
R252	16	SDIN2	0-OHM	IN_1M	NP
C95			NP		1uF

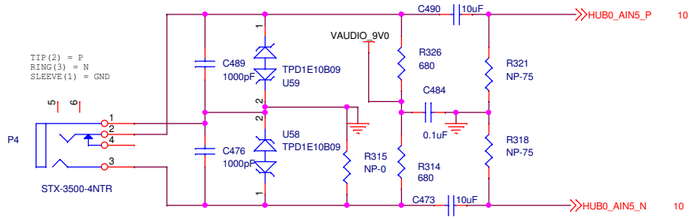
TEXAS INSTRUMENTS INCORPORATED

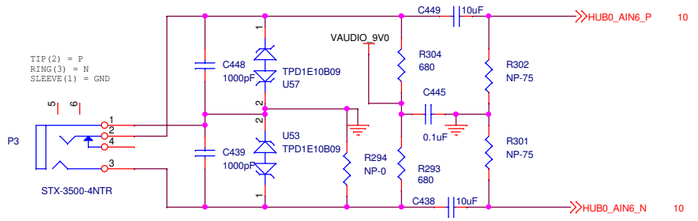
Title: DRA71x LCARD CPU Board		
Page Contents: CLASS D AMPLIFIER		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 11 of 26	



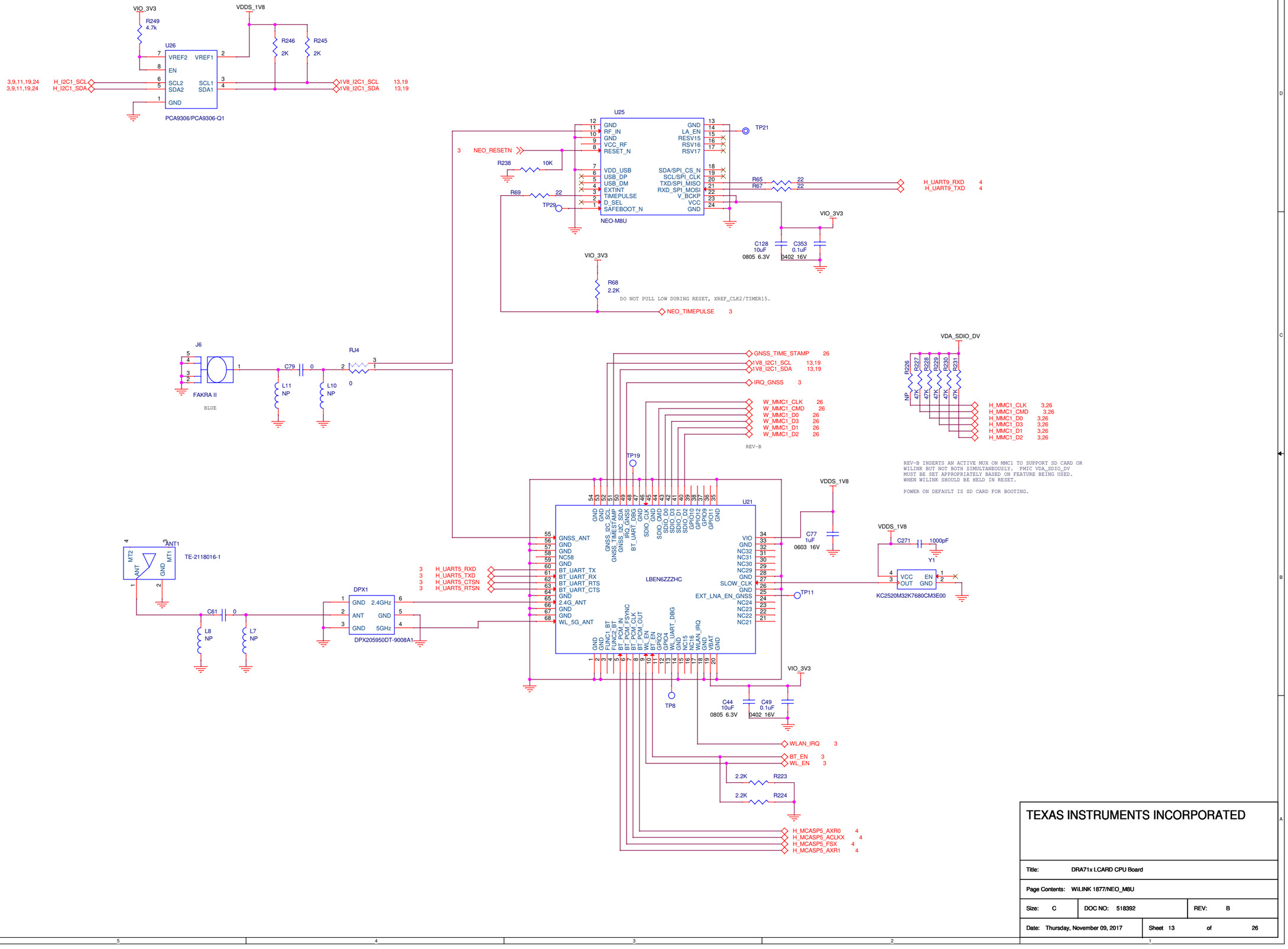






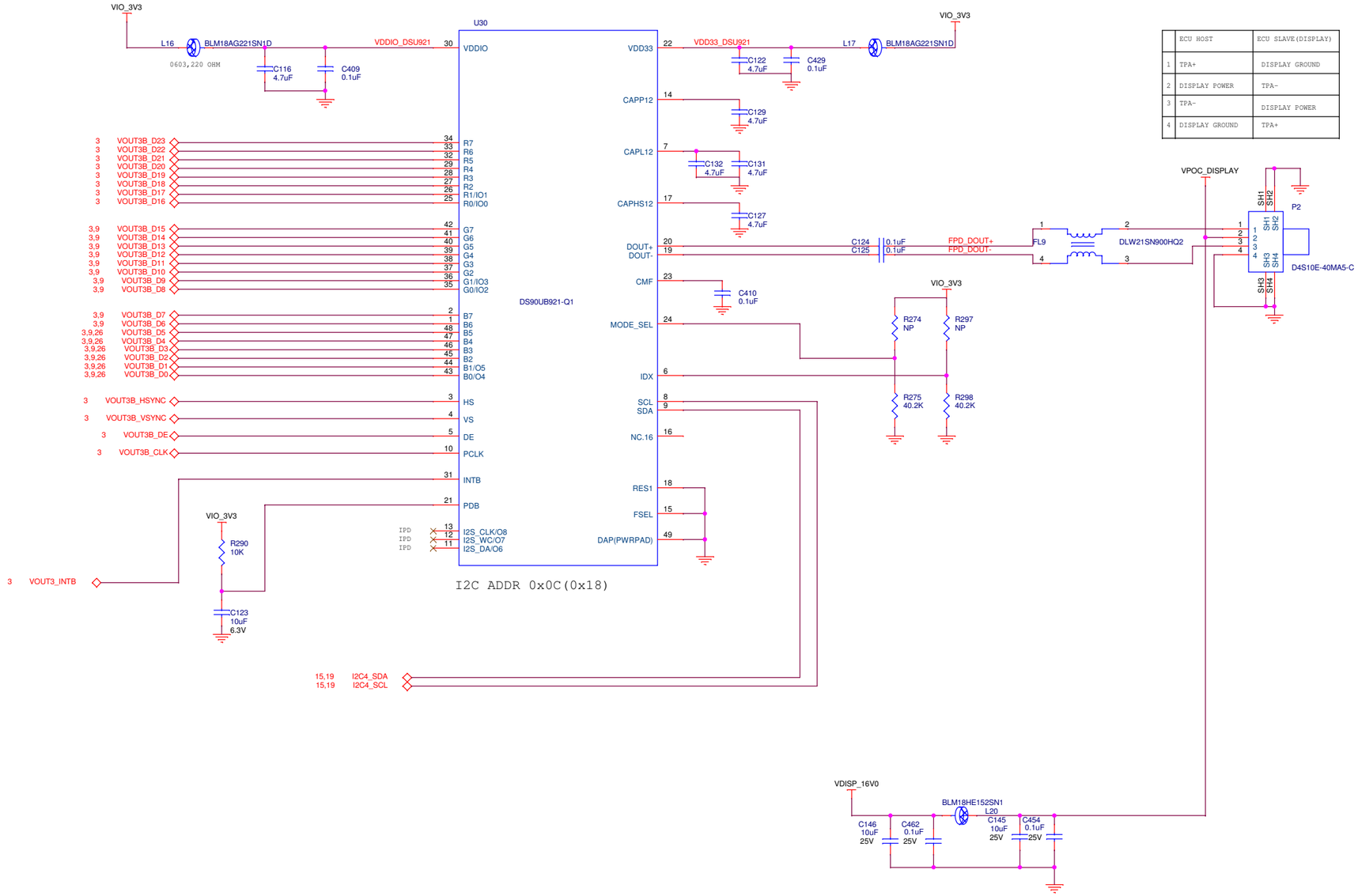


TEXAS INSTRUMENTS INCORPORATED			
Title: DRA71x LCARD CPU Board			
Page Contents: AUDIO INPUTS			
Size: C	DOC NO: 518392		REV: A
Date: Thursday, November 09, 2017	Sheet 12 of 26		



TEXAS INSTRUMENTS INCORPORATED

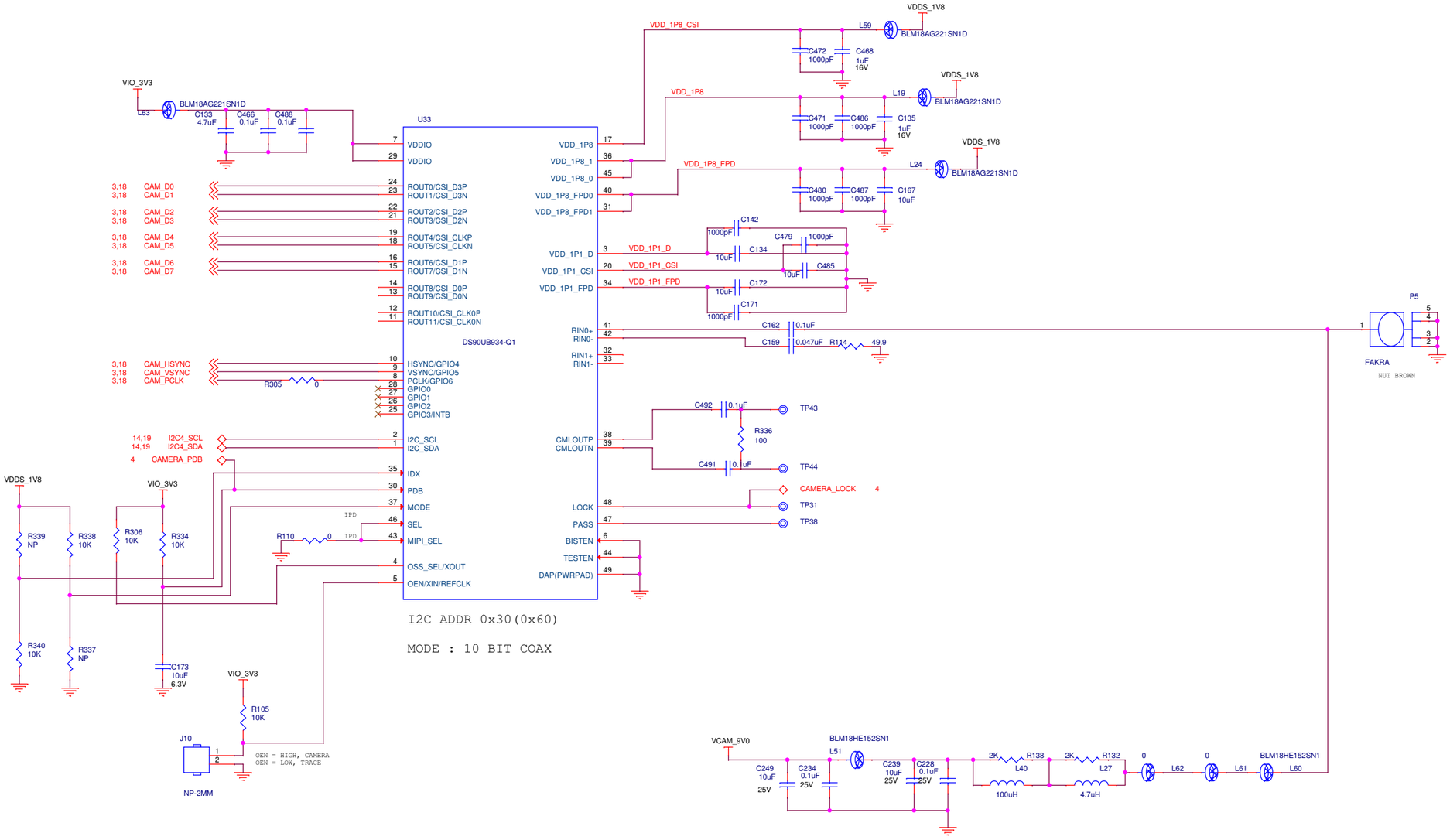
Title: DRA71x LCARD CPU Board		
Page Contents: WiLINK 1877/NEO_M8U		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 13 of 26	



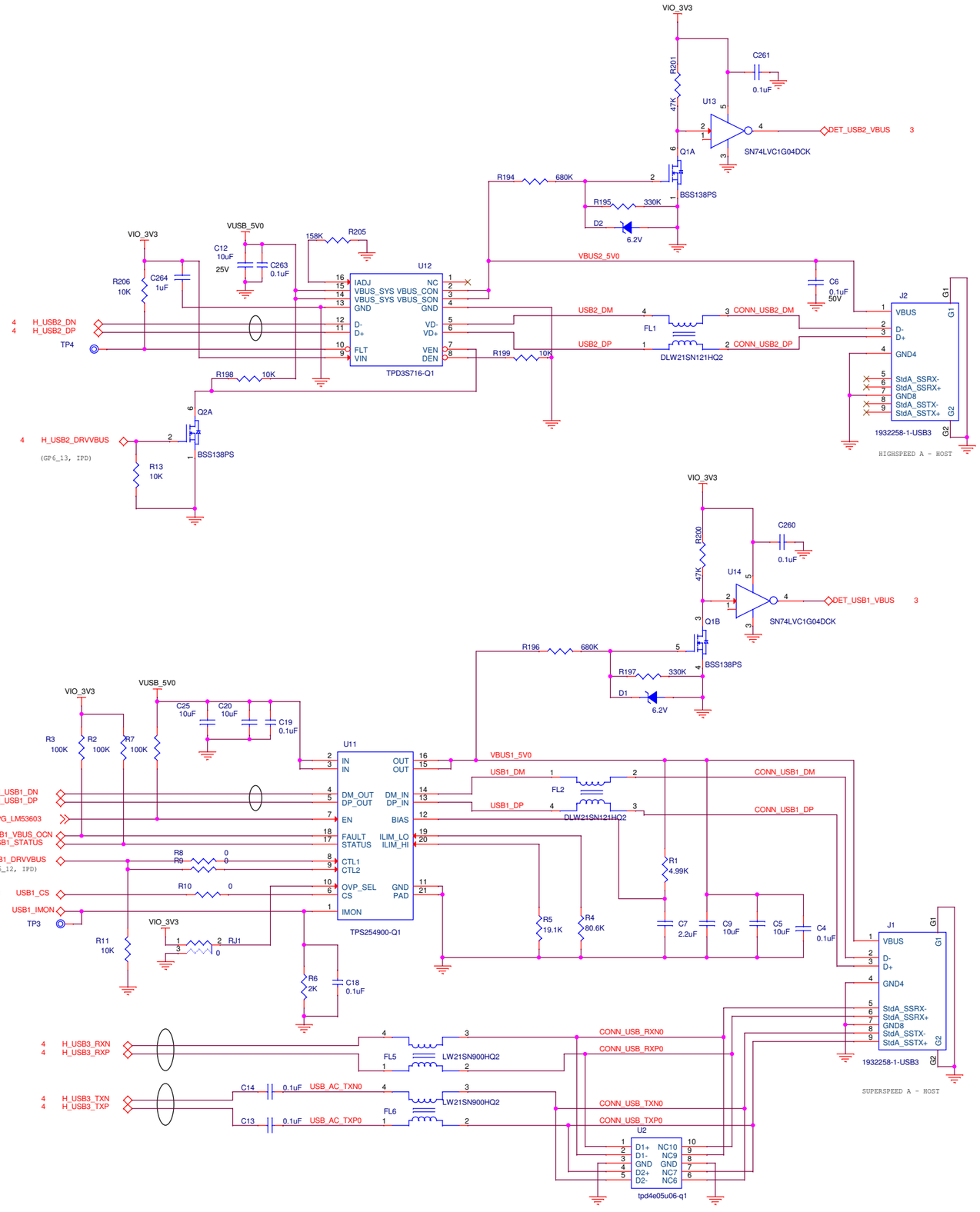
	ECU HOST	ECU SLAVE(DISPLAY)
1	TPA+	DISPLAY GROUND
2	DISPLAY POWER	TPA-
3	TPA-	DISPLAY POWER
4	DISPLAY GROUND	TPA+

TEXAS INSTRUMENTS INCORPORATED

Title: DRA71x LCARD CPU Board		
Page Contents: FPD LINK DISPLAY		
Size: C	DOC NO: 518392	REV: A
Date: Thursday, November 09, 2017	Sheet 14 of 26	



TEXAS INSTRUMENTS INCORPORATED		
Title: DRA71x LCARD CPU Board		
Page Contents: FPD LINK CAMERA		
Size: C	DOC NO: 518392	REV: A
Date: Thursday, November 09, 2017	Sheet 15 of 26	



SuperSpeed standard A plug pinout

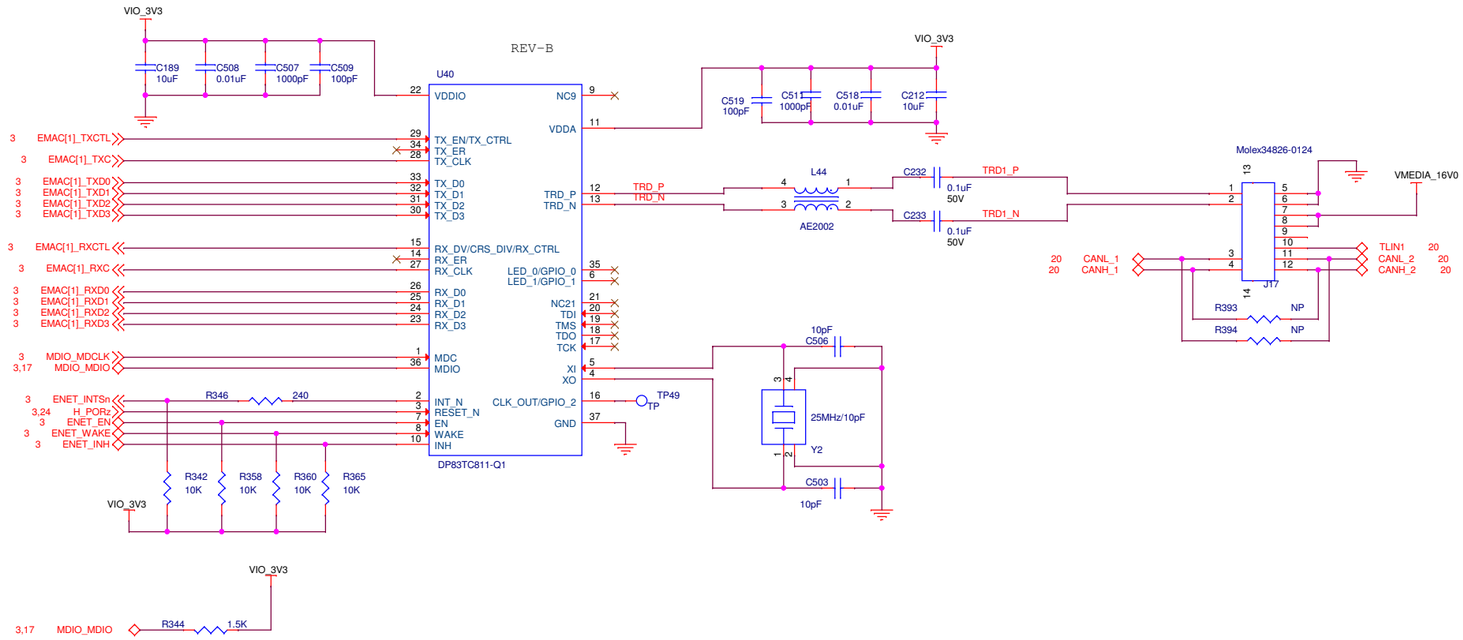
SuperSpeed standard B plug pinout

1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSRX-	Blue
6	StdA_SSRX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSTX-	Purple
9	StdA_SSTX+	Orange
Shell	Shield	Connector Shell

1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSTX-	Blue
6	StdA_SSTX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSRX-	Purple
9	StdA_SSRX+	Orange
Shell	Shield	Connector Shell

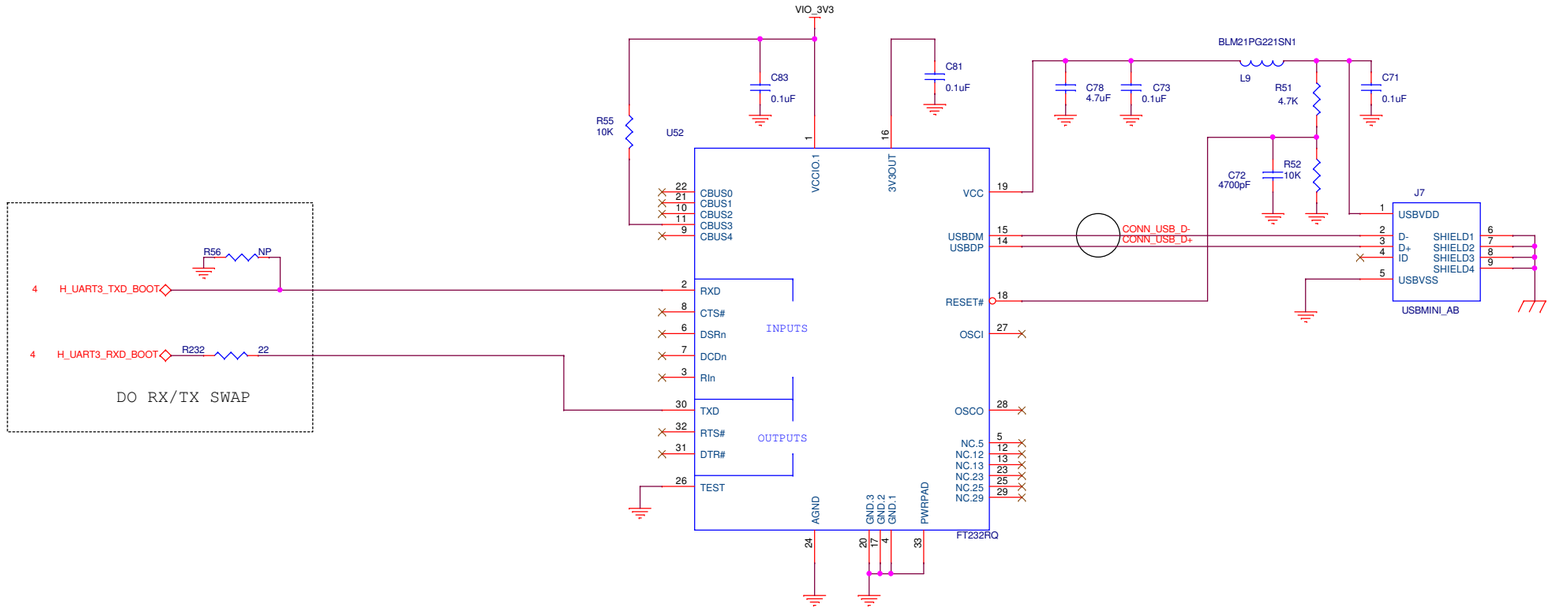
TEXAS INSTRUMENTS INCORPORATED

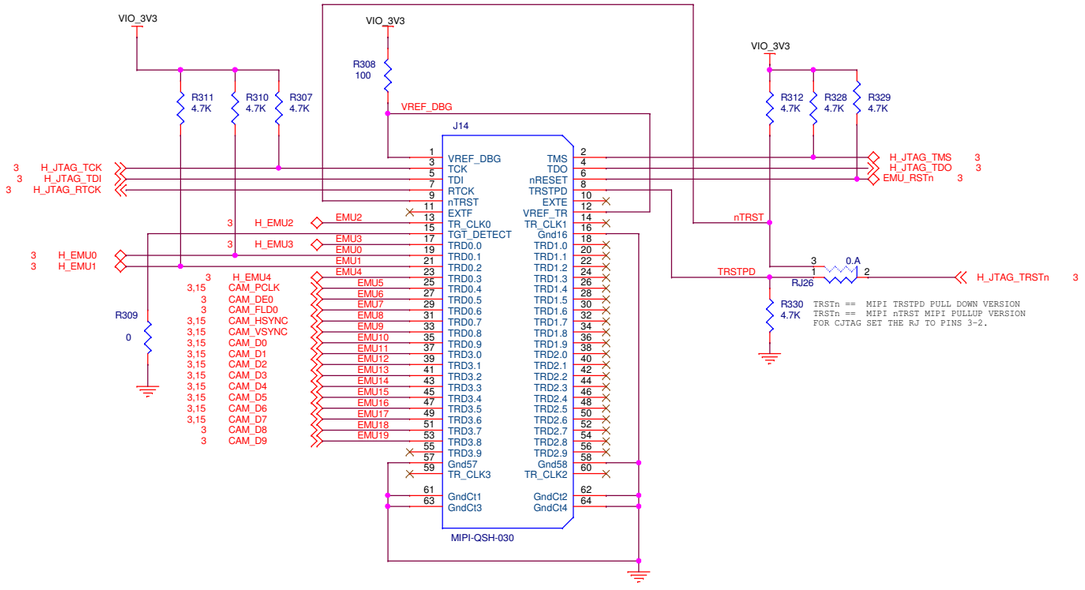
Title:	DRA71x LCARD CPU Board		
Page Contents:	USB MEDIA		
Size: C	DOC NO: 518392		REV: B
Date: Thursday, November 09, 2017	Sheet 16	of	26



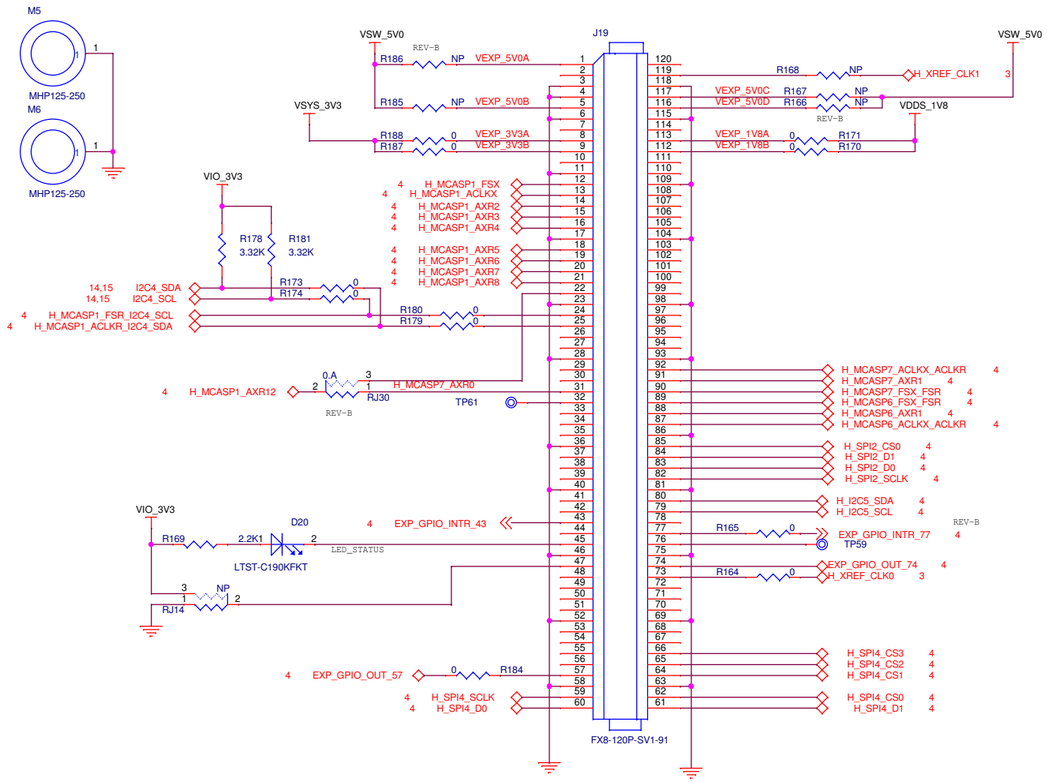
TEXAS INSTRUMENTS INCORPORATED		
Title: DRA71x LCARD CPU Board		
Page Contents: ENET DP83TC811		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 17 of 26	

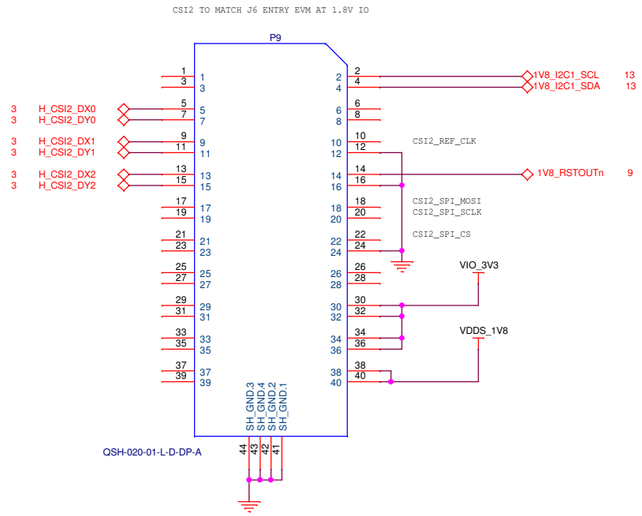
Terminal/UART-BOOT Connector

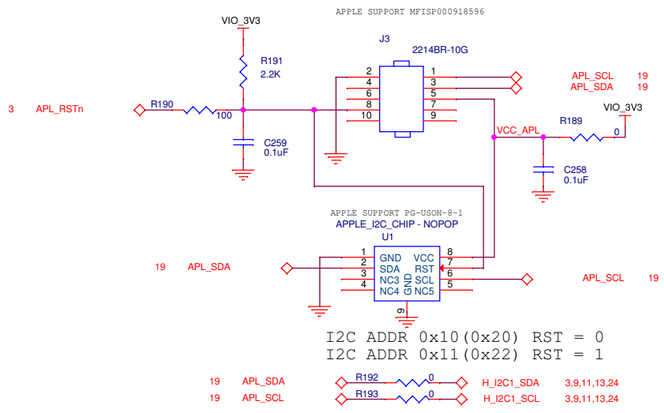




TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA71x LCARD CPU Board		
Page Contents:	USB-UART/JTAG		
Size: C	DOC NO: 518392		REV: A
Date: Thursday, November 09, 2017		Sheet 18 of	26

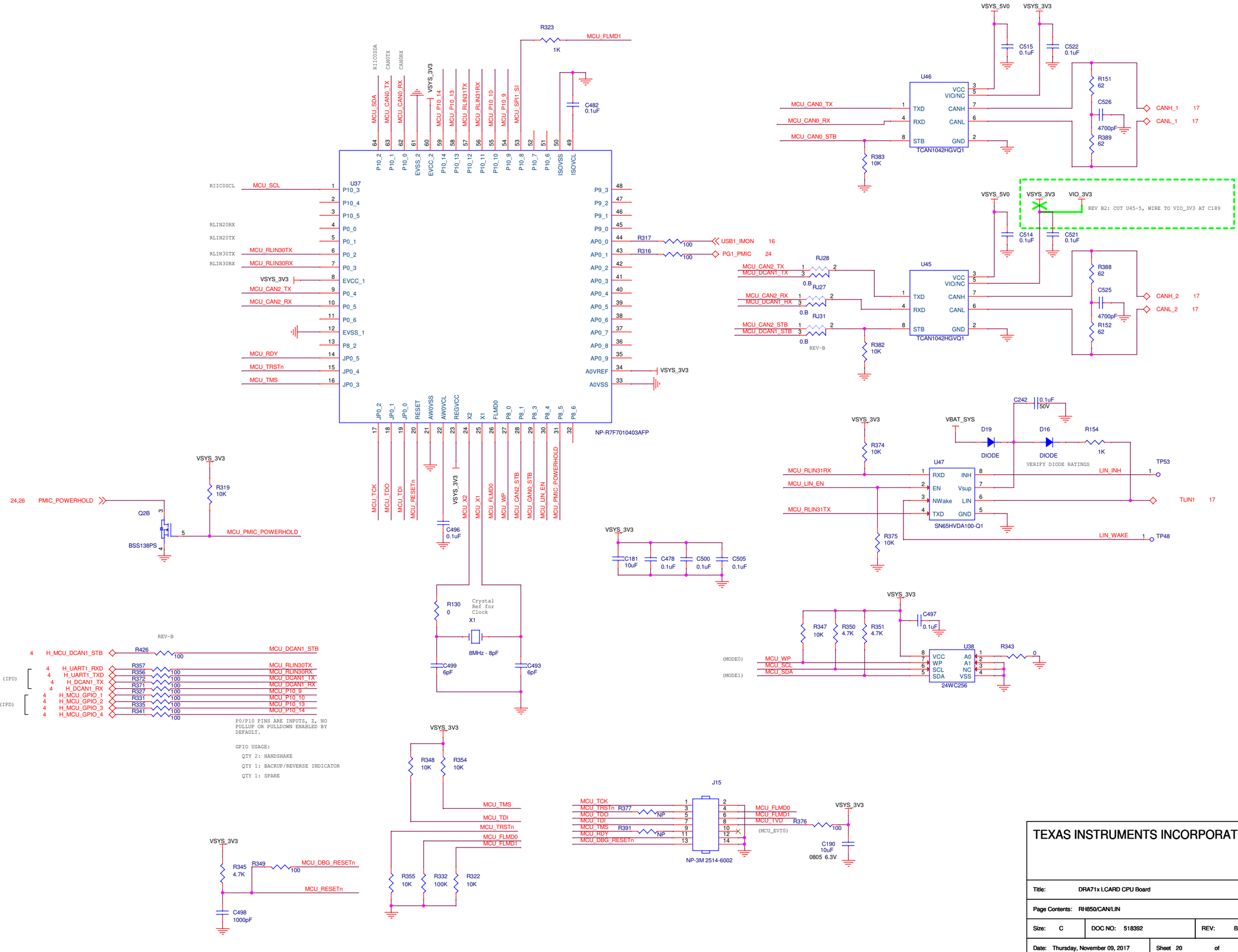




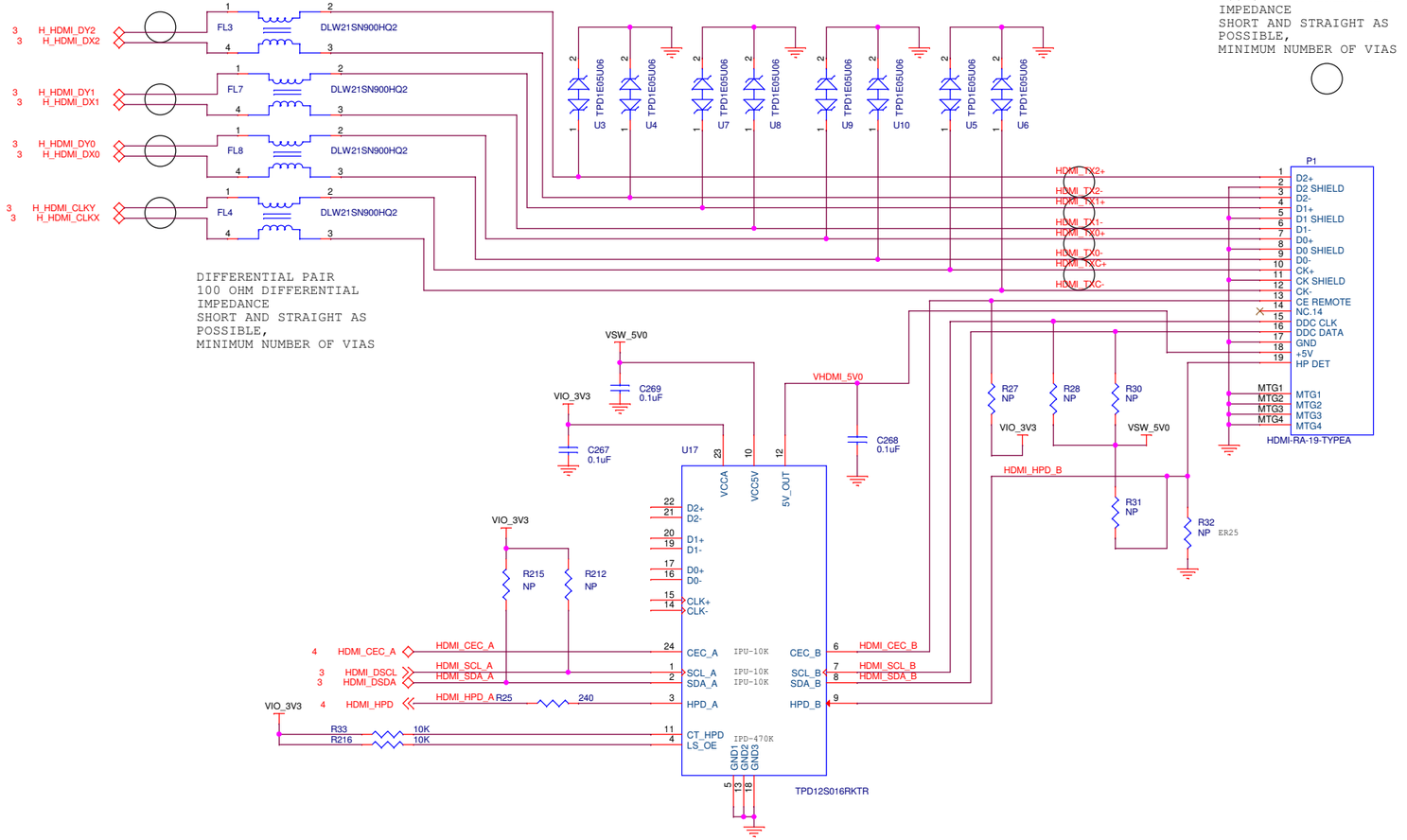


TEXAS INSTRUMENTS INCORPORATED

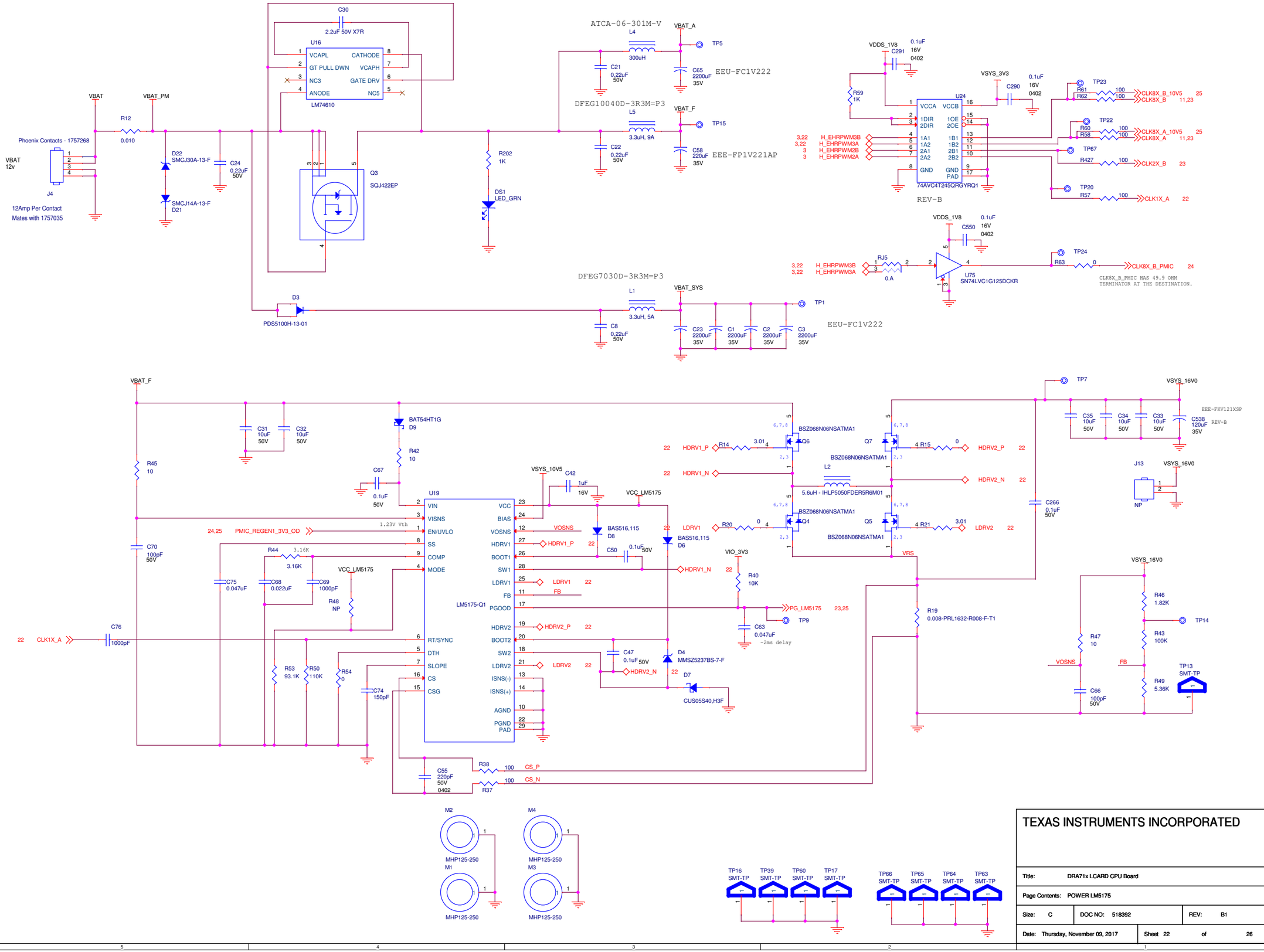
Title: DRA71x LCARD CPU Board		
Page Contents: EXPANSION		
Size: C	DOC NO: 518392	REV: B
Date: Thursday, November 09, 2017	Sheet 19 of 26	



TEXAS INSTRUMENTS INCORPORATED			
Title:	DRA71x LCARD CPU Board		
Page Contents:	RH850/CAN/LIN		
Size: C	**DOC NO:** 518392		**REV:** B2
Date: Thursday, November 09, 2017	**Sheet** 20	**of**	26



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA71x LCARD CPU Board			
Page Contents: HDMI			
Size: C	DOC NO: 518392		REV: A
Date: Thursday, November 09, 2017		Sheet 21 of 26	



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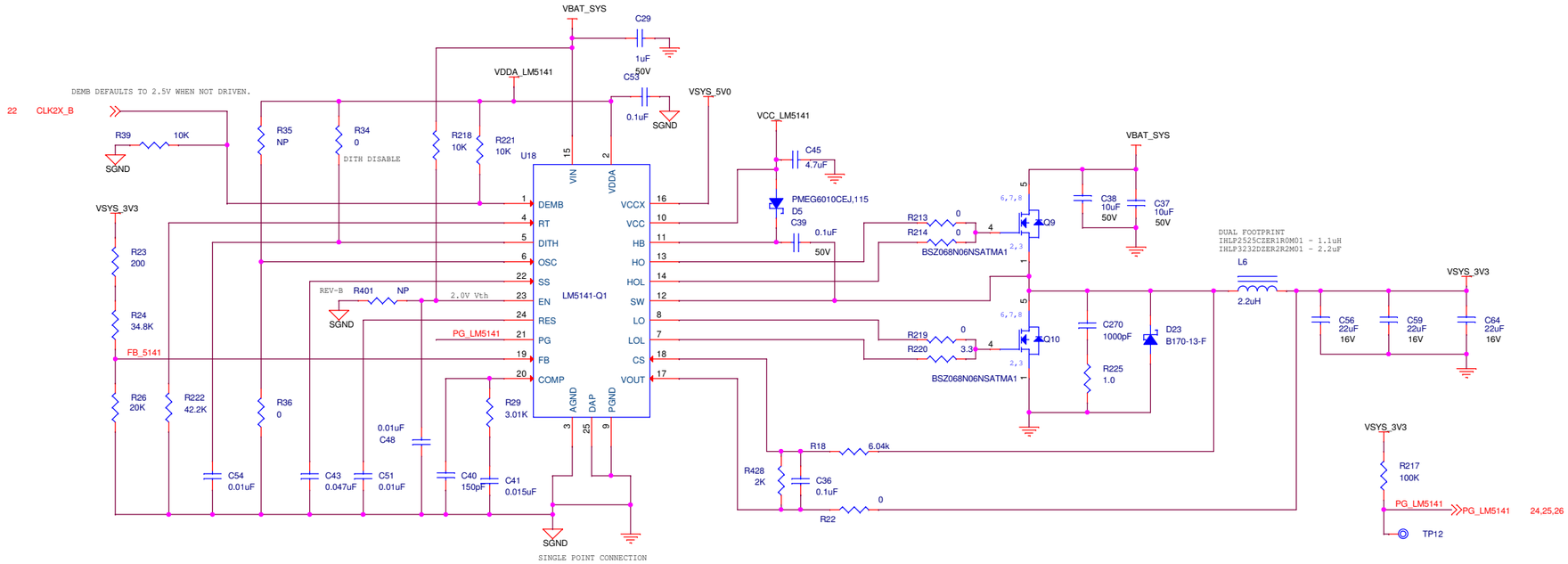
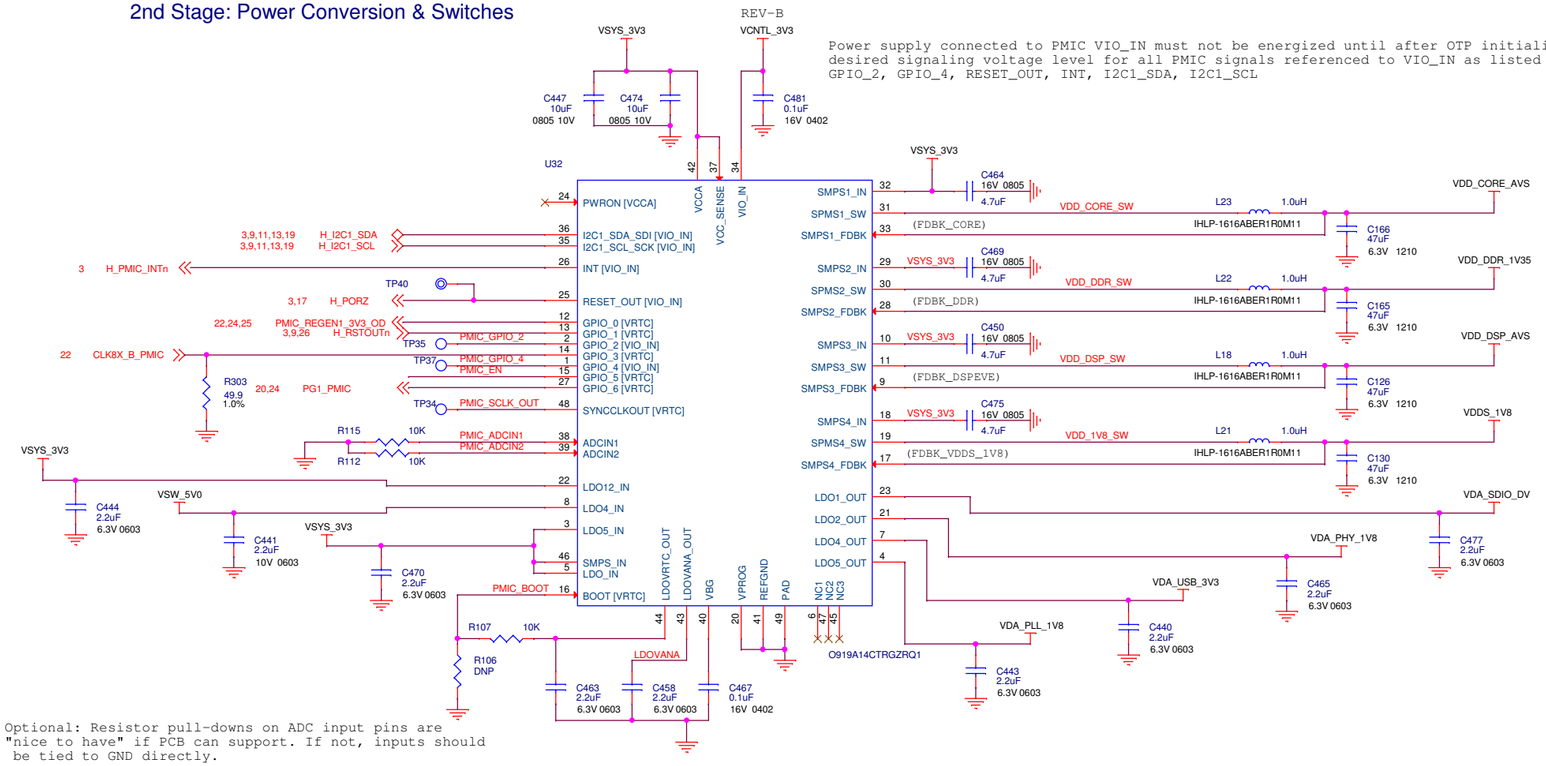
Title:	DRA71x LCARD CPU Board		
Page Contents:	POWER LM5175		
Size: C	DOC NO: 518392	REV: B1	
Date: Thursday, November 09, 2017	Sheet 22 of 26		



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA71x LCARD CPU Board			
Page Contents: POWER LM5141			
Size: C	DOC NO: 518392		REV: B1
Date: Thursday, November 09, 2017	Sheet 23 of 26		

Power - 2nd Stage Resources

2nd Stage: Power Conversion & Switches



Power supply connected to PMIC VIO_IN must not be energized until after OTP initialization and be aligned with desired signaling voltage level for all PMIC signals referenced to VIO_IN as listed below:
GPIO_2, GPIO_4, RESET_OUT, INT, I2C1_SDA, I2C1_SCL

Route the voltage nets with "(FDBK_xxxx)" labels as traces using 4-8mil trace widths for remote sensing voltages only (not current carrying) and connected as close as possible to SoC power balls or Dcaps located very close to power ball (point of load).

=> VDDS_1V8
=> VDDS_DDR_1V8
=> VDDS_PoP_1V8
=> VDD_SHV_1V8
=> VPRH_1V8

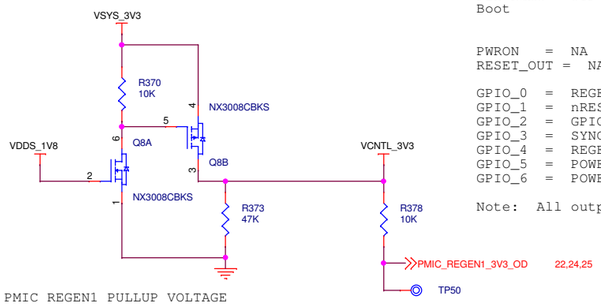
VDDS_1V8 AND VIO_1V8 TIED TOGETHER PER SYSTEM POWER V.04.

Optional: Resistor pull-downs on ADC input pins are "nice to have" if PCB can support. If not, inputs should be tied to GND directly.

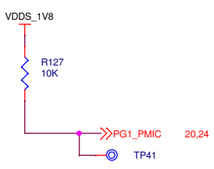
REV-B Orderable P/N: O919A14CTRGZRQ1 (Automotive)
Orderable P/N: TPS659163RGZR (Catalog)
OTP ID = 0x4C for DRA71x/AM570x Reference Board optimized systems using DDR3/3L memory and following PMIC functions mapped to GPIO_x assignments per OTP:

Pin Name	OTP Defined Function	System Feature/Operation
Boot		Dedicated input pin, BOOT=0 - LDO1=1V8 BOOT=1 - LDO1=BYPASS (assumes 3.3v LDO12_IN)
PWRON	= NA	Dedicated input pin, no connect pin since Power ON & OFF to be controlled by logic signal input to POWERHOLD function
RESET_OUT	= NA	Dedicated output pin, system power on reset (PORz) generated by OTP timing, asserted Low during entire power up seq, sets High at end of power up seq
GPIO_0	= REGEN1, OD (5.25Vmax)	Output signal for controlling external power resource, Open-Drain type with 5.25V max reference.
GPIO_1	= nRESWARM	Input control, a low sets PMIC into warm reset state, rising edge re-intializing SoC voltage domains
GPIO_2	= GPIO, PU En [VIO_IN ref]	Unassigned, available as SW controlled GPIO, referenced to VIO_IN supply
GPIO_3	= SYNCDCDC	Input signal for synchronization of SMPS switching
GPIO_4	= REGEN2 [VIO_IN ref]	Output signal for controlling external power resource, Push-Pull type referenced to VIO_IN supply.
GPIO_5	= POWERHOLD	Input control, High = PMIC holds active power state; Low = PMIC begins power down seq before entering OFF state
GPIO_6	= POWERGOOD, OD (1.8V max)	Output status signal, Open-Drain type with 1.8V max reference, High = valid output voltages; Low = an invalid output voltage

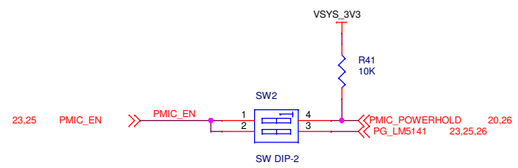
Note: All outputs are push-pull by default unless specified otherwise.



DELAY PMIC REGEN1 PULLUP VOLTAGE UNTIL AFTER PMIC 1V8 IS STABLE. THIS PREVENTS ANY DOWN STREAM REGULATORS/SWITCHES FROM TURNING ON MOMENTARILY WHILE PMIC BOOTS.

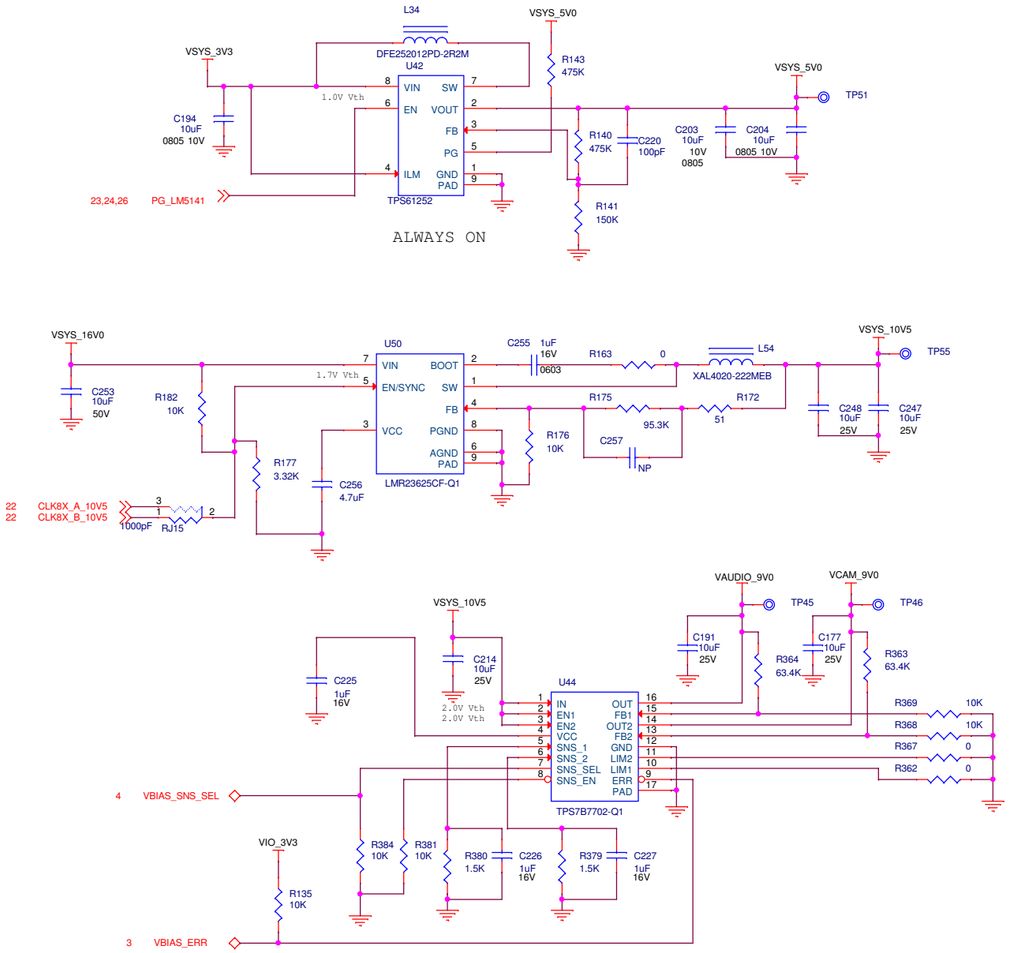


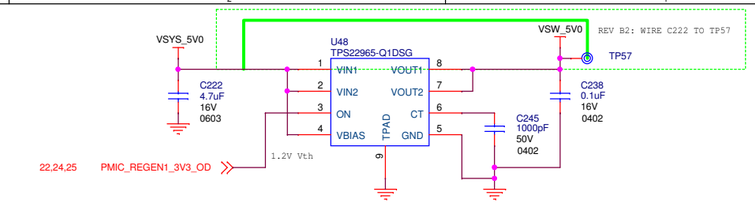
uCNTLR STATUS (NOT FOR REG ENABLES)

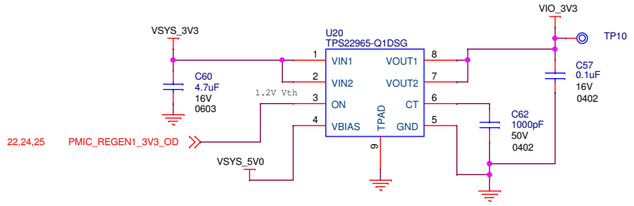


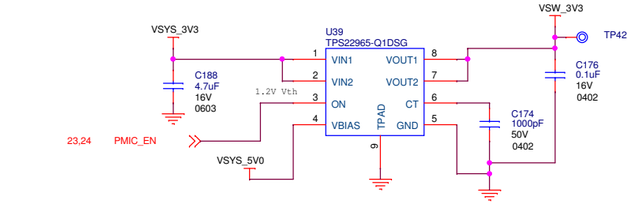
TEXAS INSTRUMENTS INCORPORATED

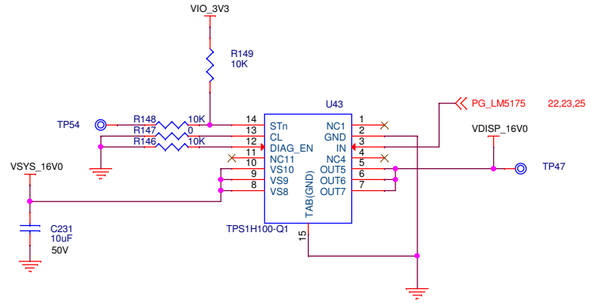
Title: DRA71x LCARD CPU Board		
Page Contents: PMIC		
Size: C	DOC NO: 518392	REV: B1
Date: Thursday, November 09, 2017	Sheet 24 of 26	

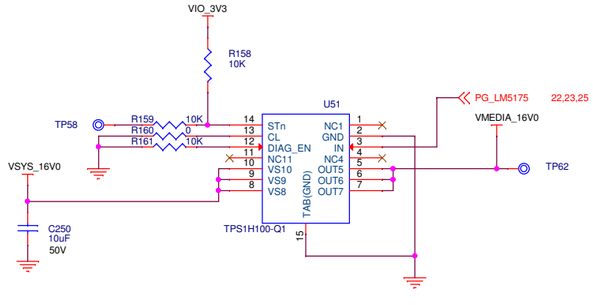


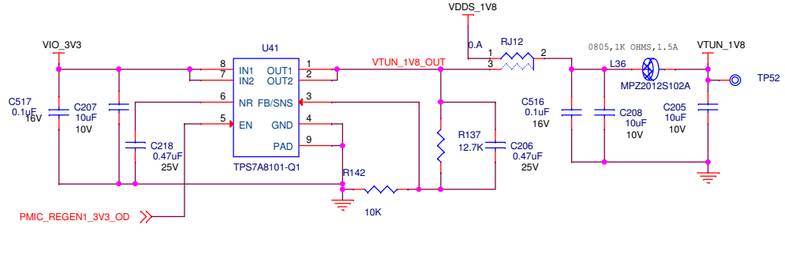


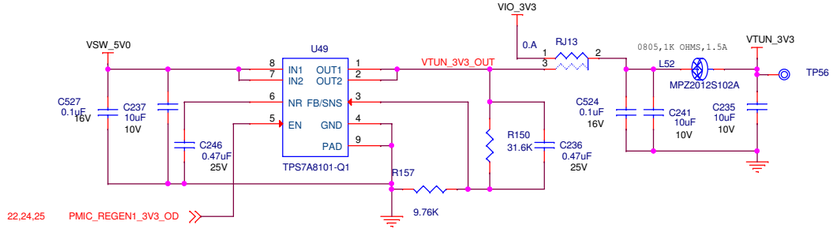








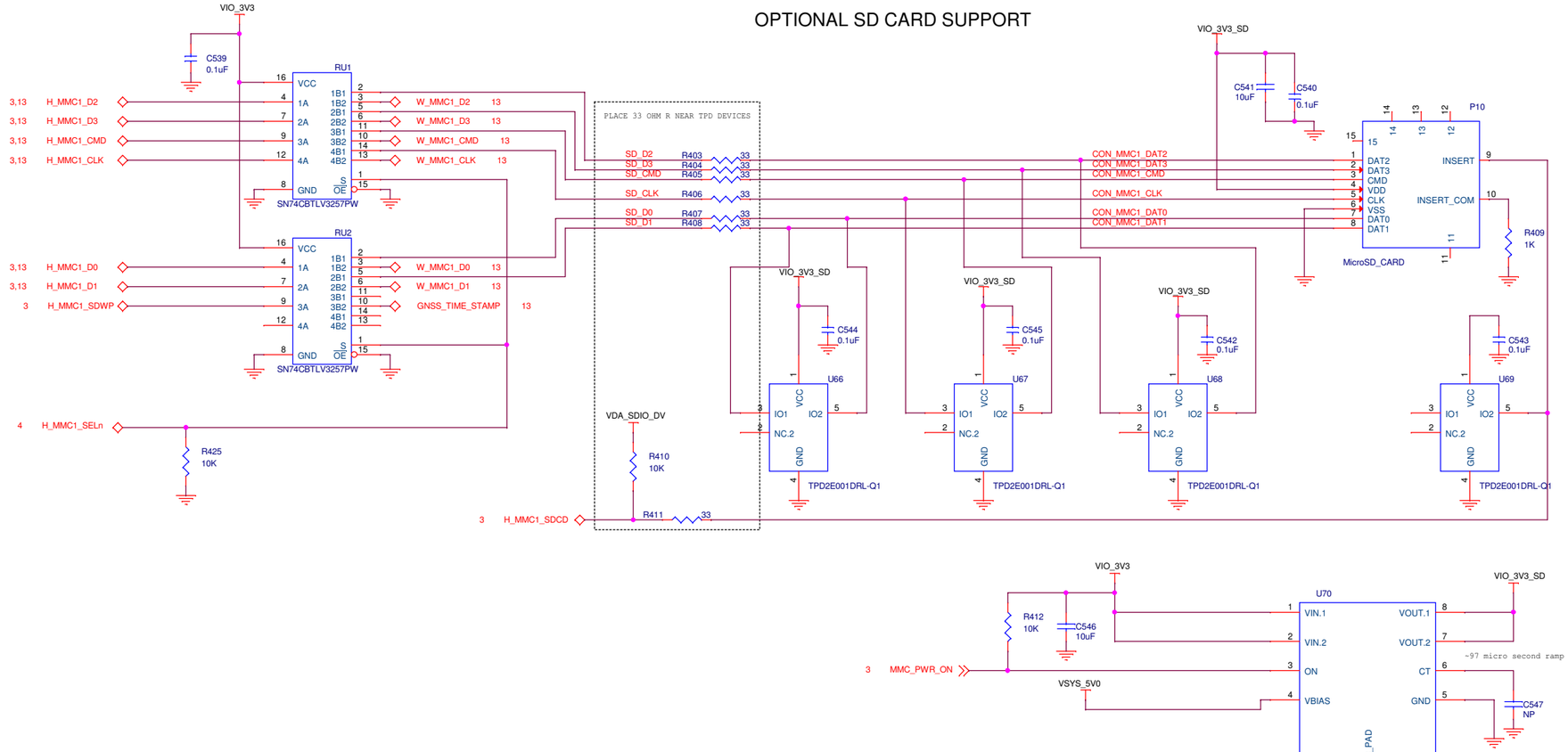




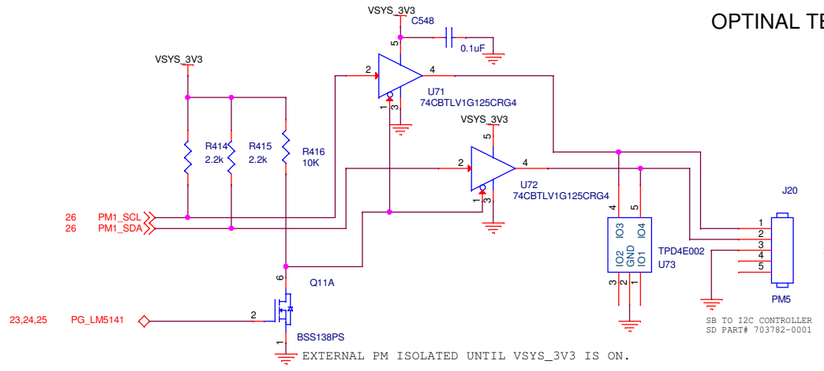
TEXAS INSTRUMENTS INCORPORATED

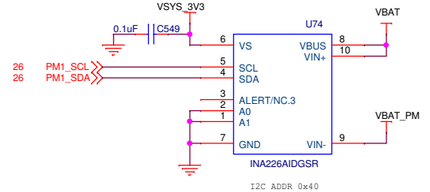
Title: DRA71x LCARD CPU Board		
Page Contents: SECONDARY LDO'S/SWITCHES		
Size: C	DOC NO: 518392	REV: B2
Date: Thursday, November 09, 2017	Sheet 25 of 26	

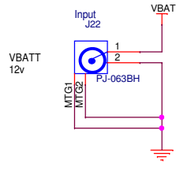
OPTIONAL SD CARD SUPPORT



OPTINAL TEST AUTOMATION SUPPORT



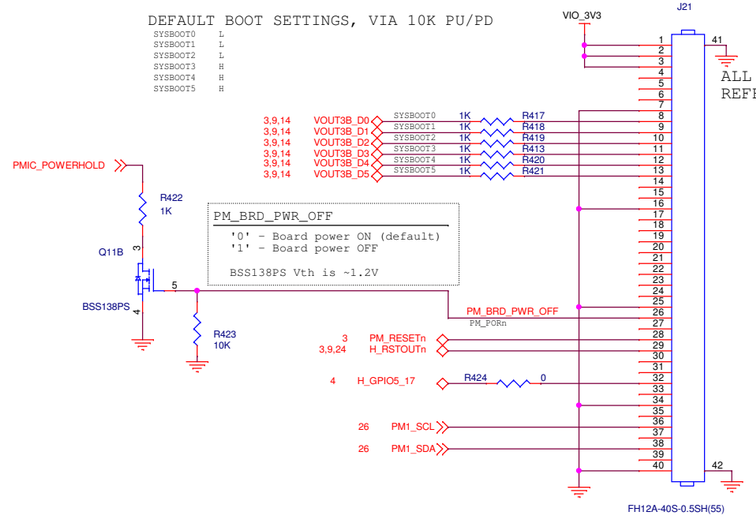




BOOT SWITCHES SHOULD BE SET TO OFF, Cable : Parlex-050R40-76B, .5mm 3"
AUTOMATION WILL OVERRIDE THE DEFAULTS.

DEFAULT BOOT SETTINGS, VIA 10K PU/PD

SYSBOOT0	L
SYSBOOT1	L
SYSBOOT2	L
SYSBOOT3	H
SYSBOOT4	H
SYSBOOT5	H



ALL SIGNALS SHOULD BE
REFERENCED TO VIO_3V3

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA71x LCARD CPU Board		
Page Contents:	LDCP SUPPORT		
Size: C	DOC NO: 518392		REV: B1
Date: Thursday, November 09, 2017	Sheet 26	of	26

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