NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P2V" represents connection to the +1.2V power plane.
2. The netname "P1P9V" represents connection to the +1.9V power plane.
3. The netname "P3P3V" represents connection to the +3.3V power plane.
4. The netname "P2P5V" represents connection to the +2.5V power plane.
5. The netname "P5V" represents connection to the +5.0V power plane.
6. The netname "P12V" represents connection to the +12.0V power plane.
7. The netname "GND" represents connection to the ground plane.
8. A "Z" suffix on a signal name indicates an active low signal.
9. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.
10. All components with designators above 500 are mounted solder side of the board.
11. All resistor values are in ohms.
12. All capacitor values in microfarads unless otherwise specified.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

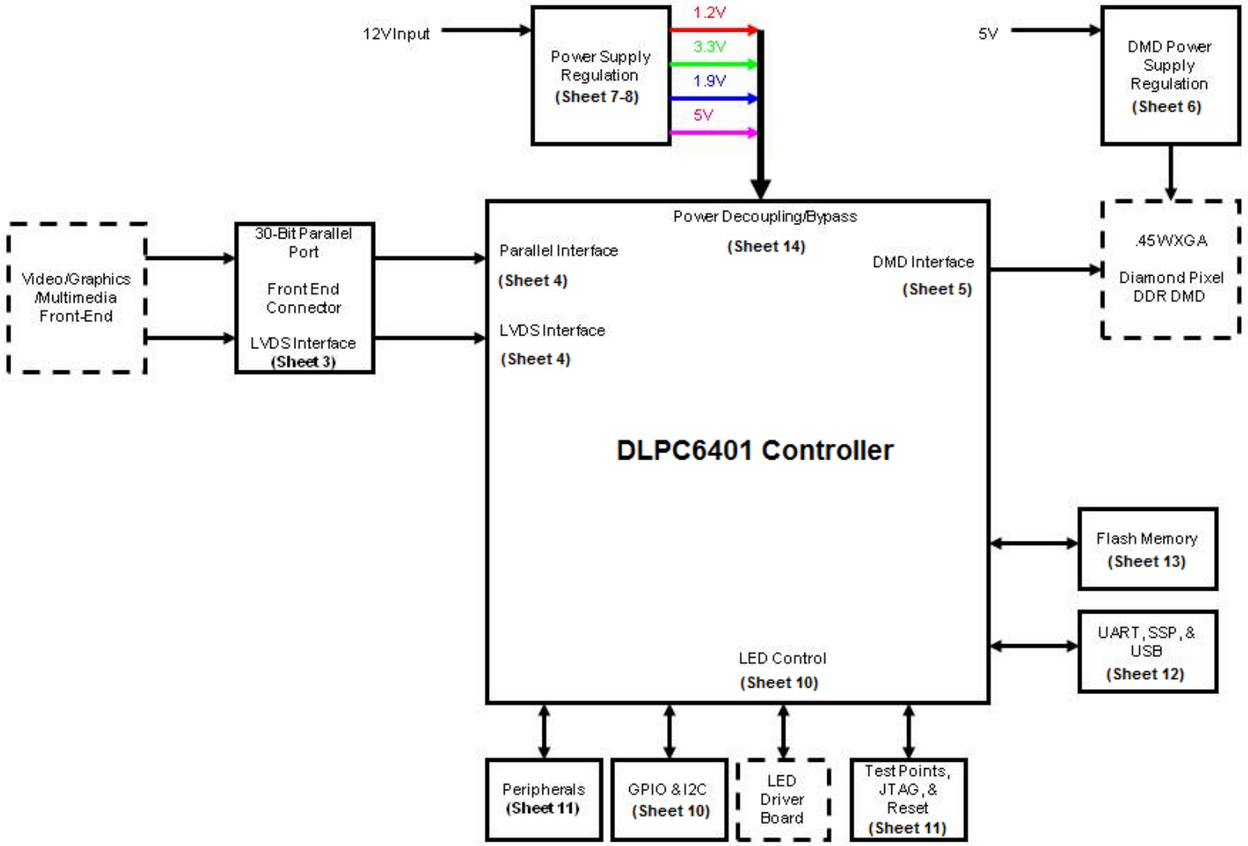
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO TIDA-00782 DLPC6401 Reference Design	10/13/2011	

REFERENCE DESIGN

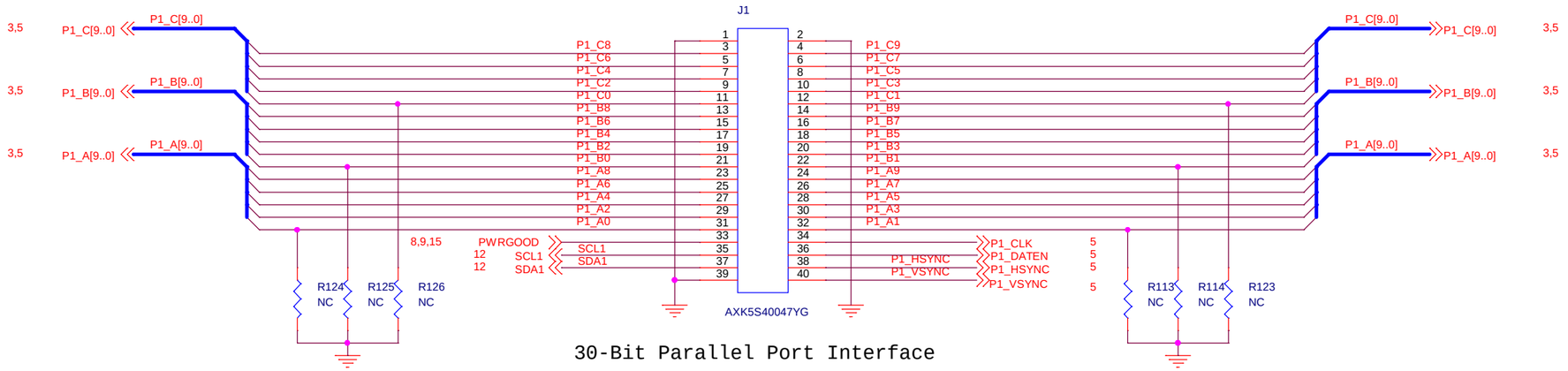
DWN Roger Perry	DATE 10/13/2011	**TEXAS INSTRUMENTS - DLP® Products**	
ENGR Roger Perry	10/13/2011		
SYS		TITLE TIDA-00782 DLPC6401 Reference Design	
APVD		DRAWING NO	REV A
QA		11 x 17 Orcad Capture 16.6	SHEET 1 of 16

BLOCK DIAGRAM

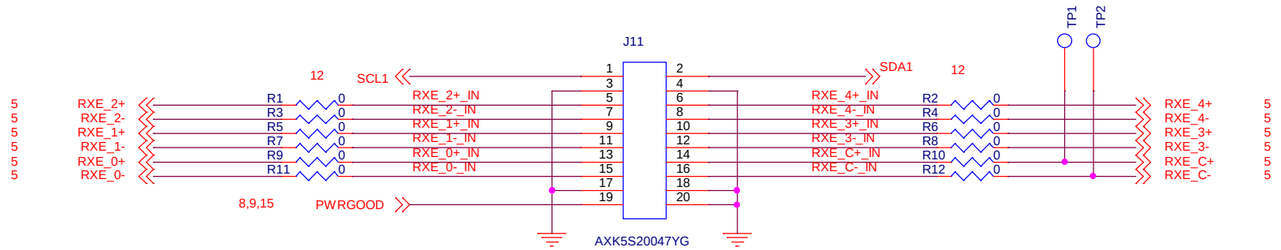


INDEX

TEXAS INSTRUMENTS	DWN	DATE		DRAWING NO	REV
	Perry Roger	10/13/2011			A
	ISSUE DATE				
	08/31/2015		SIZE A3	SHEET 2 OF 16	

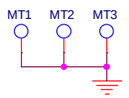


30-Bit Parallel Port Interface



LVDS Front End Interface

CCA MOUNTING HOLES



Front End Interface Connector

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 3 OF 16

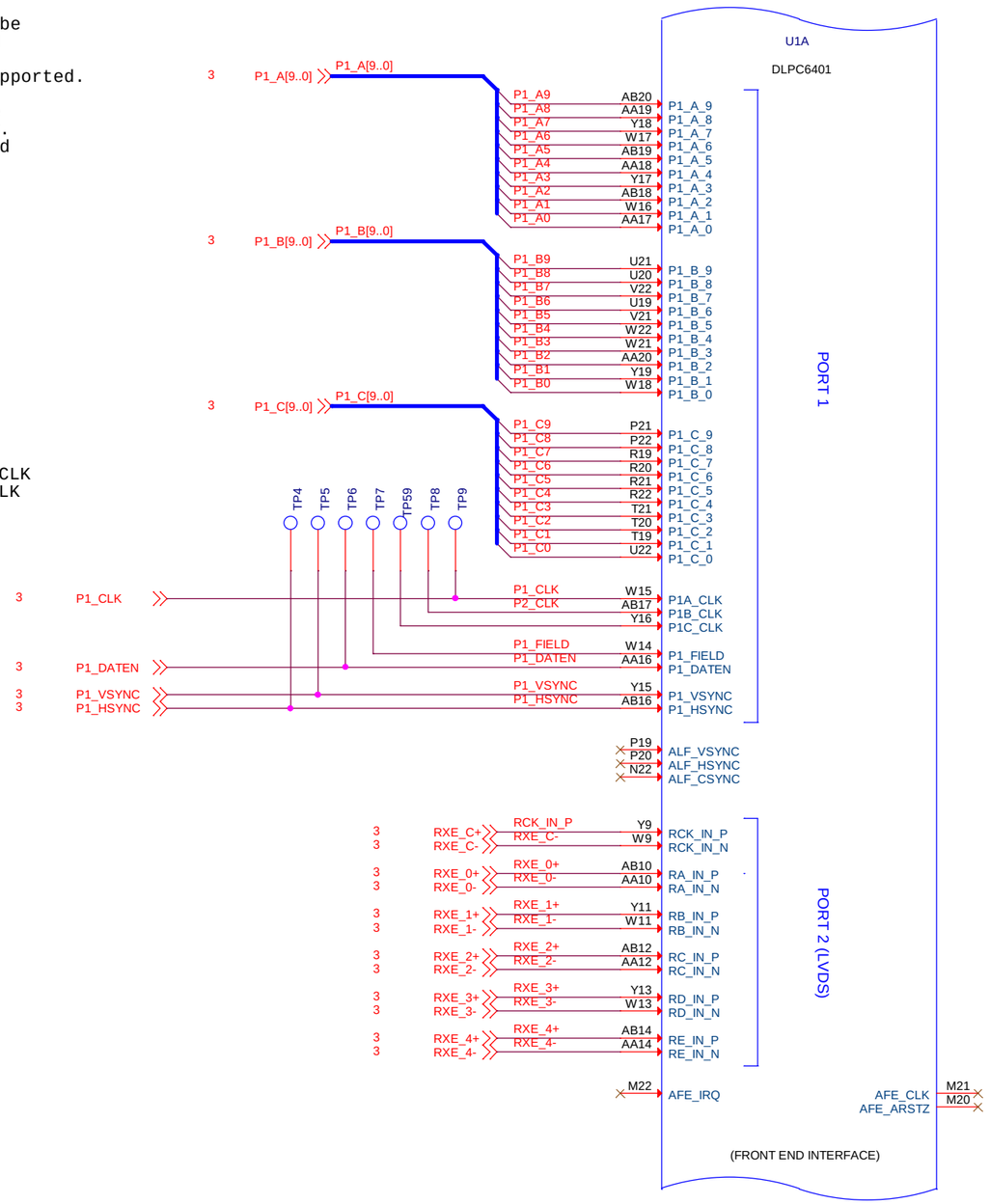
NOTE:

The input data channels can be configured to optimize board layout for each port.
Bitwise reordering is not supported.

For example, Y data could be connected to Port A, B, or C.
Port configuration is handled in the API Software.

NOTE:
If only one input clock is used, then P1A_CLK should be connected, and P1B_CLK and P1C_CLK should not be connected.

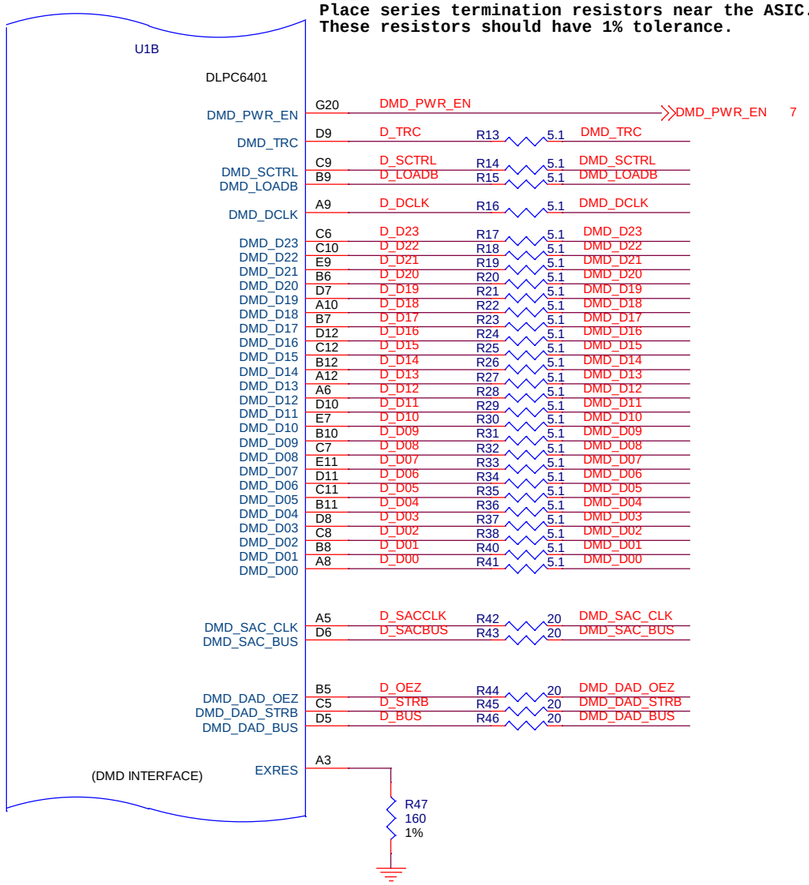
Front End Clocks	
P1A_CLK	P1_CLK
P1B_CLK	P2_CLK
P1C_CLK	P3_CLK
RCK_IN_P	LVDS+ CLK
RCK_IN_N	LVDS- CLK

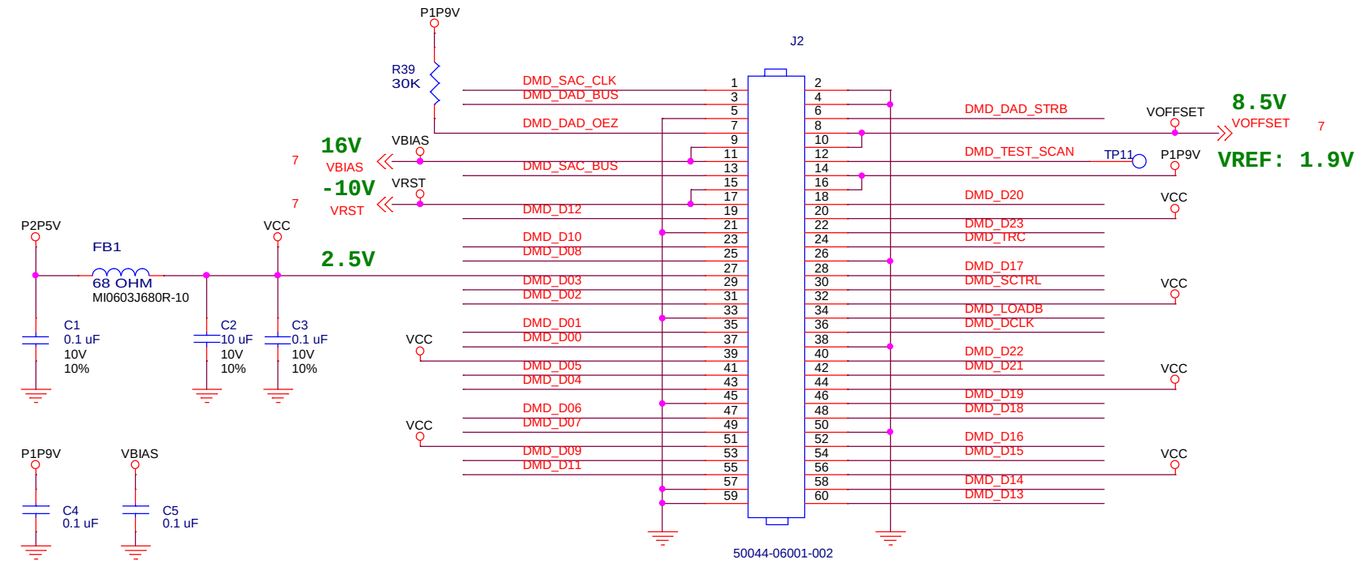


DPP6401 Front End Interface

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 4 OF 16

NOTE:
Place series termination resistors near the ASIC.
These resistors should have 1% tolerance.





DMD BOARD CONNECTOR

DMD Connector Interface

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 5 OF 16

Do Not Install Resistor
if DMD is mounted

P5V
R48
NC

P5V
C9
10UF
25V,10%

L1
22 uH

C8
1 uF

DRV_D

8.5V

U2

4 Vin
23 ENR
24 EN
22 COMP
17 C1-
16 C1+
15 C2-/MODE
14 C2+
7 PGND
8 PGND
11 GND
19 GND

5 SW0
6 SW1
9 SUP OUT1
1 FB1
18 DRV
21 FB2
13 OUT3
12 FB3
10 PG
20 REF
2 FB4
3 BASE

TPS65145

6,7 DMD_PWR_EN
R49
10K

DMD_PWR_EN

C13
1000PF
R51 15K

C14 0.1 uF 50V

C17 0.1 uF 50V

DMD_PWR_EN_INV

D1
STPS0540Z

Q18
DMP2160UW

C10
6.2 PF

R50
360K

R52
56.0K

C12
22UF
16V,20%

C11
0.1 uF

TP12
VOFFSET

VOFFSET 6,7

C15
1 uF

DN1
BAT54SW

C16
1 uF

BAT54SW
DN2

DRV_D

C18
1 uF

TP13
VRST

-10V

VRST 6,7

C19
10UF
25V,10%

C20
0.1 uF
50V, 20%
0.1 OHM

DMD_PG

TP15

R53
75K

R54
620K

C23
0.22 uF

TP14
VBIAS

16.0V

VBIAS 6,7

R55
680K

R56
56.0K

C25
10UF
25V,10%

C26
0.1 uF
50V, 20%
0.1 OHM

P5V
R142
2.2K

DMD_PWR_EN_INV

DMD_PWR_EN

Q17
FDV303N

P5V
C27
1 uF

Q1
BCP68

FB9
68 OHM
MI0603J680R-10

C28
4.7 uF
6.3V
10%

P3P3V
C81
100 uF
16V
10%

TPS 2.5V GENERATION

P3P3V

U3
1 IN
3 EN
4 NR
5 OUT
2 GND
TPS73025

P2P5V

C21
0.1 uF
10V
10%

C24
0.1 uF
10V
10%

C22
2.2 uF
10V

POWER DOWN CIRCUITRY

6,7 VOFFSET

P5V
R58
10K
R59
12
R63
3.3K
Q3
2N2907A
Q6
2N2222A
R65
6,7 DMD_PWR_EN
Q9
2N2222A
10K
D2
MAZ80330HL

6,7 DMD_PWR_EN
R57
10K
Q2
2N2907A
R62
3.3K
Q4
2N2222A
Q7
2N2222A
R66
33K
R67
12
6,7 VRST

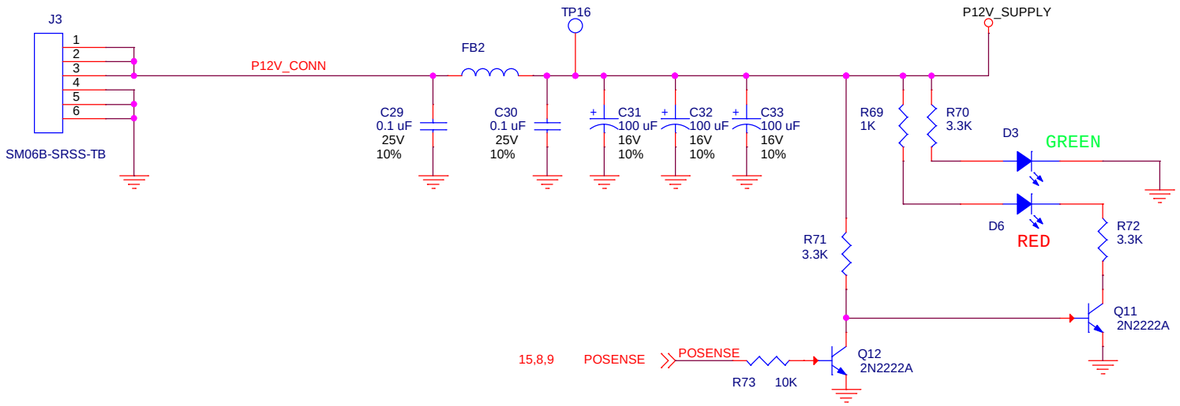
6,7 VBIAS

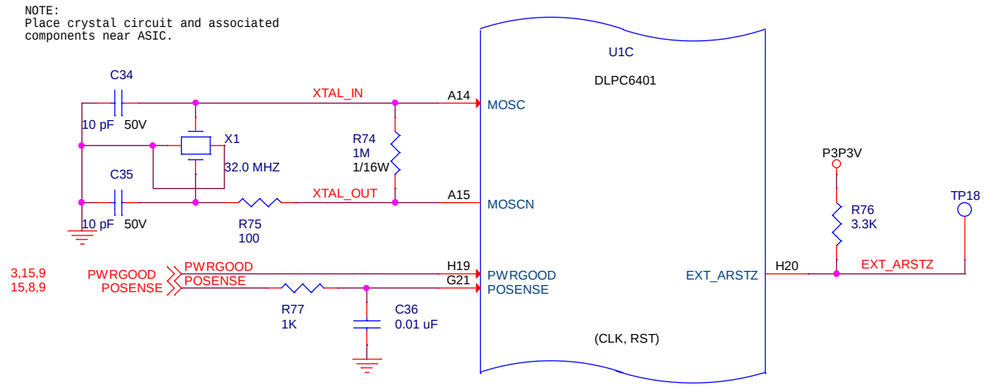
P5V
R60
10K
R61
12
R64
2.2K
Q5
2N2907A
Q8
2N2222A
R68
6,7 DMD_PWR_EN
Q10
2N2222A
10K

DMD Power Supplies

TEXAS INSTRUMENTS

DWN	DATE		DRAWING NO	REV
Roger Perry	10/13/2011			A
ISSUE DATE 08/31/2015		SIZE A3	SHEET 6 OF 16	





Input Power and Oscillator Input

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015	SIZE A3	SHEET 7 OF 16	

NOTE:
Place capacitors near IC device.

P12V_SUPPLY

U4

C38 10 uF 25V
C39 10 uF 25V
C40 10 uF 25V
C37 10 uF 25V

32 VIN_32
33 VIN_33
34 VIN_34
13 VIN1

C43 4.7 nF — 11 EN1
C44 4.7 nF — 9 SS1
R79 100K — 10 RLIM1

NOTE:
4.7nF capacitor on EN1 pin causes about 8ms of delay.

BUCK 1

LX1_14 14
LX1_15 15
BST1 12
FB1 7
COMP1 8

L2 4.7 uH SRR1005-4R7M
C41 47 nF 16V 10%
R81 20K — C46 4.7 nF
C48 100 pF

R78 40.2K 1%
C42 22 uF 16V 10%
R82 80.6K 1%
P1P2V

NOTE:
Use 40.2K and 32.4K values for 1.8V operation.
Use 40.2K and 29.4K values for 1.9V operation.

P12V_SUPPLY

C49 10 uF 25V

18 VIN2

C53 10 nF — 20 EN2
C54 4.7 nF — 22 SS2
R85 150K — 21 RLIM2

NOTE:
10nF capacitor on EN2 pin causes about 16ms of delay.

BUCK 2

LX2_16 16
LX2_17 17
BST2 19
FB2 24
COMP2 23

L3 4.7 uH SRR1005-4R7M
C52 47 nF 16V 10%
R86 20K — C55 4.7 nF
C56 100 pF

R84 40.2K 1%
C50 22 uF 16V 10%
R87 29.4K 1%
P1P9V

P12V_SUPPLY

C59 10 uF 25V

38 VIN3

C61 10 nF — 40 EN3
C63 4.7 nF — 2 SS3
R90 150K — 1 RLIM3

NOTE:
10nF capacitor on EN3 pin causes about 16ms of delay.

BUCK 3

LX3_36 36
LX3_37 37
BST3 39
FB3 4
COMP3 3

L4 4.7 uH SRR1005-4R7M
C60 47 nF 16V 10%
R91 20K — C64 4.7 nF
C65 100 pF

R89 40.2K 1%
C62 22 uF 16V 10%
R92 7.68K 1%
P5V

TPS65251

5 SYNC
R93 383K — 6 ROSC
25 LOW_P

26 GND_26
31 GND_31
35 GND_35
30 AGND

P3P3V
R94 10K
27 PGOOD — PGOOD_TPS — PGOOD_TPS 9
28 V7V
29 V3V

C67 3.3 uF 16V
C68 10 uF 25V 20%

P2P5V

U5

C45 0.1 uF 10V 10%

4 IN — PG 1 — PG_P1P8V_LDO
3 NC
2 GND — OUT 5 — P1P8V_LDO

TPS79718

P3P3V
R80 10K
C47 2.2 uF 10V

P12V_SUPPLY

U6

C51 0.1 uF 25V 10%

8 VCC — RESET 5 — PG_P12V_TDS
7 SENSE
2 RESIN — RESET 6

R83 10K
R88 10K

3 CT — REF 1
GND 4

C57 47 nF 16V 10%
C58 0.1 uF 25V 10%

TL7712A

NOTE:
47nF Ct capacitance provides >600us of time delay on RESET output.

IMPORTANT NOTE:
The PCB should be designed such that the specifications are not exceeded when the DDP6401 is operated under the maximum current conditions specified in the DDP6401 datasheet.

P3P3V

U8

C69 0.1 uF 25V 10%

9 PGOOD_TPS — PGOOD_TPS — P3P3V
5 VCC
1 A — Y 4 — POSENSE — POSENSE 15,8
2 B
GND 3

SN74AHC1G08

P3P3V

U7

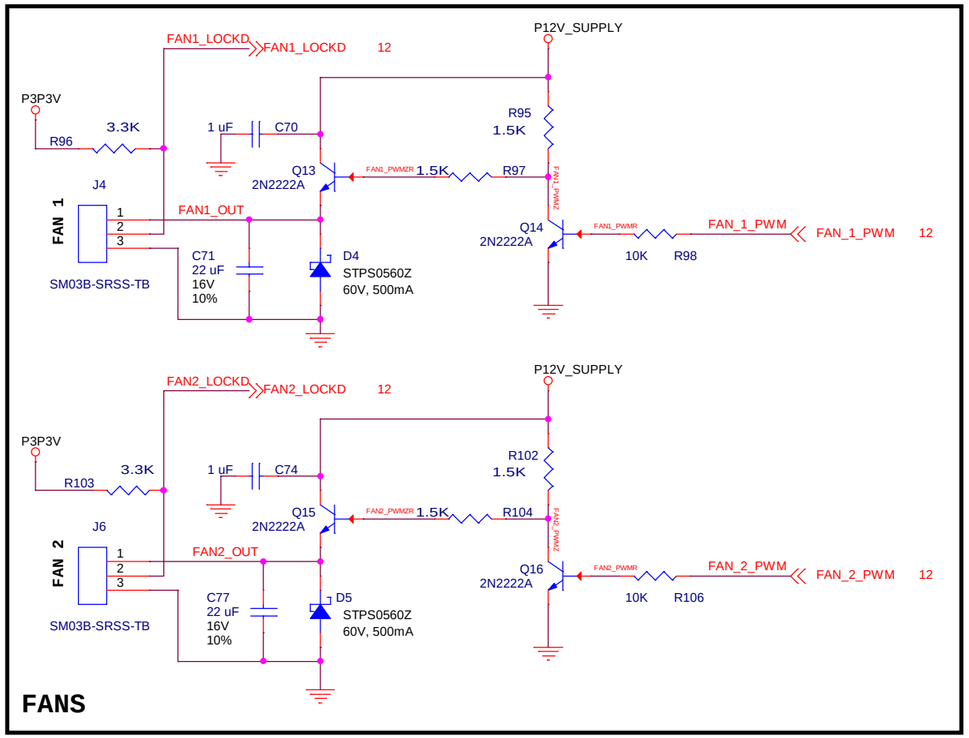
C66 0.1 uF 25V 10%

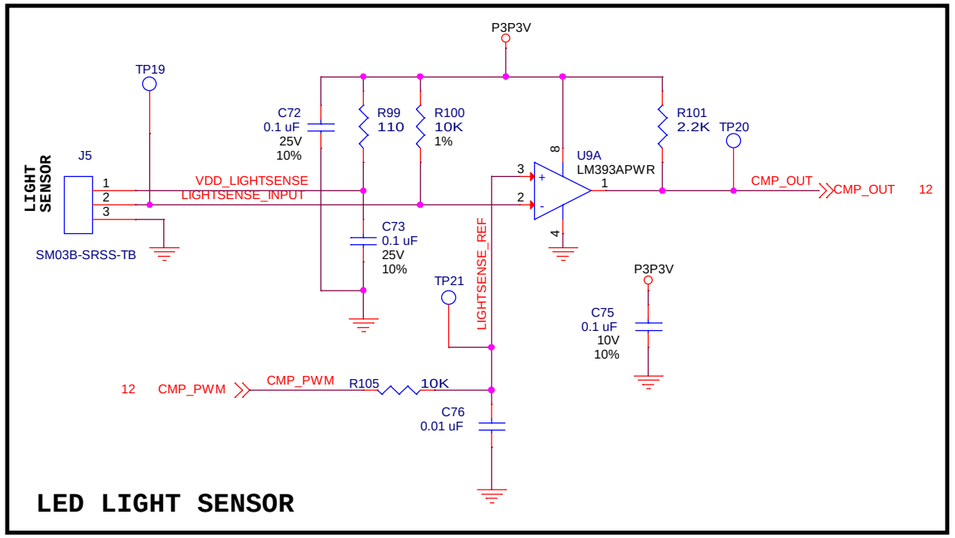
5 VCC
1 A — Y 4 — PWRGOOD — PWRGOOD 3,15,8
2 B
GND 3

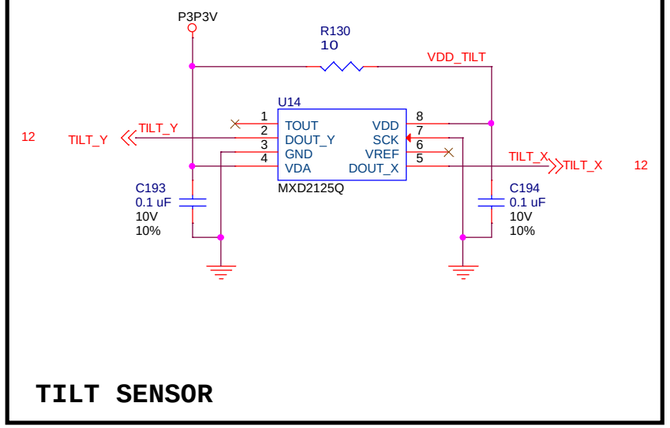
SN74AHC1G08

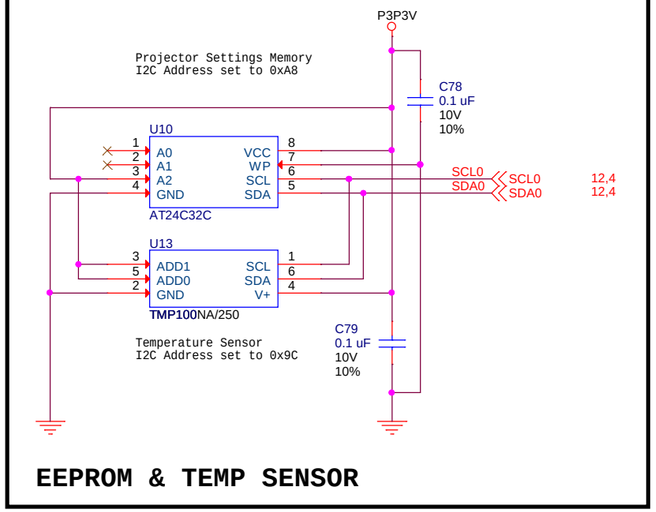
TPS Power Supplies

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 8 OF 16









Fans, Light Sensor and EEPROM

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
(C) COPYRIGHT 2014 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	ISSUE DATE 08/31/2015		SIZE A3	SHEET 9 OF 16

NOTE:
Dedicated I2C pins have I2C specific drivers.
GPIO I2C pins (GPIO_8 and GPIO_9) do not
have I2C specific drivers.

P3P3V
R107 1K
R108 1K
R109 1K
R110 1K
I2C PORT 0
J7
SM03B-SRSS-TB
SCL1 SDA1
U11
TPD2E001
VCC GND IO1 IO2
C80 0.1 uF 10V 10%

U1D
DLPC6401

TP22
TP27
INIT_DONE

P3P3V
R111 1K
J9

HOLD IN BOOT LOADER

Installed	Hold in Boot Loader
Un-Installed	Normal Operation

R112 0
R131 0
DO NOT INSTALL

TP23
TP24

(GPIO & LED CONTROL)

TP17 TP25 TP26
P12V_SUPPLY
J10
SM14B-SRSS-TB
P3P3V

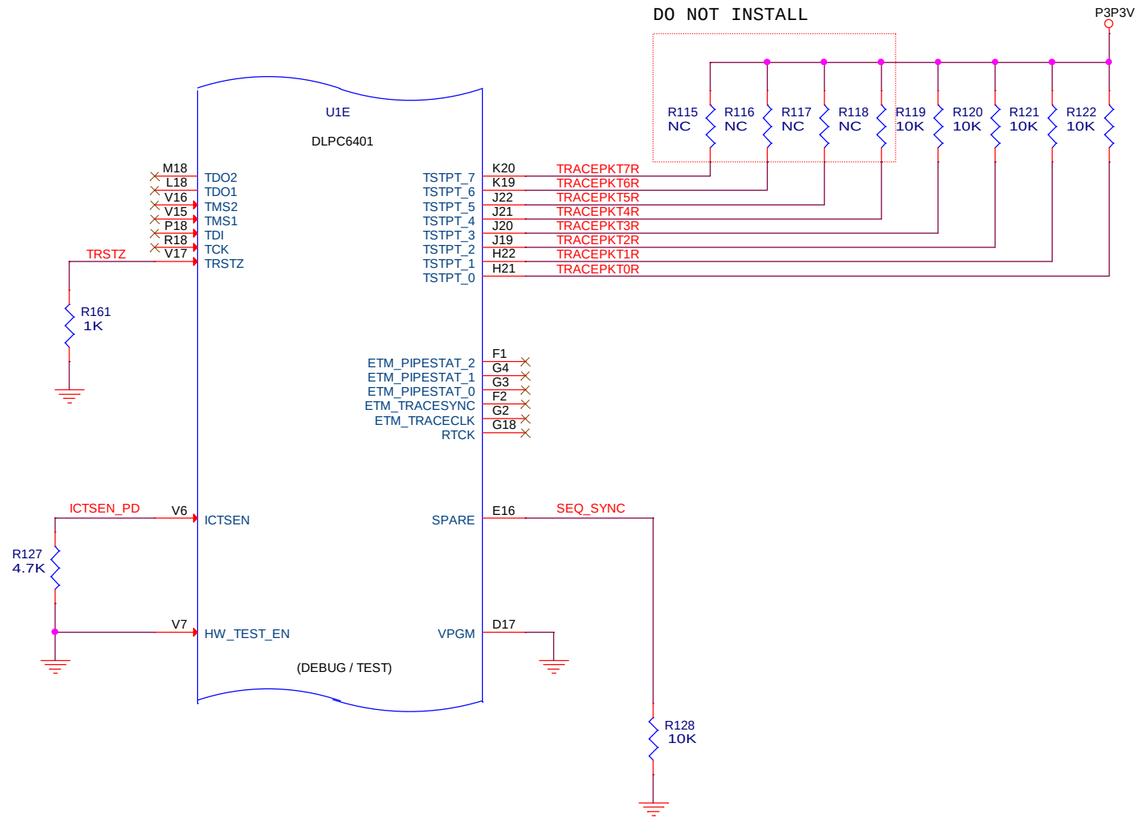
LED DRIVER INTERFACE

CMP_OUT
CMP_PWM

GPIO, I2C, and LED Control

TEXAS INSTRUMENTS	DWN	DATE		DRAWING NO	REV
(C) COPYRIGHT 2014 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	Roger Perry	10/13/2011			A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 10 OF 16	

MANUAL RESET JUMPER	
INSTALLED	HOLD IN RESET
NOT INSTALLED	NORMAL OPERATION (DEFAULT)

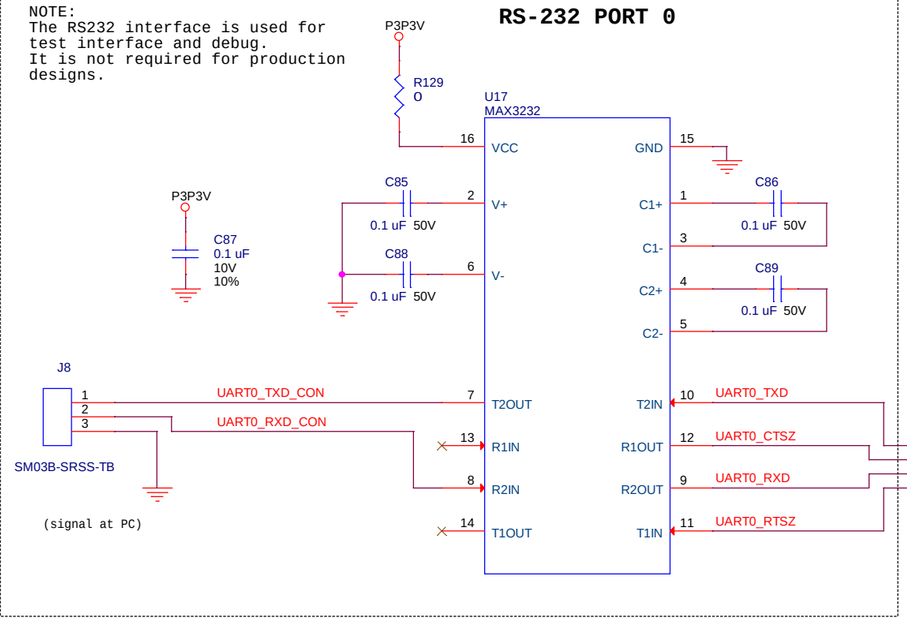


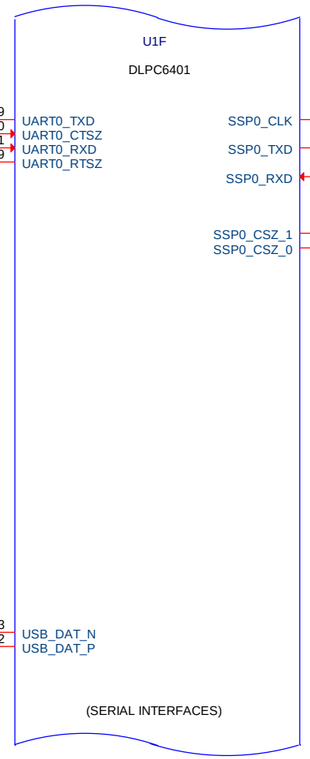
Test Points, ARM Trace JTAG and Reset

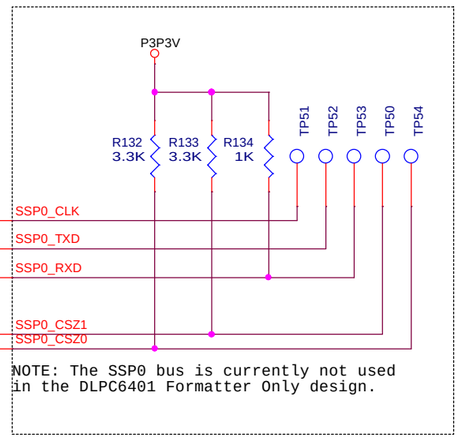
TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 11 OF 16

RS-232 PORT 0

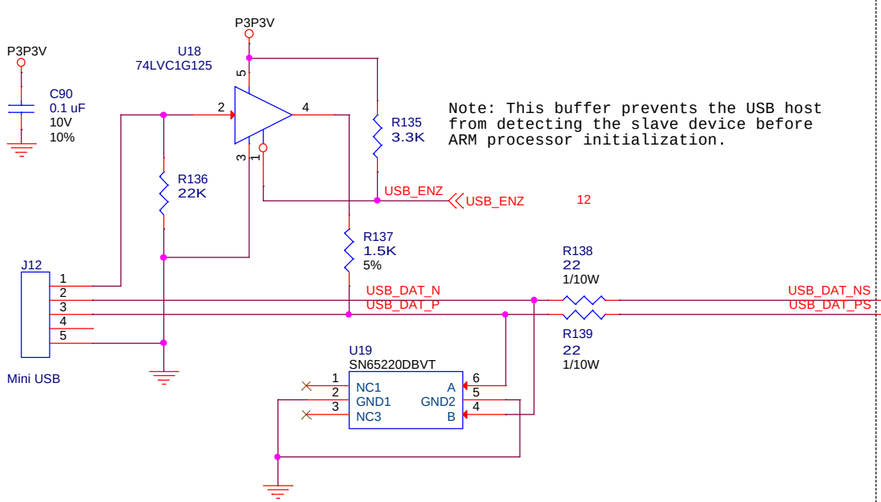
NOTE:
The RS232 interface is used for test interface and debug. It is not required for production designs.







NOTE: The SSP0 bus is currently not used in the DLPC6401 Formatter Only design.



Note: This buffer prevents the USB host from detecting the slave device before ARM processor initialization.

NOTE:
The USB interface is used for test interface, debug and high-speed flash memory programming capability. It is not required for production designs where I2C is the primary communication bus.

RS-232, Synchronous Serial Port, and USB

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 12 OF 16

PM_ADR_[22..0]

PM_DAT_[15..0]

PM_ADR_[22..0]

U1G

DLPC6401

PM_DATA_15	M1	PM_DAT_15
PM_DATA_14	N1	PM_DAT_14
PM_DATA_13	N2	PM_DAT_13
PM_DATA_12	N3	PM_DAT_12
PM_DATA_11	N4	PM_DAT_11
PM_DATA_10	P1	PM_DAT_10
PM_DATA_9	P2	PM_DAT_9
PM_DATA_8	P3	PM_DAT_8
PM_DATA_7	P4	PM_DAT_7
PM_DATA_6	R2	PM_DAT_6
PM_DATA_5	R3	PM_DAT_5
PM_DATA_4	R4	PM_DAT_4
PM_DATA_3	T1	PM_DAT_3
PM_DATA_2	T2	PM_DAT_2
PM_DATA_1	T3	PM_DAT_1
PM_DATA_0	T4	PM_DAT_0

GPIO_17	V3	PM_ADR_22
GPIO_16	W1	PM_ADR_21
PM_ADDR_20	W2	PM_ADR_20
PM_ADDR_19	Y1	PM_ADR_19
PM_ADDR_18	AB2	PM_ADR_18
PM_ADDR_17	AA3	PM_ADR_17
PM_ADDR_16	Y4	PM_ADR_16
PM_ADDR_15	W5	PM_ADR_15
PM_ADDR_14	AB3	PM_ADR_14
PM_ADDR_13	AA4	PM_ADR_13
PM_ADDR_12	Y5	PM_ADR_12
PM_ADDR_11	W6	PM_ADR_11
PM_ADDR_10	AB4	PM_ADR_10
PM_ADDR_9	AA5	PM_ADR_9
PM_ADDR_8	Y6	PM_ADR_8
PM_ADDR_7	W7	PM_ADR_7
PM_ADDR_6	AB5	PM_ADR_6
PM_ADDR_5	AA6	PM_ADR_5
PM_ADDR_4	Y7	PM_ADR_4
PM_ADDR_3	AB6	PM_ADR_3
PM_ADDR_2	W8	PM_ADR_2
PM_ADDR_1	AA7	PM_ADR_1
PM_ADDR_0	AB7	PM_ADR_0

PM_BLSZ_1	AA8	
PM_BLSZ_0	AB8	

PM_WEZ	V2	PM_WEZ	R150 33.2	PM_WESZ	PM_WESZ 15
PM_OEZ	U4	PM_OEZ	R152 33.2	PM_OESZ	PM_OESZ 15

PM_CSZ_0	U3				
PM_CSZ_1	U2	FLASH_CSZ	R155 33.2	FLASH_CSSZ	FLASH_CSSZ 15
PM_CSZ_2	U1				

(MEMORY INTERFACE)

R140 10K PM_ADR_22

R141 10K PM_ADR_21

U12

PM_ADR_21	13	A21
PM_ADR_20	10	A20
PM_ADR_19	9	A19
PM_ADR_18	16	A18
PM_ADR_17	17	A17
PM_ADR_16	48	A16
PM_ADR_15	1	A15
PM_ADR_14	2	A14
PM_ADR_13	3	A13
PM_ADR_12	4	A12
PM_ADR_11	5	A11
PM_ADR_10	6	A10
PM_ADR_9	7	A9
PM_ADR_8	8	A8
PM_ADR_7	18	A7
PM_ADR_6	19	A6
PM_ADR_5	20	A5
PM_ADR_4	21	A4
PM_ADR_3	22	A3
PM_ADR_2	23	A2
PM_ADR_1	24	A1
PM_ADR_0	25	A0

DQ15/A-1	45	PM_DAT_15
DQ14	43	PM_DAT_14
DQ13	41	PM_DAT_13
DQ12	39	PM_DAT_12
DQ11	36	PM_DAT_11
DQ10	34	PM_DAT_10
DQ9	32	PM_DAT_9
DQ8	30	PM_DAT_8
DQ7	44	PM_DAT_7
DQ6	42	PM_DAT_6
DQ5	40	PM_DAT_5
DQ4	38	PM_DAT_4
DQ3	35	PM_DAT_3
DQ2	33	PM_DAT_2
DQ1	31	PM_DAT_1
DQ0	29	PM_DAT_0

P3P3V

R146 10K

R147 10K

14 WP/ACC

BYTE 47 BYTE

15 PM_WESZ PM_WESZ 11 WE

15 PM_OESZ PM_OESZ 28 OE

15 FLASH_CSSZ FLASH_CSSZ 26 CE

15 FLASH_RSTZ FLASH_RSTZ 12 RESET

BUSY	15	
VCC	37	P3P3V
GND	27	
GND	46	

S29JL032H

P3P3V

R156 10K

C161 0.1 uF 10V 10%

P3P3V

C91 0.1 uF 10V 10%

3,8,9 PWRGOOD PWRGOOD

R159 NC

DO NOT INSTALL

FLASH_RSTZ FLASH_RSTZ 15

R160 0

8,9 POSENSE POSENSE

Flash Memory Interface

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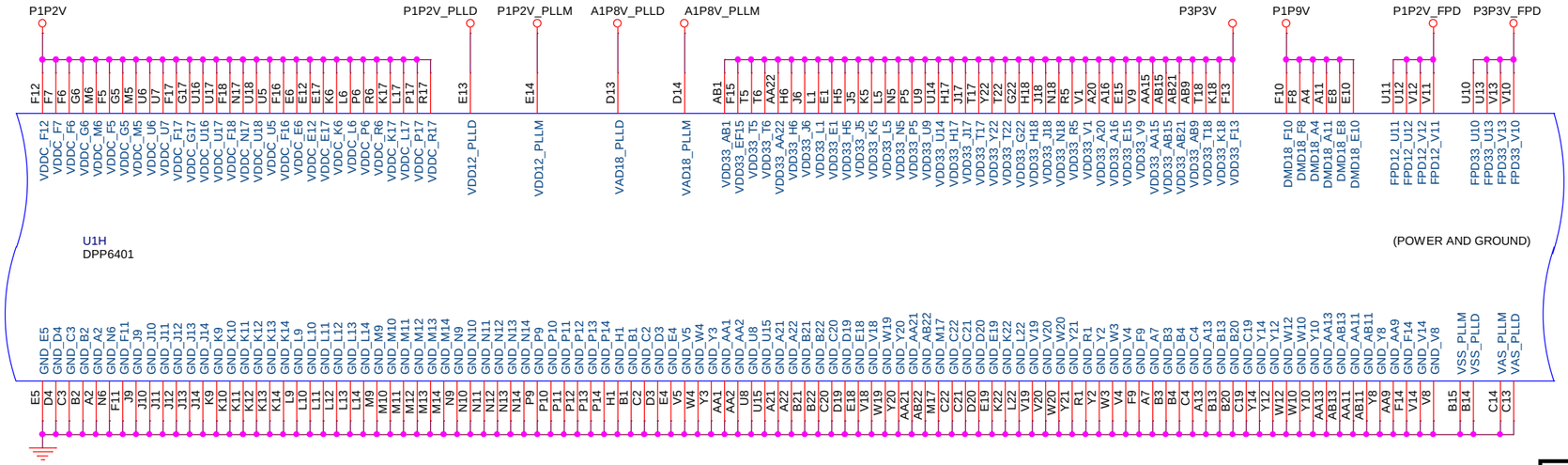
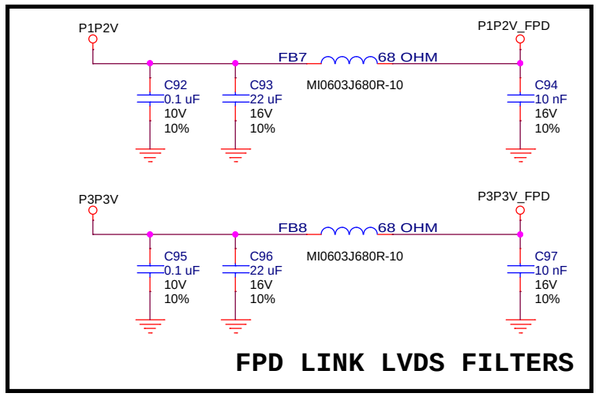
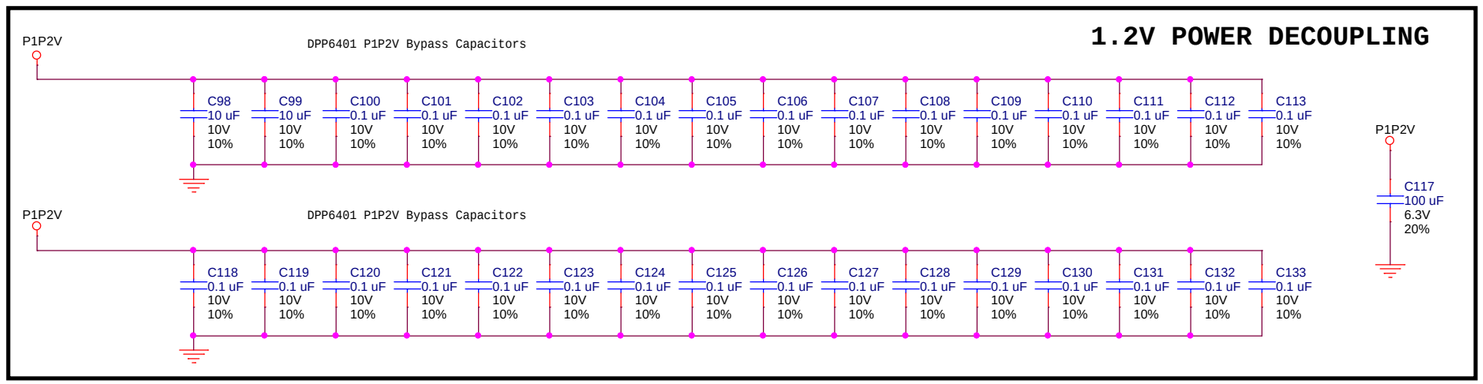
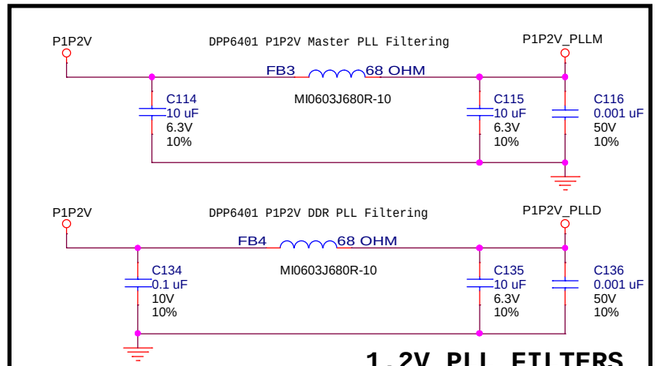
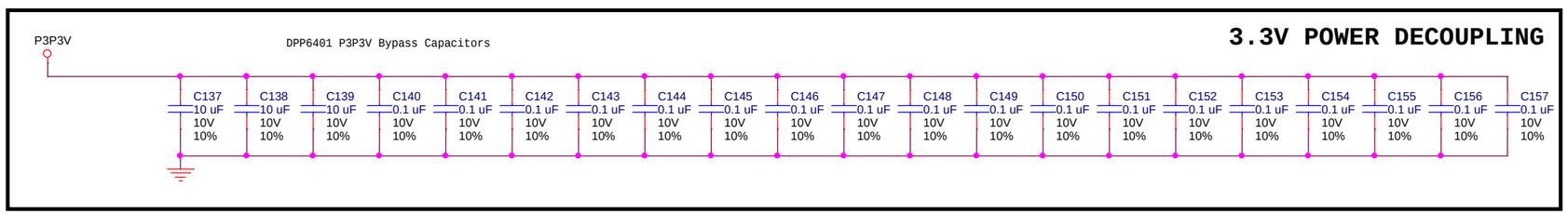
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 13 OF 16

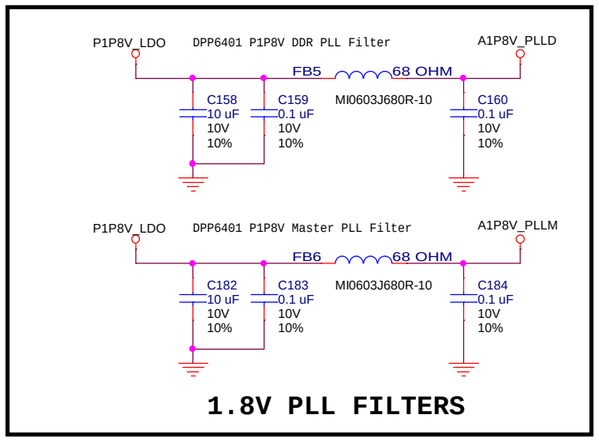


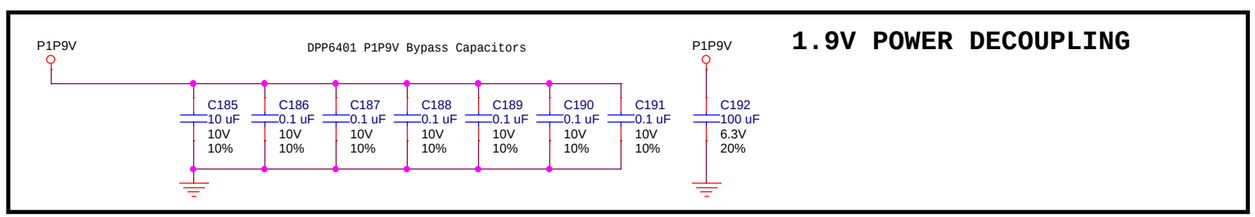










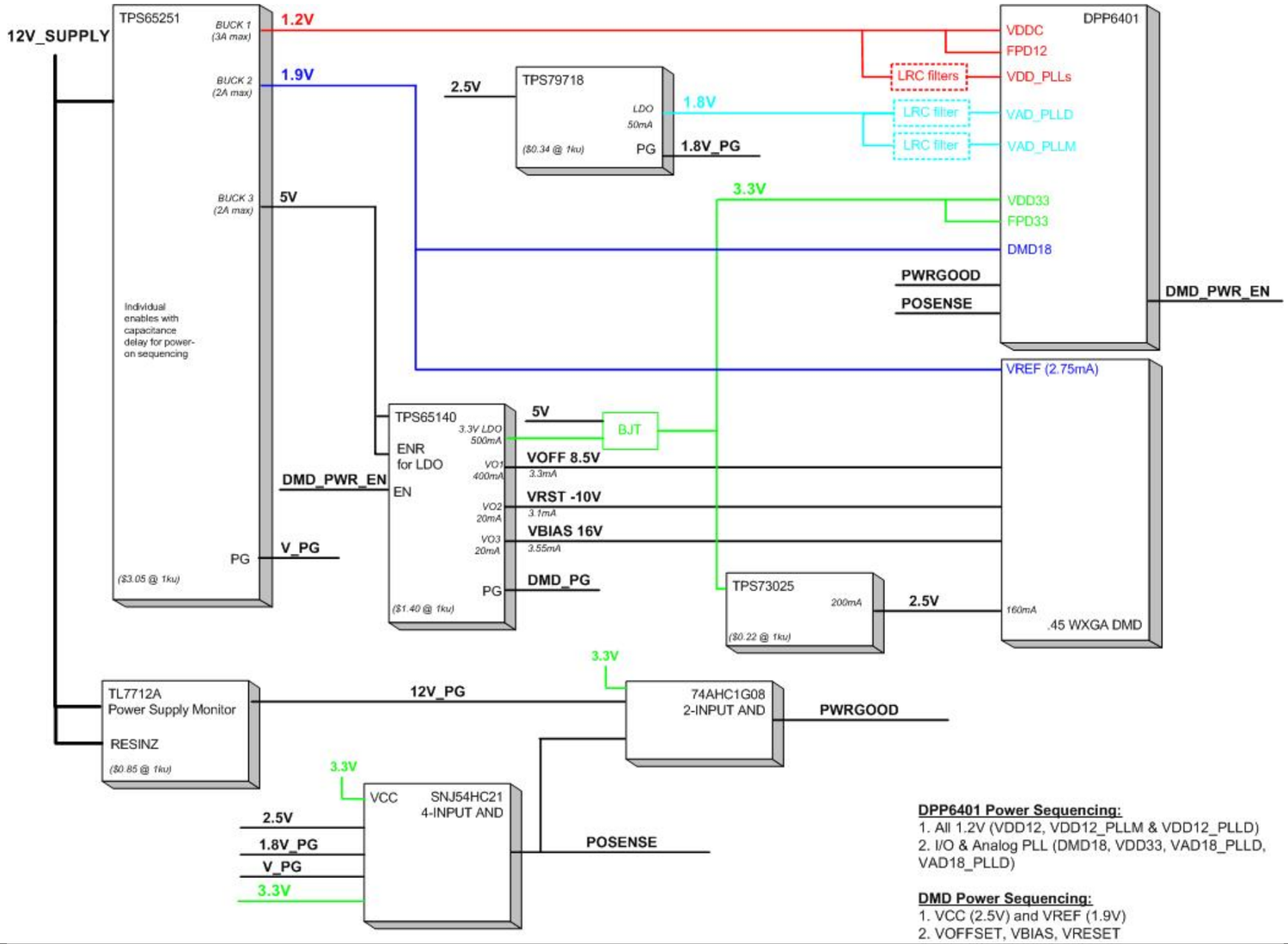


DPP6401 Power and Bypass Capacitors

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO
	ISSUE DATE 08/31/2015		REV A
		SIZE A3	SHEET 14 OF 16

POWER TREE

TPS Architecture



DPP6401 Power Sequencing:

1. All 1.2V (VDD12, VDD12_PLLM & VDD12_PLLD)
2. I/O & Analog PLL (DMD18, VDD33, VAD18_PLLD, VAD18_PLLD)

DMD Power Sequencing:

1. VCC (2.5V) and VREF (1.9V)
2. VOFFSET, VBIAS, VRESET

Power Tree

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 15 OF 16

Revision History

Rev. A: Initial Release

Schematic Revision History

TEXAS INSTRUMENTS	DWN Roger Perry	DATE 10/13/2011	DRAWING NO	REV A
	ISSUE DATE 08/31/2015		SIZE A3	SHEET 16 OF 16

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