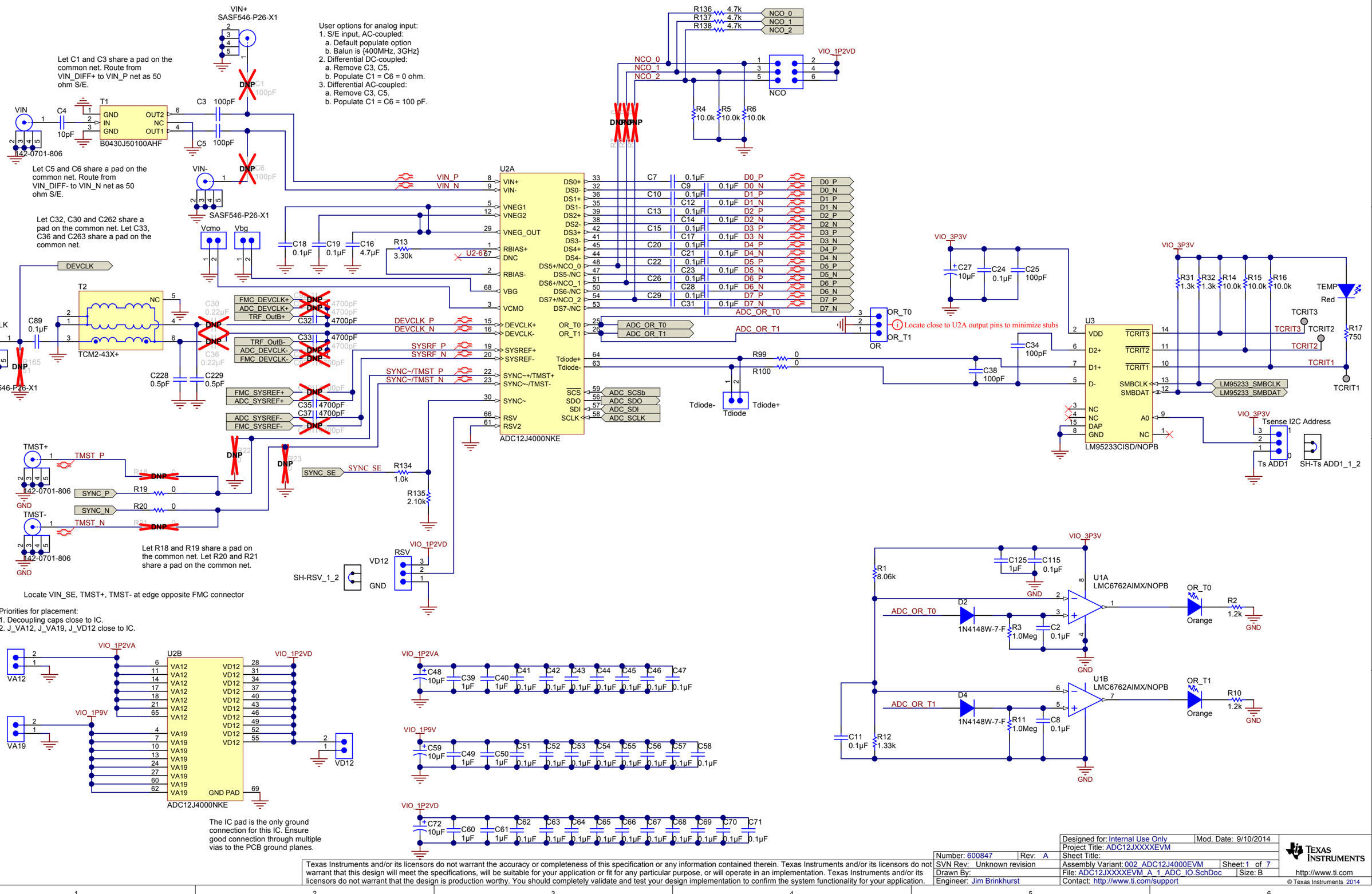
User options for analog input:
1. S/E input, AC-coupled:
a. Default populate option
b. Balun is {400MHz, 3GHz}
2. Differential DC-coupled:
a. Remove C3, C5.
b. Populate C1 = C6 = 0 ohm.
3. Differential AC-coupled:
a. Remove C3, C5.
b. Populate C1 = C6 = 100 pF.
Let C1 and C3 share a pad on the common net. Route from VIN_DIFF+ to VIN_P net as 50 ohm S/E.
Let C5 and C6 share a pad on the common net. Route from VIN_DIFF- to VIN_N net as 50 ohm S/E.
Let C32, C30 and C262 share a pad on the common net. Let C33, C36 and C263 share a pad on the common net.
Let R18 and R19 share a pad on the common net. Let R20 and R21 share a pad on the common net.
Locate VIN_SE, TMST+, TMST- at edge opposite FMC connector
Priorities for placement:
1. Decoupling caps close to IC.
2. J_VA12, J_VA19, J_VD12 close to IC.
The IC pad is the only ground connection for this IC. Ensure good connection through multiple vias to the PCB ground planes.
Locate close to U2A output pins to minimize stubs
U2A
ADC12J4000NKE
U2B
ADC12J4000NKE
U3
LM95233CISD/NOPB
U1A
LMC6762AIMX/NOPB
U1B
LMC6762AIMX/NOPB
T1
B0430J50100AHF
T2
TCM2-43X+
OR
NCO
SH-RSV_1_2
SH-Ts ADD1_1_2
Ts ADD1
Tsense I2C Address
Tdiode
Red
Orange
Orange
VIN+
VIN-
VIN
TMST+
TMST-
DEVCLK
VCMO
VBG
VA12
VA19
VD12
GND
VIO_1P2VD
VIO_1P2VA
VIO_1P9V
VIO_3P3V
VIO_1P2VD
VIO_1P2VA
VIO_1P9V
VIN_P
VIN_N
DEVCLK_P
DEVCLK_N
SYSREF_P
SYSREF_N
SYNC~/TMST_P
SYNC~/TMST_N
SYNC_SE
TMST_P
TMST_N
SYNC_P
SYNC_N
D0_P
D0_N
D1_P
D1_N
D2_P
D2_N
D3_P
D3_N
D4_P
D4_N
D5_P
D5_N
D6_P
D6_N
D7_P
D7_N
ADC_OR_T0
ADC_OR_T1
ADC_SCSb
ADC_SDO
ADC_SDI
ADC_SCLK
LM95233_SMBCLK
LM95233_SMBDAT
TCRIT3
TCRIT2
TCRIT1
NCO_0
NCO_1
NCO_2
RSV
VD12
DNP
SASF546-P26-X1
I42-0701-806
TCM2-43X+
Tdiode-
Tdiode+
Designed for: Internal Use Only
Mod. Date: 9/10/2014
Project Title: ADC12JXXXXEVM
Sheet Title:
Assembly Variant: 002_ADC12J4000EVM
Sheet: 1 of 7
File: ADC12JXXXXEVM_A_1_ADC_IO.SchDoc
Size: B
Number: 600847
Rev: A
SVN Rev: Unknown revision
Drawn By:
Engineer: Jim Brinkhurst
Contact: http://www.ti.com/support
http://www.ti.com
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The D<7:0> connections polarity have
been swapped from the TI standard
FMC ADC guidelines to ease routing.
This is accounted for in the FPGA code.

FMC_RX1A

DP1_M2C_P / DP1_M2C_N — D1_N / D1_P
DP2_M2C_P / DP2_M2C_N — D2_N / D2_P
DP3_M2C_P / DP3_M2C_N — D3_N / D3_P
DP4_M2C_P / DP4_M2C_N — D4_N / D4_P
DP5_M2C_P / DP5_M2C_N — D5_N / D5_P
D7_N / D7_P — DP7_M2C_P / DP7_M2C_N
D6_N / D6_P — DP6_M2C_P / DP6_M2C_N

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FMC_RX1B

DP0_M2C_P / DP0_M2C_N — D0_N / D0_P
GBTCLK0_M2C_P
DEVCLKARX_P
DEVCLKARX_N
GBTCLK0_M2C_N
ADC_OR_T1
KC705_JTAG
FMC_SCL
FMC_SDA
3P3VAUX
12P0V_RX
EE_ADDR0_RX
EE_ADDR1_RX
3P3V_RX 3P3RX
R132
0

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PG_RX1
PG_C2M_RX
PG_M2C_RX
VADJ_RX
RR6
4.99k

FMC_RX1C

NCO_0
NCO_1
NCO_2
VADJ_RX

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FMC_RX1D

LA00_P_CC / LA00_N_CC — DEVCLKBRX_P / DEVCLKBRX_N
LA03_P / LA03_N — SYSREFRX_P / SYSREFRX_N
LA08_P / LA08_N — SYNC_P / SYNC_N
ADC_OR_T0
FMC_SPI_CLK
FMC_SPI_SCSb1
FMC_SPI_SCSb2
FMC_ADC_SDI
FMC_ADC_SDO
SYNC_SE
FMC_SPI_SDIO
FMC_ADC_CLK
FMC_ADC_SCSb0

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PRSNT_M2C_L_RX

FMC_RX1E

LMK04828_SYNC
LMK04828_RESET
FMC_DEVCLK_P / FMC_DEVCLK_N — FMC_DEVCLK+ / FMC_DEVCLK-
FMC_SYSREF_P / FMC_SYSREF_N — FMC_SYSREF+ / FMC_SYSREF-

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VIO_B_M2C_RX
RR7
0

3P3VAUX
C143
1µF
U16
DNP
24C65T/SM
FMC_SDA
FMC_SCL
EE_ADDR1_RX
EE_ADDR0_RX
J1
TSW-104-07-G-S
3P3VAUX

Number: 600847	Rev: A
SVN Rev: Unknown revision	
Drawn By:	
Engineer: Jim Brinkhurst	

Designed for: Internal Use Only	Mod. Date: 9/10/2014
Project Title: ADC12JXXXXEVM	
Sheet Title:	
Assembly Variant: 002_ADC12J4000EVM	Sheet: 2 of 7
File: ADC12JXXXXEVM_A_2_FMC.SchDoc	Size: C
Contact: http://www.ti.com/support	

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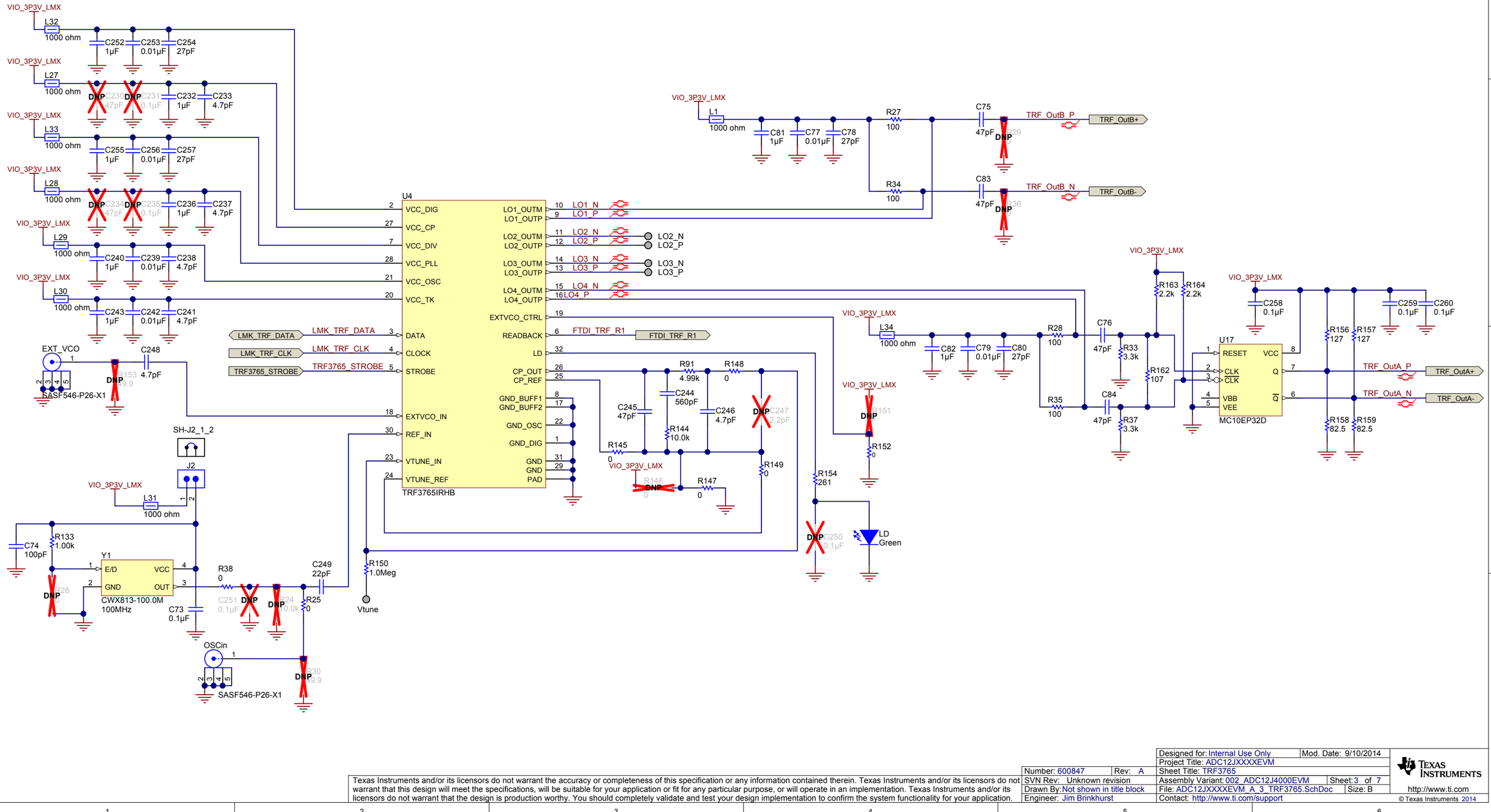

Number: 600847	Rev: A	Designed for: Internal Use Only	Mod. Date: 9/10/2014
SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By: Not shown in title block		Sheet Title: TRF3765	
Engineer: Jim Brinkhurst		Assembly Variant: 002_ADC12J4000EVM	Sheet: 3 of 7
		File: ADC12JXXXXEVM_A_3_TRF3765.SchDoc	Size: B
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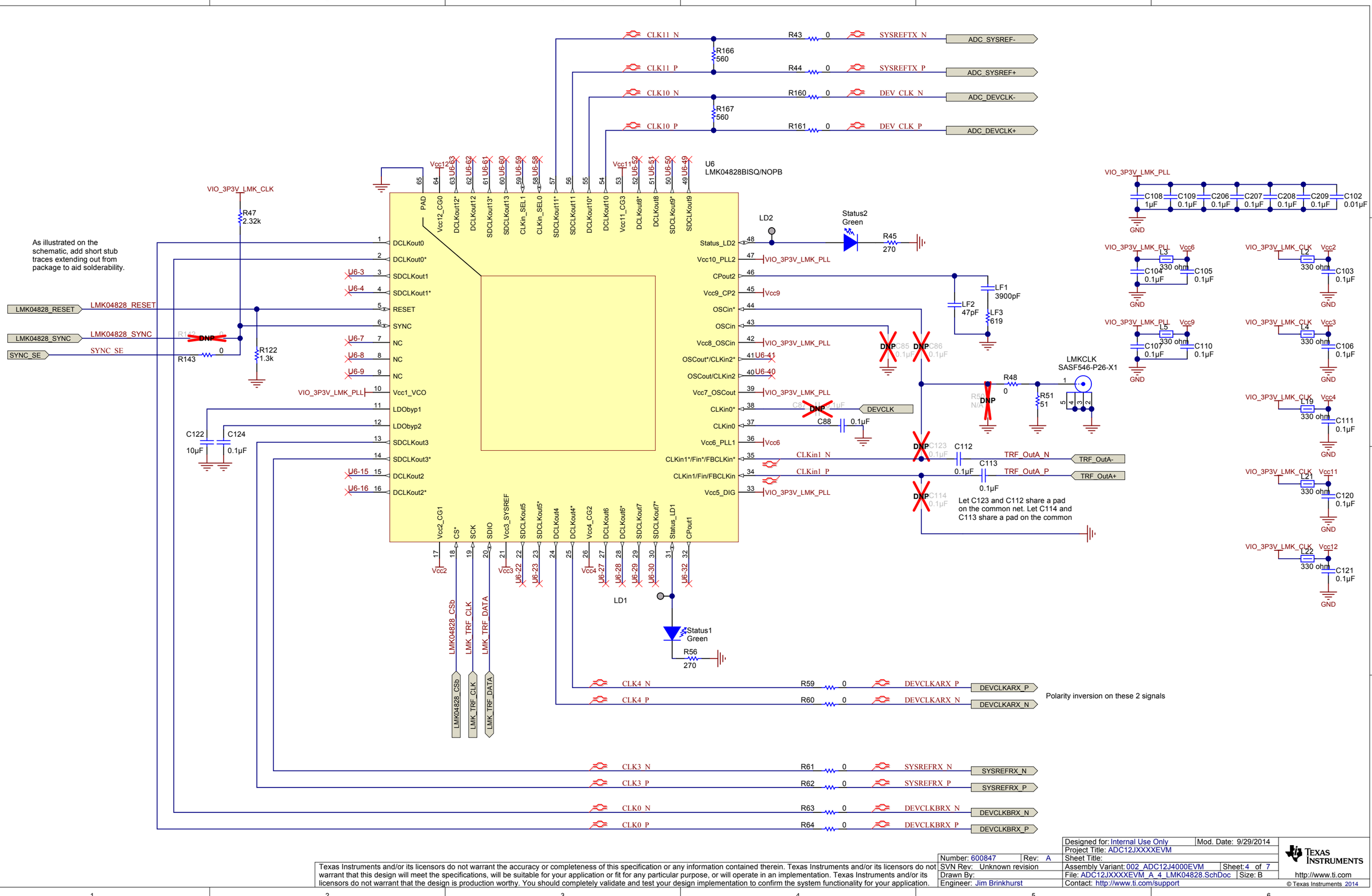

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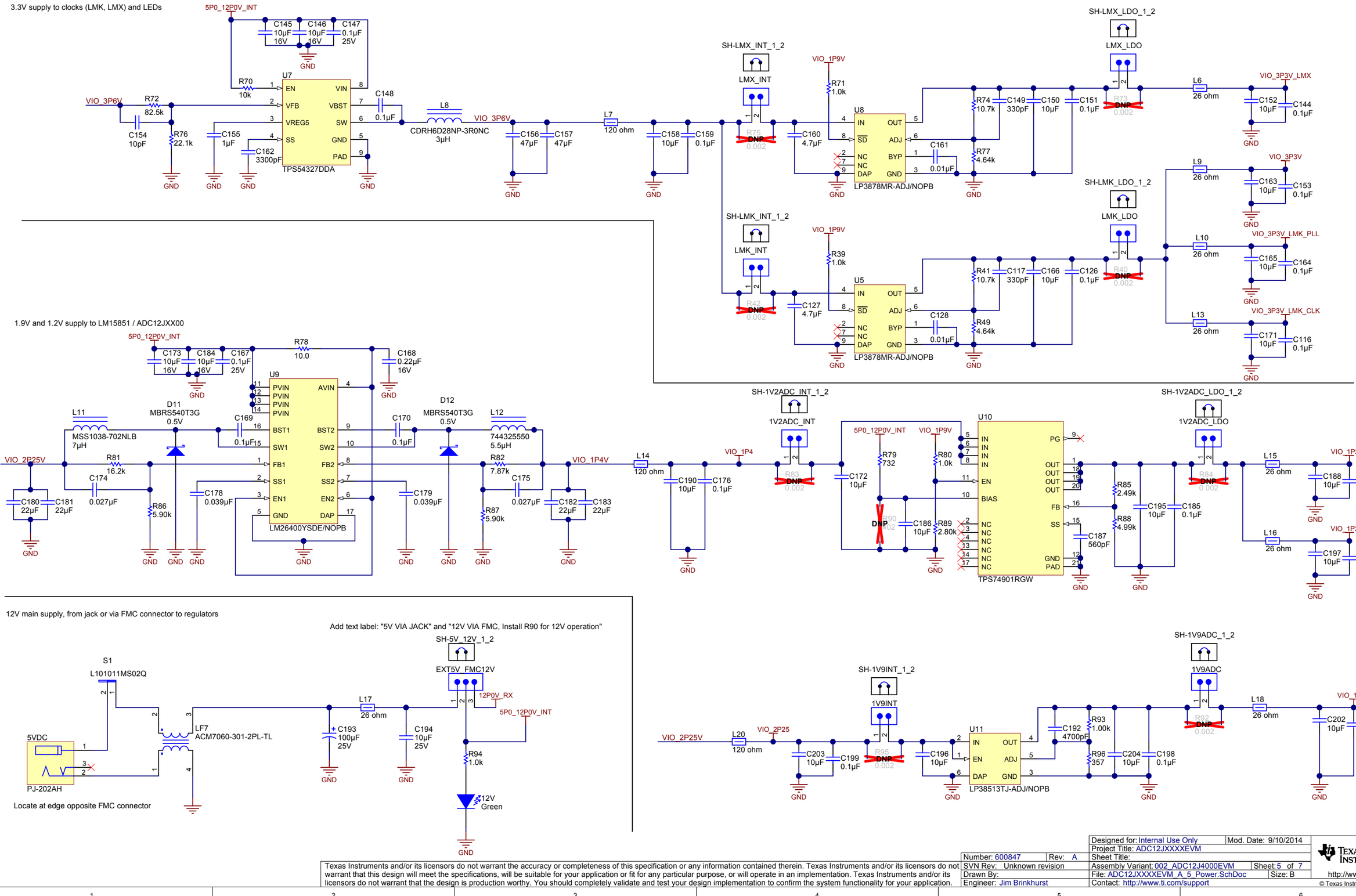
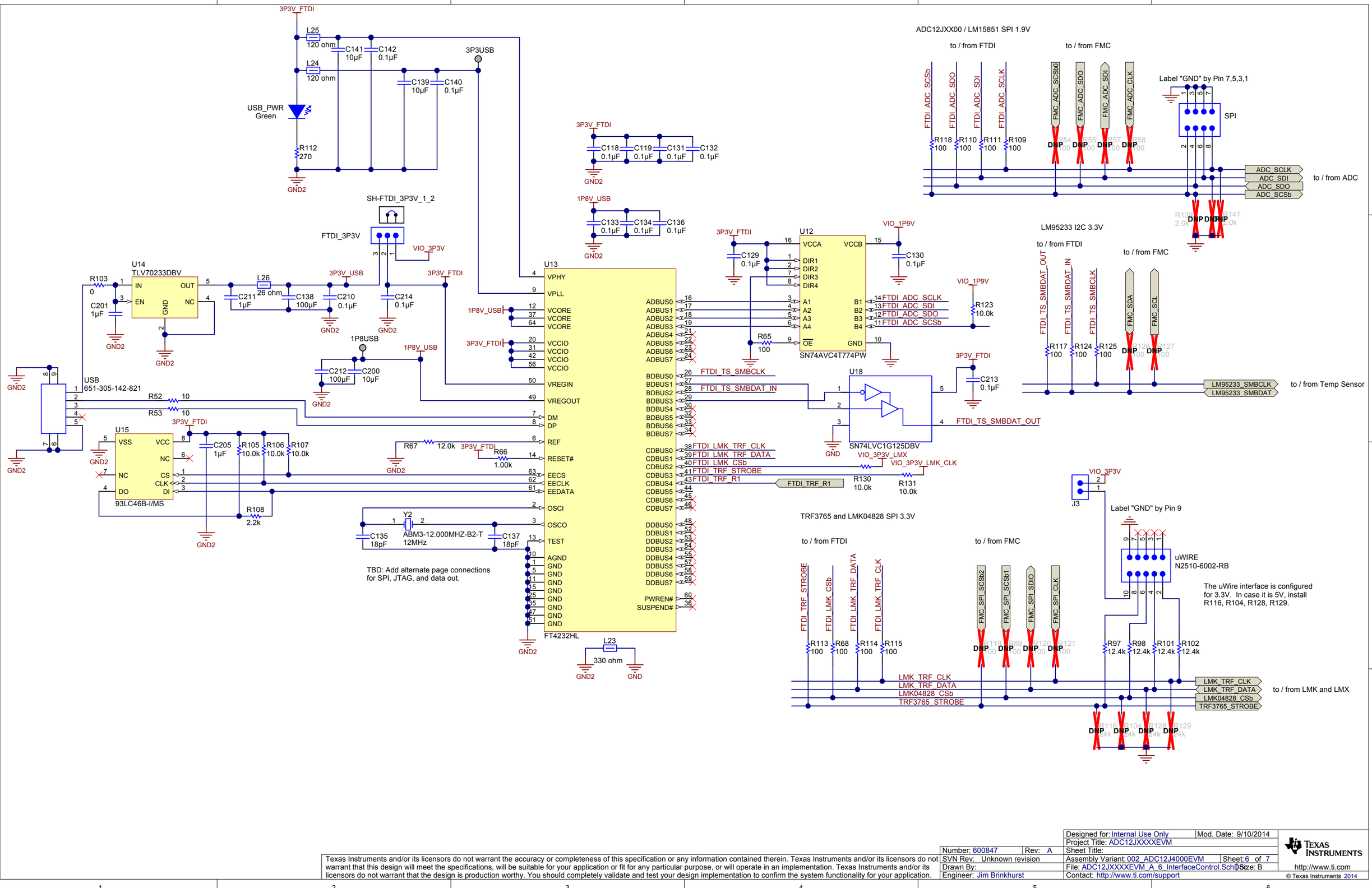
SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 002_ADC12J4000EVM	Sheet: 4 of 7
		File: ADC12JXXXXEVM_A_4_LMK04828.SchDoc	Size: B
		Contact: http://www.ti.com/support	



Number: 600847	Rev: A	Designed for: Internal Use Only	Mod. Date: 9/10/2014
SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 002_ADC12J4000EVM	Sheet: 5 of 7
		File: ADC12JXXXXEVM_A_5_Power.SchDoc	Size: B
		Contact: http://www.ti.com/support	http://www.ti.com



Number: 600847	Rev: A
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Drawn By:	
Engineer: Jim Brinkhurst	

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Project Title: ADC12JXXXEVM	
Sheet Title:	
Assembly Variant: 002_ADC12J4000EVM	Sheet: 6 of 7
File: ADC12JXXXEVM_A_6_InterfaceControl.SchDoc	Size: B
Contact: http://www.ti.com/support	

DNP
FID1

PCB Number: 600847
PCB Rev: A

PCB
ESD LOGO
ESD Susceptible

PCB
LOGO
Texas Instruments

H4
H6
1648-440-AL
NY PMS 440 0025 PH
DNP
FID2

H3
H5
1648-440-AL
NY PMS 440 0025 PH
DNP
FID3

H9
MECH
FMC - FMC Screw
PMSS 256 0075 PH

H10
MECH
FMC - FMC Nut

H11
MECH
FMC - FMC Screw
PMSS 256 0075 PH

H12
MECH
FMC - FMC Nut

GND GND1 GND2 GND3

Place at least two of the GND test points in the power section.

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2., unless otherwise specified.

VIO_3P3V C215 0.1µF GND
VIO_3P3V C216 0.1µF VIO_3P3V_LMX
VIO_3P3V C217 0.1µF VIO_3P3V_LMX
VIO_3P3V C218 0.1µF GND
VIO_1P4 C219 0.1µF VIO_3P3V
VIO_3P3V C220 0.1µF 5P0_12P0V_INT
VIO_1P4 C221 0.1µF 5P0_12P0V_INT
5P0_12P0V_INT C94 0.1µF 12P0V_RX

VIO_2P25 C222 0.1µF 5P0_12P0V_INT
VIO_2P25 C223 0.1µF 5P0_12P0V_INT
VIO_1P4 C224 0.1µF VIO_3P3V
VIO_1P4 C225 0.1µF 5P0_12P0V_INT
VIO_2P25 C226 0.1µF 5P0_12P0V_INT
VIO_2P25 C227 0.1µF 5P0_12P0V_INT
5P0_12P0V_INT C261 0.1µF GND
VIO_3P3V C95 0.1µF VIO_1P2VD
VIO_3P3V C96 0.1µF VIO_1P2VD

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SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 002_ADC12J4000EVM	Sheet: 7 of 7
		File: ADC12JXXXXEVM_A_7_Hardware.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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