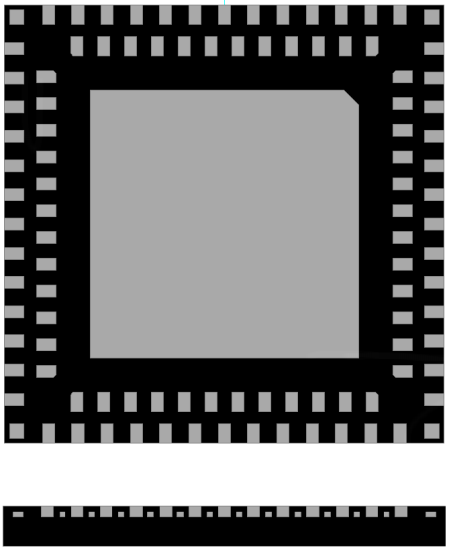
Design Summary Multi-row Quad Flat No-lead (MRQFN)

ABSTRACT

Texas Instruments Incorporated (TI) introduces the Multi-row Quad Flat No-lead (MRQFN) series of packages. MRQFNs are compact yet accommodating plastic encapsulated packages that use bottom terminations, without peripherally protruding leads, within their construction. This assembly results in a cost-effective advanced packaging solution maximizing board utilization with added benefits of supporting multi functional designs and improved electrical and thermal performance over traditional leaded packages. MRQFN packages have an exposed pad that enhances both thermal and electrical characteristics while enabling high-power and high-frequency applications within a compact design. This document offers a point of reference for design considerations enabling robust surface mount assembly. For more information, visit www.ti.com



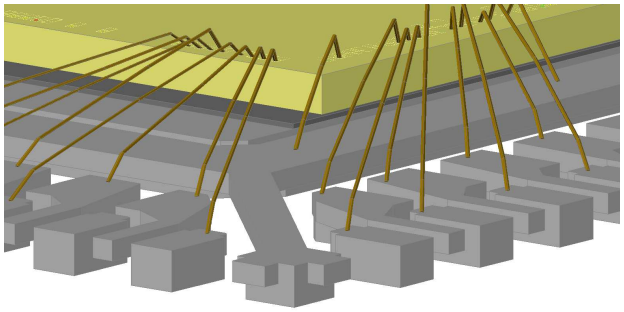
Example: 100 Pin (MRQFN) Package

MRQFN Package Details[(1)]

	100 Pin (MRQFN)
Total Number of Pins	100
Package *Length (L) mm	9
Package *Width (W) mm	9
Package Thickness (T) mm	0.80 Max
Pitch mm	0.55 Inner row, 0.60 Outer row
Lead Finish	NiPdAu
RoHS/Green	Yes
Moisture Sensitivity Level (JEDEC)	MSL 3 / 260 C

(1) Nominal Dimensions Shown (See Package Drawing for full information)

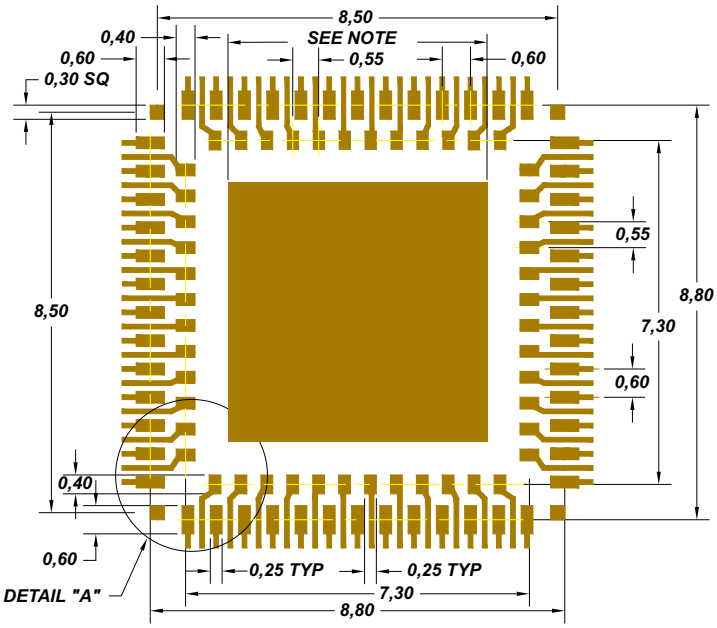
MRQFN Package Illustrated

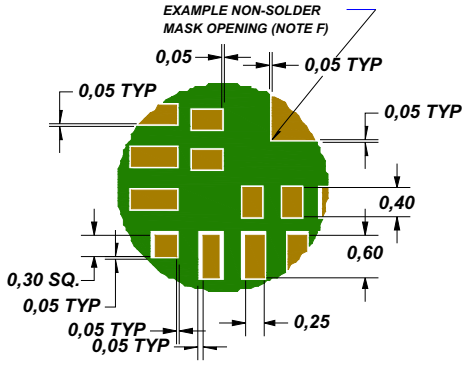


The MRQFN Package maximum thickness is 0.80 mm. The package seating height will be dependent upon the solder paste volume and land pad design.

PCB DESIGN GUIDELINES

Although TI recommends NSMD (Non Solder Mask Defined) pads over SMD (Solder Mask Defined) pads when surface mounting MRQFN's both can be utilized. NSMD allows tighter tolerance on copper etching and by design provides a larger solderable area due to the exposed edges being free from solder mask. When routing signals between periphery pads the trace should be centered in order to maximize solder mask coverage for board fabrication purposes.





PCB LAND PAD DETAIL "A"

Note: The PCB land pattern illustrated is specifically designed by part number therefore, variations in thermal pad dimensions may exist between part numbers. The exposed pad sizes can be confirmed within the product data sheet. Additionally, contact your TI customer representative for further details.

100 Pin MRQFN EXAMPLE PCB LAND PAD DESIGN

PCB Land Pad / Stencil Design Notes

(A) All dimensions are in millimeters.

(B) These drawings are subject to change without notice.

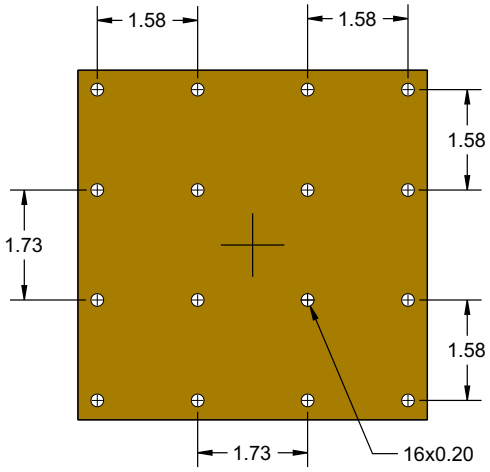
(C) Publication IPC-7351 is an alternate information source for PCB land pattern designs.

(D) These packages are designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com.

(E) Laser cutting apertures with trapezoidal walls and rounded corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

(F) Customers should contact their board fabrication site for recommended solder mask tolerances, recommended via sizes, and any via tenting recommendations for vias placed in thermal pad.

Example MRQFN Thermal Via Design



Example Via Layout Design Via layout may vary depending on layout constraints (Note D, F above)

In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias are recommended to be incorporated into the thermal pad design. The number of thermal vias will depend on the application, power dissipation, and electrical requirements. For temperature-critical applications via pitch down to 1mm can be used and vias may be filled or plugged.

Vias filled or plugged help prevent solder loss and protrusions. This often produces the best thermal performances but is not necessary or recommended due to increased PCB cost and because solder tends to wet the upper surface area prior to filling the vias.

Solder mask tenting is optional and if used top side is recommended to eliminate the risk of solder loss or protrusions thru the via onto the opposite side of the PCB. Trials have shown that via tenting from the top is less likely to produce voids between the exposed pad and PCB pad when compared to via tenting from the bottom.

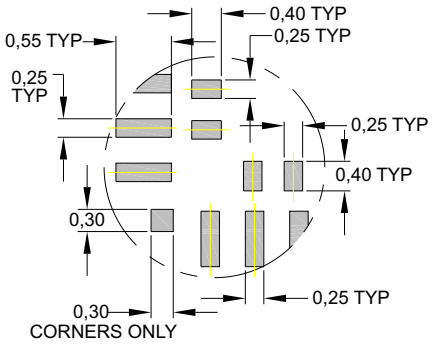
For this specific design TI recommends a 0,2 mm diameter drill size to limit or control solder loss.

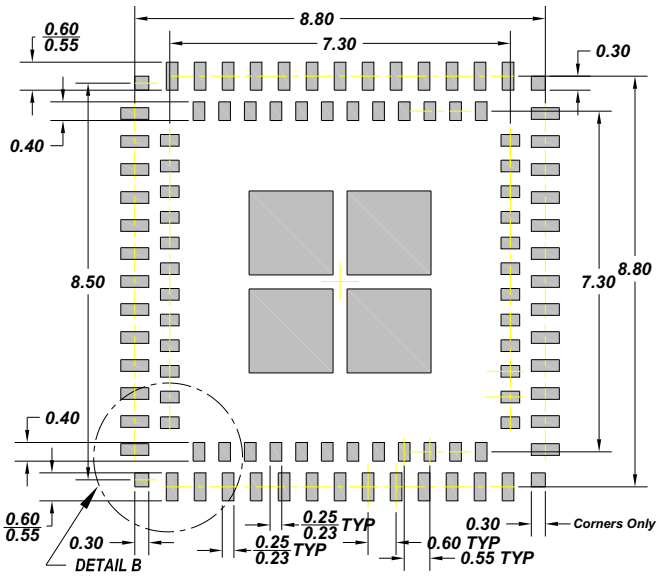
Thermal vias should interconnect to a ground plane typically but must be checked using the electrical schematic within the devices product datasheet .

100 PIN MRQFN EXAMPLE STENCIL DESIGN

See note D & F “PCB Land Pad/Stencil Design Notes” Example Stencil Design 0,1 - 0,125mm Thick Stencil (Note “E” above)

PCB Solder Mask Stencil Detail “B”





Solder Paste Recommendations

TI recommends the use of type 3 or finer solder paste when mounting a MRQFN. The use of paste offers the following advantages:

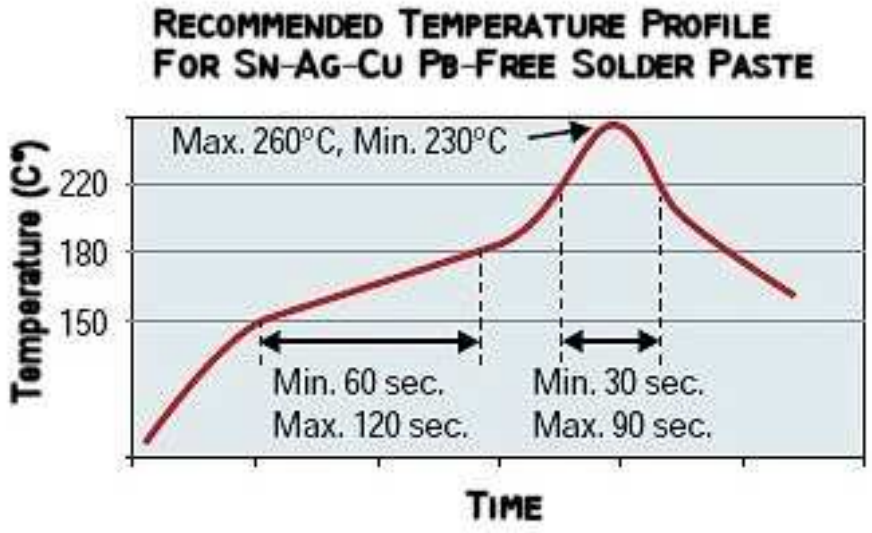
- Contains flux to aid wetting of the solder to the PCB land.
- The adhesive properties of the paste will hold the component in place during manufacture.
- Paste by volume contains ~50% metal load and can be varied thru aperture design and stencil thickness. MRQFN’s are typically manufactured with printed center pad volumes between 50% and 80% by area to facilitate wetting of the periphery solder joints and to maintain a standoff from the board surface.
- Paste selection is normally driven by overall system assembly requirements. In general, "no clean" compositions are preferred due to the difficulty in cleaning under low profile mounted components. Customers should check with your solder paste and cleaning chemistry supplier for recommendations when cleaning is necessary.

IR REFLOW PROFILES

The MRQFN lead finish (NiPdAu) is compatible with both lead and lead-free solder pastes.

	Pb Free
Ramp Rate	3°C/sec. Max.(1)
Preheat	150 to 180°C
	60 to 120 sec.
Time Above Liquidus	220°C
	30 to 90 sec.
Peak Temperature	255°C ±5°C
Time Within 5°C Peak Temperature	10 to 20 sec.
Ramp Down Rate	6°C/sec. Max.

(1) No testing using a forced cool down of 6°C per second has been conducted



TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Figure above illustrates a range of temperatures that TI packages are capable of with-standing without risk to package reliability but TI prefers parts to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact profile would depend on the maximum peak temperature for the component as rated on the MSL label, the solder paste manufacturer's recommendation, complexity of the PWB, and capability of the reflow equipment to be confirmed by the SMT assembly operation.

SOLDER JOINT QUALITY AND INSPECTION

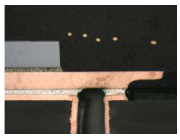
For inner and outer row of signal pins X-ray inspection should be performed looking for shorts, opens, or any abnormal solder geometries per IPC-A610. For the center thermal pad x-ray inspection should be performed looking for voids. Voiding should be limited to less than 50% of die attach pad (DAP) area to avoid thermal performance degradation during operation.

RESULTS BOARD ASSEMBLY DOE

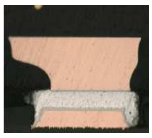
To insure customers achieve optimal performance when surface mounting MRQFN's, Texas Instruments conducted a series of DOE's utilizing several different SMT parameters including: stencil thickness, stencil opening, PCB pad size, SMT release mechanisms and reflow conditions. A total of 960 components were assembled during these tests with no solder related issues found using the conditions denoted below.

SMT Assembly DOE Parameters		
PCB	Outer row PAD	0.23 x 0.6 or 0.25 x 0.6 mm
	Inner row PAD	0.25 x 0.4 mm
	DAP	4.6 or 5.5 mm
	Thermal VIA on DAP	0.2 or 0.3 mm
	VIA	plug or non-plug
	Inner row traces routed between outer rows	trace width = 0.1 mm
Stencil	Outer row	0.23 x 0.55 or 0.25 x 0.6 mm
	Inner Row	0.25 x 0.38 or 0.25 x 0.4 mm
	DAP	3 x 3 or 2 x 2 pattern
	Thickness	0.1 or 0.125 mm
Reflow	Environment	Air or N2
SMT	Release mechanism	force ≤ 3N or
		component thickness + .05mm

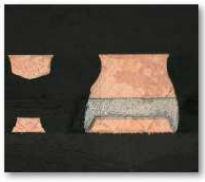
Photographic Cross Section Examples



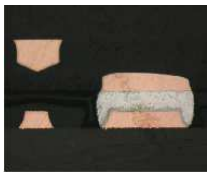
Thermal Via



Inner Row Length



Pin Outer Row



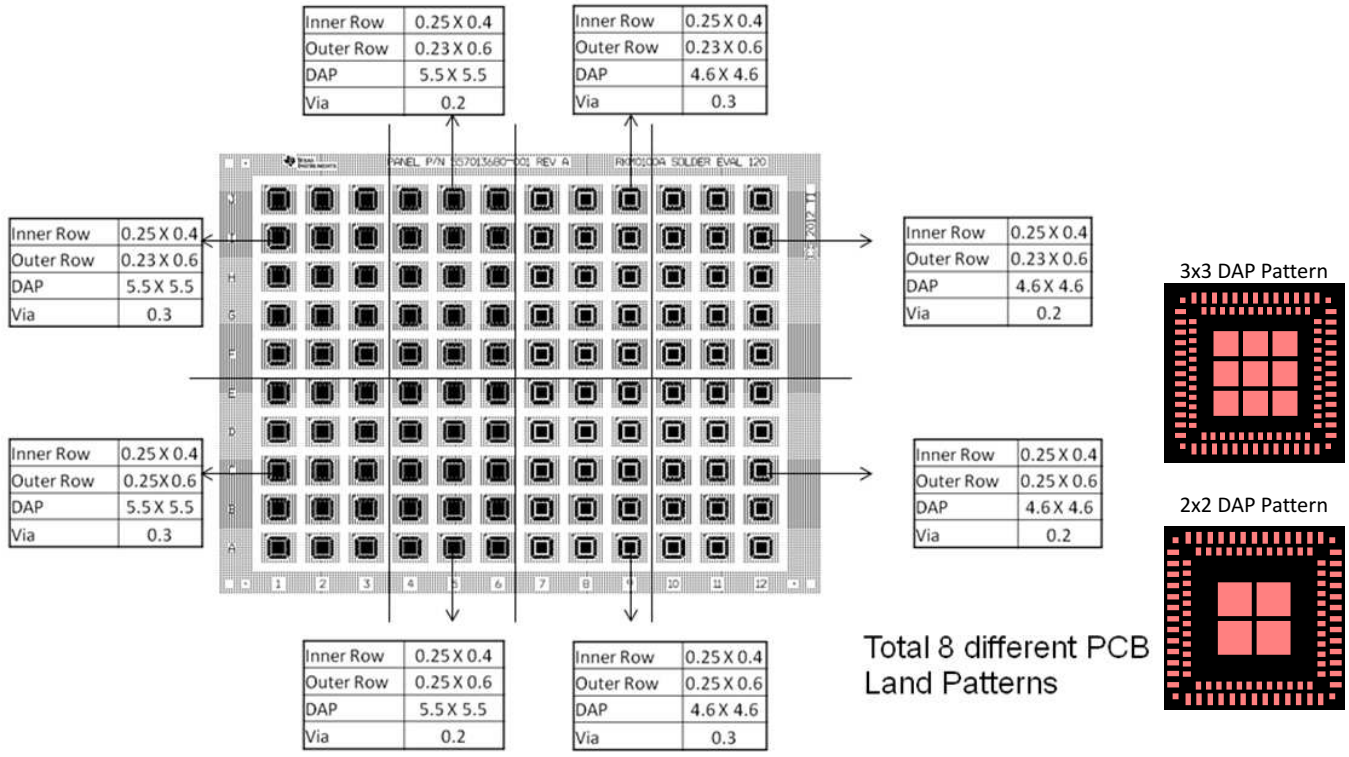
Pin Inner Row

Equipment and Settings

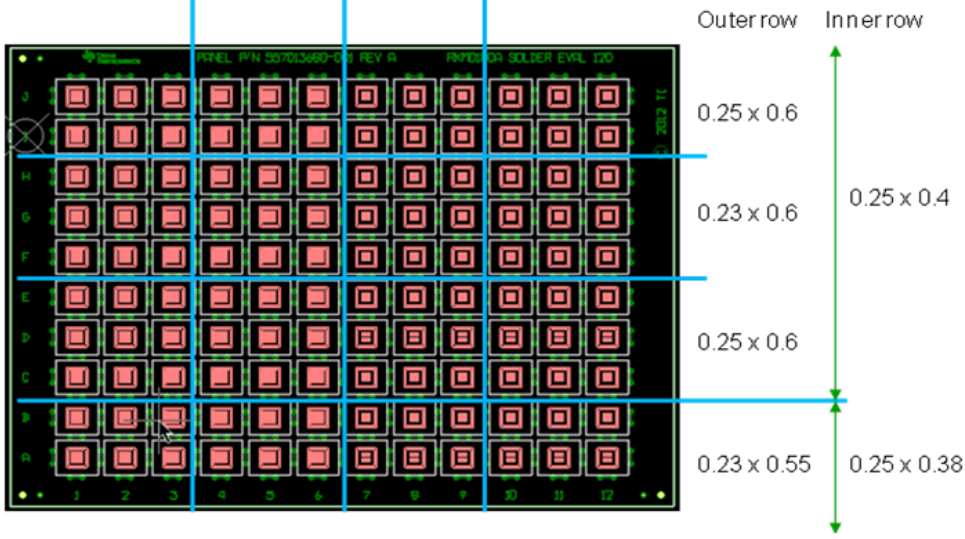
Solder Paste & Printer

- Model: MPM Ultra Print 3000 Series
- Paste: Senju M705-GRN-360-KV
- SAC305 Type 3
- Speed : 0.8 in/sec (20.32mm/sec)
- Pressure : 22 lb (97.86N)
- Separation : 0.13 in/sec SMT Equipment (3.3mm/sec)
- Universal GSM2 4688A
- Reflow Model : BT
- International: 10 zones
- X-ray for screen print and placement verification

PCB Layout



PCB	Outer row	0.23x0.6	0.25x0.6	
	Inner row	0.25x0.4		
	DAP	4.6	5.5	
	VIA on DAP	0.2	0.3	
Stencil	Outer row	0.23x0.55	0.23x0.6	0.25x0.6
	Inner row	0.25x0.38	0.25x0.4	



THERMAL CHARACTERISTICS

JEDEC 2S2P [1]	
	100-RKM
Die Size	5000µm x 5000µm
Theta-JA (deg C/W)	21.6

(1) Thermal values are modeled results. Model simulated a JEDEC test board (JEDEC51-5) utilizing a dual sided metal 10 x 10 thermal via array at 3watt power & 20°C ambient.

PACKAGE REPAIR GUIDELINES

MRQFN Repair Procedure

A package repair/rework station is strongly recommended for this process. (i.e. Air-Vac Engineering, Metcal, or Den-On Inst.)

Package Replacement Procedure:

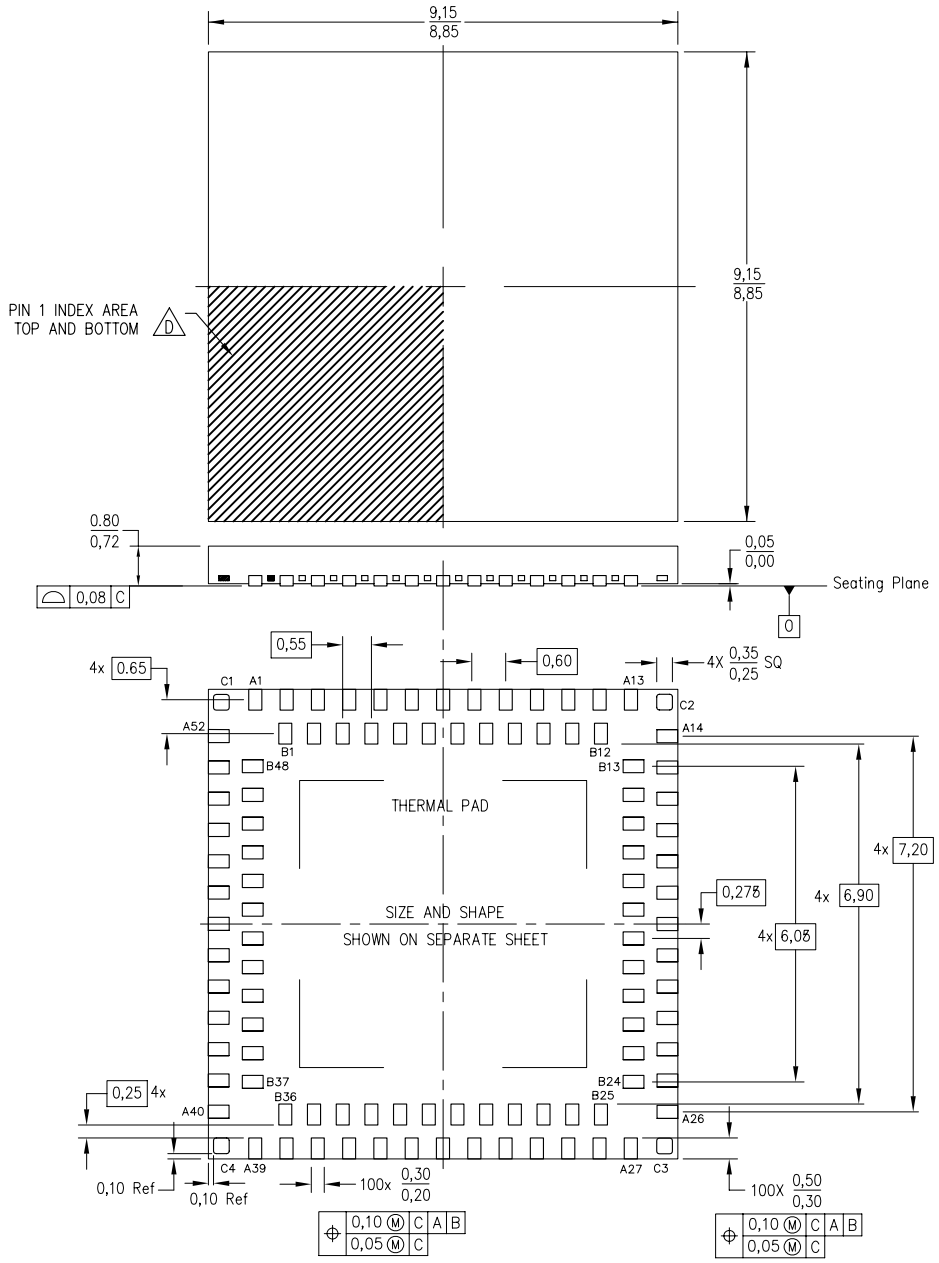
- Bake PWB & package at 125°C for 9 hours prior to rework.
- Board preheat (pre-bake is recommended)
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PWB lands
- Screening of solder paste either onto the part or onto the board
- Placement and reflow of new component
- Inspection of solder joints

MRQFN Repair Procedure Notes:

- Reuse of a removed package is not recommended.
- Use a new package for the repair process. The new package should be kept dry and should not exceed stated floor life after dry pack has been opened. If package has exceeded the floor life, re-bake(2) for 9 hours at 125ºC. Only re-bake a package a maximum of 3 times.
- In space restricted areas where printing paste via stencil may not possible, options of pre-bumping package or paste dispensing may be alternatives.
- Because leads are not visible from top side, the use of a split beam optical system is recommended for package alignment.
- A no clean solder is recommended for SMT rework due to difficulty in cleaning underneath mounted components.

(2) Care should be taken to insure all components on PWB can withstand the bake out temperature used

100 Pin MRQFN Package Drawing



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) staggered multi–row package configuration.
D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

See Texas Instruments Inc web site (http://www.ti.com) for the latest information on 100-RKM (MRQFN) package and product data sheet to confirm size of exposed die pad for specific applications.

QUESTIONS AND ANSWERS

Q. Is package rework possible? Are tools available?

A. Yes, rework is possible, and there are several semi-automatic SMT rework machines and profiles available. However, TI does not guarantee the reliability of re-used packages. It is best to discard and replace any package that fails test.

Q. What alignment accuracy is possible?

A. Alignment accuracy for the 0.60 / 0.55 mm pitch package is dependent upon board level pad tolerance, placement accuracy, and lead position tolerance. Nominal lead position tolerances are specified at ±50 microns. These packages are somewhat self aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q. What size land pad for these packages should I design on my board?

A. Pad size and stencil aperture design is the key to optimal assembly yields. Texas Instruments strongly recommends following the guidance within this document and should reference the device datasheet for specific stencil and land pattern examples.

Q. Can the solder joints be inspected after reflow?

A. Many customers are achieving satisfactory results during process setup using X-ray to aid in inspection.

Q. Is TI developing a lead-free/Green/ RoHS compliant version of MRQFN?

A. Yes, Texas Instruments has developed MRQFN's with an external plating finish that is Pb-Free and using no Antimony nor Bismuth within its construction in order to comply with lead-free / RoHS environmental policies. Check with your local TI Field Sales representative for sample availability.

Q. How do the board assembly yields of MRQFNs compare to QFPs?

A. Many customers are initially concerned about assembly yields. However, once they had MRQFN in production, most of them report improved process yields compared to QFPs. This is due to the elimination of bent and misoriented leads typically found with QFPs and the ability of these packages to self-align during reflow.

Q. What are the time requirements for floor life on these packages?

A. Moisture absorption is a significant factor in popcorn type defects during reflow. Since this package is to be classified as moisture level 3, the 1st and 2nd reflow must be completed within a week (168 hours) after opening the moisture barrier bag. If this timeframe cannot be met, it is highly recommenced to bake the packages at 125C for 9 hours before using.

Q. Can customers mount MRQFN packages on the bottom side of the PCB board?

A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st (a convection profile is recommended in this bulletin).

Q. What factors can increase MRQFN assembly yields?

A. TI recommends the following Quality factors to be considered:

- Solder Paste Quality - Uniform viscosity, free from foreign materials, and processed before drying out per solder paste vendors recommendations.
- PCB Quality - Clean, flat, plated or coated solder land area. Attachment surface must be clean and free of solder mask residue.
- Placement Accuracy - MRQFN packages self-center as long as a major portion (more than 50 percent) of the lead is in contact with the solder paste covered land area on the board.
- Solder Reflow Profile - A reflow profile must be developed for each PCB type using various MRQFN packages within the solder paste manufacturers recommendations.
- Solder Volume is important to ensure optimum contact of all intended solder connections.
- Excess amount of solder paste on the thermal pad during customer's board assembly may contribute to opens while excessive paste on the periphery leads may cause shorts.

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?

A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:

- Solid ground and power planes can be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.
- Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
- Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.

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