16-Bit Widebus™ Logic Families in 56-Ball, 0.65-mm Pitch, Very Thin Fine-Pitch BGA (VFBGA) Packages

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ABSTRACT

TI's 56-ball MicroStar Jr.™ package, registered under JEDEC MO-225, has demonstrated through modeling and experimentation that it is an optimal solution for reducing inductance and capacitance, improving thermal performance, and minimizing board area usage in integrated bus functions. Multiple functions released in the 56-ball MicroStar Jr.™ package have superior performance characteristics, compared to the same functions in 48-pin and 56-pin TSSOP and TVSOP packages.

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1 Introduction

As system and circuit complexity increases, and competitive pressures force the reduction of system prices, the requirement for cost-effective bus-interface technology creates the necessity for new solutions to system needs. Today, the major challenge to the digital-processing industry is the reduction of overall system costs as complexity and functionality increase. These marketplace forces have resulted in circuit integration and board miniaturization becoming a necessary trend. To address these rapidly evolving customer requirements, TI has defined a very thin fine-pitch BGA (VFBGA) package solution, known as the MicroStar Jr.™ package, to best serve customers' needs. Modeling and experimentation show that the MicroStar Jr. package is an optimal solution for reducing inductance and capacitance, improving thermal performance, and minimizing board area in support of integrated bus functions. Our objective is to provide significant improvements over existing packages, as well as cost savings to the OEM manufacturing process.

The purpose of this document is to introduce our first VFBGA solution, the 56-ball MicroStar Jr. package. Thirty-one devices in the 56-ball MicroStar Jr. package have been released to production. Additional products will be released, depending on market interest and customer demand. Both 48-pin and 56-pin functions have been released in the 56-ball MicroStar Jr. package. Functions in both pin counts have identical physical dimensions, but differ only by pin-to-ball assignment and substrate design, allowing the no-connects on the 48-pin functions to serve as an enhancement to board-level reliability.

The definition of the 56-ball VFBGA package is discussed in this application report. The definition of the MicroStar Jr. package in terms of standardization, both physical and mechanical, was developed by TI to provide the industry with compatible package solutions. The products released to date are listed in Table 1, and include bus-hold options.

Table 1. 56-Ball MicroStar Jr.™ Package Releases To Date

FAMILY		RELEASED FUNCTIONS
ALVC	Advanced low-voltage CMOS technology	16244, 16834, 16835, 16245, 16269, 16373, 16374, 16501, 16835
ALVT	Advanced low-voltage BiCMOS technology	16244, 16373, 16374
AVC	Advanced very low-voltage CMOS logic	16244, 16373, 16374
CBT	Crossbar technology	16211, 16212
LVC	Low-voltage CMOS technology	16244, 16245, 16373, 16374, 16543
LVT	Low-voltage BiCMOS technology	16244, 16245, 16373, 16374

2 Application Examples

2.1 Industry Requirements

The requirement to reduce board area usage necessitates a package solution that integrates logic and addresses improved electrical and thermal characteristics of the package. The selection of the 56-ball MicroStar Jr. package addresses these issues with improved performance and standardized pinouts. In 1999, an initial study of OEMs and worldwide subcontractors revealed that customers desired BGA solutions with pin 1 identified on both top and bottom sides, a pinout with ground and V_{CC} balls located on the inside of the matrix, and signal balls at peripheral areas of the package. MicroStar Jr. packages provide this with single-layer routing for all pins. TI has found that a 0.65-mm pitch and 0.117-mm (4.6-mil) trace width/spacing and a 0.381-mm finished via (15 mil) is both desired by OEMs and is feasible to manufacture. Via technology has progressed to the point that a 10-mil drill is economical technology for 1.5748-mm (62-mil) boards, and micro-via technology employing lasers has reduced costs for vias of 0.2032-mm (8-mil) diameter and less. More recently, it has been established that current technology has progressed even further with respect to trace width and spacing. Many offshore printed circuit board (PCB) manufacturing companies currently produce 0.0559-mm (2.2-mil) boards with via-in-pad interconnect. However, this capability is more expensive and must be balanced with production volumes and payback considerations. Because of these reduced-pitch efforts, the 0.117-mm (4.6-mil) capabilities have experienced increased yields through similar process and material innovations, and have become even more common. Informal discussions with United States PCB manufacturers reveal that the majority of the domestic industry now has process capabilities down to the 0.107-mm (4.4-mil) level. The percentage is even higher in the Asian market. By not imposing unrealistic requirements on PCB vendors, we have determined that the 0.65-mm pitch is the optimal choice at this time, given current technology and raw board yields.

The MicroStar Jr. package offered by TI supports customer requirements and enables easier, more economical PCB design/layout, along with improved solder-joint reliability based on life cycle studies, all while reducing consumption of valuable board area. Experiments and modeling also have shown a 3× improvement in board-level reliability over land grid array (LGA) packages due to the increased seating height. The VFBGA also provides significant improvements in parasitic capacitance and inductance compared to 48-pin and 56-pin TSSOP and TVSOP packages. Improved thermal performance and an overall height of less than 1 mm makes the MicroStar Jr. package ideal for height-constrained applications such as PCMCIA. A more detailed package comparison is provided in the other subsections of this application report.

2.2 Customer Requirements

Each customer has unique requirements; however, there are common issues across the industry to be addressed, and TI's goal was to provide a targeted solution to these needs. Within the personal computer (PC) industry, the trend is to integrate as much logic as possible into smaller packages to save space on motherboards and peripheral cards. Due to space constraints, PC cards require dense integration and small footprints, with improved electrical and thermal performance. Commonality of package types for clocks, registers, and for memory chips on dual inline memory modules (DIMMs) can be achieved by using the MicroStar Jr. package, thus creating cost-effective and common manufacturing processes for OEMs. In the telecommunications industry, base stations are becoming small and ubiquitous, requiring the repackaging of many circuits into denser boards. Also, within the telecommunications industry, new, complex, and smaller equipment must interface with legacy systems to provide cost-effective upgrade solutions to existing capabilities.

2.3 Comparison of Alternative Solutions

Footprint areas for the 56-ball MicroStar Jr. packages show space savings up to 72% compared to the 56-pin TSSOP, and 56% compared to the very thin small-outline package (TVSOP). Table 2 provides a comparison of physical dimensions and area savings of the 56-ball MicroStar Jr. package to alternative packages.

Table 2. Area Savings From 56-Ball MicroStar Jr.™ Package

PIN COUNT	PACKAGE TYPE	PITCH (mm)	PACKAGE DIMENSION (mm)	FOOTPRINT (mm^2)	MAXIMUM HEIGHT (mm)	AREA SAVINGS (%)
56	MicroStar Jr.	0.65	4.5×7	31.5	1.0	–
48	TVSOP	0.4	6.4×9.7	62.1	1.2	49.3
48	TSSOP	0.5	8.1×12.5	101.3	1.2	68.9
56	TVSOP	0.4	6.4×11.3	72.3	1.2	56.4
56	TSSOP	0.5	8.1×14.0	113.4	1.2	72.2

The MicroStar Jr. package offers significant area savings over alternative packaging technologies available in today's market, as well as superior area/bit ratios less than 2 mm^2/bit. Weight savings is 2× to 4× (see Table 3).

Table 3. Comparison of Area/Bit Ratios and Weights

PIN COUNT	PACKAGE TYPE	FOOTPRINT (mm^2)	AREA/BIT (mm^2)	WEIGHT (g)
56	MicroStar Jr.	31.5	1.9688	0.057
48	TVSOP	62.1	3.8813	0.118
48	TSSOP	101.3	6.3313	0.191
56	TVSOP	72.3	4.5188	0.135
56	TSSOP	113.4	7.0875	0.235

3 Physical Description

3.1 Package Characteristics

Figure 1 shows a cross-section view of the MicroStar Jr. package.

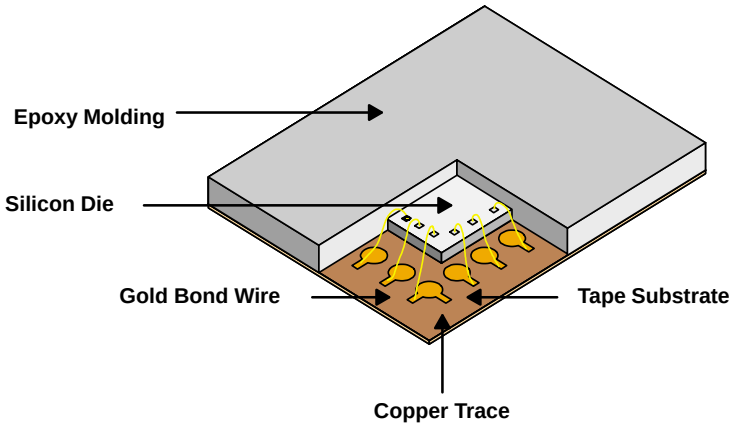


Figure 1. MicroStar Jr.™ Package Cross Section

Table 4 summarizes the package attributes of the 56-ball MicroStar Jr. package.

Table 4. MicroStar Jr.™ Package Attributes

ATTRIBUTE	MicroStar Jr.
Ball count	56
Ball configuration (rows, columns)	6 x 10, depopulated
Ball-to-ball pitch (mm)	0.65
Square/rectangular	Rectangular
Ball diameter (mm)	0.35 minimum
Package body width (mm)	4.5
Package body length (mm)	7
Package thickness (total height, mm)	1 maximum
Package weight (mg)	56.9
Shipping media, tape and reel (units/reel)	1000
Desiccant packing	Level 2A†

† Package qualified at JEDEC Level 2 moisture condition, 220°C reflow

3.1.1 MicroStar Jr.™ Package Dimensions

Figures 2 and 3 show the physical dimensions of the 56-ball MicroStar Jr. package. The missing via hole identifies the pin A1 quadrant.

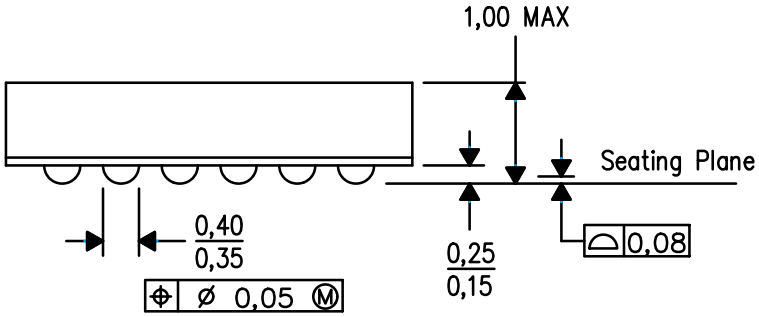


Figure 2. 56-Ball MicroStar Jr.™ Package Profile

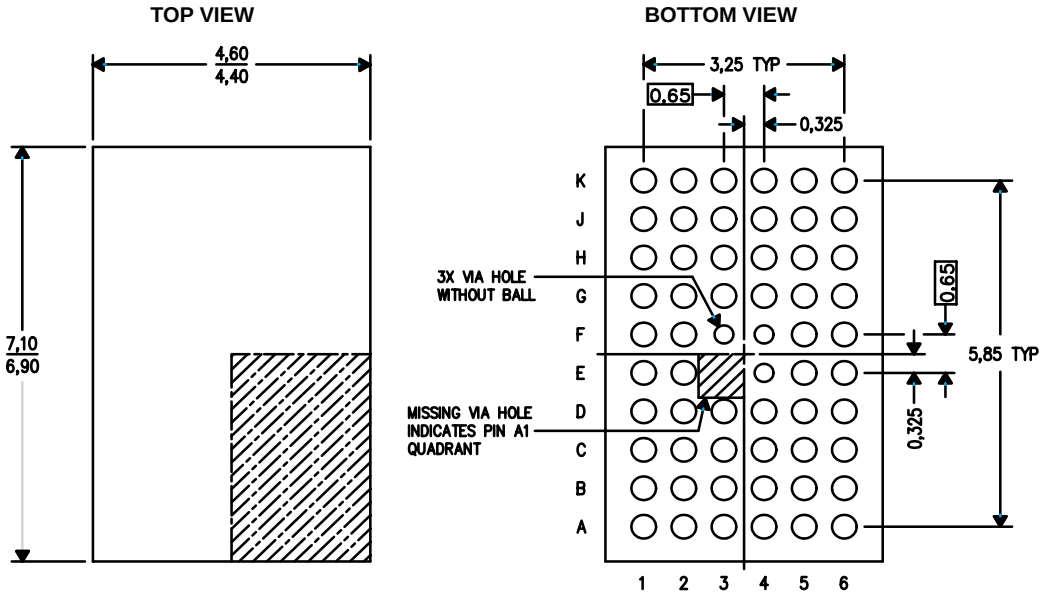


Figure 3. 56-Ball MicroStar Jr.™ Package, Top and Bottom Views

3.1.2 MicroStar Jr.™ Package Pinouts

The pinout configuration in Figure 4 adopts the same naming convention applied in the industry to logic devices in 48-pin TSSOP, TVSOP, and SSOP packages.

	A	B	C	D	E	F	G	H	J	K
6	A48‡	A46	A43	A40	A37	A36	A33	A30	A27	A25‡
5	NC	A47	A44	A41	A38	A35	A32	A29	A26	NC
4	NC	A45§	A42†	A39§	NC	NC	A34§	A31†	A28§	NC
3	NC	A4§	A7†	A10§	NC	NC	A15§	A18†	A21§	NC
2	NC	A2	A5	A8	A11	A14	A17	A20	A23	NC
1	A1‡	A3	A6	A9	A12	A13	A16	A19	A22	A24‡

† = V_{CC}
‡ = Control
§ = Ground
NC = No Connection

Figure 4. 48-Pin Function Pin Assignment, Top View

The pinout configuration in Figure 5 adopts the same naming convention applied in the industry to logic devices in 56-pin TSSOP, TVSOP, and SSOP packages.

	A	B	C	D	E	F	G	H	J	K
6	A54‡	A51	A48	A45	A43	A42	A40	A37	A34	A31‡
5	A55‡	A52	A49	A47	A44	A41	A38	A36	A33	A30‡
4	A56‡	A53	A50†	A46§	NC	NC	A39§	†A35	A32§	A29‡
3	A1‡	A4	A7†	A11§	NC	NC	A18§	†A22	A25§	A28‡
2	A2‡	A5	A8	A10	A13	A16	A19	A21	A24	A27‡
1	A3‡	A6	A9	A12	A14	A15	A17	A20	A23	A26‡

† = V_{CC}
‡ = Control
§ = Ground
NC = No Connection

Figure 5. 56-Pin Function Pin Assignment, Top View

3.1.3 Package Reliability

The 56-ball MicroStar Jr. package was qualified at Joint Electronics Device Engineering Council (JEDEC) Moisture Level 2, and released at Level 2A. For optimum reliability, reflow(s) should be completed as soon as practical after removing components from dry pack; however, JEDEC Level 2A allows up to four weeks before baking is required (assuming ambient conditions of 30°C and 60% relative humidity).

Table 5 summarizes package reliability data obtained from qualification testing. The test chip was ALVCH16501, B die revision, 85 × 107 mils, preconditioned at JEDEC Level 2 [85°C and 60% relative humidity and three infrared (IR) reflows at 220°C].

Table 5. Package Reliability Qualification Results

RELIABILITY QUALIFICATION TEST		SAMPLE SIZE/FAILS		
		QUALIFICATION LOT 1	QUALIFICATION LOT 2	QUALIFICATION LOT 3
Steady-state life test (150°C, 300 hours)		39/0	39/0	39/0
Highly Accelerated Stress Test (HAST) (130°C and 85% relative humidity)		39/0	39/0	39/0
Temperature cycle (–65 to 150°C, 1000 hours)		77/0	77/0	77/0
Autoclave (121°C, 96 hours)		77/0	77/0	77/0
Solderability (8 hours steam age)		8/0	8/0	8/0
Flammability	UL	5/0	5/0	5/0
	IEC	5/0	5/0	5/0
Thermal shock (–65°C to 150°C, 1000 cycles)		26/0	26/0	26/0
X-ray		5/0	5/0	5/0
Physical dimensions		15/0	15/0	15/0
Manufacturability		Pass	Pass	Pass
High-temperature storage (150°C, 1000 hours)		45/0	45/0	45/0

Board Level Reliability (BLR) testing was conducted using a daisy-chained package soldered with eutectic solder on a nonsolder-mask defined (NSMD) single-sided, 0.7874-mm (31-mil) thick board with organic solder preservative (OSP) finished copper pads of 0.40-mm diameter. The temperature-cycling parameters were –40° to +125°C, with a 10-minute dwell at the extremes and 5-minute transition time. The sample population was tested to characteristic life, which is 63.2% of the samples experiencing a continuity failure. Table 6 summarizes the results.

Table 6. Board-Level Reliability Results

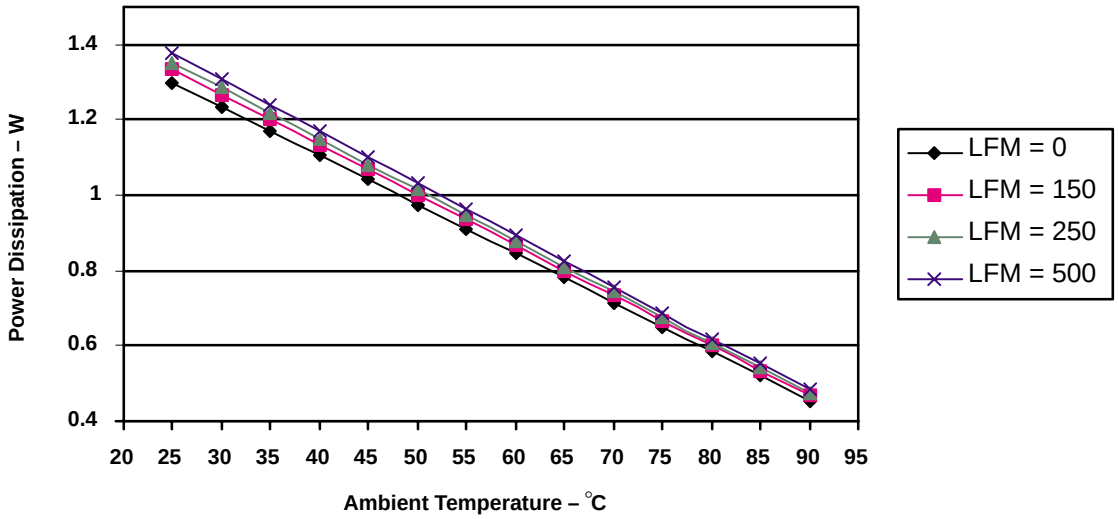
CYCLES TO FIRST FAILURE	CYCLES TO 1% POPULATION FAILURE	CYCLES TO 63.2% POPULATION FAILURE
1847	1808	2833

In Table 6, the cycles-to-1%-population-failure value is statistically derived from the failure distribution, while the cycles-to-first-failure value is an experimentally derived data point.

3.1.4 Power Dissipation

Because of its small size, convective cooling per unit area is more efficient with the 56-ball MicroStar Jr. package than for larger packages. However, conduction still is the dominant mode of transfer, with a minor contribution from radiation. In the conduction mode, the balls serve as the sink path to the PCB. The number and weight of the metal layers, plus component layout and proximity to other power sources have a significant effect on dissipation. Thermal performance is also significantly influenced by die size because conduction efficiency depends on the number of balls overlapped by the chip. However, PCB design has the largest effect, and models show that the introduction of thermal vias of 0.30-mm (12-mils) diameter at the ground balls can improve performance up to an additional 7% to 10% on multimetal-layered PCBs. Performance data was modeled using the JEDEC 1S2P test board with thermal conductivity of approximately 18 W/mK. It must be emphasized that system-level performance is extremely dependent upon PCB design, component layout and proximity to other power sources, airflow, PCB orientation, and board-to-board spacing in the system's upper level assembly. Values for thermal impedance should be used only as guidelines for further system-level modeling, not as an indication of total system thermal performance.

Figures 6 through 8 compare the 56-ball MicroStar Jr. package thermal performance to alternative packages, and illustrate the effect of forced-air cooling on power dissipation, both with and without thermal vias (see Tables 7 and 8).

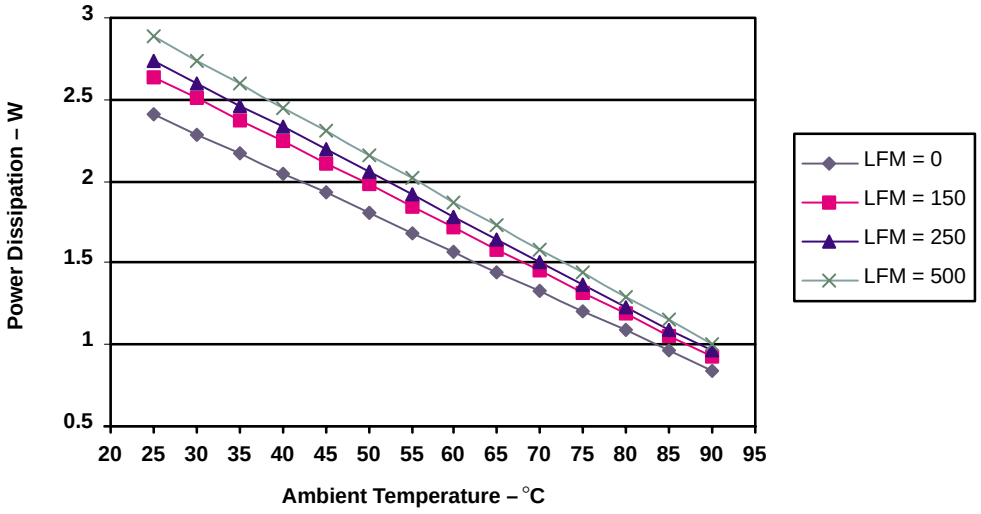


Note A: Power dissipation is calculated using a junction temperature of 125°C and die size = 2.2 mm × 5 mm.

Figure 6. MicroStar Jr.™ Package Thermal Comparisons on Multilayer JEDEC 1S2P Test Board, No Thermal Vias and Zero Airflow

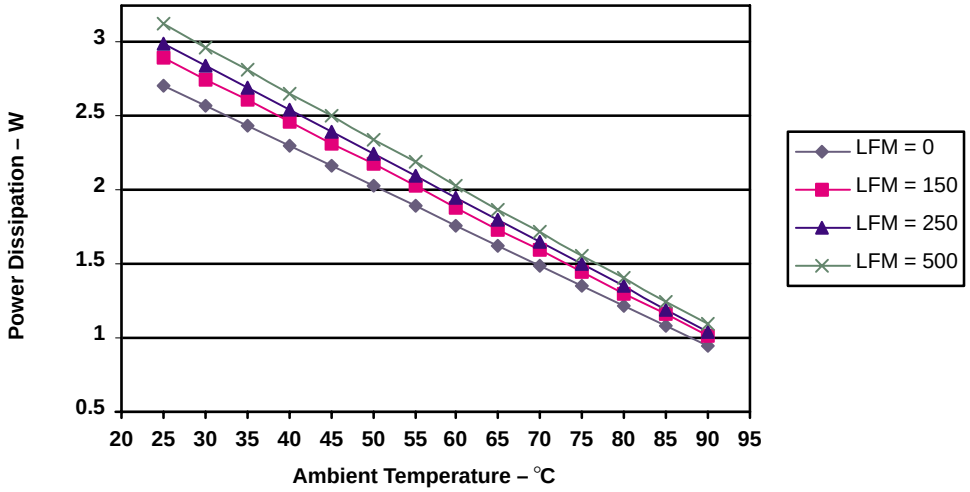
Table 7. 56-Ball (VFBGA) MicroStar Jr.™ Package Thermal Performance

	AIR VELOCITY (ft/min)			
	0	150	250	500
θ_{JA} (°C/W)	41.5	37.9	36.5	34.7
θ_{JC} (°C/W)	21.6			
θ_{JB} (°C/W)	10.0			



Note A: Power dissipation is calculated using a junction temperature of 125°C and die size = 2.2 mm × 5 mm.

Figure 7. MicroStar Jr.™ Package Thermal Performance on Multilayer JEDEC 1S2P Test Board, No Thermal Vias and Various Airflow Velocities



Note A: Power dissipation is calculated using a junction temperature of 125°C and thermal vias at ground pins D3, D4, G3, and G4.

Figure 8. Effect of Thermal Vias on MicroStar Jr.™ Package Thermal Performance Using a JEDEC 1S2P Test Board at Various Airflow Velocities

Table 8. Effect of Thermal Vias at Various Airflows

	AIR VELOCITY (ft/min)			
	0	150	250	500
θ_{JA} (°C/W) with vias	37	34.5	33.4	32
Via effectiveness	10.8%	9%	8.5%	7.8%

A comparison of the area-normalized thermal dissipation for TSSOP, TVSOP, and 56-ball MicroStar Jr. packages shows that the 56-ball VFBGA package at 25°C, with no thermal vias and zero airflow, exceeds the TVSOP package by 60% and exceeds the TSSOP package by 80% (see Figure 9).

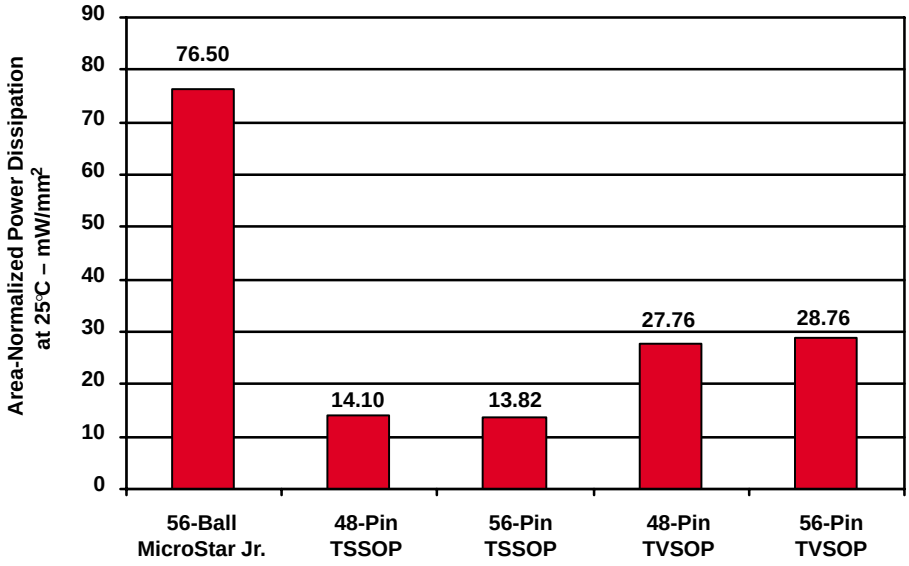


Figure 9. Area-Normalized Power Dissipation at 25°C Ambient Temperature Using a JEDEC 1S2P Test Board

3.2 Electrical Performance

3.2.1 Package Parasitics

Table 9 summarizes the parasitic inductance and capacitance characteristics of the 56-ball MicroStar Jr. package. Minimum, mean, and maximum values are given for all 56 balls in the package.

Table 9. Electrical Characteristics of the 56-Ball MicroStar Jr.™ Package

	56-PIN FUNCTIONS		48-PIN FUNCTIONS	
	L (nH)	C (pF)	L (nH)	C (pF)
Minimum	1.000	0.162	1.398	0.117
Mean	1.952	0.283	2.264	0.306
Maximum	3.191	0.434	2.722	0.404

Tables 10 and 11 summarize the differences between the 56-ball MicroStar Jr. package and the 48-pin and 56-pin TSSOP and TVSOP packages. The 56-ball MicroStar Jr. package offers 41% less inductance and 49% less capacitance than 56-pin TSSOP. Resistance values, which were virtually unchanged, are omitted.

Table 10. Comparison of 56-Ball MicroStar Jr.™ Package to 56-Pin Function Alternative Packaging

PACKAGE	INDUCTANCE (mh)	CAPACITANCE (pF)	%ΔL	%ΔC
56-Ball MicroStar Jr. package (56-pin function)	1.952	0.283		
56-pin TVSOP	2.945	0.391	33.72	27.62
56-pin TSSOP	3.324	0.564	41.28	49.82

Table 11. Comparison of 56-Ball MicroStar Jr.™ Package to 48-Pin Function Alternative Packaging

PACKAGE	INDUCTANCE (mh)	CAPACITANCE (pF)	%ΔL	%ΔC
56-Ball MicroStar Jr. package (48-pin function)	2.264	0.306		
48-pin TVSOP	3.013	0.371	24.86	17.52
48-pin TSSOP	3.019	0.507	25.01	39.64

3.2.2 Simultaneous-Switching Behavior

Figure 10 shows the simultaneous-switching measurement setup and the position of the outputs examined using the LVCH16244A device.

3.2.3 Simultaneous-Switching Procedure and Graphs

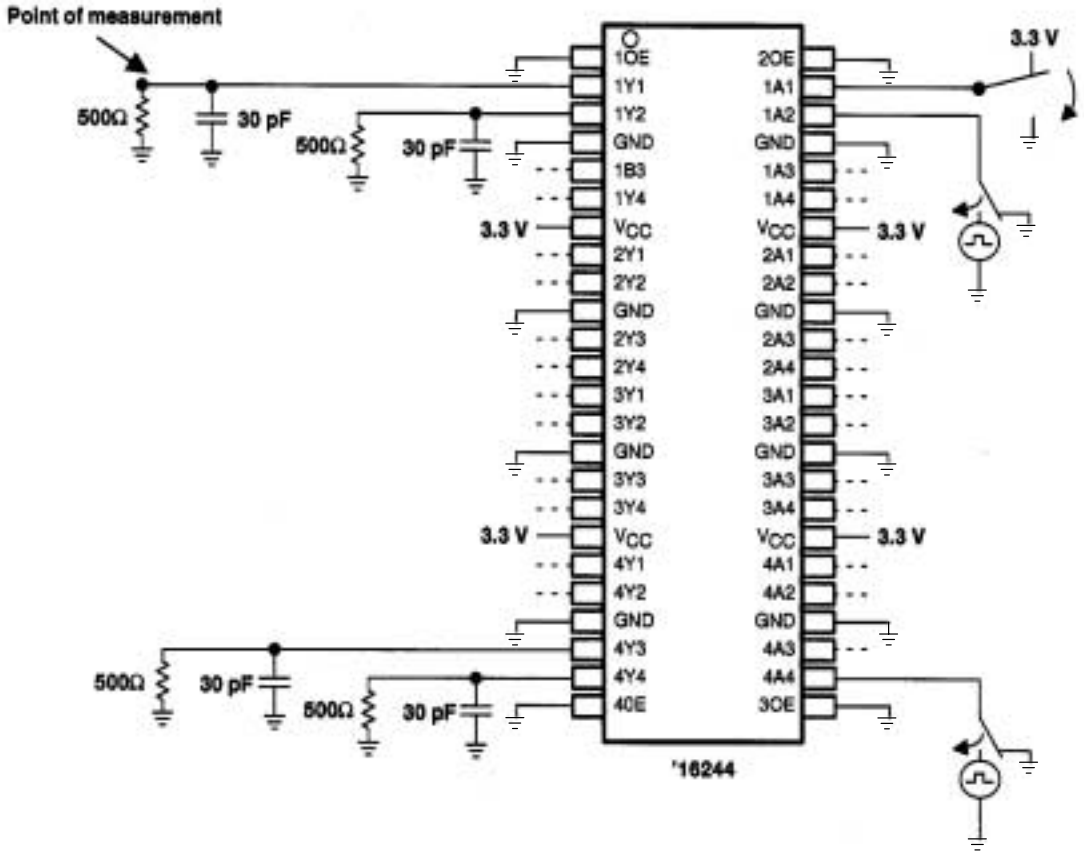


Figure 10. Simultaneous-Switching Measurement Setup

For this measurement procedure, one input is connected to a fixed low (L) state, or a high (H) state, while all other inputs are switched simultaneously. See Figure 10 for the test setup. The outputs of the connecting driver react to the changes in the various inputs with a certain delay, while the nonswitched output should maintain a constant low or high state.

However, three factors lead to a reaction by the nonconnected input:

- Crosstalk between neighboring pins
- A brief notch in the supply voltage, not measurable from the outside, caused by the inductance of the V_{CC} lead
- A brief increase in the grounding level, not measurable from the outside, caused by the ground lead

Figure 11 sets out the parameters and definitions of significance for this measurement procedure. Points on the curve are defined as:

PARAMETER		DEFINITION
V_{OHP} (voltage output high peak)	High bounce	Peak output voltage value during a static high at the nonswitched output
V_{OHV} (voltage output high valley)	High bounce	Minimum output voltage during a static high at the nonswitched output
V_{OLP} (voltage output low peak)	Ground bounce	Peak output voltage value during a static low at the nonswitched output
V_{OLV} (voltage output low valley)	Ground bounce	Minimum output voltage value during a static low at the nonswitched output
V_{IH} (voltage input high)	Threshold	Minimum input voltage value, ensuring a high output state
V_{IL} (voltage input low)	Threshold	Maximum input voltage value, ensuring a low output state

The critical parameters are V_{OLP} for the low static state and V_{OHV} for the high static state because their worst case switching thresholds exceed the V_{IL} maximum or V_{IH} minimum levels.

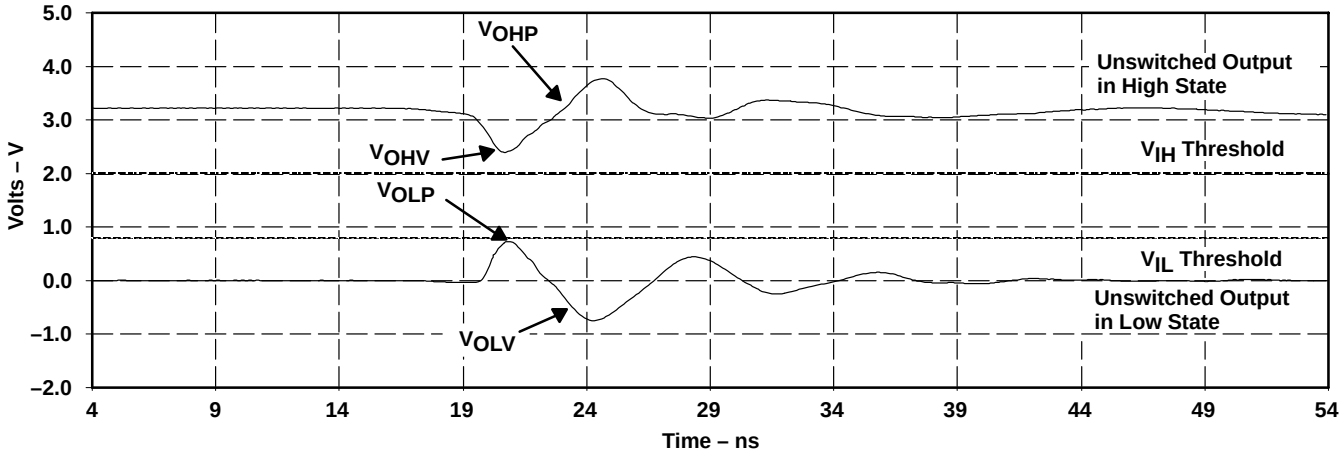


Figure 11. Simultaneous-Switching Parameters

The ground-bounce and high-bounce measurements for the simultaneous switching of several outputs are shown in Figures 12 through 19 for the 48-pin TVSOP, TSSOP, SSOP, and 56-ball VFBGA packages investigated for this application report.

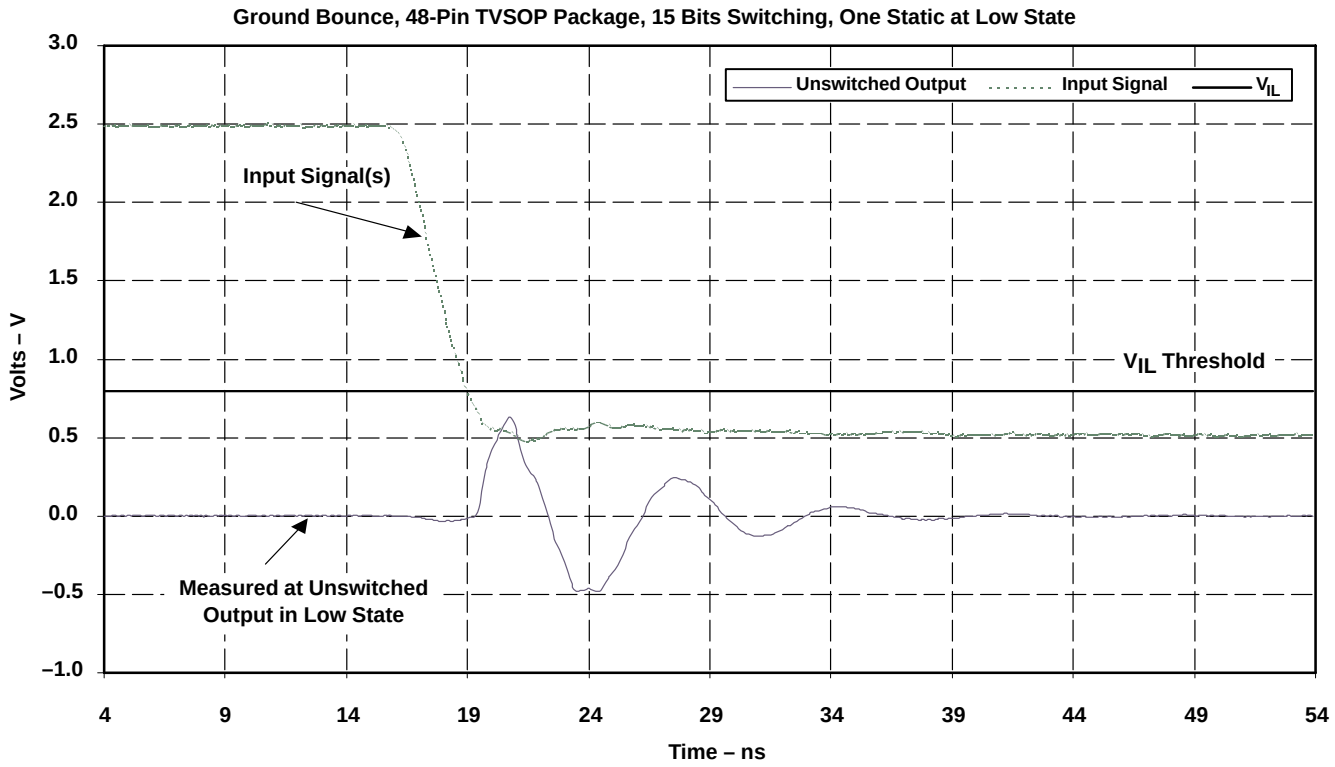


Figure 12. Measured Simultaneous-Switching Ground Bounce, 48-Pin TVSOP Package

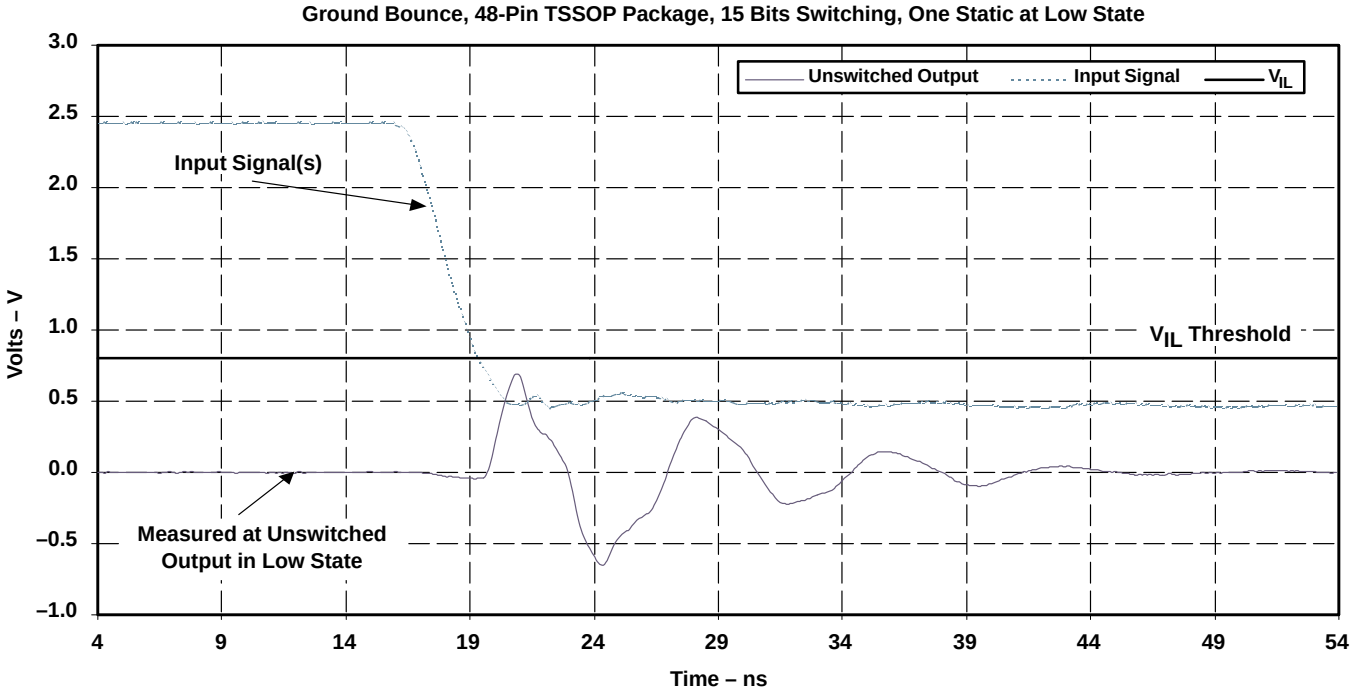


Figure 13. Measured Simultaneous-Switching Ground Bounce, 48-Pin TSSOP Package

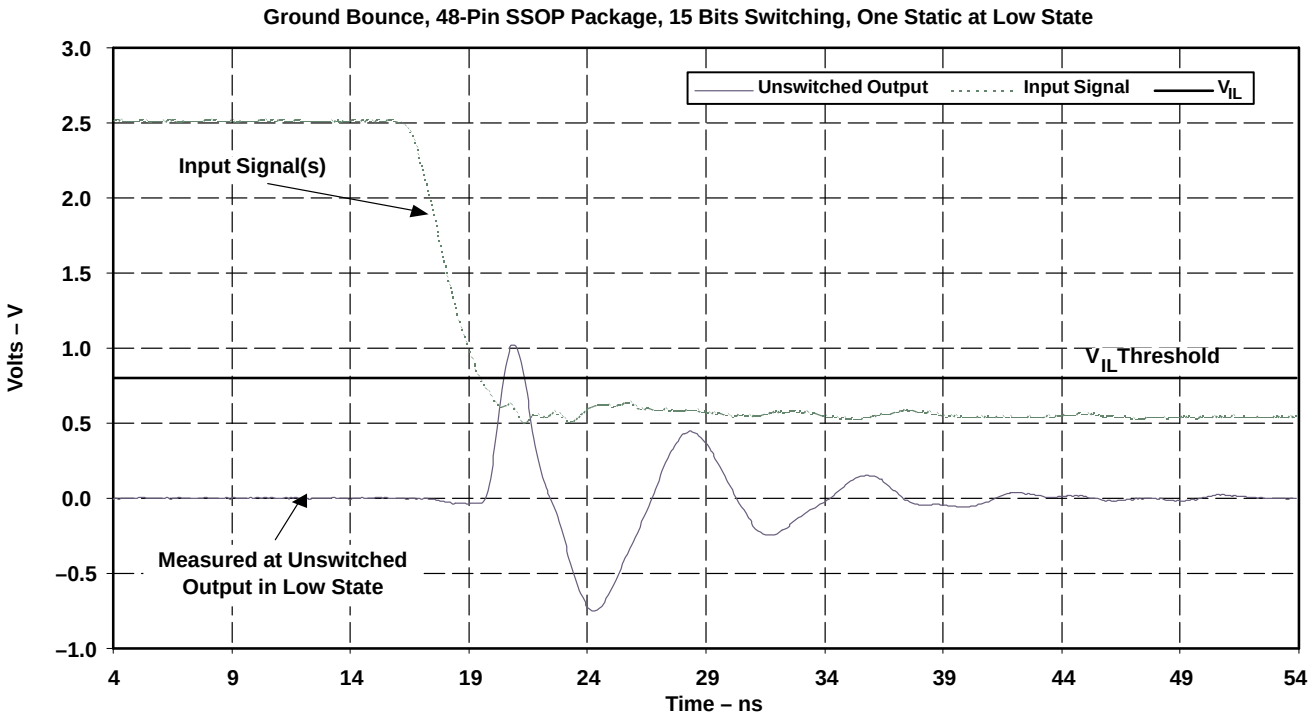


Figure 14. Measured Simultaneous-Switching Ground Bounce, 48-Pin SSOP Package

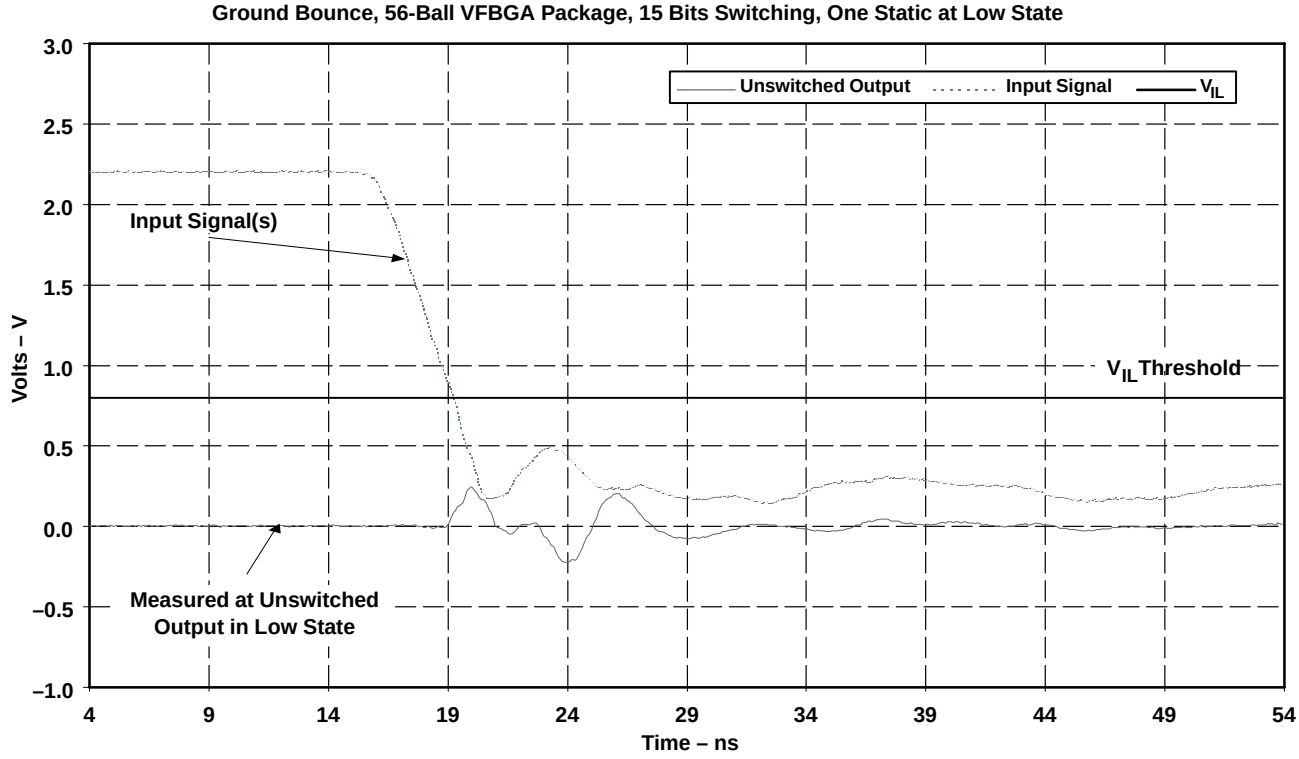


Figure 15. Measured Simultaneous-Switching Ground Bounce, 56-Ball VFBGA Package

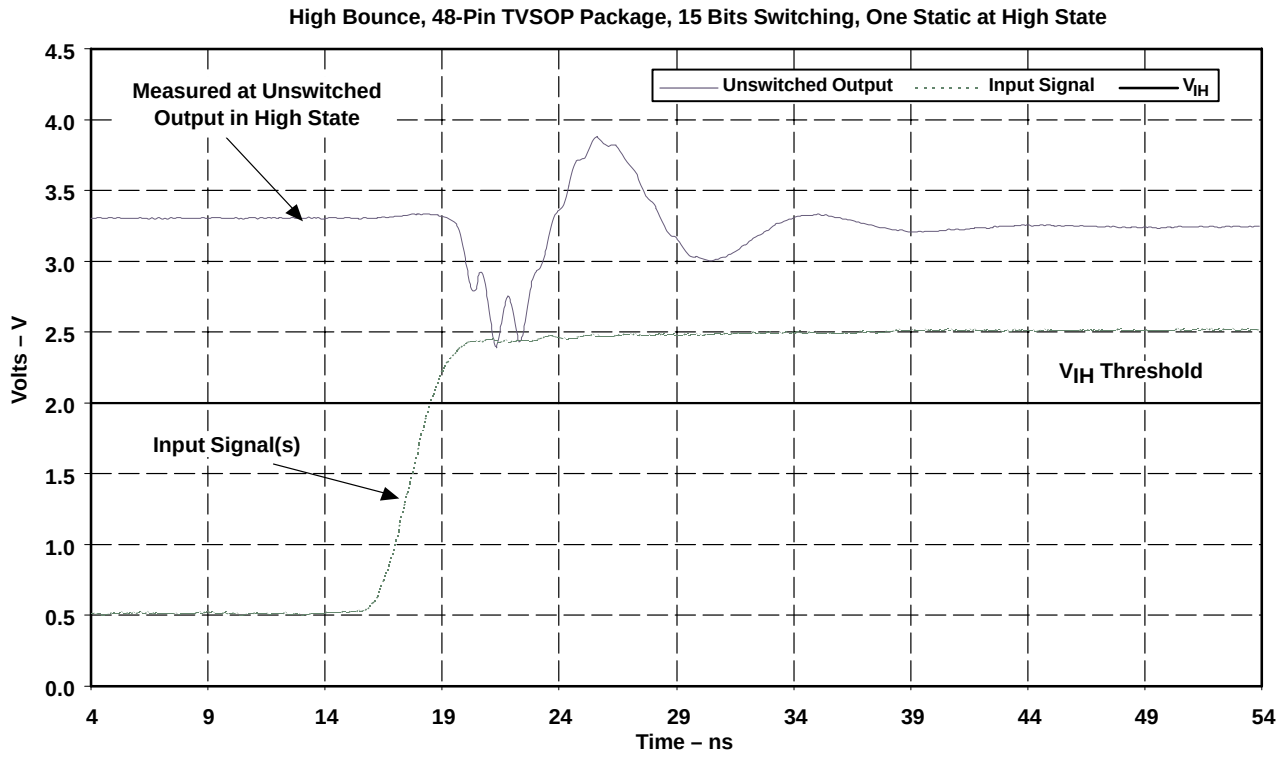


Figure 16. Measured Simultaneous-Switching High Bounce, 48-Pin TVSOP Package

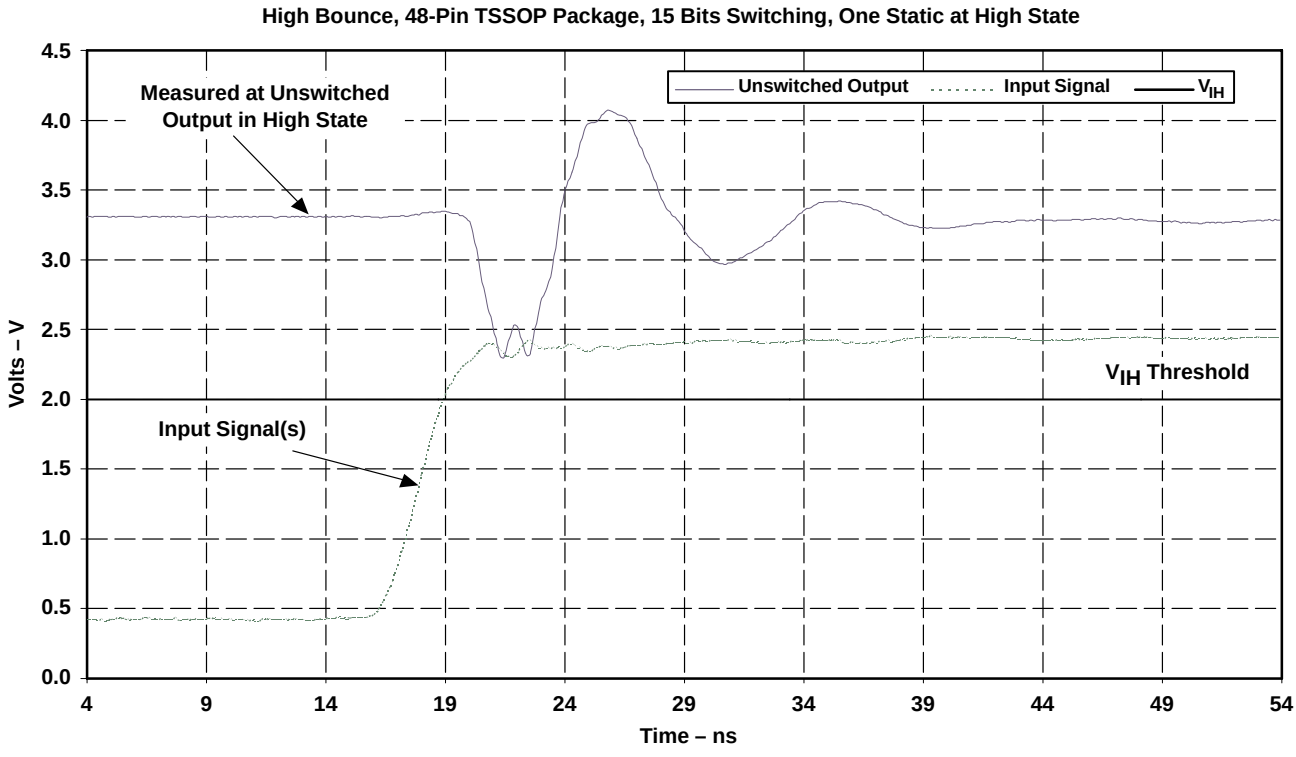


Figure 17. Measured Simultaneous-Switching High Bounce, 48-Pin TSSOP Package

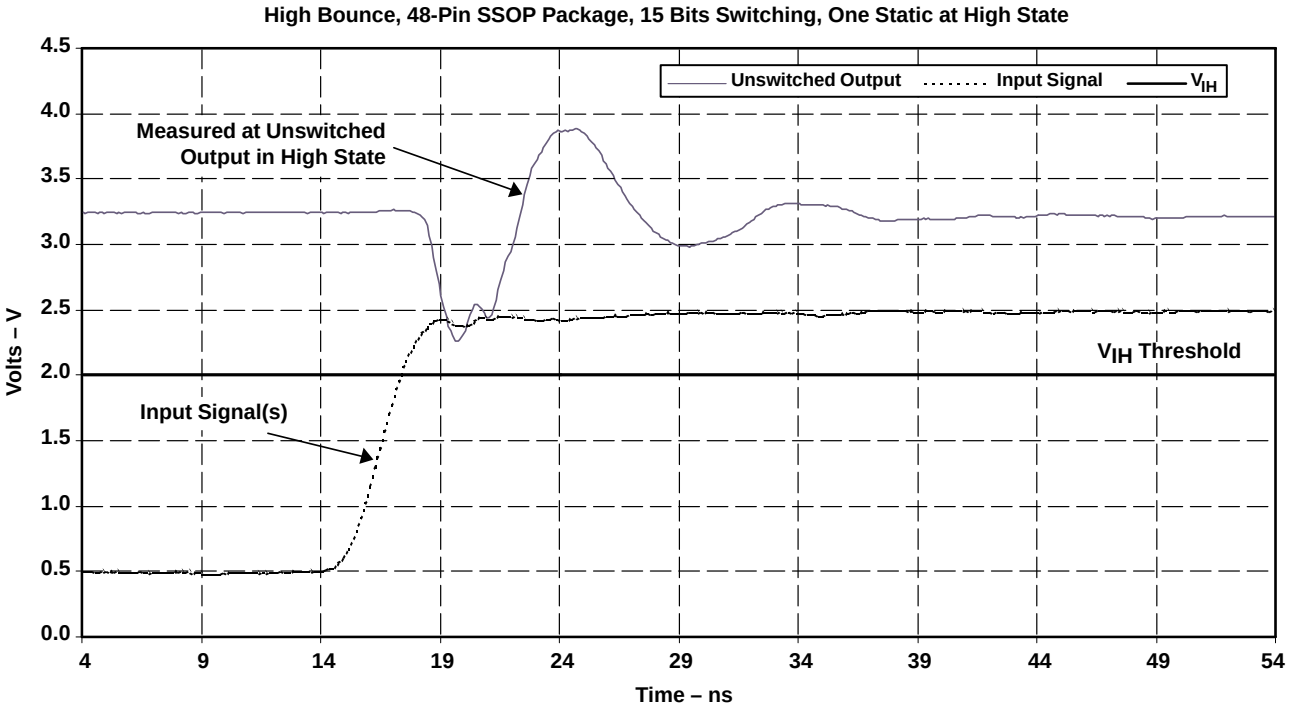


Figure 18. Measured Simultaneous-Switching High Bounce, 48-Pin SSOP Package

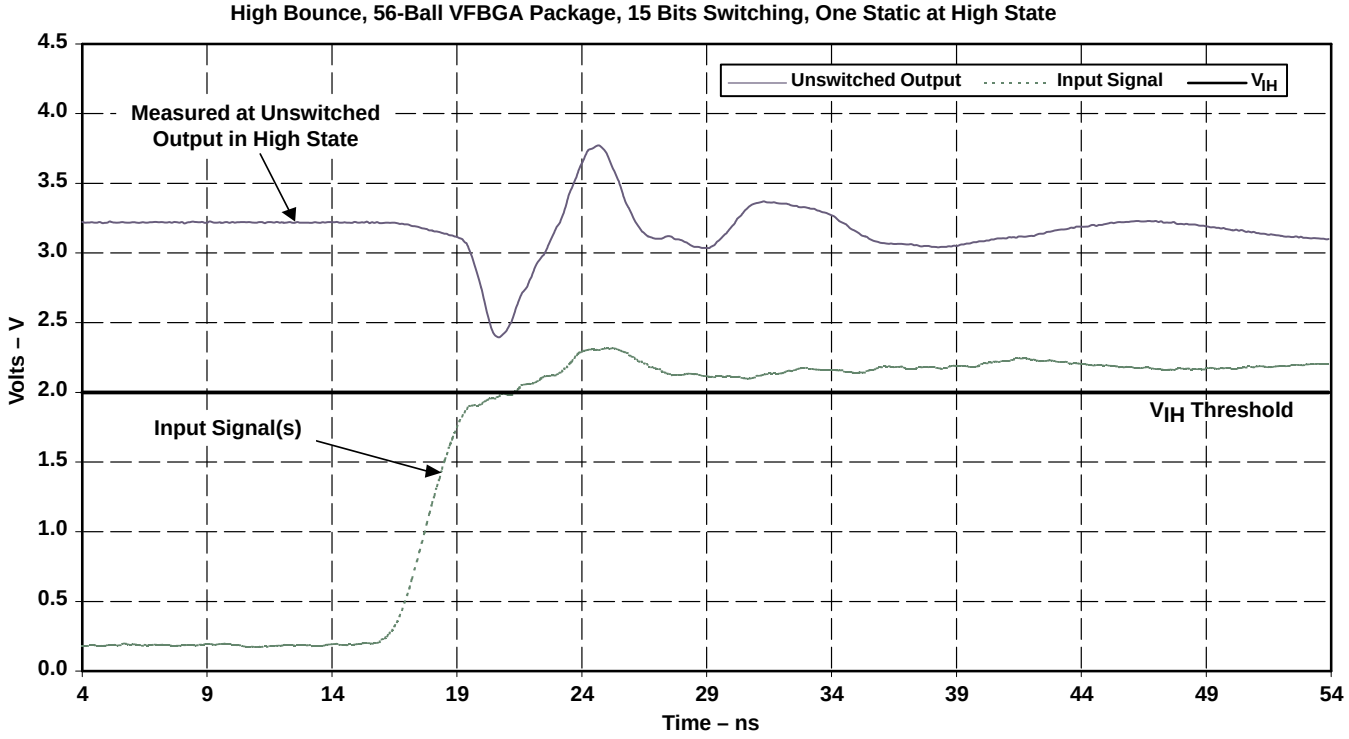


Figure 19. Measured Simultaneous-Switching High Bounce, 56-Ball VFBGA Package

Additional data was taken to show the results of the switching noise caused as the number of pins increased from 1 to 16. The resulting graphs are in Figures 20 through 23. Figures 20 and 21 show the V_{OL} graphs of both the V_{OLP} and V_{OLV} voltage levels as the number of output pins increases. Figures 22 and 23 show the V_{OH} graphs of both the V_{OHP} and V_{OHV} voltage levels as the number of output pins increases.

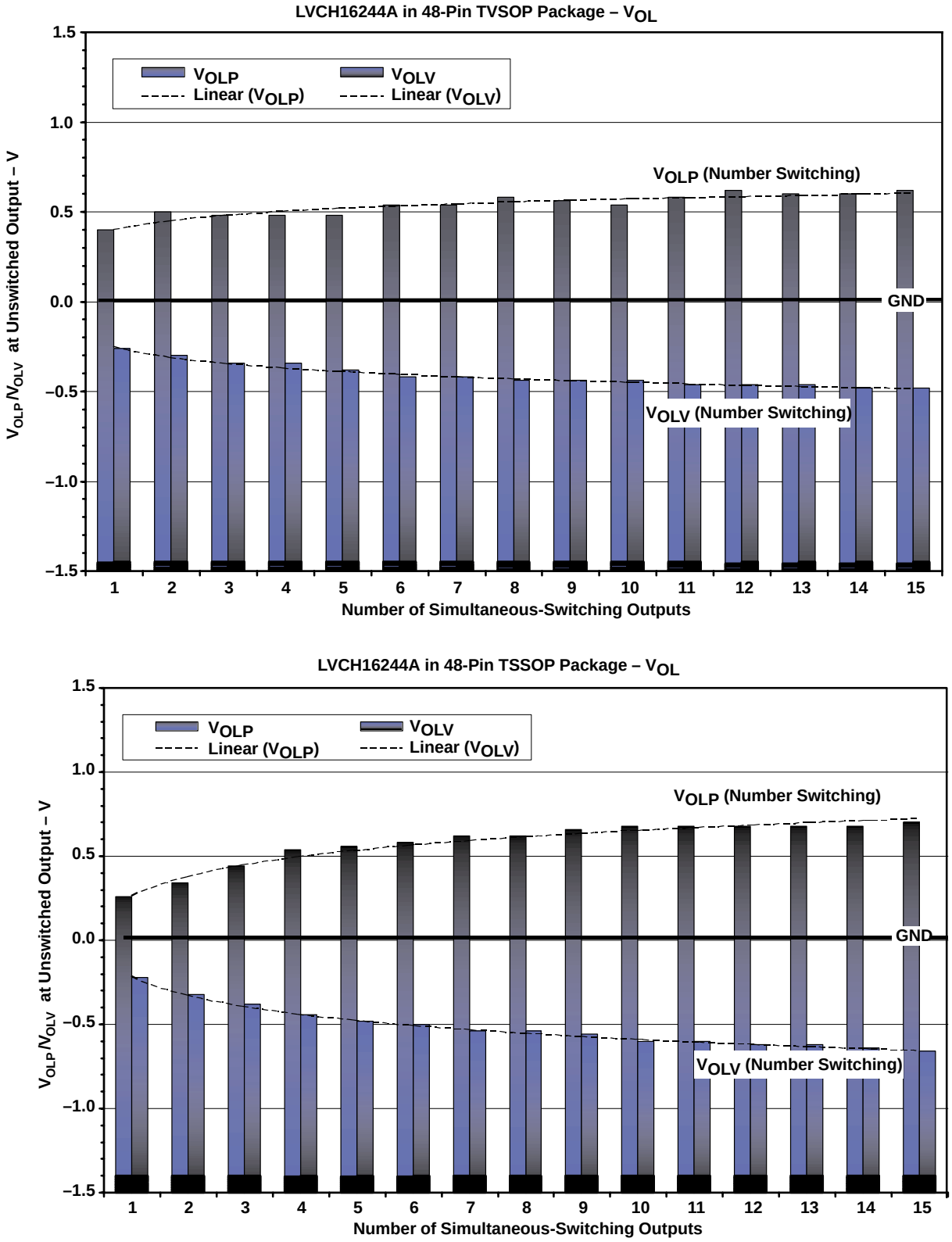


Figure 20. Simultaneous-Switching Ground Bounce, 48-Pin TVSOP (top), 48-Pin TSSOP (bottom)

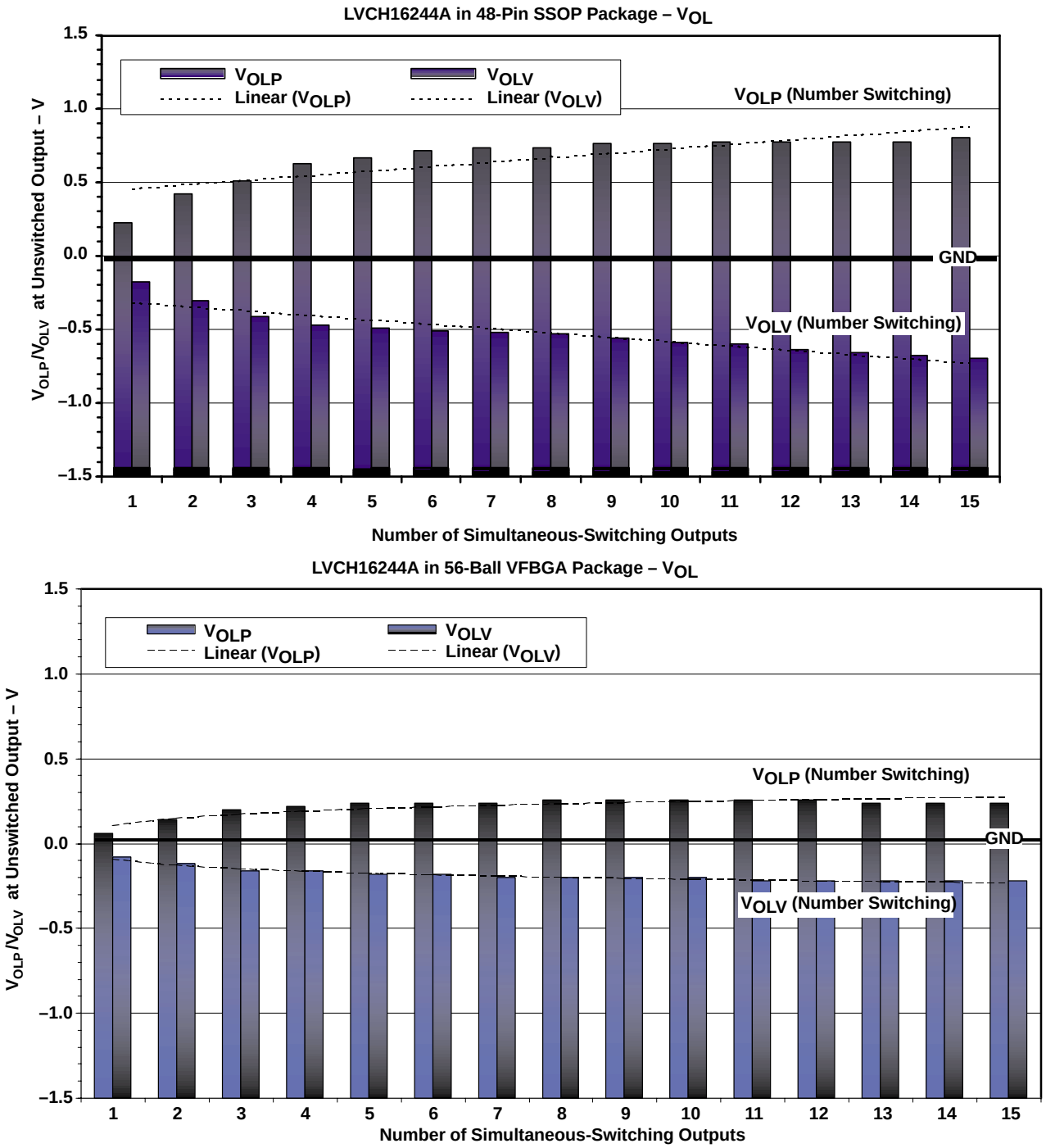


Figure 21. Simultaneous-Switching Ground Bounce, 48-Pin SSOP (top), 56-Ball VFBGA (bottom)

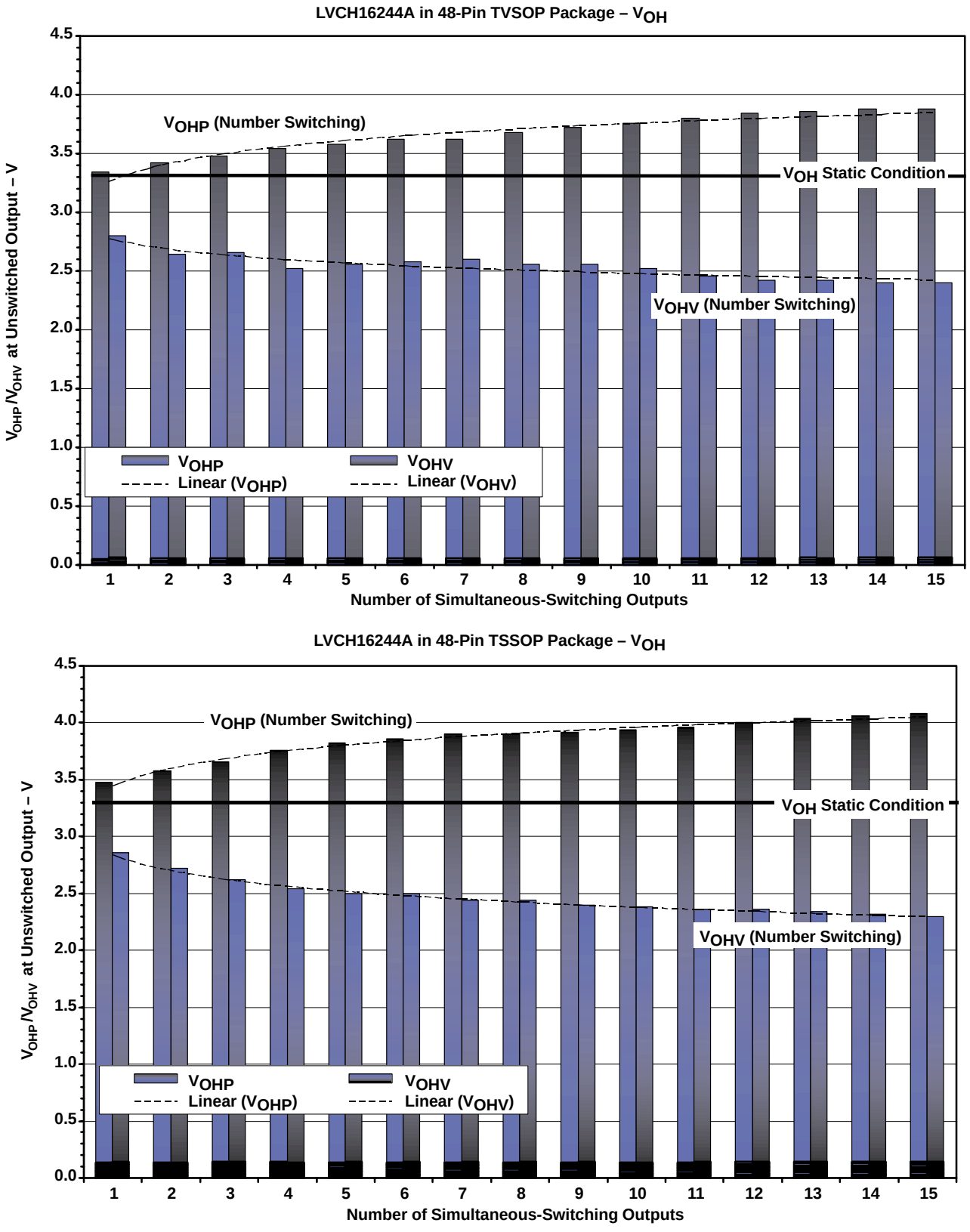


Figure 22. Simultaneous-Switching High Bounce, 48-Pin TVSOP (top), 48-Pin TSSOP (bottom)

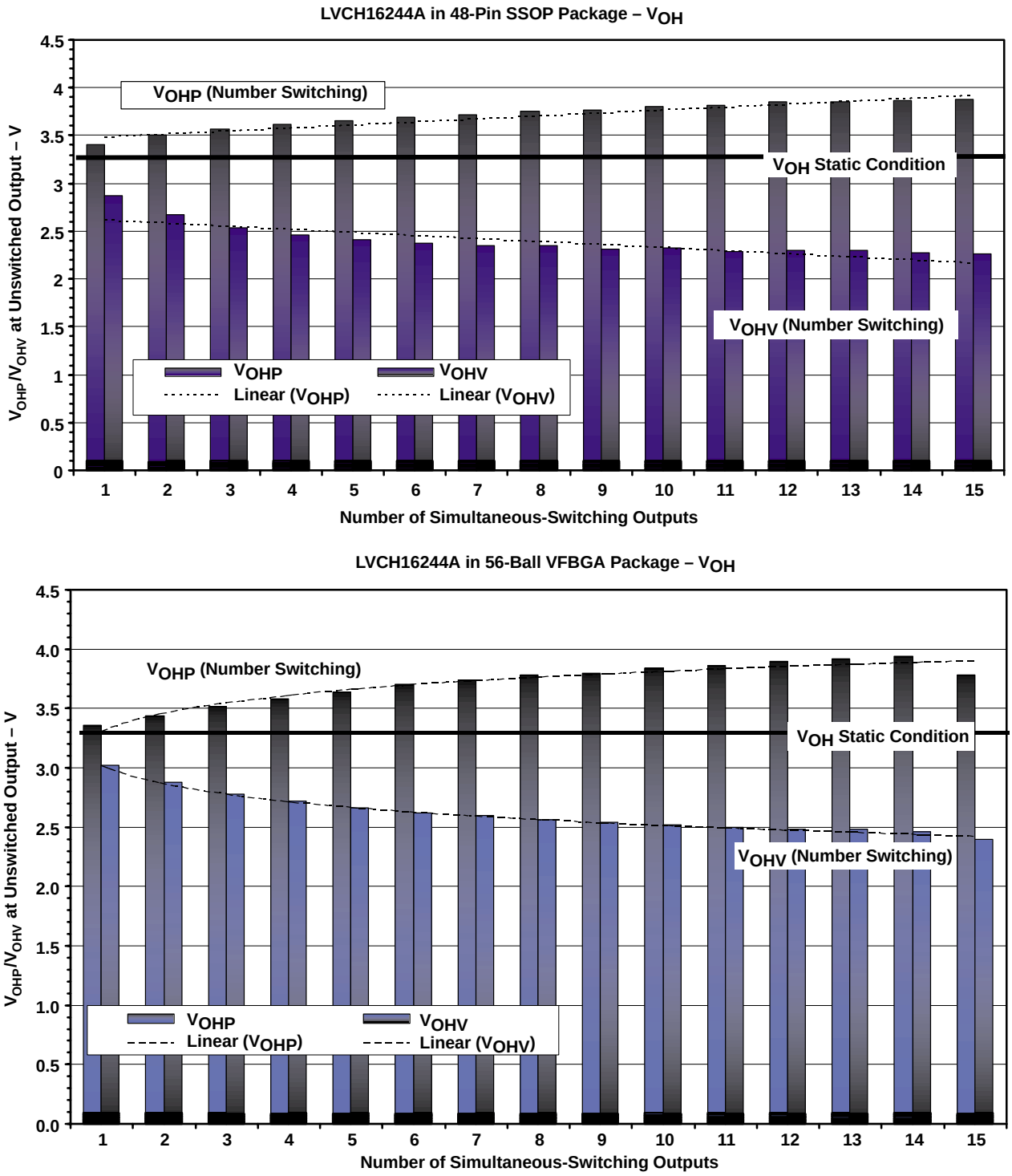


Figure 23. Simultaneous-Switching High Bounce, 48-Pin SSOP (top), 56-Ball VFBGA (bottom)

The ground-bounce and high-bounce interference voltages produced by the simultaneous switching must not exceed the threshold-voltage range for the subsequent input stage (1.4 V to 1.5 V). All the package types investigated meet this requirement for the investigated SN74LVCH16244A logic function. Although the components in the SSOP and TSSOP packages slightly exceed the input voltage threshold for the relevant logic states, switching of the subsequent stage is not expected because the typical threshold voltage of 1.5 V is not reached under any circumstances.

The best result obtained in this investigation was for the ball grid array package. The positive effect of the favorable ball arrangement, with additional GND balls, is evident.

A small part of the differences measured could be due to component spread rather than being exclusively the result of the package being measured.

The process technology involved also has a decisive effect on the interference level. However, the results here give an idea of the general tendencies that apply to other logic families.

3.2.4 Propagation Delay

The package type also influences the increase in propagation delay that occurs when several outputs switch simultaneously. The inductance of the supply and ground leads is the decisive factor. To measure this behavior for various packages, the relation between propagation delay and the number of outputs switching was measured. (see Figures 24 and 25). In all cases, the outputs were, in accordance with the data sheet, loaded with 50 pF and 500 Ω for the SN74LVCH16244A Widebus packages.

The Y-axis shows the increase in propagation delay time (additional switching time required) and the X-axis shows the number of outputs switching. The representation of the increase in propagation delay time was selected to eliminate fluctuations in absolute switching speed that occur as a result of variations in component tolerances. Because the absolute increase in propagation delay time for the rising edges was 0.1 ns to 1.65 ns, and 0.03 ns to 1.15 ns for the falling edge, the measurements are at the upper limits of achievable measurement accuracy given the measurement setup and the measuring instruments used. This is the reason for the nonlinearities of the data curves.

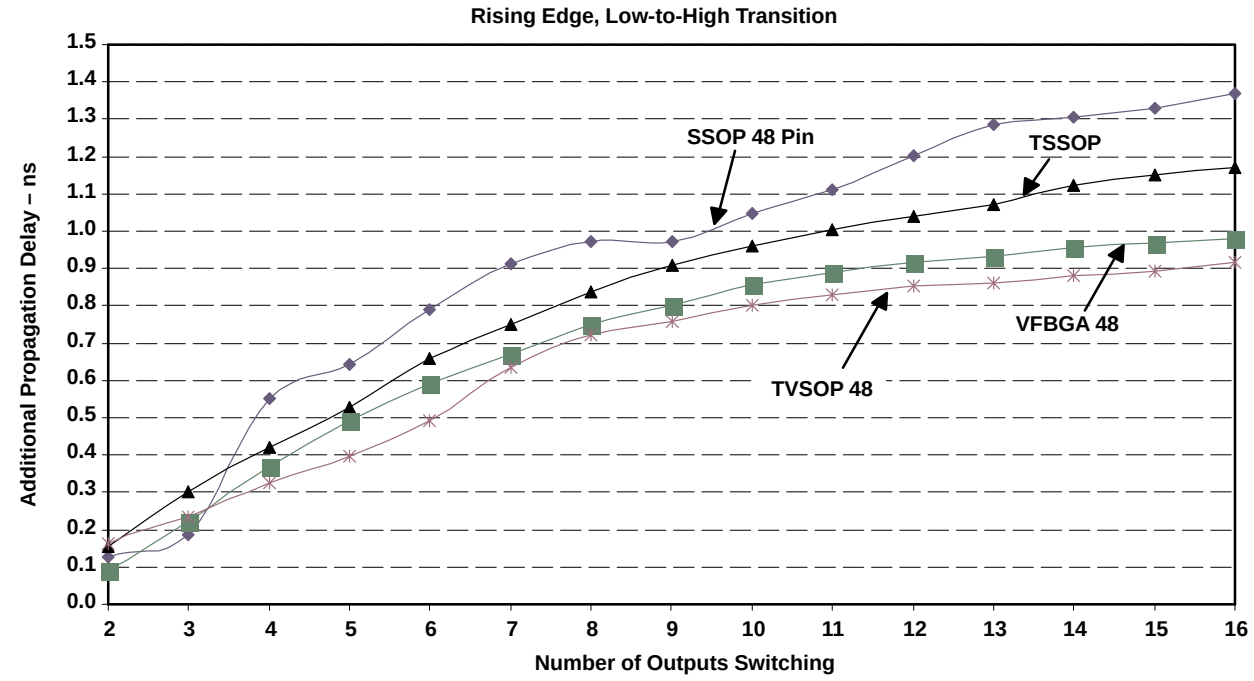


Figure 24. Rising Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and VFBGA Packages

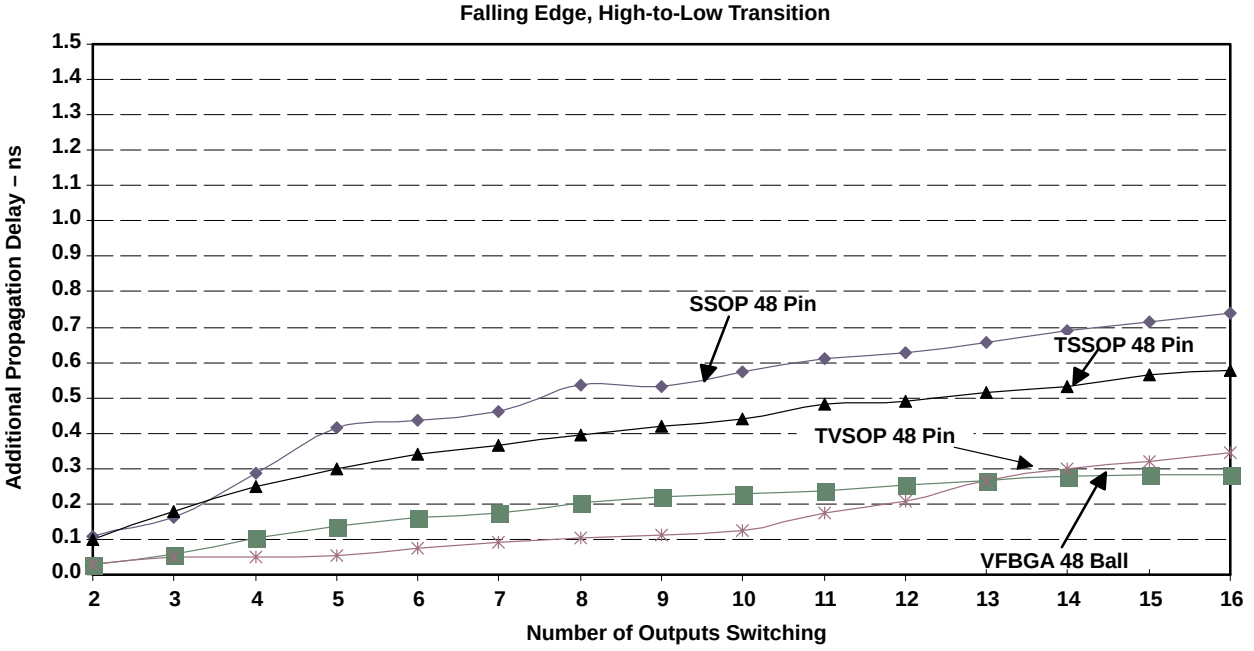


Figure 25. Falling Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and VFBGA Packages

3.3 JEDEC Definition

The 56-ball VFBGA variation has received final registration from JEDEC JC-11 under semiconductor package standard MO-225. The device pinout was submitted to the JC-40 Council, and passed final council vote in March 2001.

3.4 Benefits

Key features and corresponding advantages for logic products assembled in the 56-ball MicroStar Jr. (VFBGA) package are:

- Minimum footprint in the industry: Allows the smallest use of board space among all industry standard packages. Required trace width and spacing capability is well defined for major PCB manufacturers.
- MicroStar Jr. package VFBGA packages have vastly improved parasitic capacitance and inductance, providing better high-speed performance.
- JEDEC standard package, under MO-225, meets worldwide mechanical and pinout specifications.
- No external components required, other than decoupling capacitors. Translates to lower cost, lower maintenance, and higher reliability.
- Improved thermal dissipation improves device reliability.
- Lower ground bounce provides more noise margin.
- Minimized skew pattern provides additional design margin for high-speed buses.
- High board assembly yields, with documented defect levels of ≤4 PPM.

3.5 Evaluation Units

For evaluation units, contact authorized distributors or, for more information, refer to:

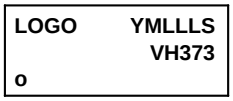
http://www.ti.com/sc/msjunior

4 MicroStar Jr.™ Package Marking and Packing

4.1 Marking

TI uses a laser to mark the product number, year and month manufactured, lot trace code, manufacturing site, and pin-1 location.

A device marking example for the ALVCH16373 is shown in Figure 26.



Part number: ALVCH16373
Year, Month, Lot Code, Site
o = Pin 1 location

Figure 26. Device Marking Example

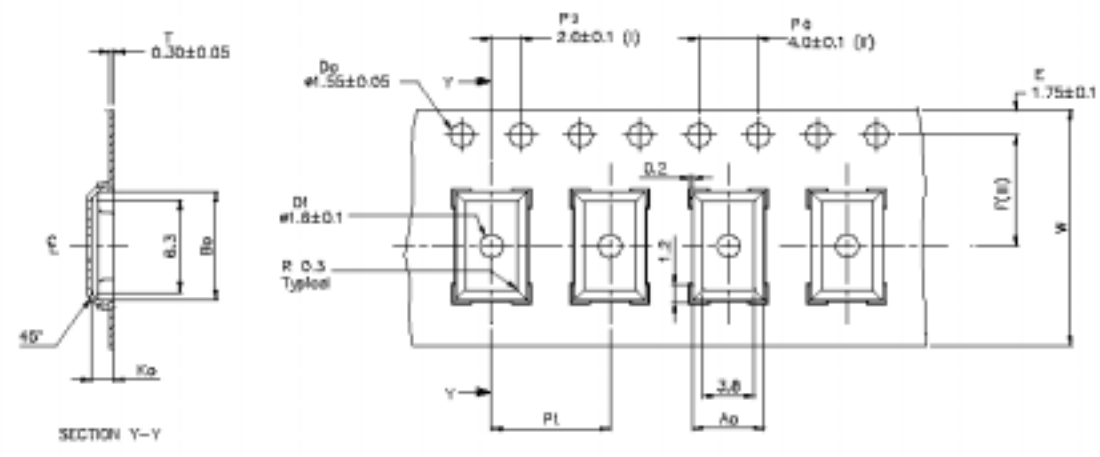
The namerule for the 56-ball MicroStar Jr. package is rule C1, with 10 characters maximum. Table 12 shows the namerule logic and how each marking is derived. The key to the naming convention is to first note the alphanumeric code under namerule A. This code under namerule A is condensed into the codes under namerules B and C, and the remaining function numbers are added in place of the asterisks. For example, to mark an LVC16244A VFBGA device, note that the code under namerule A is SN74LVC16***. Namerule C applies to VFBGA, therefore, SN74LVC16 is replaced by the code LD found under namerule C. The remaining function numbers (244A) are added onto LD to get LD244A.

Table 12. Name Markings for Various MicroStar Jr.™ Package VFBGA Offerings

DEVICE NAME	NAMERULE A	NAMERULE B	NAMERULE C	MARKING
LVC16244A	SN74LVC16***	LVC16***	LD***	LD244A
LVCH16245A	SN74LVCH162***	LVCH162***	LN2***	LN245A
ALVC16244A	SN74ALVC162***	ALVC162***	VC2***	VC244A
LVTH16245A	SN74LVTH162***	LVTH162***	LL2***	LL245A
CBT16211A	SN74CBT16***	CBT16***	CY***	CY211A

4.2 Tape and Reel

Embossed-tape-and-reel feed is the preferred method for automatic pick and place machines. TI offers tape-and-reel packaging for the 56-ball MicroStar Jr. package. The standard quantity is 1000 units per reel. Packaging materials used include the carrier tape, cover tape, and reel. All materials used meet industry guidelines for ESD protection, and comply fully with EIA Standard 481-A, *Taping of Surface Mount Components for Automatic Placement*. The dimensions of interest to the end-user are tape width (W), pocket pitch (P), and quantity per reel. Figure 27 and Table 13 give tape dimensions for the 56-ball MicroStar Jr. package packing.



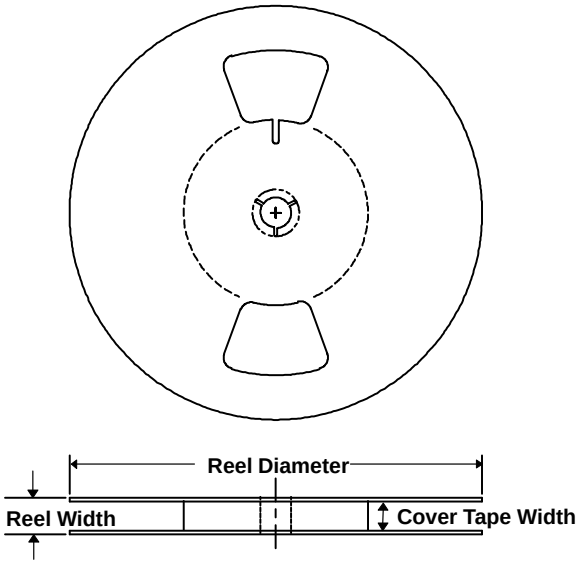
NOTE A: All dimensions are in mm.

Figure 27. Tape Dimensions

Table 13. Carrier Tape Dimensions†

CARRIER TAPE WIDTH (W)	POCKET PITCH (P1)	POCKET WIDTH (A0)	POCKET LENGTH (B0)	POCKET DEPTH (K0)	HOLE-TO-POCKET CENTERLINE (P2)	HOLE-TO-POCKET CENTERLINE (F)	SPROCKET HOLE PITCH (P0)	QUANTITY PER REEL
16.00 ± 0.3	8.00 ± 0.1	4.80 ± 0.1	7.30 ± 0.1	1.50 ± 0.1	2.0 ± 0.1	7.50 ± 0.1	4.0 ± 0.1	1000

† All dimensions are in millimeters.



REEL WIDTH	REEL DIAMETER
16.4 +2.0/–0	330 max

NOTES: A. All dimensions are in millimeters.
B. Standard quantity is 1000 devices per reel; however, this is subject to change per market demand.

Figure 28. Reel Dimensions

4.3 Sockets and Socket Ordering Information

Yamaichi Socket number: VFBGA-56 PN# IC280-056-237
Yamaichi Electronics USA Inc.
2235 Zanker Road
San Jose, CA 95131 Tel: (408) 456-0797

5 Conclusion

This application report shows that the 56-ball MicroStar Jr. package is the optimal solution for addressing performance and economic issues such as:

- PCB area savings of up to 72% over TSSOP
- Minimized skew by reducing pin-to-pin inductance, thereby enabling support for high-speed applications with greater bandwidth
- Improved thermal dissipation
- Improved board-mount assembly yields due to beneficial characteristics inherent in BGA processes.

The spacing between balls for this 0.65-mm VFBGA package is equal to that of other 0.8-mm-pitch BGA packages, therefore, defect rates due to solder bridging are similar to those of larger pitch BGA packages. The simultaneous-switching data and graphs clearly show this smaller package, with its lower capacitance and inductance, has both speed and noise advantages over the SSOP, TSSOP, and TVSOP packages. Designers using the MicroStar Jr. (VFBGA) package can take advantage of the win-win combination of electrical and physical properties offered.

With the introduction of the MicroStar Jr. package by TI, OEMs are assured of a standardized JEDEC package, pinout, and availability of the previously stated product families and functions. More device families and functions will be included in the MicroStar Jr. package as market interest dictates.

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