CC1010 Errata Note 001, rev. 1.1

Switching between certain combinations of frequency words (FREQ) in CC1010 may cause the PLL never to be able to lock. This is most likely to occur in frequency hopping systems. A software fix solves the problem.

Description and reason for the problem
When a new frequency is selected by updating the FREQ registers or changing the MAIN.F_REG bit, a non-valid value can be latched due to internal clock skew. This non-valid value may put the PLL in a deadlock situation and prevent the PLL from locking.

The deadlock situation can happen if the 3 most significant bits of the FREQ words are different for the two frequencies. If the 3 most significant bits are equal, the deadlock will not occur. To ensure that the most significant bits are equal, use the same reference frequency divider value (REFDIV) for all channels.

Suggested workarounds
Alternative 1:
As the problem only rise when the MSBs of the FREQ words are different, the first solution is to select the same reference frequency divider value (REFDIV) for all channels. Using a crystal frequency of 14.7456 MHz or above make it possible to generate 50 channels with the same REFDIV value, see AN011.

Alternative 2:
If the three MSBs of the FREQ words cannot be made the same for all channels, a software workaround must be used.

Alternative 2a:
The general software workaround is to write a "safe" frequency value to the FREQ register before the new frequency is written. The "safe" frequency word is FREQ_2A (or FREQ_2B) = E0h. This workaround involves only one additional write operation:

This is the suggestion for a software workaround:
1. Write FREQ_2A (register CCh) = E0h. (Presuming that frequency A is used.)
2. Write new frequency word to FREQ_A, or set RFMAIN.F_REG = 1 (register C8h) in order to swap the frequency word and use FREQ_B.

Alternative 2b:
An alternative software workaround is to reset the frequency synthesiser. After the new frequency word is programmed, the FS_RESET_N bit must be toggled by writing to the FSCTRL register, first setting the bit low, then high. This means two write operations to the register.

This is the suggestion for a software workaround:
1. Write new frequency word to FREQ_A or FREQ_B
2. First write FSCTRL (register ECh) = 00h
3. Then write FSCTRL (register ECh) = 01h

Fix
This problem is solved by a software workaround.

Batches affected
This errata note applies to all chip batches and revisions of the chip.

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