CC1070 Errata Note 001, rev. 1.0

December 6, 2005

When performing PLL calibration it has been verified that waiting at least 100 µs after initiating the calibration is necessary to avoid an unreliable PLL calibration result. Still, there exists a small, but finite probability that the CC1070 PLL will not LOCK. Checking LOCK and recalibrating if LOCK is not achieved is therefore necessary.

Description and reason for the problem

CC1070 PLL calibration and lock can be monitored using one of the following methods:

Method A:

1. Start calibration
2. Monitor [STATUS.CAL_COMPLETE]
3. Monitor [STATUS.LOCK_CONTINUOUS]

or

Method B:

1. Start calibration
2. Monitor [STATUS.CAL_COMPLETE]
3. Monitor LOCK pin

When using a 14.7456 MHz crystal frequency the CC1070 calibration (monitored by steps 2 and 3) typically lasts 3.9 ms when using the fast calibration routine (CAL_SELECT = 1). However, it has been observed that the CAL_COMPLETE indicator in the STATUS register is unreliable during the first 100 µs after initiating the calibration. As a result step 2 might indicate calibration complete too early, i.e. before the actual calibration has actually completed. In such a situation step 3 (LOCK monitoring) is executed during instead of after calibration. In order to avoid this inconsistency, a waiting period of at least 100 µs between calibration start and the start of the polling should be applied using one of the following methods:

Method A:

1. Start Calibration
2. Wait at least 100 µs before starting to monitor [STATUS.CAL_COMPLETE]
3. Monitor [STATUS.LOCK_CONTINUOUS]

or

Method B:

1. Start Calibration
2. Wait at least 100 µs before starting to monitor [STATUS.CAL_COMPLETE]
3. Monitor LOCK pin.

Calibration starts when CALIBRATE.CAL_START is set to 1 as shown in figure 1. The PLL is then set to open loop and the internal VCO control voltage set to a value given by CALIBRATE.CAL_ITERATE[2:0] = 4_h. Based on this value a capacitor array is selected and when the calibration is completed the PLL loop is closed.

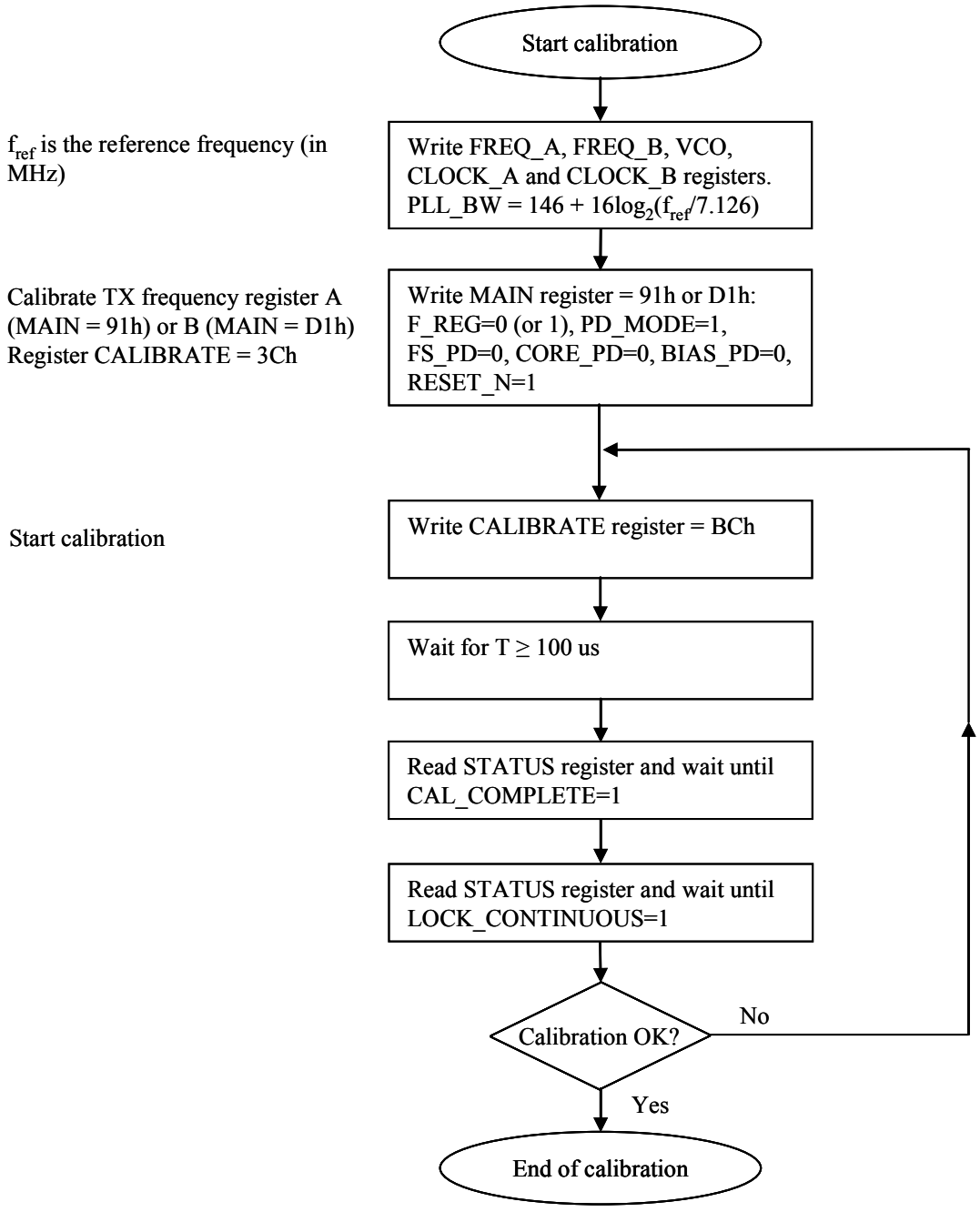

Figure 1: Recommended PLL calibration procedure

In less than 10 ppm of all PLL calibrations performed it was observed that CC1070 did not achieve LOCK even when introducing a 100 µs wait period before polling of [STATUS.CAL_COMPLETE] was initiated. The reason for no LOCK still occurring, even when calibrating the PLL with this small wait period, is due to the PLL calibration procedure making an erroneous frequency measurement causing the PLL calibration algorithm to choose a wrong capacitor array setting producing a no LOCK situation. For this reason it is important to control that the PLL calibration achieves LOCK and recalibrate if it does not.

Suggested workaround

For those users who have not already implemented a recalibration procedure in software it is strongly recommended to avoid polling [STATUS.CAL_COMPLETE] until 100 µs has elapsed following calibration start, then monitor LOCK after calibration complete and, if LOCK is not achieved, recalibrate until LOCK is successfully achieved. The recommended calibration procedure, including recalibration, is provided in figure 1.

High Reliability Applications

In high reliability applications recalibration should be performed frequently and always when retransmitting packets.

Batches affected

This errata note applies to all chip batches and revisions of the chip.

Document History

Revision	Date	Description/Changes
1.0	2005-12-06	First edition.

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