EVM User's Guide: AWR2E44PEVM

AWR2E44P Evaluation Module

Description

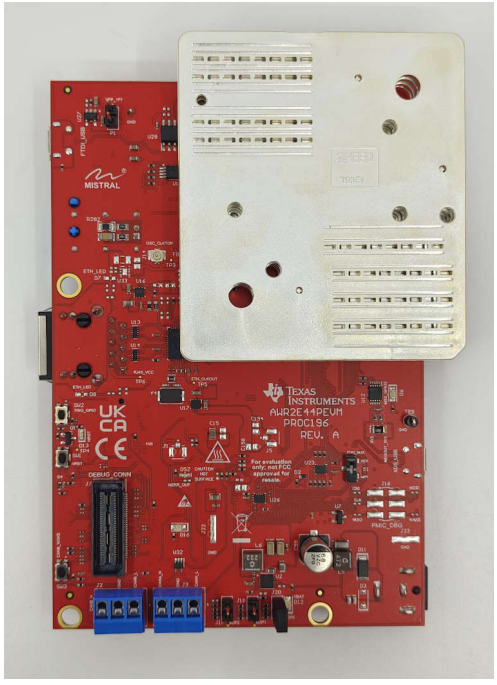
The AWR2E44PEVM is an easy-to-use evaluation board for the AWR2E4xP mmWave sensing device, with direct connectivity to the DCA1000 EVM (sold separately).This EVM kit contains everything needed to start developing software for the on-chip C66x DSP, ARM® Cortex®-R5F controller, and hardware accelerator (HWA 2.1). Also included is on-board emulation for programming and debugging as well as on-board CAN and Ethernet Interfaces, buttons, and LEDs for quick integration of a simple user interface.

Get Started

1. Visit AWR2E44PEVM product page.
2. Download the latest libraries.
3. Download the comprehensive Reference Design Files.
4. Navigate to the Radar Toolbox.
5. Explore the Radar Toolbox for more information, applications, and resources.

Features

- SPEED 3D waveguide antennd (4 receive - 4 transmit channels)
- XDS110 based JTAG emulation with Serial port for onboard 64-bit QSPI flash programming
- UART to USB Debug port for terminal access using FT4232H
- 60-pin, high-density (HD) connector for external JTAG/ Emulator Interface with TRACE and CSI2 support
- 60-pin, high-density (HD) connector for debug, SPI, I2C and LVDS
- RJ45 Ethernet connector to stream the captured data over the network to the host PC
- MATEnet Ethernet interface to stream the captured data over the network to an automotive host
- 5V/12V power jack to power the board



AWR2E44PEVM

1 Evaluation Module Overview

1.1 Introduction

The AWR2E44P evaluation module (EVM) is an easy-to-use platform for evaluating the AWR2EP44P FMCW radar sensor, which has dirrect connectivity to the DCA1000 EVM. This EVM kit contains everything required to start developing software for the on-chip ARM® Cortex®-R5F controller, and hardware accelerator (HWA 2.1). There are several debug features that are included to assist in software development and evaluation. These include on-board FTDI and XDS110, CANFD, Ethernet, temperature, current sensors, and high speed connectors to interface with the DCA1000EVM or external debuggers.

1.2 Kit Contents

- AWR2E44PEVM
- 3D waveguide Antenna
- Micro USB cable
- Ethernet Cable
- Mounting brackets, screws, spacers and nuts, to allow placing the PCB vertical

Note

A 12V, > 2.5A supply brick with a 2.1mm barrel jack (center positive) is not included. TI recommends using an external power supply that complies with applicable regional safety standards, such as UL, CSA, VDE, CCC, PSE, and more. The length of the power cable needs to be < 3m.

The following power supply has been tested to work with the AWR2E44PEVM: SDI65-12-U-P5.

1.3 Specification

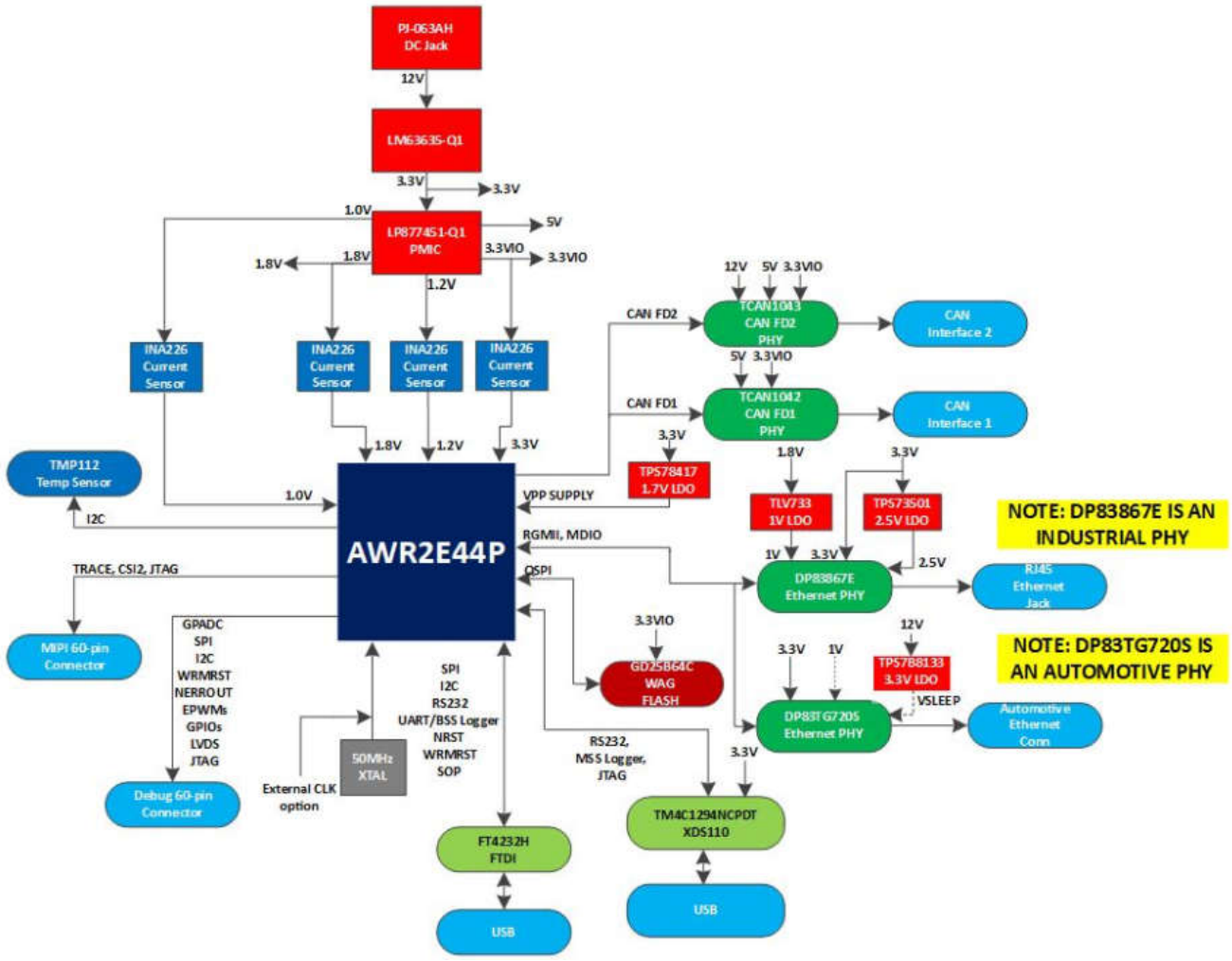


Figure 1-1. Functional Block Diagram

Figure 1-1 shows the functional block diagram. The EVM contains the essential components for the TI mmWave radar system which can be copied as is into production designs: 3D waveguide antenna, power delivery network, serial Flash, external communication interfaces (CANFD and Ethernet), and SOP control. Additionally, several debug features are included to assist in software development and evaluation. These include on-board FTDI and XDS110, temperature and current sensors, and high speed connectors to interface with the DCA1000EVM or external debuggers.

1.4 Device Information

The documents in Table 1-1 provide information regarding Texas Instruments integrated circuits used in the assembly of the AWR2E44PEVM. This user's guide is available from the TI web site under literature number SWRU631. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document.

Table 1-1. Related Device Documentation

Devices Used on the EVM	Data Sheet
TPD1E05U06QDPYR-Q1	TPD1E05U06QDPYRQ1
LM63635DQDRRR-Q1	LM63635DQDRRRQ1
TCAN1042HGVD-Q1	TCAN1042HGVDQ1
DP83TG720SWRNDR-Q1	DP83TG720SWRNDRQ1

Table 1-1. Related Device Documentation (continued)

Devices Used on the EVM	Data Sheet
TCAN1043ADYYR-Q1	TCAN1043ADYYRQ1
TM4C1294NCPDTT3	TM4C1294NCPDTT3
LP877451A1RXVR-Q1	LP877451A1RXVRQ1
INA226AIDGSR	INA226AIDGSR
DP83867ERGZR	DP83867ERGZR
TPS73501DRVR	TPS73501DRVR
TLV73310PQDRVR-Q1	TLV73310PQDRVRQ1
TPS79601DRBR	TPS79601DRBR
TS3A5018RSVR	TS3A5018RSVR
TMP112AIDRLR	TMP112AIDRLR
TPS78417QDBVR-Q1	TPS78417QDBVRQ1
SN74LVC1G04DCKR-Q1	SN74LVC1G04DCKRQ1
TPD1E05U06QDPYR-Q1	TPD1E05U06QDPYRQ1
TPS7B8133QDRVRQ1	TPS7B8133QDRVRQ1
TPD4E004DRYR	TPD4E004DRYR
TPD4E05U06DQAR	TPD4E05U06DQAR

2 Hardware

CAUTION HOT SURFACE
CONTACT MAY CAUSE BURN
DO NOT TOUCH

Note

During operation, a minimum separation distance of 20 centimeters must be maintained between the user and the EVM.

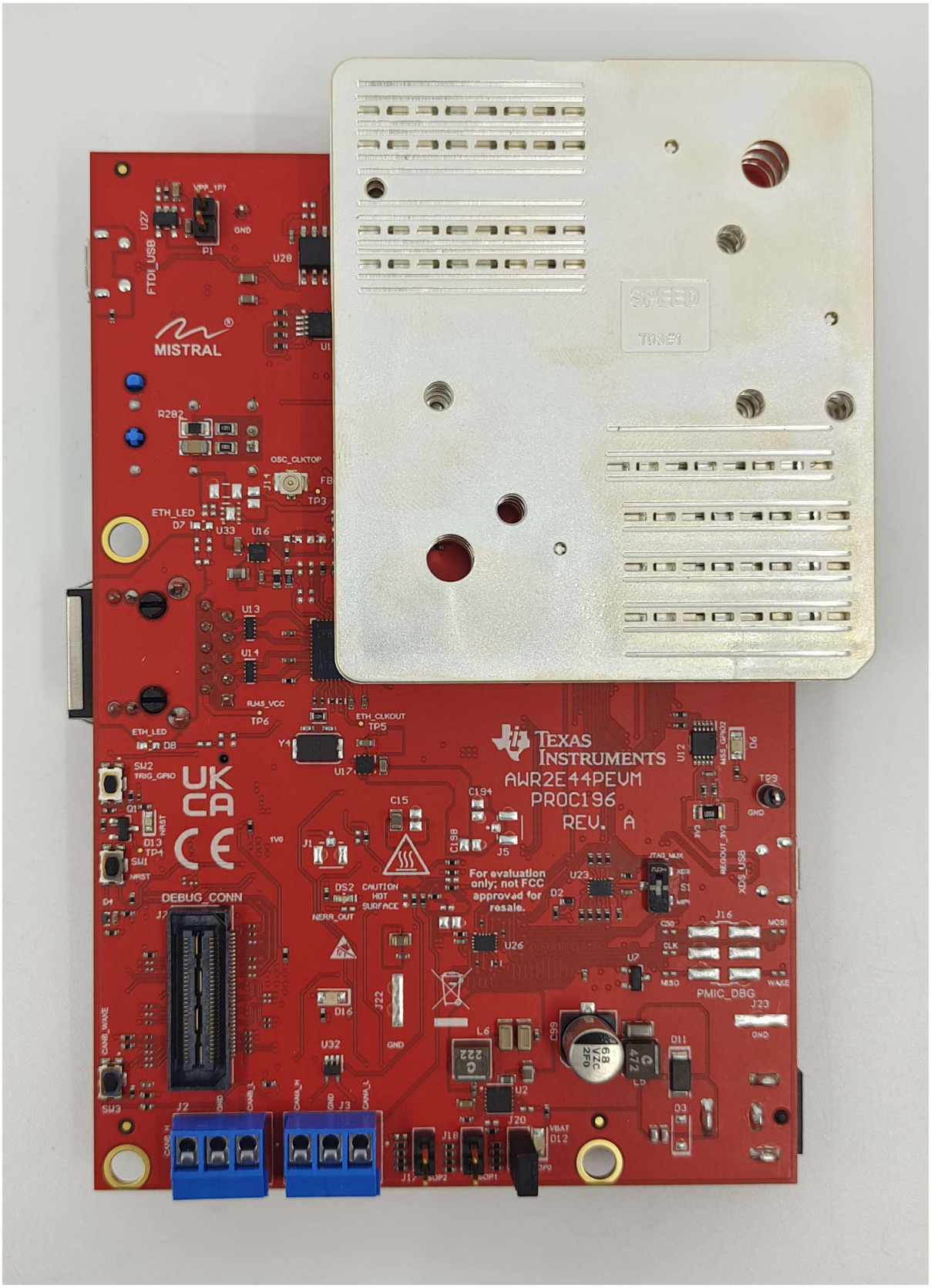


Figure 2-1. AWR2E44PEVM Front View

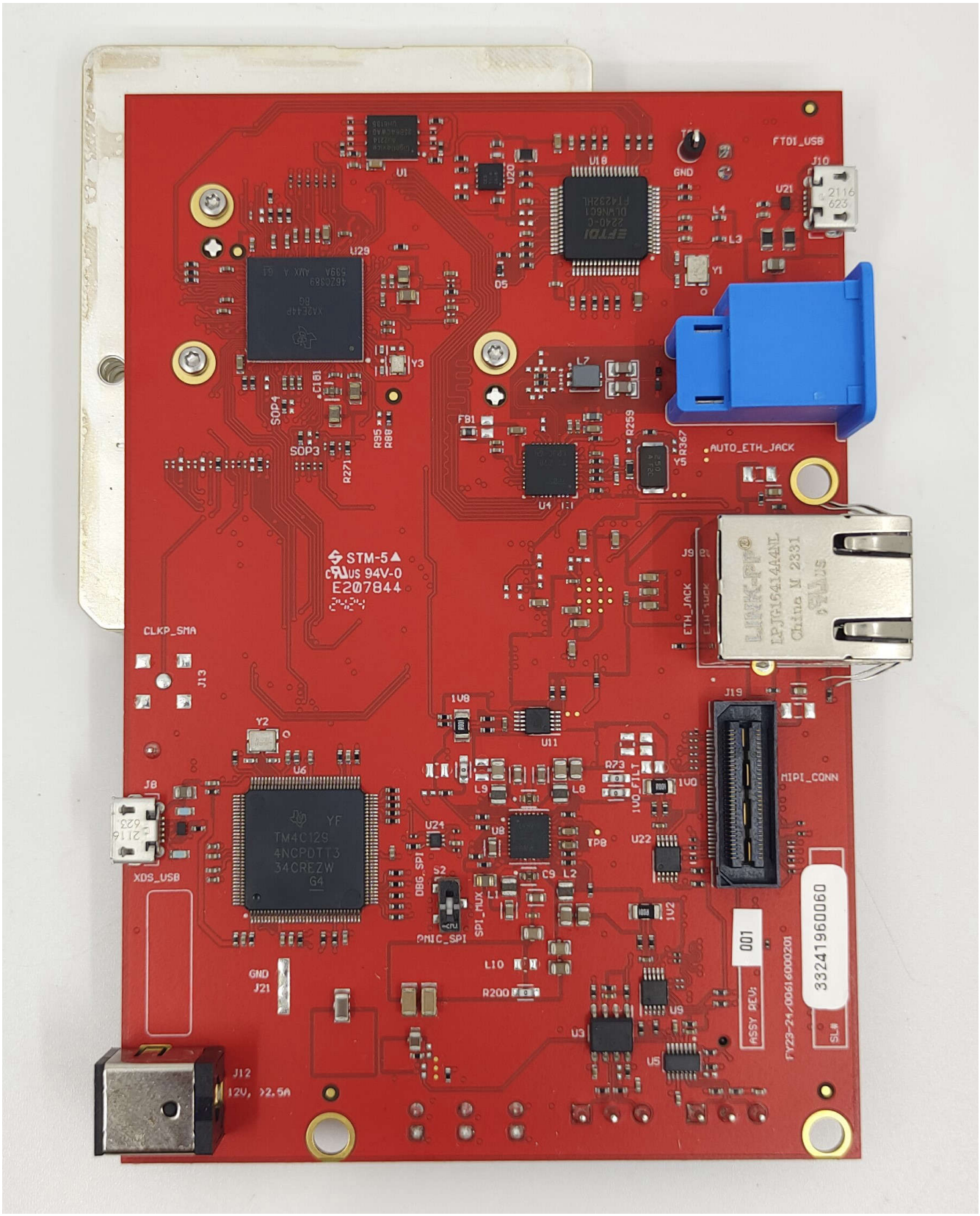


Figure 2-2. AWR2E44PEVM Back View

2.1 PCB Handling Recommendations

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in the supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA010A.

2.2 Power Connections

The AWR2E44PEVM is powered by the 12V power jack (>2.5A current capability). When power is provided the AR_NRST, VBAT_INT, and 5V0 LEDs glow, indicating that the board is powered up.

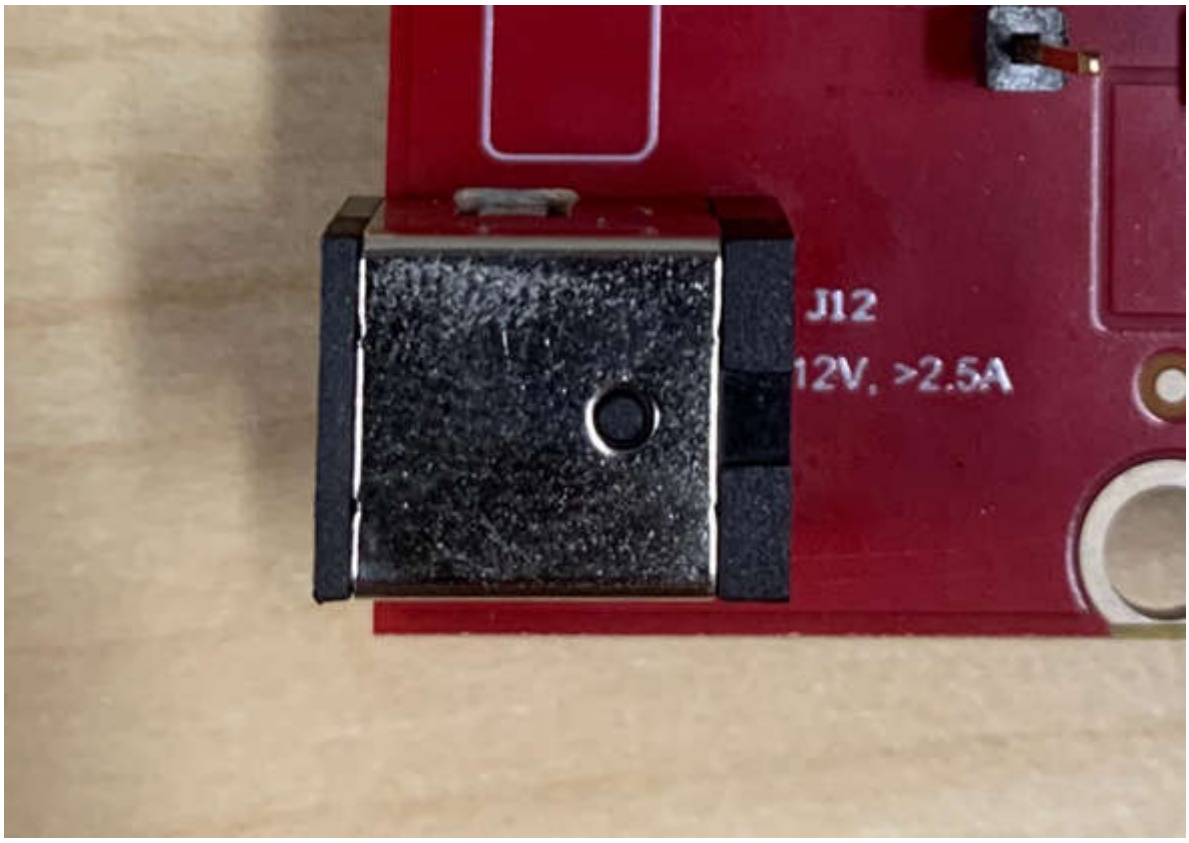


Figure 2-3. 12-V Power Connector

Note

After the 12V power supply is provided to the EVM, TI recommends to press the NRST switch (SW1) one time to provide for a reliable boot-up state.

2.3 Connectors

2.3.1 MIPI 60-Pin Connector (J19)

This connector provides the standard MIPI 60-pin interface, as shown in Figure 5, for JTAG and trace capability through emulators such as the XDS560pro. Further information on the emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.

To use this interface, the JTAG lines from the AWR2E44PEVM needs to be muxed to MIPI 60-pin connector. Refer to Section 2.7.1 for more details.

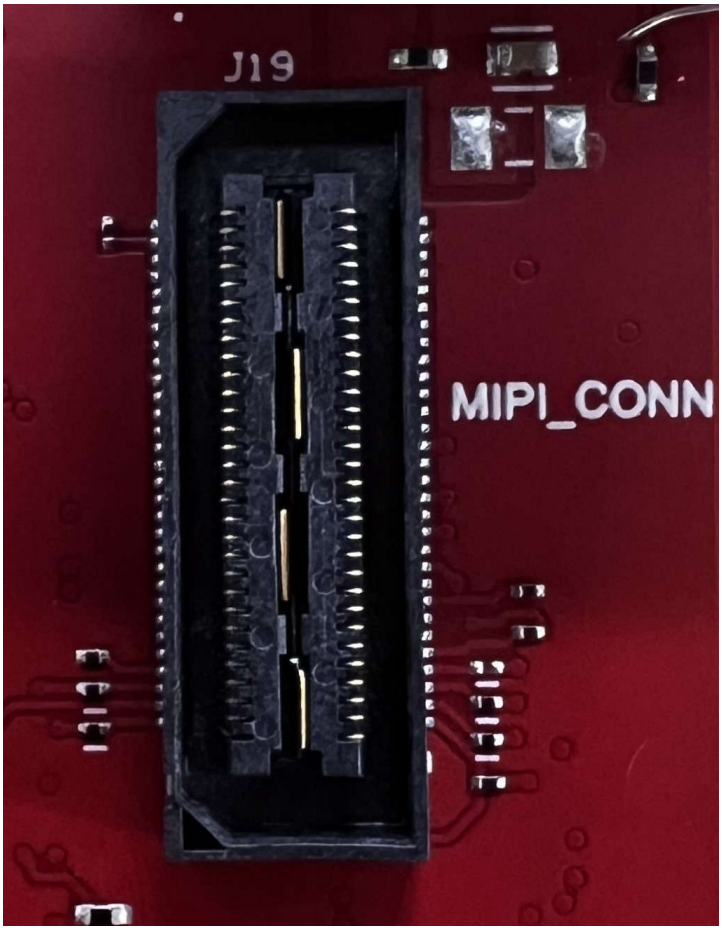


Figure 2-4. 60-pin MIPI Connector

Table 2-1 provides the pin assignment details for the MIPI 60-pin connector.

Table 2-1. J19 Pin Assignment

Pin Number	Description	Pin Number	Description
1	MIPI_VREF_DEBUG	2	MIPI_TMS
3	MIPI_TCK	4	MIPI_TDO
5	MIPI_TDI	6	MIPI_NRST
7	MIPI_RTCK	8	MIPI_TRSTPD
9	MIPI_JTAG_NRST	10	NC
11	NC	12	MIPI_VREF_DEBUG
13	TRACE_CLK	14	NC
15	MIPI_DBG_DETECT	16	GND
17	TRACE_CTL	18	NC
19	TRACE_DATA0	20	NC
21	TRACE_DATA1	22	NC
23	TRACE_DATA2	24	NC
25	TRACE_DATA3	26	NC
27	TRACE_DATA4	28	NC
29	TRACE_DATA5	30	NC
31	TRACE_DATA6	32	NC
33	TRACE_DATA7	34	NC
35	NC	36	NC

Table 2-1. J19 Pin Assignment (continued)

Pin Number	Description	Pin Number	Description
37	NC	38	NC
39	NC	40	NC
41	NC	42	GND
43	NC	44	NC
45	NC	46	NC
47	NC	48	GND
49	NC	50	NC
51	NC	52	NC
53	NC	54	GND
55	NC	56	NC
57	GND	58	NC
59	NC	60	GND

2.3.1.1 MIPI TRACE ECO List

By default, the TRACE signals are not brought out to the MIPI Connector. To enable the TRACE interface on the MIPI Connector, the following changes should be made.

1. Remove R165 and populate R216
2. Remove R218 and populate R220
3. Populate R227
4. Populate R231
5. Remove R233 and populate R235
6. Populate R217
7. Remove R21 and populate R221
8. Remove R25 and populate R228
9. Populate R232
10. Populate R236

2.3.2 Debug Connector-60 pin (J7)

This connector enables interfacing of LVDS signals to the DCA1000 EVM for data capturing purposes.

Also, the connector has SPI, I2C, JTAG, GPADC, WRMRST, NRROUT, EPWM, and other control signals from AWR2E44PEVM for debug purpose.

The SPI is multiplexed to the Debug Connector. For more details refer to Section 2.7.1.

The debug connector supports direct connection to the TMDS273GPEVM for CSI2 data processing. For more details refer to CSI2 FE Connector ECO List.

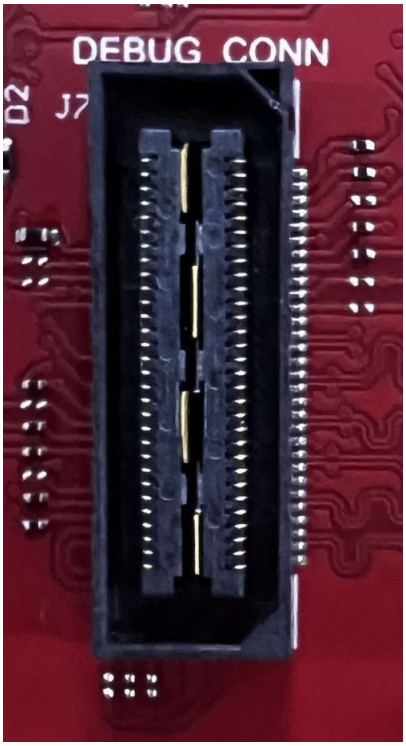


Figure 2-5. 60-pin Debug Connector

Table 2-2 provides the pin assignment details for the Debug 60-pin connector.

Table 2-2. J7 Pin Assignment

Pin Number	Description	Pin Number	Description
1	NC	2	NC
3	NC	4	XREF_CLK0
5	GND	6	MSS_EPWMA0
7	DBG_SPI_CS0	8	GND
9	DBG_SPI_CLK	10	MSS_SPIA_HOSTIRQ
11	DBG_SPI_PICO	12	DBG_SPI_POCI
13	3.3V PULL_UP	14	XREF_CLK1
15	EMU_TCK	16	AR_SYNCIN
17	EMU_TDI	18	GND
19	GPADC1	20	EMU_TMS
21	GPADC2	22	EMU_TDO
23	NC	24	GND
25	NC	26	CSI2_TX2_CLK_LVDS_FRCLK_P
27	GPADC5	28	CSI2_TX2_CLK_LVDS_FRCLK_N
29	GPADC6	30	GND
31	NC	32	CSI2_TX3_P
33	MCU_CLKOUT	34	CSI2_TX3_N
35	NC	36	GND
37	MSS_SPIB_CS1	38	CSI2_TX2_CLK_LVDS_FRCLK_P

Table 2-2. J7 Pin Assignment (continued)

Pin Number	Description	Pin Number	Description
39	SOP1_MSS_SPIB_CS2	40	CSI2_TX2_CLK_LVDS_FRCLK_N
41	MSS_GPIO_0	42	GND
43	MSS_GPIO_1	44	CSI2_TX4_LVDS_CLK_P
45	AR_WRMRST	46	CSI2_TX4_LVDS_CLK_N
47	NC	48	GND
49	AR_NERROUT	50	CSI2_TX1_LVDS_TX1_P
51	MSS_I2CA_SCL	52	CSI2_TX1_LVDS_TX1_N
53	MSS_I2CA_SDA	54	
55	MSS_EPWMB0	56	CSI2_TX0_LVDS_TX0_P
57	MSS_EPWMA1	58	CSI2_TX0_LVDS_TX0_N
59	MSS_GPIO_3	60	GND

2.3.2.1 CSI2 FE Connector ECO List

This connector can also support a direct connection to the TMDS273GPEVM high density FE connectors (J1 and J11) for CSI2 HIL (Playback) data streaming. In order to properly interface with the FE connector, the following changes should be made.

1. Populate R51
2. Populate R135
3. Remove R351 and populate on R138
4. Remove R361 and populate on R160
5. Populate R164
6. Populate R167

2.3.3 Ethernet Ports (J4 and J9)

The AWR2E44PEVM supports two RGMII Ethernet ports to provide the connection to the network. The J4 connector provides access over a MATEnet port (9-2304372-9 connector) via a DP83TG720SWRNDR-Q1 PHY. The J9 port provides access over an RJ45 port via a DP83867ERGZR PHY. By default, the RGMII interfaces are connected to the J9 port only. To access the RGMII interface, over the J4 connector several resistors must be populated. For more details please see ECOs to Enable the DP83TG720SWRNDR-Q1 PHY and refer to the Schematic, BOM, and Assembly and Database and Layout sections.

This RGMII interface is intended to operate primarily as a 1000Mbps ECU interface and can also be used as an Instrumentation Interface.

The RGMII interface supports following features:

- Full Duplex 10/100/1000Mbps wire rate Interface to Ethernet PHY over RGMII, parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support

The Ethernet port is interfaced to the AWR2E44P through the Ethernet PHY and is used to stream the captured data over the network to the host PC.

Figure 2-6 shows the Ethernet RJ45 Mag-Jack connector, and Table 2-3 provides the connector pin details.

Table 2-3. J9 Pin Assignment

Pin Number	Description	Pin Number	Description
1	GND	2	Test point
3	ETH_D4P	4	ETH_D4N
5	ETH_D3P	6	ETH_D3N
7	ETH_D2P	8	ETH_D2N
9	ETH_D1P	10	ETH_D1N
11	LED_ACTn	12	GND

Table 2-3. J9 Pin Assignment (continued)

Pin Number	Description	Pin Number	Description
13	GND	14	LED_LINKn
15	ETH_GND	16	ETH_GND

Figure 2-6. J9 Connector

Figure 2-7 shows the Ethernet MATEnet connector, and Table 2-4 provides the connector pin details.

Table 2-4. J4 Pin Assignment

Pin Number	Description	Pin Number	Description
1	TRD_P	2	TRD_M
S1	GND	S2	GND
S3	GND	S4	GND
S5	GND	S6	GND

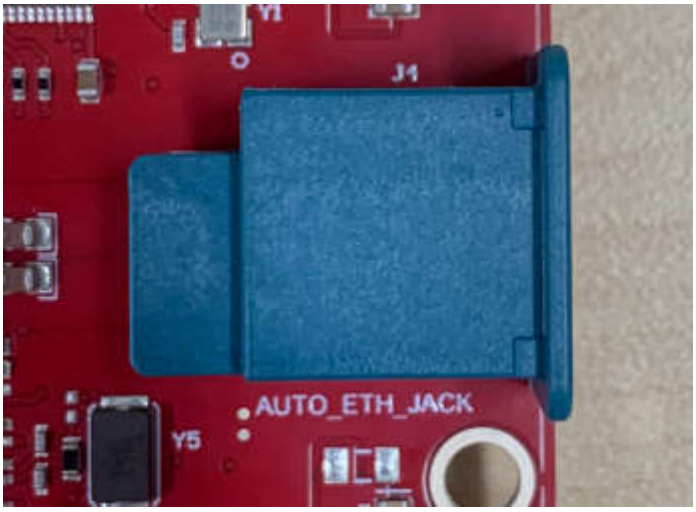


Figure 2-7. MATEnet Connector

2.3.3.1 ECOs to Enable the DP83TG720S-Q1 PHY

By default, the board is designed to be used with the DP83867E PHY with the RJ45 connector. To enable the DP83TG720S-Q1 PHY with the MATEnet connector, the following hardware changes must be made. For help with locating these components on the PCB, refer to the provided Schematic, BOM, and assembly files.

1. Remove R98 and populate on R74
2. Remove R101 and populate on R230

3. Remove R103 and populate on R96
4. Remove R105 and populate on R100
5. Remove R121 and populate on R178
6. Remove R122 and populate on R225
7. Remove R195 and populate on R245
8. Remove R290 and populate on R234
9. Remove R325 and populate on R237
10. Remove R336 and populate on R238
11. Remove R338 and populate on R239
12. Remove R339 and populate on R240
13. Remove R413 and populate on R247
14. Remove R369 and populate on R249
15. Populate D18 and D19 ESD diodes
16. Populate C55
17. The bootstrap configuration pins can be populated/removed as needed depending on the use case

Note

The automotive Ethernet PHY (U4) and port (J4) on the AWR2E44PEVM have not been tested by Texas Instruments to be compliant with any regional standards such as Radio Equipment Directive 2014/53/EU. If the user wishes to populate the components necessary to utilize this port, it is up to the user to do any necessary testing to ensure that the port is compliant with all applicable regional standards before use. Any modifications done to enable the J4 port will invalidate the existing RED 2014/53/EU certification of the AWR2E44PEVM.

2.3.4 USB Connectors (J8, J10)

The AWR2E44PEVM has two standard micro USB connectors.

Micro USB Connector J10 provides access to the AWR2E44P UART, SPI, I2C, RS232, and SOP interfaces through the FTDI chip.

Table 2-5. J10 Pin Assignment

Pin Number	Description	Pin Number	Description
1	FTDI_VBUS	2	FTDI_USBD_N
3	FTDI_USBD_P	4	FTDI_USBID
5	GND	6	GND
7	GND	8	GND
9	GND	10	GND
11	GND		

Figure 2-8. FTDI USB Port

Micro USB connector J8 provides access to the JTAG, MSS_UARTA, and MSS_UARTB interfaces of the AWR2E44P via the XDS110 emulator.

This is the UART interface used to flash the binary to the onboard serial flash and for Out-of-box (OOB) demo.

Note

The OOB demo requires only J8 to be connected to the PC. J10 is not used for the OOB demo.

Table 2-6. J8 Pin Assignment

Pin Number	Description	Pin Number	Description
1	XDSET_VBUS	2	XDSET_D_N
3	XDSET_D_P	4	XDSET_ID
5	GND	6	GND
7	NC	8	NC
9	GND	10	GND
11	GND		

Figure 2-9. XDS USB Port

2.3.5 OSC_CLK_OUT Connector (J2)

Connector J2 provides access to measure oscillator clock out signal from the AWR2E44P device.

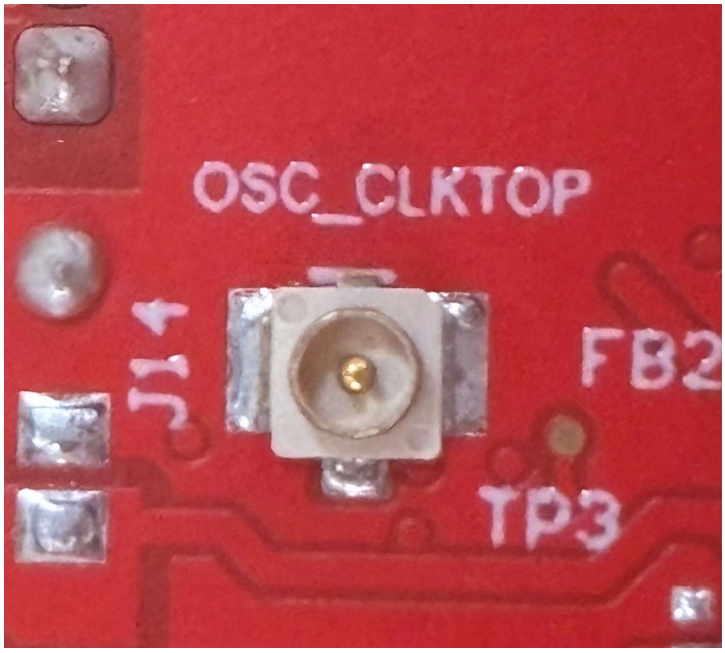


Figure 2-10. OSC_CLK_OUT Port

2.3.6 Voltage Rails Ripple Measurement Connectors (J1, J3, J5) (DNP)

J1 Provides access to measure ripple on 1V0_FILTERED (1.0V analog RF supply for AWR2E44P) voltage rail.

J5 Provides access to measure ripple on 1V8_FILTERED (1.8V analog supply for AWR2E44P) voltage rail.

These connectors are not populated on the board by default. To populate these connectors with the appropriate part, please refer to the Schematic, BOM, and assembly files.

2.4 Antenna

The AWR2E44PEVM includes a 3D waveguide antenna produced by SPEED for the four receivers and four transmitters, which enables tracking multiple objects with their distance and angle information. This antenna design enables estimation of both azimuth and elevation angles, which enables object detection in a 3-D plane (see Figure 2-11). **Note: RX1 and RX4 are 180 degrees out of phase which should be compensated for in post processing.**

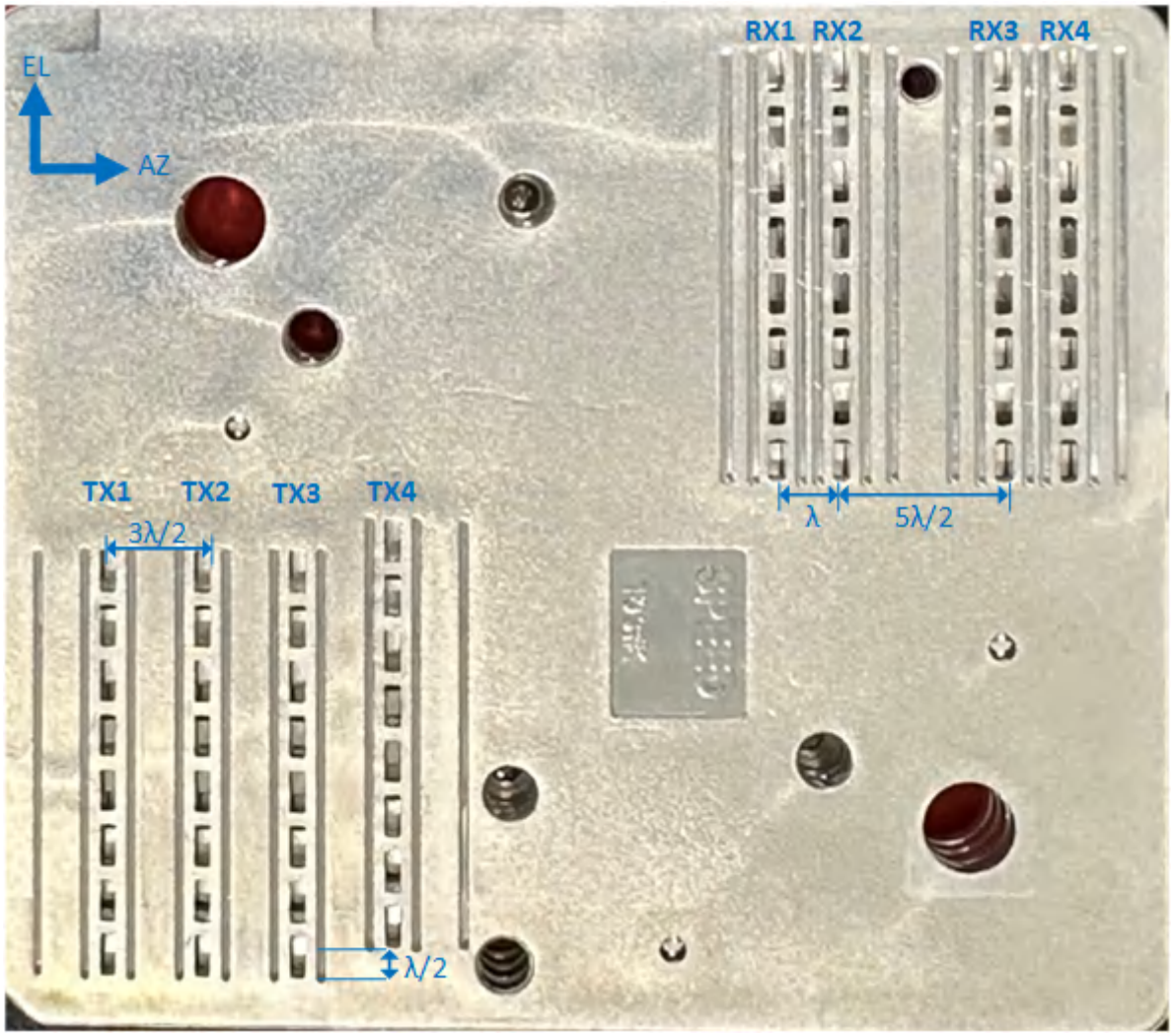


Figure 2-11. AWR2E44PEVM Antenna Design

The antenna design shown in Figure 2-11 results in the virtual antenna array shown in Figure 2-12. The distance between two adjacent cells is lambda/2.

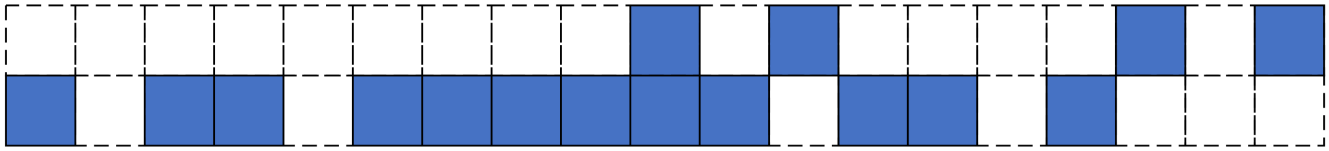


Figure 2-12. Virtual Antenna Array

The antenna peak gain is 15 dBi across the frequency band of 76 to 81GHz. The radiation pattern of the antenna in the horizontal plan (H-plane) and elevation plan (E-plane) is as shown in Figure 2-13 and Figure 2-14, respectively.

The beamwidth of the antenna design can be determined from the radiation patterns provided below. For example, based on 3-dB drop in the gain as compared to bore sight, the horizontal 3dB-beamwidth is approximately ±35 degrees (see Figure 2-13), and elevation 3dB-beamwidth is approximately ±3 degrees (see Figure 2-14). Similarly, the horizontal 6 dB beamwidth is approximately ±42 degrees (see Figure 2-13) and the elevation 6dB-beamwidth is approximately ±5 degrees (see Figure 2-14).

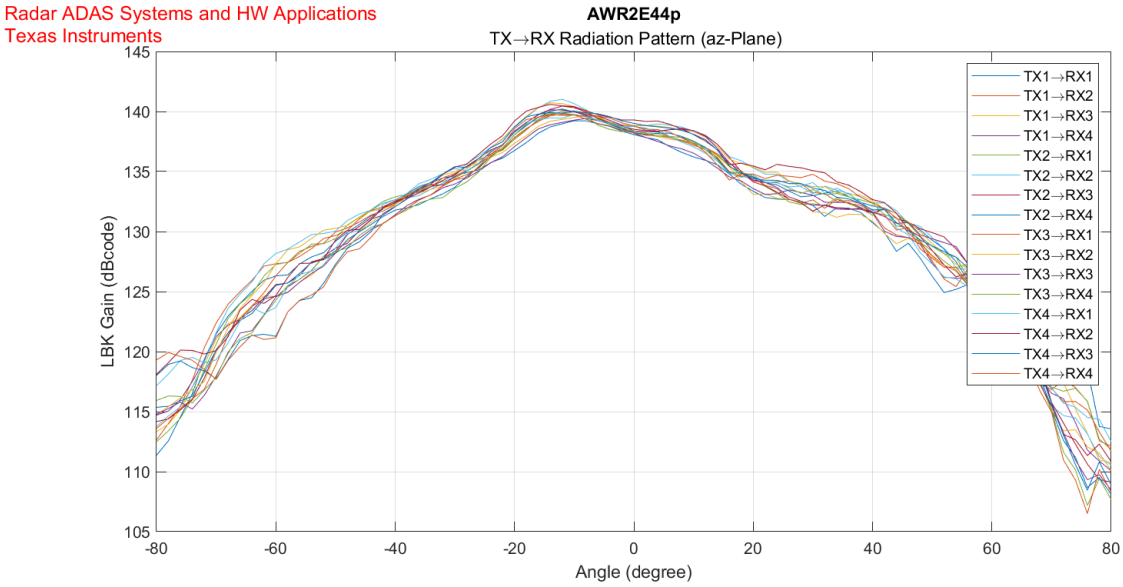


Figure 2-13. Azimuth Radiation Pattern (77GHz to 80GHz)

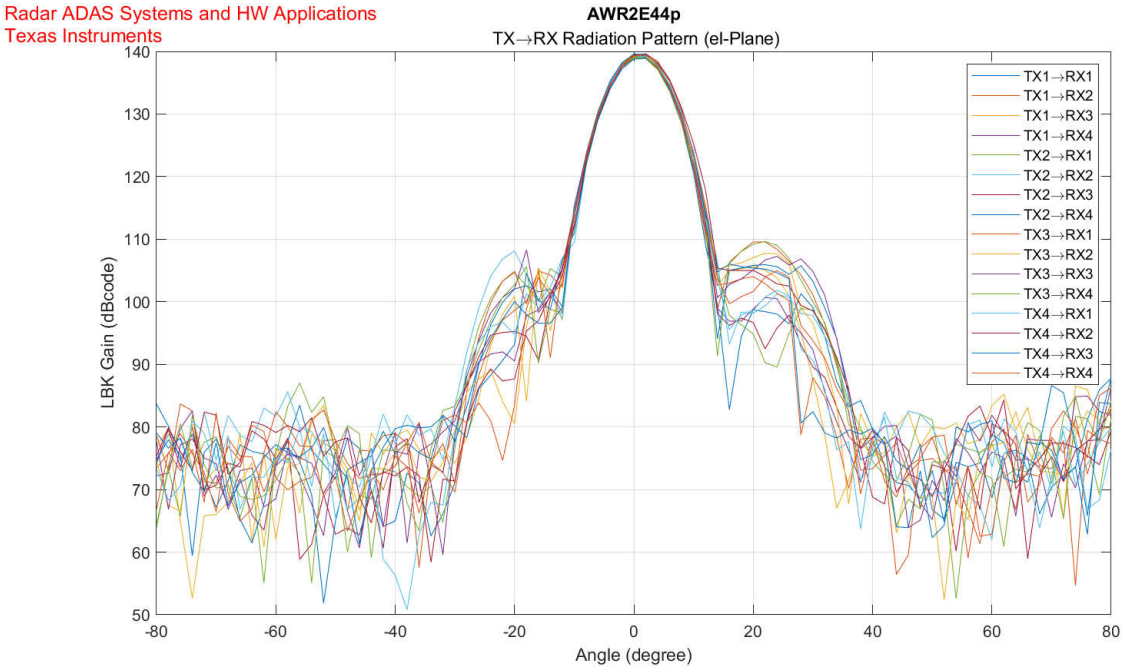


Figure 2-14. Elevation Radiation Pattern (77GHz to 80GHz)

2.5 PMIC

Power to the AWR2E44P is provided by the LP87745-Q1 PMIC. This is a functional safety compliant PMIC that supports ASIL-B/SIL-2 applications. For more details, visit the LP87725-Q1 product page (https://www.ti.com/product/LP87725-Q1).

2.6 On-Board Sensors

The AWR2E44PEVM provides access to an on-board temperature sensor (TMP112AIDRLR) and four on-board current sensors (INA228AIDGST). These sensors can be controlled by the radar via I2C. For details about the I2C addresses of these sensors, refer to Section 2.9.3.

The current sensors are designed to measure the current being supplied to the various power rails of the AWR2E44P device. For details on the supply nodes that can be measured using the current sensors, refer to Table 2-7.

Table 2-7. Current Sensor Supply Details

Reference Designator	Supply Node	PCB Net Name	I2C Address
U9	AWR 1.2-V Supply	1V2	0x40
U11	AWR 1.8-V Supply	1V8	0x41
U12	AWR 3.3-V Supply	3V3	0x44
U22	AWR 1.0-V Supply	1V0	0x42

2.7 PC Connection

The PC connectivity is provided via two micro USB connectors, J8 and J10.

2.7.1 XDS110 Interface

J8 provides access to the onboard XDS110 (TM4C1294NCPDT) emulator. This connection provides the following interfaces to the PC:

- JTAG for CCS connectivity
- MSS logger UART (can be used to get MSS code logs on the PC)

When the J8 USB is connected to the PC the device manager should recognize two XDS110 COM ports under Ports (COM & LPT).

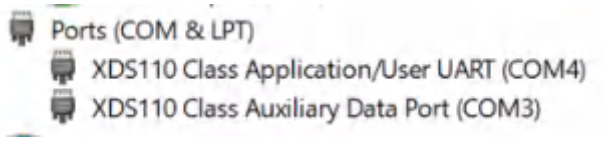


Figure 2-15. XDS110 COM Ports

XDS110 debug probe and data port are detected under Texas Instruments Debug Probes.

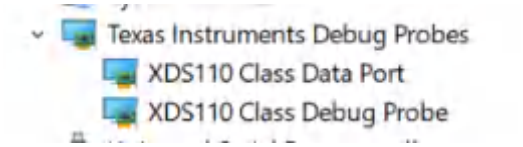


Figure 2-16. TI Debug Probes

If the PC is unable to recognize the above COM ports, install the latest EMUpack.

2.7.2 FTDI Interface

J10 provides access to the onboard FTDI ports. This provides the following interfaces to the PC:

- FTDI Port A -> MSS_SPIA interface
- FTDI Port B-> MSS_I2C interface; Host INTR signal.

- FTDI Port C -> BSS_UART port; DSS_UART port (not populated by default); NRESET and WARMRST control signals.
- FTDI Port D -> MSS_RS232 port; SOP0, SOP1, and SOP2 control signals

When the USB is connected for the first time to the PC, Windows® maybe not be able to recognize the device. This is indicated in the device manager with yellow exclamation marks, as shown in Figure 2-17.

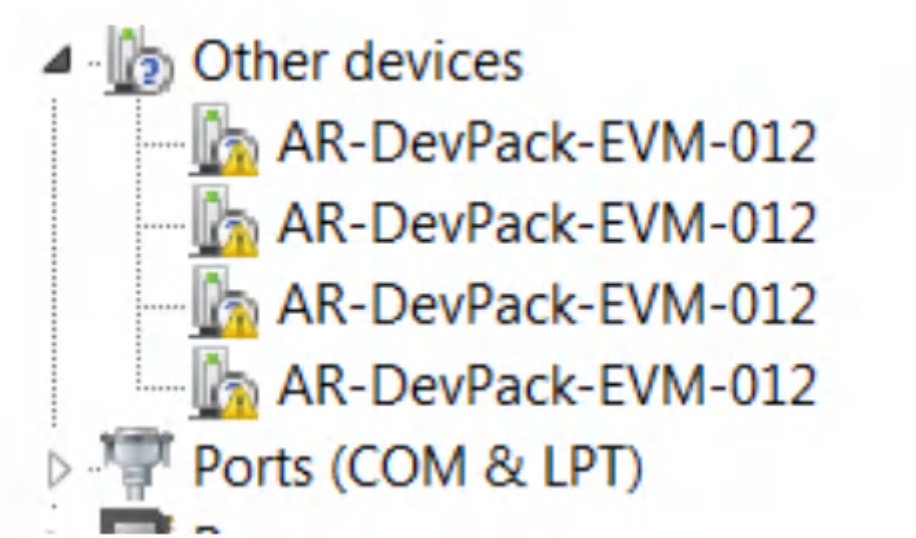


Figure 2-17. Uninstalled FTDI Drivers

To install the devices, download the latest FTDI drivers available in the mmWave SDK package. Right click on these devices, and update the drivers by pointing to the location where the FTDI drivers were installed (**C:\ti\mmwave_mcuplus_sdk_<version_number>\mmwave_mcuplus_sdk_<version_number>\tools\ftdi**). This must be done for all four COM ports. When all four COM ports are installed, the device manager recognizes these devices and indicates the COM port numbers, as shown in Figure 2-18.

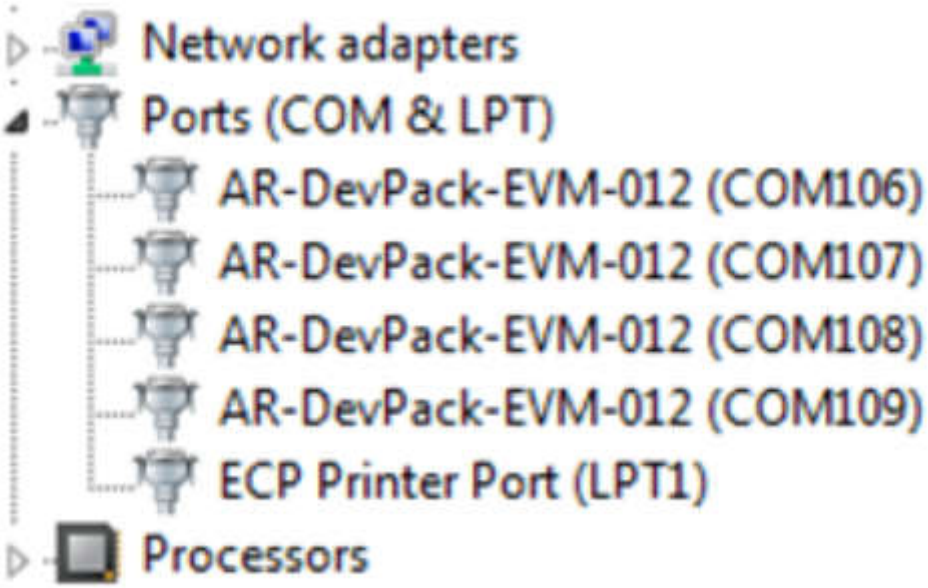


Figure 2-18. Installed FTDI Drivers

2.8 Connecting the AWR2E44PEVM to the DCA1000 EVM

The AWR2E44PEVM can be connected to the DCA1000 EVM platform to allow for LVDS data streaming. Figure 2-19 shows the AWR2E44PEVM interfaced to the DCA1000 EVM.

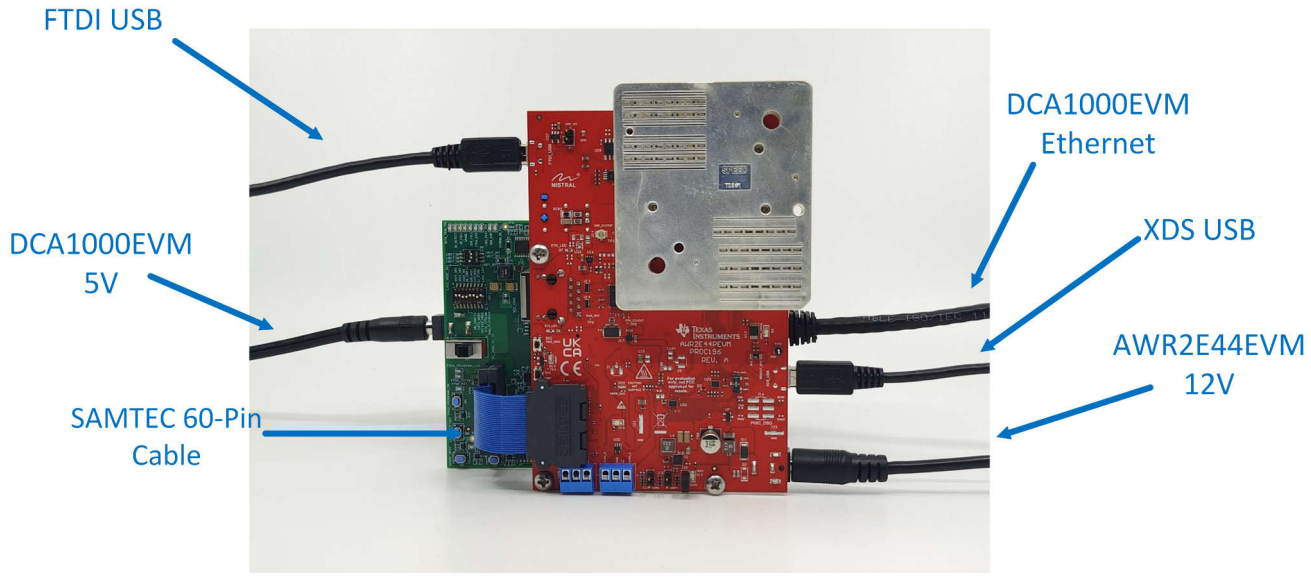


Figure 2-19. AWR2E44PEVM and DCA1000 EVM

When using the AWR2E44PEVM with the DCA1000 EVM and mmWave Studio, the following settings must be used.

1. Set the AWR2E44PEVM to SOP2 mode.

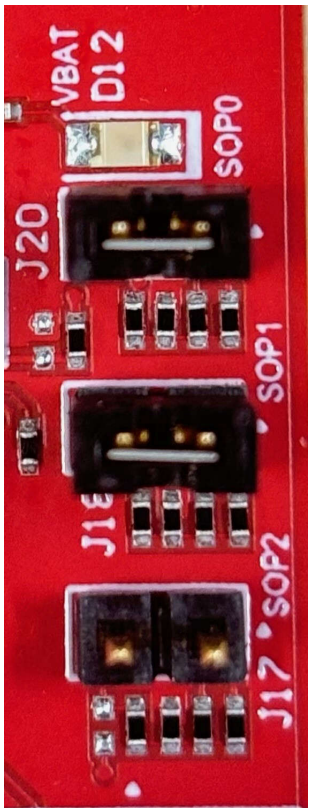


Figure 2-20. SOP2 Mode

2. Set the AWR2E44PEVM switch S2 to FTDI_SPI Mode

Figure 2-21. SPI_MUX

3. Set the DCA1000 EVM switches to the following configuration.

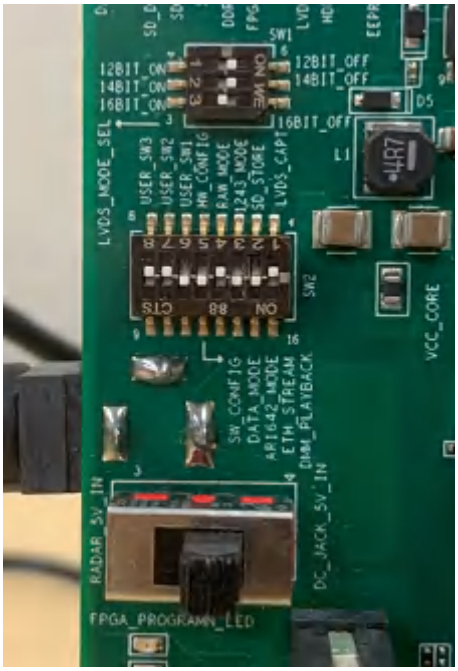


Figure 2-22. DCA1000 Switch Settings

4. The 5-V/12-V supply must be connected to J12 on the AWR2E44PEVM
5. A 5-V supply must be connected to J2 on the DCA1000 EVM **(Do Not Exceed 5-V)**
6. A micro USB cable must be connected to the FTDI port on the AWR2E44PEVM (J10)
7. The Samtec ribbon cable must be connected to J7 on the AWR2E44PEVM and J3 on the DCA1000 EVM
8. An RJ45 cable must be connected to J6 on the DCA1000 EVM

2.9 Jumpers, Switches, and LEDs

2.9.1 Switches

The AWR2E44PEVM contains two switches to mux various interfaces to different connectors on the EVM.

Table 2-8. MUX Switches

Reference	Usage	Comments
S1	JTAG	When set to ‘MIPI’ position, the JTAG interface is routed to the MIPI 60-pin connector (J19). When set to ‘XDS’ position, the JTAG interface is routed to the XDS110 USB interface (J8)
S2	SPI	When set to ‘DBG_SPI’ position, the MSS_SPIB interface is routed to the debug connector (J7). When set to ‘FTDI_SPI’, the MSS_SPIB interface is routed to the FTDI USB port (J10)

2.9.2 Sense On Power (SOP) Jumpers (J17, J18, J20)

The AWR2E44PEVM can be set to operate in different modes based on the state of the SOP [2:0] lines. These lines are sensed ONLY during boot up of the AWR2E44P device. The state of the device is described in Table 2-9.

A closed jumper refers to a '1' and open the jumper refers to a '0' state of the SOP signal going to the AWR2E44P device.

Note

The SOP[2:0] pins can also be controlled via the on-board FTDI. In this case the FTDI settings would override the jumper settings.

Table 2-9. SOP[0:2] Modes

Reference	Usage	Comments
J17 (SOP 2), J18 (SOP 1), J20 (SOP 0)	SOP[2:0]	101 (SOP mode 5) = Flashing mode 001 (SOP mode 4) = Functional mode 000 (SOP mode 3) = Reserved 011 (SOP mode 2) = Development mode 010 (SOP mode 1) = Reserved

Figure 2-23. SOP Jumpers

Additionally, the SOP[4:3] signals defines the XTAL clock input as per the below configurations provided in Table 2-10.

Table 2-10. SOP[4:3] Modes

Reference	Usage	Comments
R303, R312 Populated. R301,R309 unpopulated	SOP[4:3]	00 = 40MHz
R301, R312 Populated. R303,R319 unpopulated		01 = 45.1584MHz
R303, R309 Populated. R301,R312 unpopulated		10 = 49.152MHz
R301, R309 Populated. R303,R312 unpopulated		11 = 50MHz **(Default State)**

2.9.3 I2C Connections

The board features temperature sensor for measuring onboard temperature, current sensors for current measurement for 1.2V, 1.8V, 3.3V, 1V0_RF1, and 1V0_RF2 AWR2E44P supply rails and EEPROM for storing board ID. These are connected to the AWR2E44PEVM through I2C bus.

Table 2-11 shows the list of I2C devices available in AWR2E44PEVM board and the address.

Table 2-11. I2C Device Addresses

Sensor Type	Reference Designator	Part Number	Target Address
Temp sensor	U24	TMP112AIDRLR	0x49
Current sensor for 3.3-V rail	U12	INA228AIDGST	0x44
Current sensor for 1.8-V rail	U11	INA228AIDGST	0x41
Current sensor for 1.2-V Digital rail	U9	INA228AIDGST	0x40
Current sensor for 1.0-V RF1 rail	U22	INA228AIDGST	0x42
Current sensor for 1.0-V RF2 rail	U30	INA228AIDGST	0x43
EEPROM	U28	CAV24C02WE-GT3	0x50

2.9.4 Push Buttons

Table 2-12. Push Button Switches

Reference	Usage	Comments
SW1	RESET	This Switch is used to RESET the AWR2E44P, PMIC, XDS110 and FTDI device.
SW2	GPIO_28	When pushed, the GPIO_28 shall be pulled to High.

2.9.5 LEDs

Table 2-13. On Board LEDs

Ref	Color	Usage	Comments
D12	Green	12-V supply indication	This LED indicates the presence of 12-V supply input
D13	Yellow	NRST	This LED is used to indicate the state of NRST pin. If this LED is glowing, the device is out of reset.
DS2	Red	NERROUT	Glows if there is any HW error in the AWR2E44P device
D9	Yellow	WRMRST	Open drain fail safe warm reset signal
D6	Green	GPIO_2	Glows when the GPIO_2 is logic-1
D1	Yellow	FTDI_SUSPEND_N	Glows when FTDI is in suspend state

3 Software

3.1 Software, Development Tools, and Example Code

To enable quick development of end applications on the on-chip the on-chip ARM® Cortex®-R5F controller and hardware accelerator (HWA 2.1), TI provides a software development kit (SDK) that includes demo codes, software drivers, emulation packages for debug, and more. These can be found at mmwave-sdk. User can find other set of application, tools, experiments over TI's Resrouce Explorer (Radar Toolbox).

4 Hardware Design Files

4.1 Design Files

To view the schematics, assembly drawings, and BOM, see AWR2E44PEVM Schematic, Assembly Files, and BOM.

To view the design database and layout details, see AWR2E44PEVM Database and Layout Files.

5 Additional Information

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
Nov 2024	*	Initial Release

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