Application Report

SimpleLink™ Wi-Fi® CC32xx ADC

ABSTRACT

This application report is divided into two parts. The first part gives an overview of the functionality of the ADC and its implementation in the CC3220. It also explains of the Successive-Approximative-Register (SAR) ADC architecture that is used the CC3220 and other devices in the SimpleLink™ platform. The second part gives some examples of different ways this peripheral can be used as well as design considerations given the characteristics of this ADC.

The CC3220 device is part of the SimpleLink microcontroller (MCU) platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, and host MCUs. All share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink platform enables you to add any combination of the portfolio's devices into your design. The ultimate goal of the SimpleLink platform is to achieve 100 percent code reuse when your design requirements change. For more information, visit www.ti.com/simplelink.

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Trademarks

1 Introduction

1.1 Basics of the SAR ADC Architecture

The Successive-Approximation Register Converter or the SAR ADC is essential to general-purpose mixed signal circuits. SAR ADCs are common in data acquisition applications such as power monitoring and low to medium frequency analysis. SAR ADCs offer moderate speeds of up to 4 mega samples per second while also offering medium to high resolutions with a high level of DC and AC accuracy. One of its most appealing advantages is the negligible to zero latency and low power consumption which makes it ideal for battery-powered applications. For most SAR ADCs power consumption is directly proportional to the sampling rates, so configurations at lower sampling rates allows for ultra-low power consumption.

The SAR conversion process consists of two phases: The sampling phase and the conversion phase. During the sampling phase switch S_2 opens and switch S_1 closes. The analog input signal Vin then charges the sampling and hold capacitor CSH to the voltage level of the input. Once this acquisition phase is complete switch S_1 opens and switch S_2 closes, disconnecting the sample and hold capacitor from the external circuit. C_{SH} is then connected to the internal comparator and the conversion phase begins.

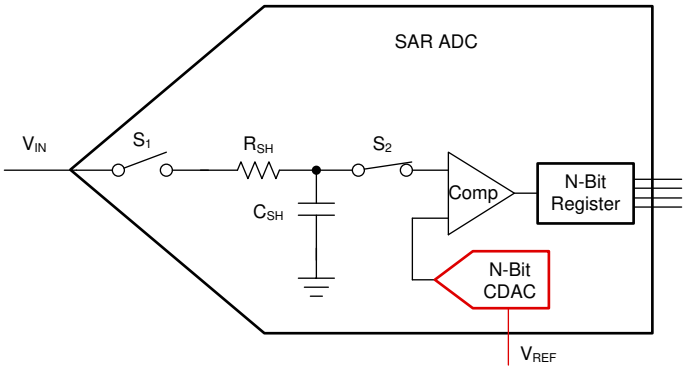

Figure 1-1. Simplified SAR ADC Internal Architecture

The N-bit search stack produces binary weighted analog voltages proportional to a reference as each bit decision is made in the binary weighted search. The binary search starts with the most significant bit decision and the tests are repeated for each binary weighted bit until the least significant bit decision is made. The value of each binary weight bit is based on whether the analog input signal is higher or lower than the DAC voltage. The successive approximation register provides the digital code to the internal DAC during each conversion clock cycle. The conversion time is a function of the conversion clock frequency and the resolution of the ADC. . Depending on the specific SAR ADC circuit, the initial voltage on a sample and hold capacitor during the next sampling phase may be reset to a midpoint voltage where it may keep value on the latest sample voltage. The device will trigger the next conversion after the next start conversion signal is received.

To learn more, see the TI Training: Choosing the Best ADC Architecture for Your Application.

1.2 Introduction to the CC32XX ADC

1.2.1 Main Features

The CC32xx provides a general purpose, multi-channel Analog-to-Digital Converter (ADC). Each of the ADC channels supports 12-bit conversion resolution with sampling periodicity of 16 uS (62.5 Ksps/channel). Each channel has an associated FIFO and DMA. For detailed electrical characteristics of the ADC, refer to the CC3200 data sheet (SWAS032).

- Total of 8 channels:
  - 4 external analog input channels for user applications
  - 4 internal channels reserved for SimpleLink subsystem (network and Wi-Fi).
- 12-bit resolution
- Fixed sampling rate of 16 µs per channel. Equivalent to 62.5K samples/sec per channel
- Fixed round-robin sampling across all channels
- Samples are uniformly spaced and interleaved. Multiple user channels can be combined together to realize higher sampling rate. For example, all four channels can be shorted together to get an aggregate sampling rate of 250K samples/sec.
- DMA interface to transfer data to the application RAM; dedicated DMA channel for each channel.
- Capability to timestamp ADC samples using 17-bit timer running on a 40-MHz clock. The user can read the timestamp along with the sample from the FIFO registers. Each sample in the FIFO contains actual data and a timestamp.

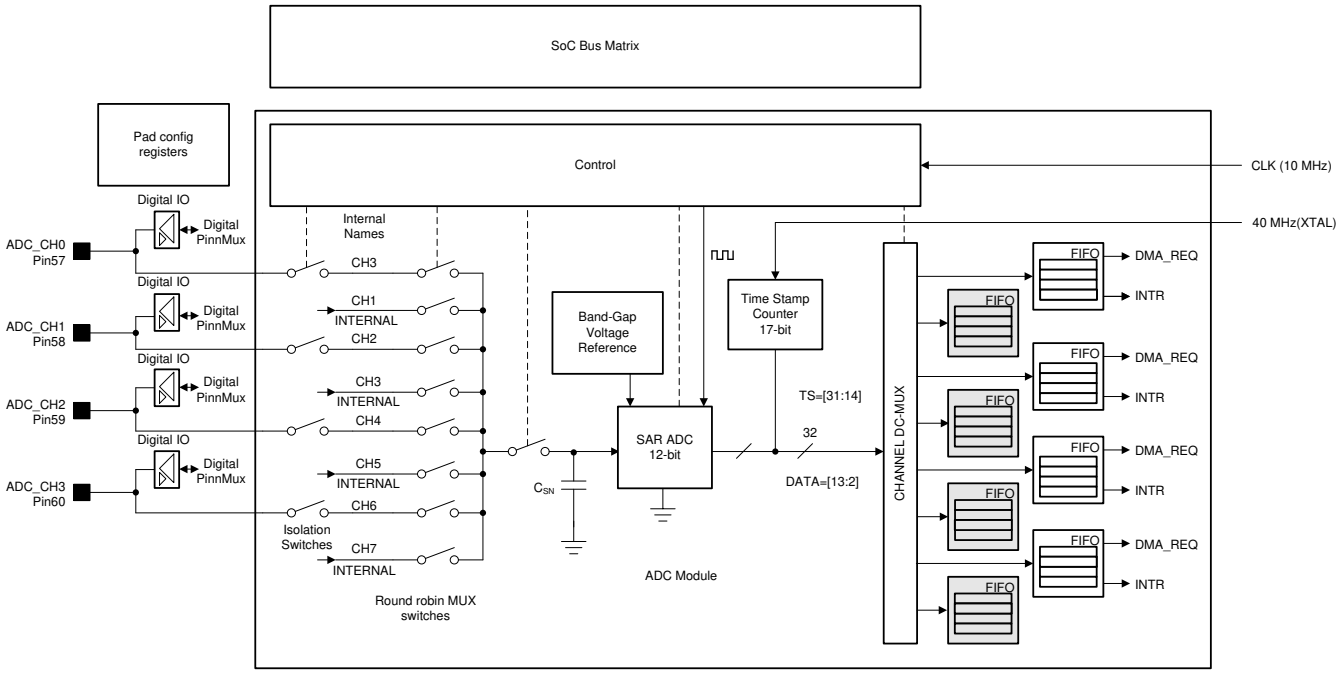

Figure 1-2. Architecture of the ADC Module in CC32xx

1.2.2 ADC Sampling Operation

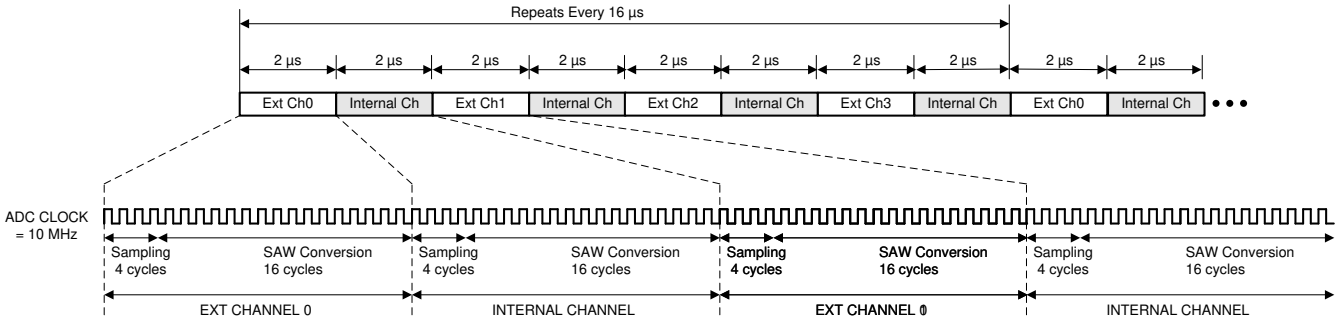

Figure 1-3. Operation of the ADC

The ADC sequencing process integrates the system interfaces with the SAR ADC modules. The full ADC module supports eight channels, but it uses a Time Division Multiplexing scheme for ADC sample selection. So while the internal ADC operates at 500 Ksps, this round robin behavior across eight channels creates an effective sample rate of 62.5 KHz at each pin. This sampling rate is static for the CC3220 ADC and always collects samples at 62,500 KSPS.

FIFO is used because of the Round Robin behavior of the ADC sampler. ADC Data register changes as it goes through the round robin process, so data is loaded into the FIFO specific to that channel. The FIFO for each channel holds up to 4 words where bits 13:2 hold the ADC sample bits and bits 30:14 has the timestamp for each ADC sample. The FIFO is a buffer, which operates in a first in first out principle. It receives data from from SAR ADC. The FIFO goes into overflow when a write is attempted to a full FIFO, this is due to the software being too slow. The content of the full FIFO is updated with new samples even after FIFO FULL. During FIFO overflow, it is still possible to read data from the FIFO. The FIFO goes into underflow when a read is attempted from an empty FIFO, this is due to software (too many read accesses). After an underflow, it is still possible to write and once the FIFO is no longer empty, it's possible to read from FIFO.

1.2.3 ADC Additional Information

The inputs to the ADC are required to be well within 1.4 V to avoid clipping, which will cause distortion. The ADC inputs can be damaged if an input voltage higher than 1.8 V is applied to these pin. The 1.8 V hard limit must be considered from both the software and hardware points of view. Always add a resistor divider/buffer to bring down the measurement signal voltage to within the ADC limits.

The internal circuit of the ADC alone is stated in the data sheet. However, in addition to the sampling capacitors, there are additional muxes in the path that add their own capacitance. All of this capacitance adds in parallel to create an equivalent capacitance of about 12 pF at the device pin.

For more information on CC32xx ADC characteristics, see the CC3220R, CC3220S, and CC3220SF SimpleLink™ Wi-Fi® Single-Chip Wireless MCU Solutions Data Sheet.

2 ADC Application Examples

2.1 Battery Voltage Measurements

The most obvious way to think about an ADC is to picture it as a multimeter. Apply an input voltage to the pin , configure the ADC to read the pin, read the output register and then convert it to an equivalent voltage using the expression V = code * Vref/2^N where, Vref is the reference voltage(1.467V), N is the number of bits (N = 12) and code refers to the output of the ADC read back from the internal register. Note that the bits 13:2 are the actual ADC codes.

Though this assumption is true to some extent, there are some pitfalls.

- The multimeter offers a high impedance input under all conditions whereas the ADC does draw current from the input.
- The multimeter does some averaging on the input signal, whereas, the ADC is a spot measurement. These two characters make the ADC a bit difficult to work with. Figure 2-1 shows the recommended example for using our ADC to measure DC voltage.

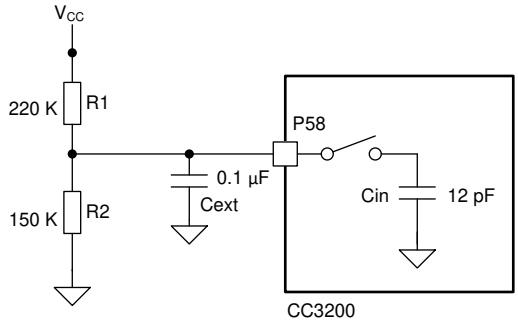

Figure 2-1. ADC Configuration

With the above circuit, the external capacitor gets charged to 1.34 V through the resistor divider while the ADC is not connected to the pin. When the ADC is connected to the pin, the internal capacitor starts to charge from the external capacitor. Since the switch resistance is negligible and the external capacitor is quite large compared to the internal one, the 12 pF cap can charge to the final value of 1.34 V.

The external capacitor is calculated based on the following calculation. Assuming that the Cin is charged from Cext fully, this will result in a charge re-distribution. Assuming that the entire charge is supplied from the Cext, we should not let the Cext voltage drop below 1LSB of the ADC. So the following can be calculated:

Cext = Cin x 4096, which gives 50 nF. For margin, it can be assumed that 2x the calculated value and use 100 nF (0.1 µF).

For more instructions on how to run this example, see the CC32xx SDK and the ADC single channel example.

2.1.1 Important Considerations

2.1.1.1 Extra Current Draw

The equivalent resistance of R1 + R2 in series draws a current of Vcc/(R1 + R2) = 3.3V/370K ~= 9 µA. If the current draw is a concern, you may be tempted to simply increase the resistor values. However, this slows down the re-charging of the capacitor Cext after the pin is disconnected from the ADC.

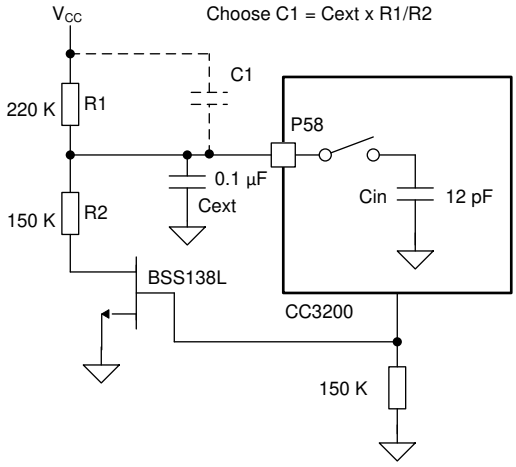

Figure 2-2. Reducing Resistive Current Draw

An alternative is to disconnect R2 from the circuit by using an NMOS transistor controlled by the CC32xx device. This circuit is shown in Figure 2-2. In this circuit, an additional optional capacitor is shown (C1) that can be used to improve the overall frequency response and speed up the charging time. This capacitor, along with R1, R2, and Cext, work as a compensated attenuator. Note that this arrangement will not offer any noise filtering and should be used with caution.

2.1.1.2 Droop Correction

Note that the internal ADC is continuously running and if the ADC is connected to the external pin, continuous current will be drawn from the external capacitor. This will cause the external capacitor to drop down the voltage with time. Each sample causes a charge re-distribution between the external capacitor Cext and the internal Cin, which causes the Cext to discharge. This will cause a measurement error.

Hence, for the DC measurement, the ADC pin should be disconnected immediately after the measurement is completed to allow the Cext to recover. This can be done by calling APIs (ADCChannelEnable() / Disable()) or changing pix-mux to GPIO. The above graph shows an example measurement using the ADC pin 58. The resistors are used as mentioned in the above sections with 0.1 µF capacitor.

Assuming the Cext is fully charged to V1 = R2/(R1+R2) x Vcc, each sample draws approximately Q = Cin x V1 charge from Cext. Assuming N samples are taken, the Cext loses NxCin x V1 charge. The voltage drop in the Cext can be calculated by the formula shown in Equation 1:

$$V_{DROP} = \frac{N \times C_{IN} \times V1}{Cext.\,(volts)} \tag{1}$$

In this example, by taking 128 samples, the Cext capacitor will drop by about 20 mV.

If a simple averaging function is used in the measurement, the measurement error would be Vdrop/2 = 10 mV. While this may be acceptable for most applications, it can be improved further by using the methods shown in the following sections.

2.1.1.3 Offset Adjustment

Based on the chosen capacitor value and the approximate value of Vcc, the expected Vdrop across N samples can be calculated by using Equation 1. Then, the Vcc can be estimated as shown in Equation 2.

$$V_{CC} = \frac{V_{AVG} + V_{DROP}}{2} \quad (2)$$

The method can be recursively used to improve the value of Vcc, if there is no prior information on Vcc.

2.1.1.4 Least Squares Fit

Using the set of values obtained from the ADC, say (Vi, ti) where i = 0,1,2.....N-1, the curve of V = F(t) can be estimated.

With that curve, the initial value of V(t) can be estimated. Although this method is more mathematically intensive, it yields be best estimate of the voltage in presence of high noise.

2.1.1.5 Choosing the Capacitor (for droop correction)

The capacitor chosen should be linear in the entire operating voltage range, that is, the capacitance should remain constant over the operating voltage range for the voltage droop calculations to hold. It is recommended to use a tantalum or a film type SMT capacitor for this application. Ceramic multilayer capacitors are prone to capacitance change with voltage. (The capacitance can drop up to 50% with only a few volts DC). If the end user is not implementing the DC offset correction using the droop calculation, then any capacitor can be used.

Also derating the capacitance by choosing one with a very high voltage rating is an option. In this case, the max voltage is 1.4V at the ADC input and we can chose a 16 V capacitor. This will reduce the capacitance change with voltage.

2.1.1.6 First Measurement

The first measurement of the ADC for the battery voltage needs to take into account the charging time of the capacitor. Assuming that the input is a step with a fast rise time (usually few ms which can be ignored), the time taken for the capacitor can be estimated from the simple capacitor charging equation. In this specific case, the charging time to reach 1% accuracy is about 45 ms. This has to be taken into account during the measurements. The wake-up from power on RESET for the CC32xx device is at least 1.1sec. So that gives more than enough time for the voltage at the capacitor to settle to its final value.

2.1.1.7 Time Between Measurements

Once the battery voltage is measured, the ADC is disconnected from the pin which enables the resistor to charge back from the resistor divider. The time taken to charge back has to be again estimated from the RC charging equation.

V(t) = Vo + V x (1-e^(-t/RC)) where Vo is the voltage at the time of disconnecting the pin and V is the thevenin equivalent voltage.

For this example, assuming V(t) to reach within 1 LSB of the ADC code, and Vo to be 1.28 V.

3 AC Measurements

As noted in the case of battery monitoring, the use of external resistor divider and capacitor severely restricts the bandwidth of measurement. This method is not suitable for AC signals that can have the bandwidth all the way to the Nyquist limit of Fs/2 or 31 KHz in this ADC. In order to drive the input, a suitable ADC buffer needs to be used. There are several application notes available on the internet in choosing the right OPAMP depending upon the bandwidth, accuracy, offset, linearity and drift requirements. It is recommended for the user to select the OPAMP driver based on their requirement by referring to the application notes below.

Input Drive Circuitry for SAR ADCs

Optimize Your SAR ADC Design

4 Useful References

4.1 Smart Thermostat

Information about Smart Thermostat

- Smart Thermostat TI Design with SimpleLink Wi-Fi Video
- SimpleLink™ Wireless MCU-Based Thermostat Reference Design (TIDM-1020)

4.2 Measuring Air Quality With the Winsen MP503 Analog Sensor

The air quality is measured through an analog sensor, Winsen MP503, that can be connected to the Grove BoosterPack. The CC3220x ADC runs at a sampling rate of 62.5 KSPS. By default in this design, the ADC is enabled and read every two seconds. The last four readings are averaged to get the actual value for the air-quality measurement. End-equipment developers can add an appropriate signal conditioning algorithm for the analog sensors.

4.3 Touch Position Detection With HMI Through Resistive Touchscreen

For more information, see *CC3220 SimpleLink™ Wireless MCU Based Thermostat+BLE Provisioning Reference Design*.

The resistive touchscreen is composed of two conductive layers separated by a gap and an insulated layer below. The two top conductive plates are coated with conductive material that provides uniform resistance across the layer. When a voltage is applied to the layer, it produces a uniform linear gradient of voltage. When the screen is touched, the pressure from the touch forces the two conductive layers to come in contact. By applying different voltage to the two conducing planes, the point of touch can be determined.

The smart thermostat uses the GPIOs and 2 channels of the ADC to read the X and Y position of the touchscreen. Multiplexing of the pins for the measurement is dynamically done. The resistors on the board must be modified to match the supply voltage.

5 References

- Texas Instruments: *Precision Analog Applications Seminar*
- Texas Instruments: *Title1 CC3220 SimpleLink™ Wireless MCU Based Thermostat+BLE Provisioning Reference Design*

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