Application Report

SWRA591–April 2019

Wide-Band DSSS Mode for FCC Digital Transmission Systems Using CC13x0

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ABSTRACT

This application report describes a wide-band modulation scheme to comply with the requirements of FCC section 15.247 for non-frequency hopping digital modulation systems utlizing datarates below 500kbps. The scheme is implemented with an MCE patch, which is a standalone program that implements the various options of the Wide-Band Direct Sequence Spread Spectrum (WB-DSSS) scheme. The patch is included in the CC1310 SDK and can be setup to be imported in the final application by Code Export option of SmartRF™ studio. This SDK can be downloaded from: http://www.ti.com/tool/SIMPLELINK-CC13X0-SDK.

The implementations and summary of performances measured on CC13x0EM [5] are provided in this document.

Contents

List of Figures

List of Tables

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1 Introduction

WB-DSSS uses a well-known method to obtain sensitivity gains by means of coding and spreading the information bits into a series of transmitted symbols.

The transmit spectrum requirements of FCC Section 15.247 for digital transmission systems operating in the 902 MHz - 928 MHz band are as follows:

- The minimum 6 dB emission bandwidth of the signal shall be at least 500 KHz.
- The maximum peak conducted output power for transmitter is +30 dBm (1 Watt).
- The maximum power spectral density is limited to 8 dBm in any 3 KHz band segment within the emission bandwidth during any interval of continuous transmission.

1.1 Acronyms Used in This Document

Table 1. Acronyms and Descriptions

Acronym	Description
(G)FSK	(Gaussian) Frequency shift keying
AWGN	Additive White Gaussian Noise
SNR	Signal to Noise Ratio
BW	Bandwidth
DSSS	Direct Sequence Spread Spectrum
PER	Packet Error Rate
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
FEC	Forward Error Correction
MCE	Modem Control Engine
XOR	Exclusive OR

2 DSSS Encoding Scheme

The DSSS scheme is depicted in Figure 1. A convolutional encoder of rate ½ is followed by a DSSS with variable spreading length. The output of the module is fed into the 2-GFSK modulator to produce the modulated GFSK signal.

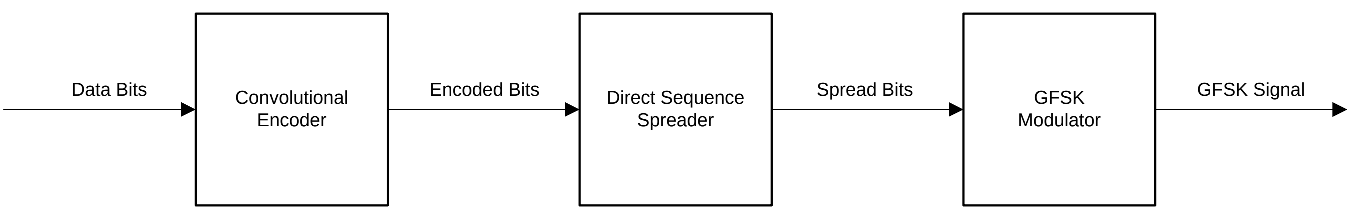

Figure 1. WB-DSSS Coding Scheme (the modulator is 2-GFSK)

The following subsections briefly discuss the workings of the first two main blocks shown in Figure 1.

2.1 Convolutional Encoder

Figure 2 shows the coder implemented in the DSSS modulation scheme. A convolutional encoder is defined by its rate, its constraint-length K (number of stages in the encoding shift register) and the connections between its internal states. The convolutional encoder used in this case has K=4 and only supports ½ rate (that is, for every input bit, the encoder produces two output bits).

The connections between internal states are a fundamental way of defining the code. The implemented encoder is based on non-systematic, non-recursive convolutional code.

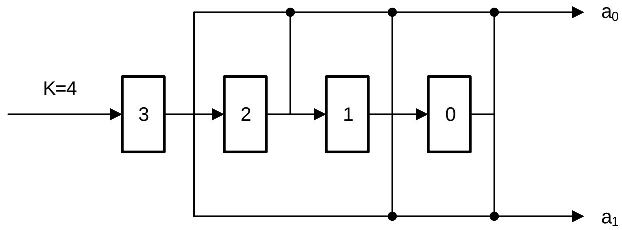

Figure 2. K=4, Rate = ½, Convolutional Encoder for WB-DSSS Modes

The black dots in Figure 2 represent logic XOR operations. The two output bits (a_0, a_1) from the encoder are serialized in a way that a_0 is transmitted first and a_1 is transmitted last.

2.2 Direct Sequence Spreader

The Direct Sequence Spreader assigns a known bit pattern to each of the incoming bits to the module. It can be considered a form of repetition code where a bit of duration t is replaced by M bits each of duration T_b. As a consequence, the rate at which information is transmitted is reduced by 1/M. If one wants to keep information rate constant, then the bit duration must be reduced by T_b/M, which subsequently increases the bandwidth by factor M. As a consequence the information bits are “chipped” into smaller duration symbols and are transmitted over the air. The ratio of symbol rate to the bit rate is called processing gain of a spread spectrum system.

The processing gain is the figure of merit that is considered when comparing narrow-band system to spread spectrum application. To appreciate intuitively how this improves the error performance we consider the slicer in a correlation receiver followed by a maximum likelihood (ML) decision block. In a DSSS system the block will make decisions on each symbol and then integrate the result over on information bit period. The probability of making a bit error therefore reduces when the bit is divided into many short duration symbols.

In the CC13x0 DSSS modes, the spreader length can be configured to be 1, 2, 4, and 8. Table 2 illustrates the bit mapping for each of the options.

The WB-DSSS scheme is implemented as 2-GFSK PHY with over the air symbol rate of 480 kbps.

Table 2. DSSS Spreading Codes

DSSS	'0'	'1'
1	'0'	'1'
2	'00'	'11'
4	'1100'	'0011'
8	'11001100'	'00110011'

3 Packet Format

A 5 byte preamble is used for testing and this is programmable. The payload in DSSS mode is byte oriented. Definition of packet lengths, headers, CRC, whitening follow the same rules as in the standard CC13x0 Generic FSK modes. The entire packet structure is illustrated in Figure 3.

Preamble	Sync Word	Payload	Termination
Variable	32 bits or 64 bits	N*8*2*DSSS bits	4*2*DSSS bits

Figure 3. WB-DSSS Packet Structure

The payload is encoded first by FEC and then spread through the DSSS block, as described in Section 2. In order to terminate the sequence, the modem automatically inserts four termination bits at the end of the payload with each termination bit resulting in 2*DSSS transmitted over-the-air symbols.

The relationship between data rate (the actual amount of information bits available to the higher protocol layers) and the symbol rate (the actual modulation rate used in the radio) can be expressed as:

$$\text{Data Rate} = \frac{\text{Symbol Rate}}{2 * \text{DSSS}} \quad (1)$$

4 Setting Up WB-DSSS in SmartRF Studio

The SmartRF studio contains the settings for the optimized WB-DSSS cases that can be tested from within the GUI. By launching the GUI and connecting CC13x0 launchpads with USB cable, the devices will show up in the GUI's console. From there, by clicking each one from the list of connected devices, the LaunchPads can be independently configured for TX and RX and a RF link test can be conducted.

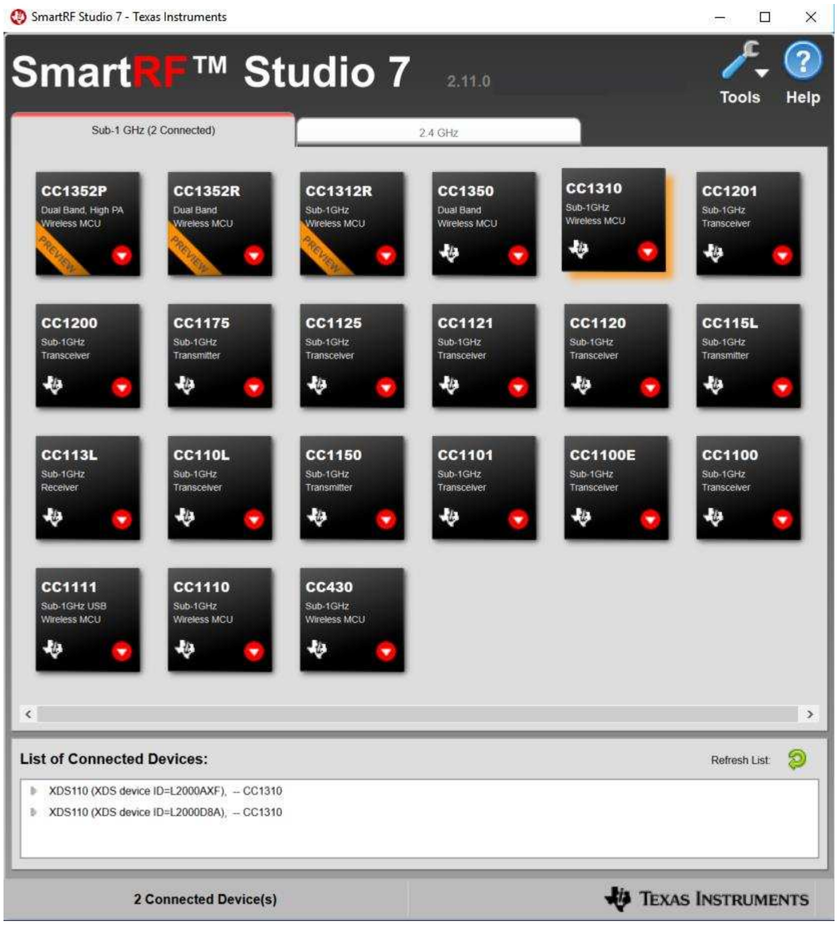

Figure 4. SmartRF GUI Showing Two CC1310 in List of Connected Devices

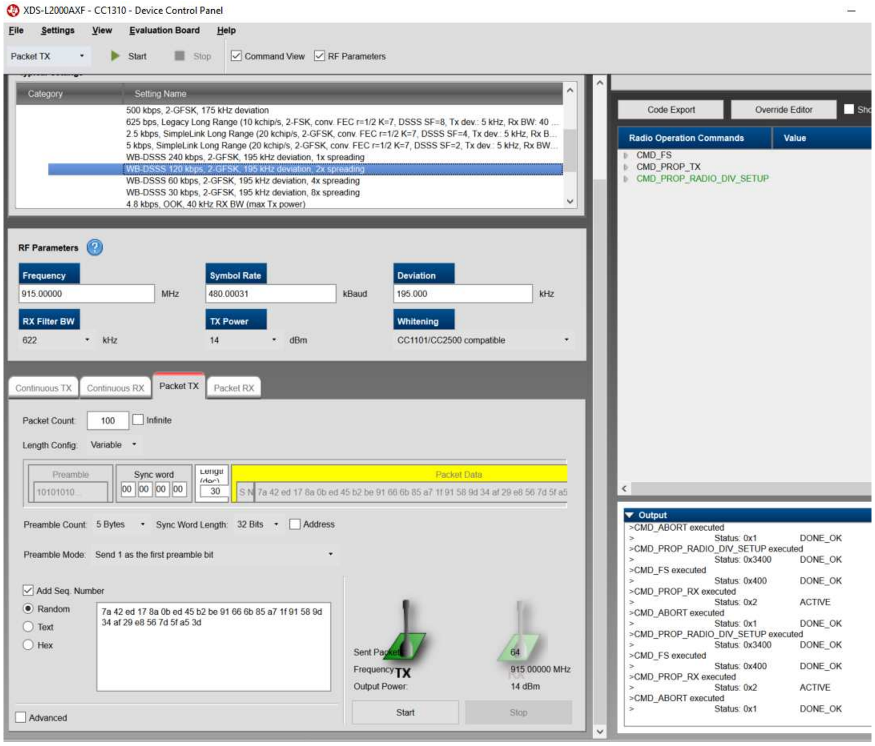

Figure 5. SmartRF Studio Showing WB-DSSS Setup in Transmit Mode

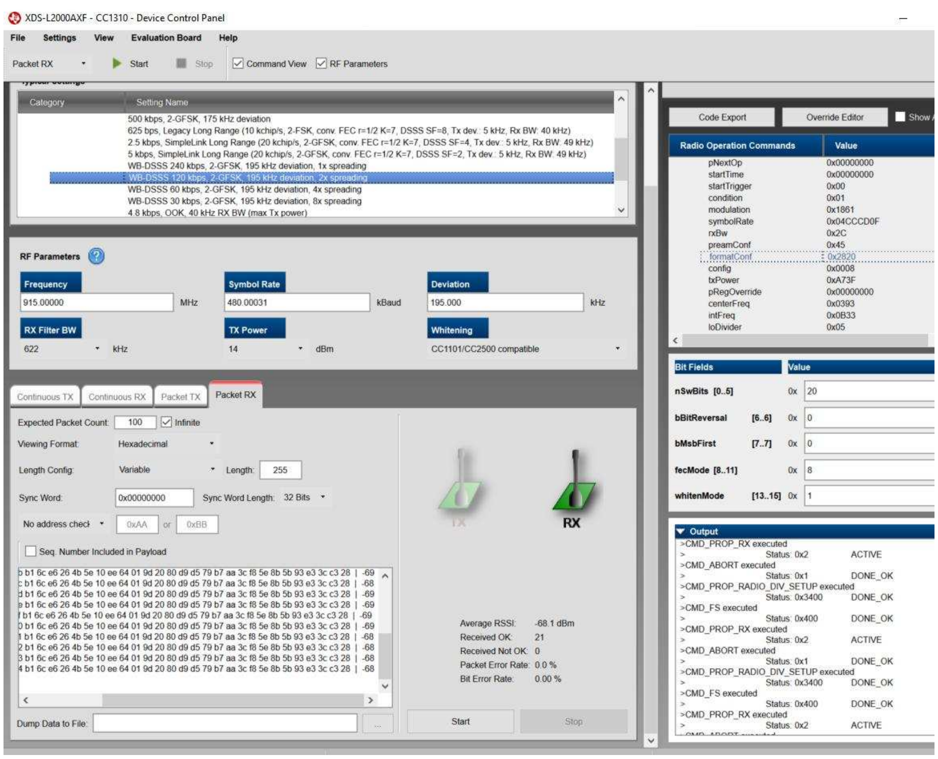

Figure 6. SmartRF Studio Showing WB-DSSS Setup in Receive Mode

Once the RF link has been tested to satisfaction, the settings can be exported and integrated into PacketRX and PacketTX examples in the SimpleLink SDK (see Section 5).

As default, the WB-DSSS settings in the SmartRF use fecMode = 0x8. In this mode, the sync word registers are not changed and the MCE patch handles everything pertaining to setting up the sync word. The CC13x0 WB-DSSS uses a 64-bit synchronization word with default value of 0x333C_3C33_3CC3_CCCC, LSB-first.

Alternatively, as shown in Figure 8 and Figure 9, the sync word can be modified by setting fecMode = 0x0. With this setting, only a 32-bit user defined syncword can be applied, which will replace the first 32 bits of the default sync word while retaining the rest (0x3CC3_CCCC will not change and will appear in the over the air packet). The SmartRF studio setup for testing this scenario is shown in Figure 8 and Figure 9.

Note that changing sync word can affect the BER performance and must be chosen with care.

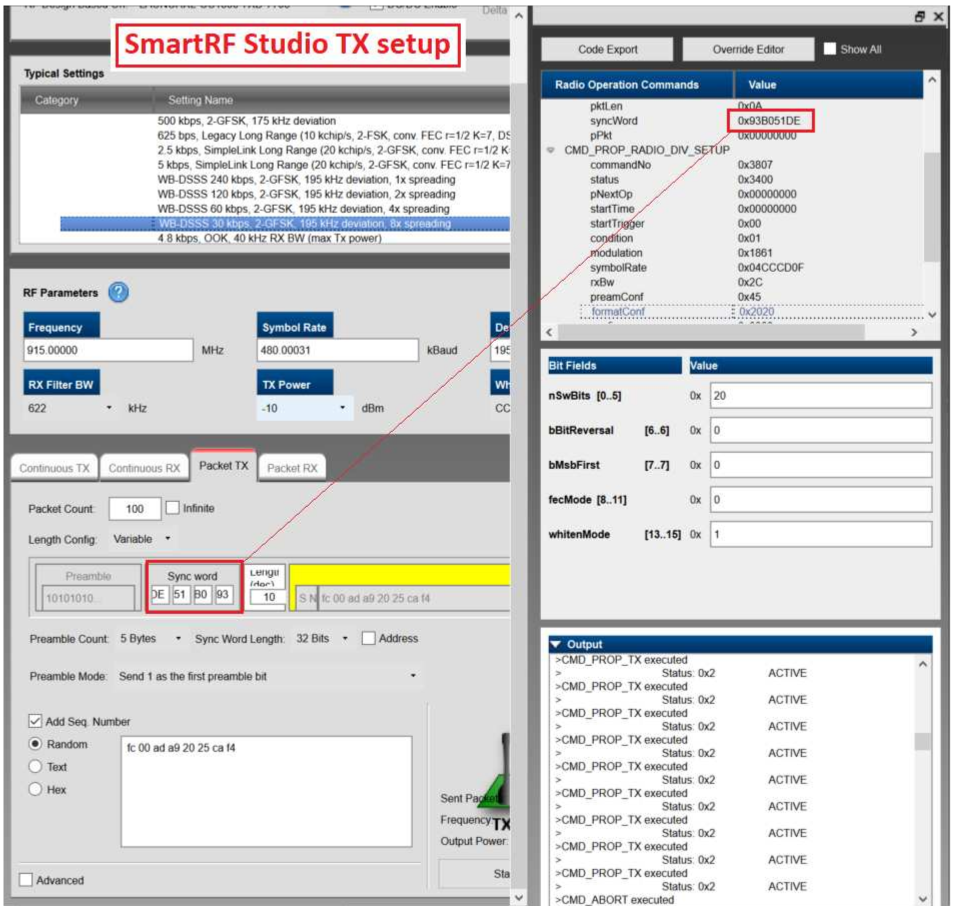

Figure 7. SmartRF Studio TX Setup Showing Configurable Sync Word

NOTE: Changing sync word can affect the BER performance and must be chosen with care.

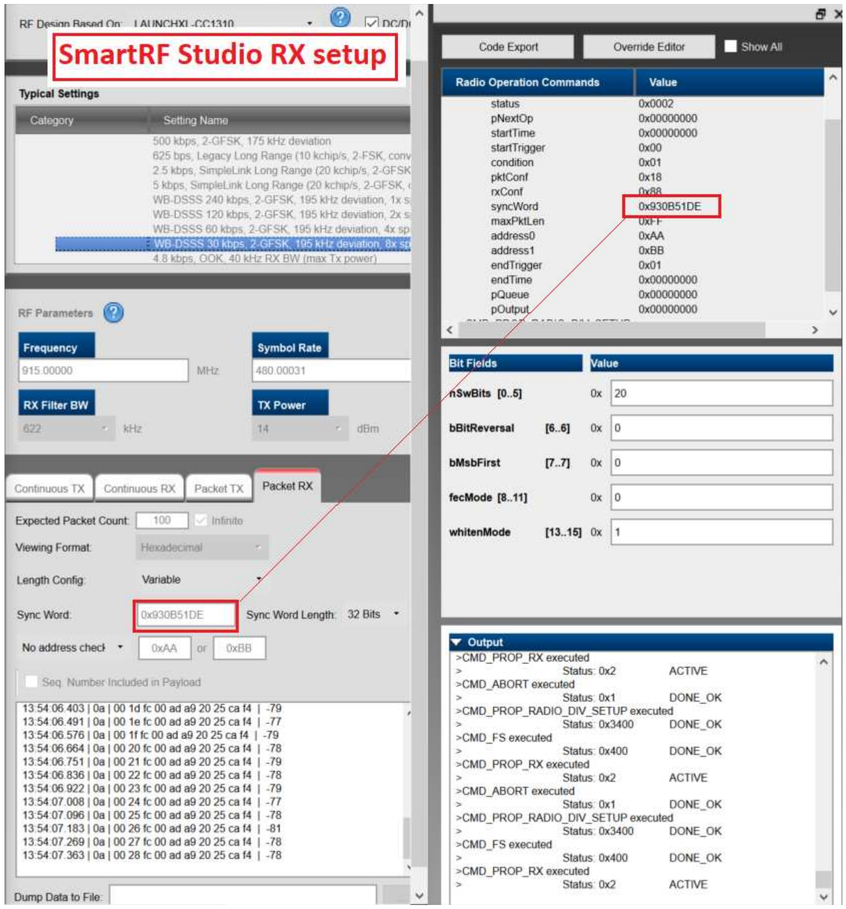

Figure 8. SmartRF Studio RX Setup Showing Configurable Sync Word

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NOTE: Changing sync word can affect the BER performance and must be chosen with care.

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5 Setting Up WB-DSSS in Code Composer Studio™

In the Simplelink SDK, there are working examples for setting up CC13x0 for evaluation. A working example for WB-DSSS scheme can be built by importing standalone rfPacketTx and rfPacketRx examples (see Figure 9) from the SDK and replacing their *smartrf_settings.c* and *smartrf_settings.h* files with those exported from the SmartRF studio. These files contain API configuration and overrides for radio parameters that are used for each DSSS modulation scheme.

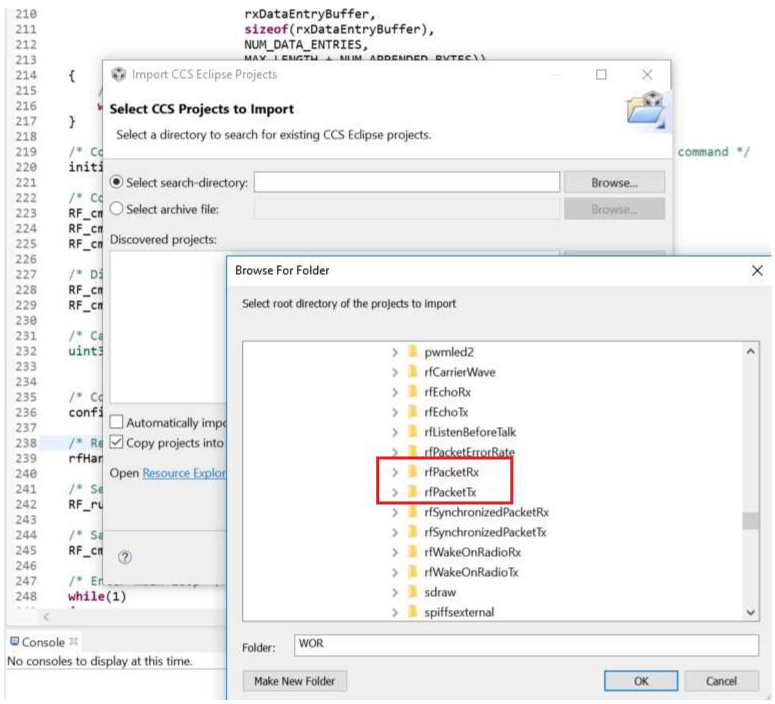

Figure 9. CCS Project Import Showing rfPakdetRX and rfPacketTX Examples

In Figure 10, make sure the file names correspond to the ones in the rfPacketRX/TX examples to avoid compilation errors.

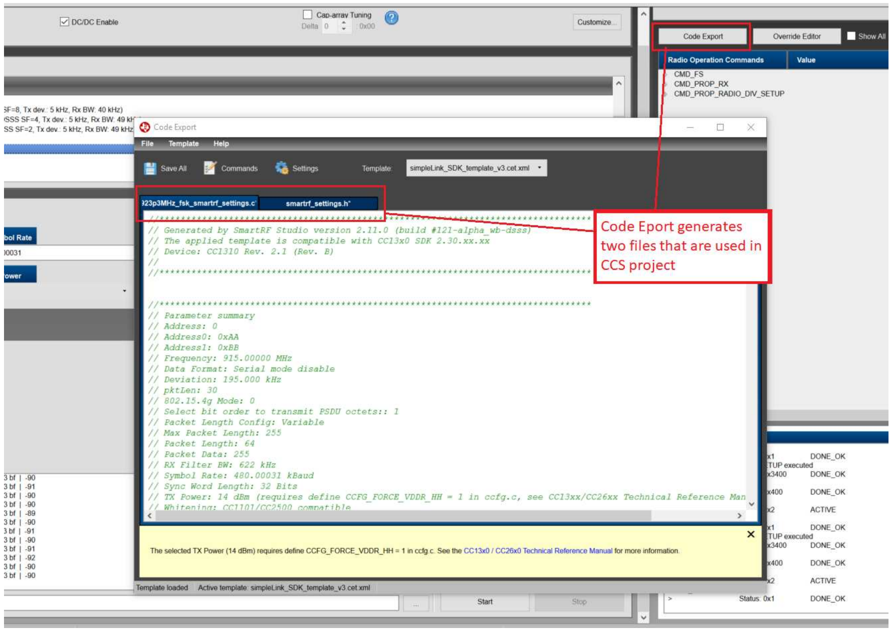

Figure 10. Shows Code Export Feature of SmartRF Studio (the exported smartrf_settings.c/.h are used in CCS projects)

Figure 11 shows two projects imported into CCS IDE: one for transmit and the other for receive. The projects can be built and downloaded to two LaunchPads for testing.

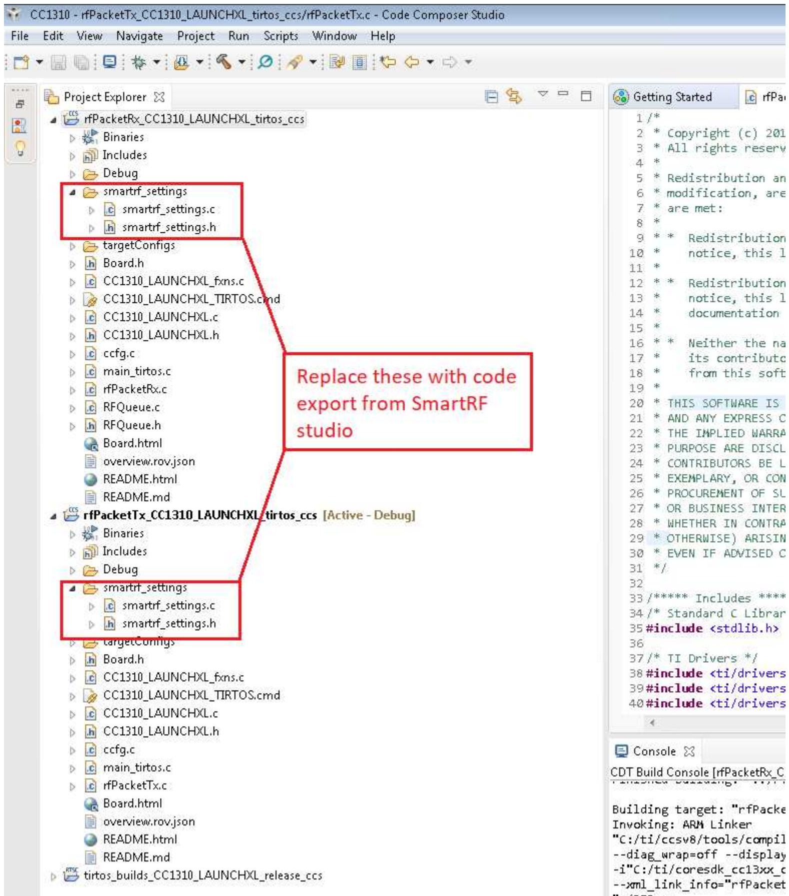

Figure 11. WB-DSSS Modes in SmartRF Studio

Various DSSS modes can be programmed by changing the value of address 0x400452AC in the *uint32_t pOverrides[ ]* array of the smartrf_settings.c file (see the following code). The valid values for the register are shown in Table 3.

Table 3. WB-DSSS Modes in SmartRF Studio

DSSS	Code	Hex Value	Sym Rate	Data Rate
1	K = 4	HW_REG_OVERRIDE(0x52C,0x0800)	480 kbps	240 kbps
2	K = 4	HW_REG_OVERRIDE(0x52C,0x0900)	480 kbps	120 kbps
4	K = 4	HW_REG_OVERRIDE(0x52C,0x0B03)	480 kbps	60 kbps
8	K = 4	HW_REG_OVERRIDE(0x52C,0x0F33)	480 kbps	30 kbps

```
// Example PA ramping of 5 µs and AGC reference level of 0x1E
HW_REG_OVERRIDE (0x6088,0x1F1E),
//Set spreading = 1, K = 4
HW_REG_OVERRIDE (0x52AC,0x800),
//TX: Configure PA ramping setting (0x08) for approximatelyl 5 µs PA ramp time
HW_REG_OVERRIDE (0x608C,0x3F13).
```

6 Measured Results

The results shown in the follow sections are measured on 6 devices at 25°C and 3 V. The measurements presented were made on CC1310EM_7XD_7793 boards. The sensitivity is given at BER = 10^{-2}, which is close to 80% PER for a 20 byte packet.

A protocol that normally uses short packets would have an acceptable packet error rate when BER is 1% where as a longer packet (200-2000 byte) would require a BER of around 10^{-5} to operate properly.

6.1 Receiver Performance

In receiver tests, the packet length was 20 bytes. Sensitivity is defined at the BER=10-2 point, which is close to 80% PER for that packet length.

6.1.1 DSSS = 1, 240 kbps, 2-GFSK, 195 kHz Deviation, 1x Spreading

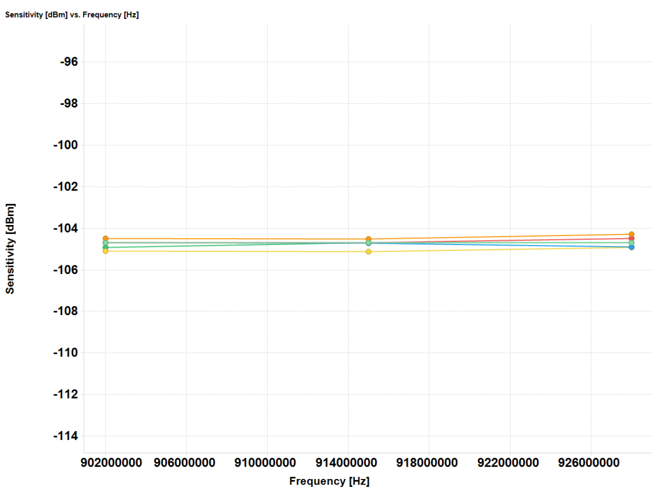

Figure 12. Sensitivity K = 4, DSSS = 1, 240 kbps

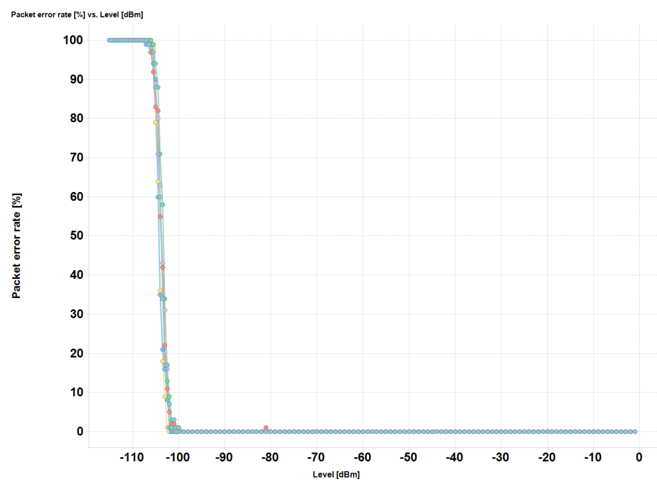

Figure 13. PER vs. Input Signal Level K = 4, DSSS = 1, 240 kbps

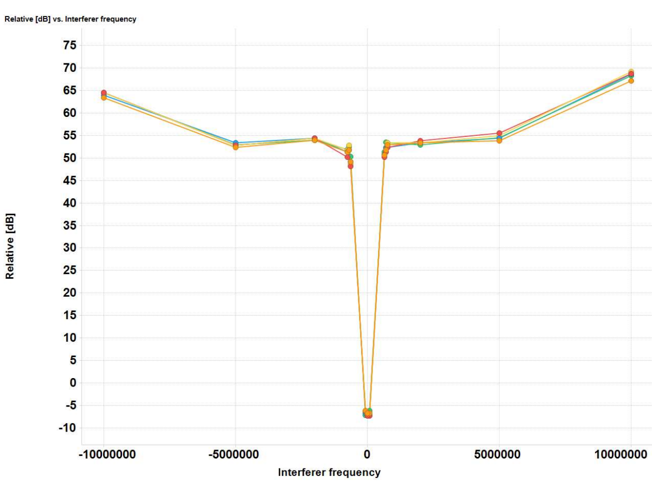

Figure 14. Blocking Performance K = 4, DSSS = 1, 240 kbps

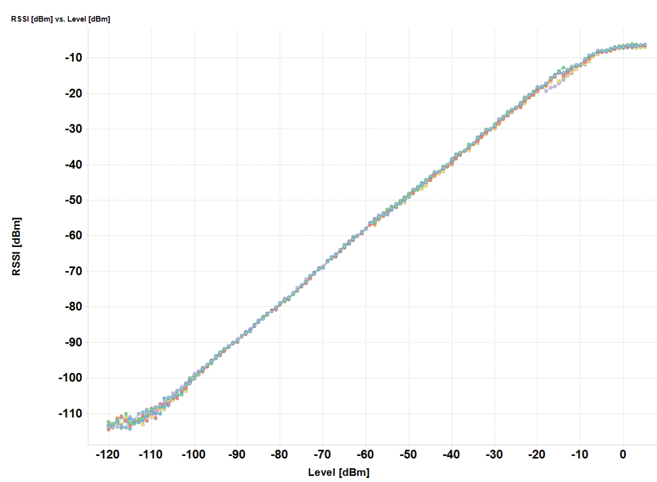

Figure 15. RSSI K = 4, DSSS = 1, 240 kbps

6.1.2 WB-DSSS 120 kbps, 2-GFSK, 195 kHz Deviation, 2x Spreading

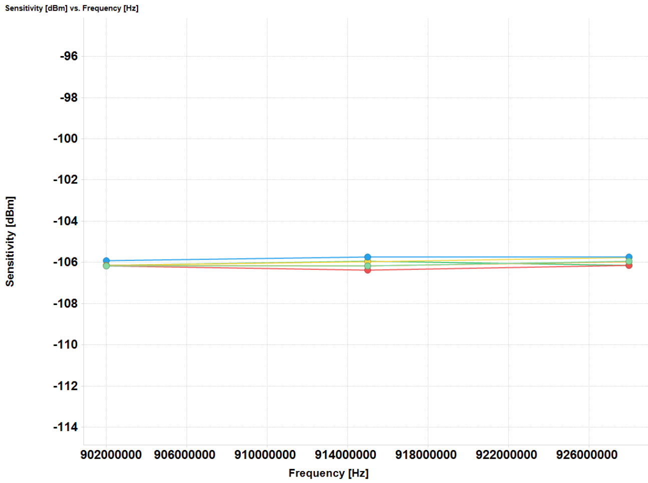

Figure 16. Sensitivity K = 4, DSSS = 2, 120 kbps

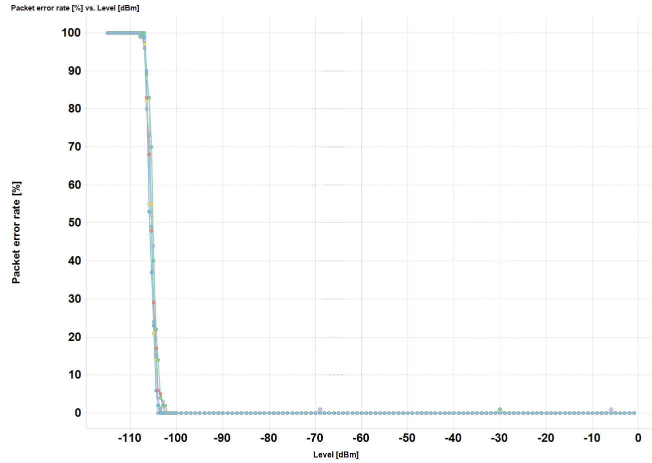

Figure 17. PER vs. Input Signal Level K = 4, DSSS = 2, 120 kbps

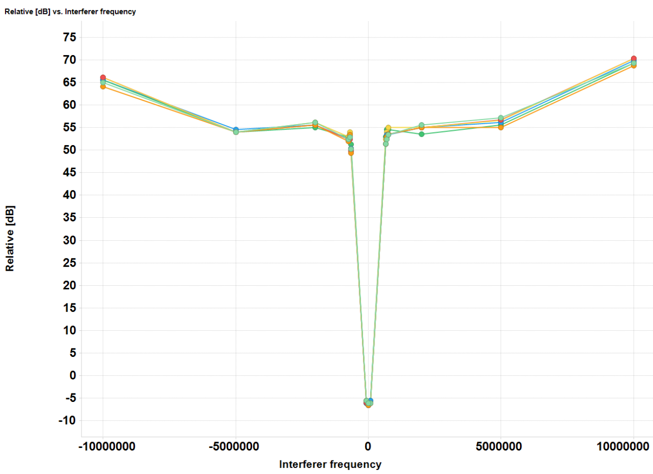

Figure 18. Blocking Performance K = 4, DSSS = 2, 120 kbps

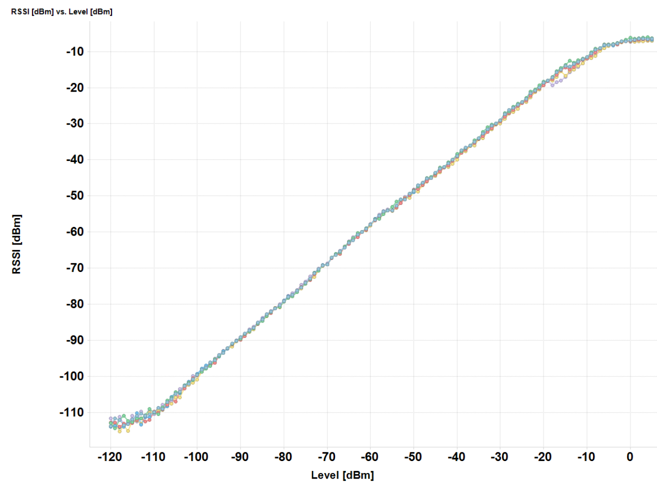

Figure 19. RSSI K = 4, DSSS = 2, 120 kbps

6.1.3 WB-DSSS 60 kbps, 2-GFSK, 195 kHz Deviation, 4x Spreading

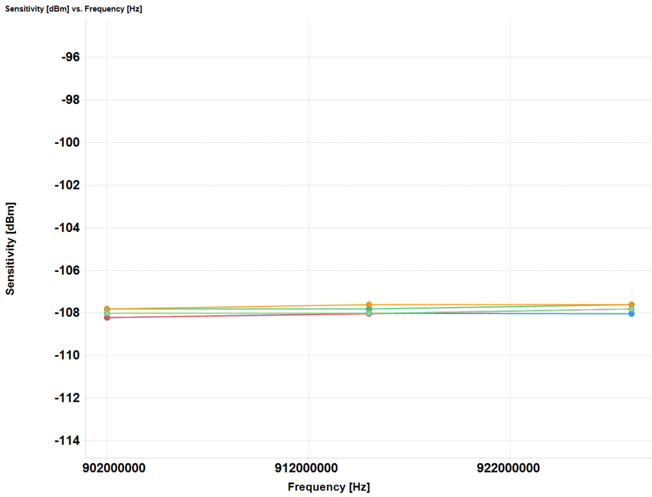

Figure 20. TC430 Sensitivity K = 4, DSSS = 4, 60 kbps

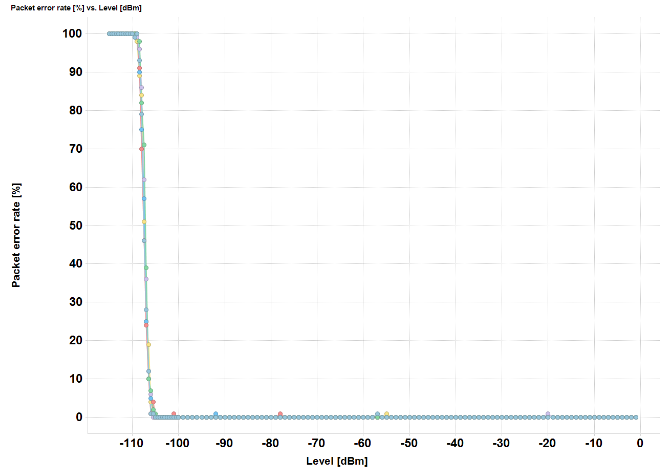

Figure 21. PER vs. Input Signal Level K = 4, DSSS = 4, 60 kbps

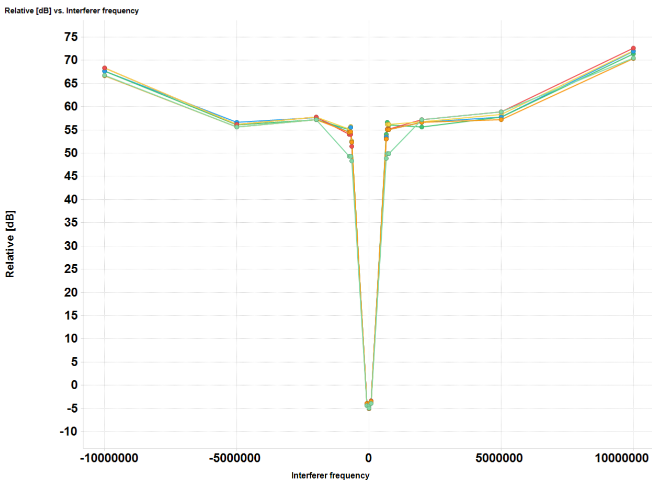

Figure 22. Blocking Performance K = DSSS = 4, 60 kbps

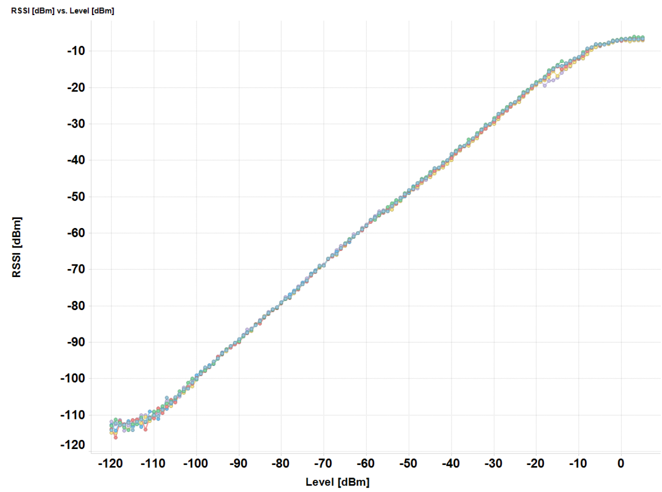

Figure 23. RSSI K = 4, DSSS = 4, 60 kbps

6.1.4 WB-DSSS 30 kbps, 2-GFSK, 195 kHz Deviation, 8x Spreading

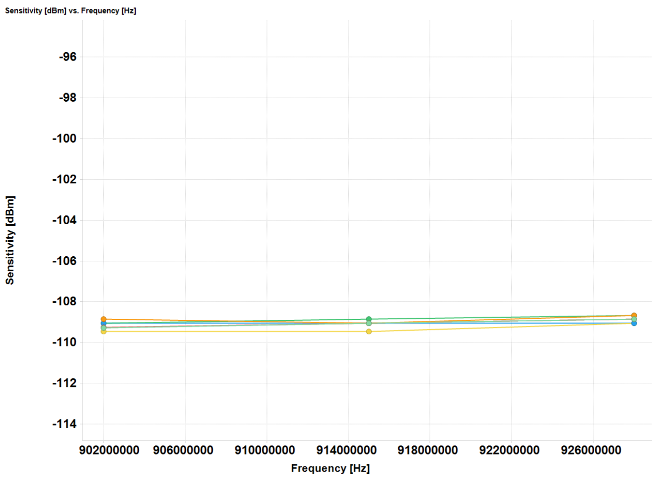

Figure 24. Sensitivity K = 4, DSSS = 8, 30 kbps

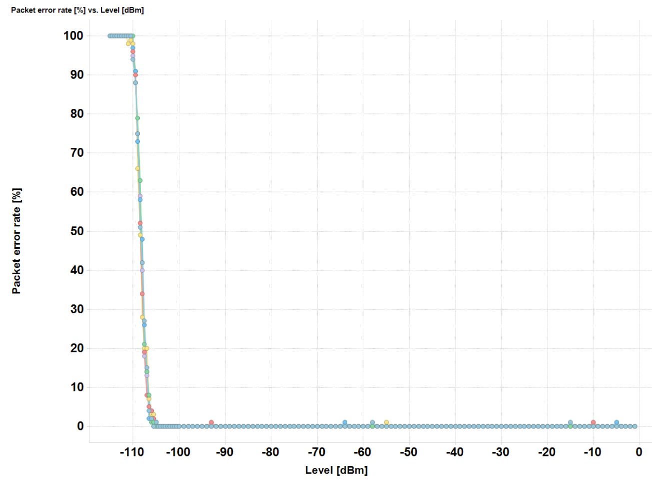

Figure 25. PER vs. Input Signal Level K = 4, DSSS = 8, 30 kbps

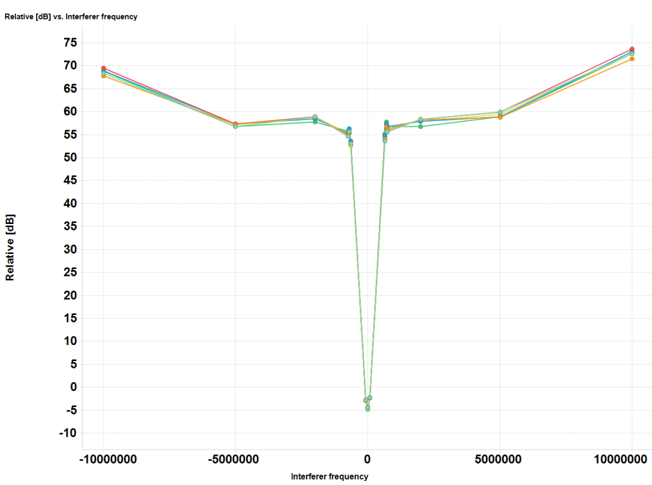

Figure 26. Blocking Performance K = 4, DSSS = 8, 30 kbps

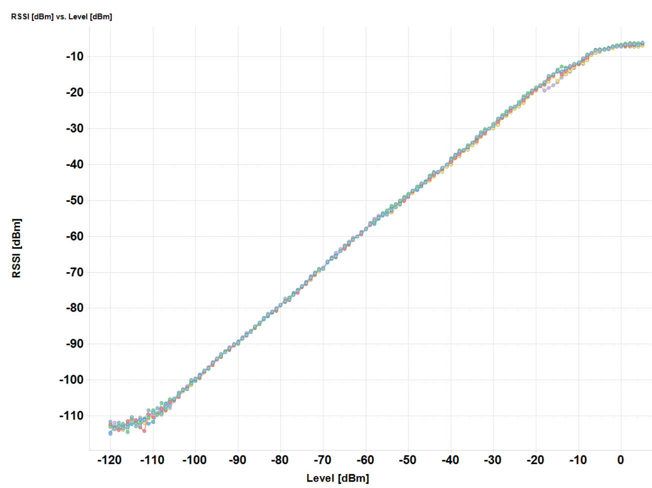

Figure 27. RSSI K = 4, DSSS = 8, 30 kbps

6.1.5 WB-DSSS Frequency Offset Tolerance

Figure 28 and Figure 29 show the frequency offset performance of WB-DSSS scheme. In contrast to narrowband low data rate systems, the crystal accuracy is not critical in this case as the RX bandwidth is relatively large.

From the results, it can be seen that sensitivity remains unchanged for considerable amount of crystal drift (±50 ppm).

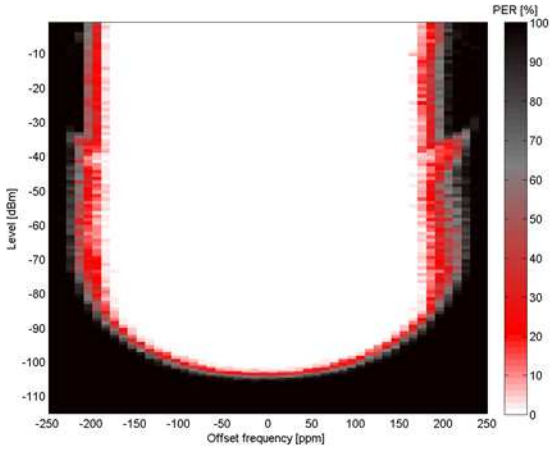

Figure 28. SimpleLink Long Range Frequency Offset Performance (915 MHz, K = 4, DSSS = 1, 240 kbps)

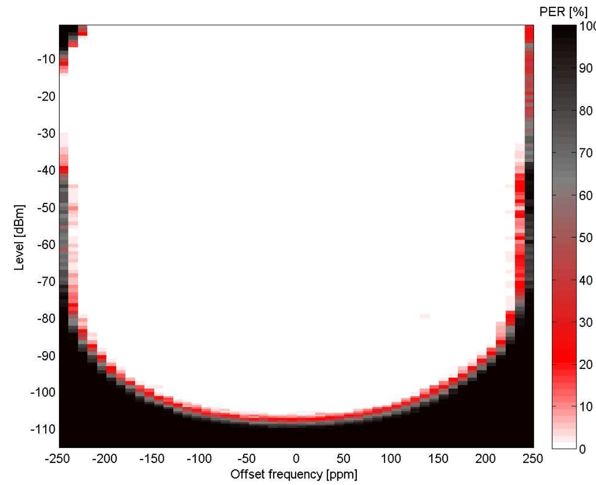

Figure 29. SimpleLink Long Range Frequency Offset Performance (915 MHz, K = 4, DSSS = 8, 30 kbps)

6.2 Transmitter Performance and FCC 15.247 Measurements

Table 4 gives the FCC 15.247 digital modulation requirements that were tested.

Table 4. FCC 15.247 Digital Modulation Requirements [3]

Section	Requirements
15.247a2	The 6 dB bandwidth shall be at least 500 kHz
15.247b3	The maximum conducted power shall not exceed 1 W (+30 dBm)
15.247e	The power spectral density (PSD) shall not be greater than 8 dBm in any 3 kHz band during any time interval during continuous transmission

Most spectrum analyzers have a measurement option that automatically measures a fixed dB bandwidth. If this is not available, the 6 dB bandwidth must be measured manually by setting up markers.

Measurement setup consisted of the following:

- Six devices were tested
- All measurements were performed at 3 V, 25°C
- Measurements were performed on CC1310EMK-7XD-7793
- Test results in Table 5 are average numbers of six devices
- SmartRF Studio was used to test the WB-DSSS cases

Table 5. FCC 15.247 Digital Modulation Requirements [ref]

DSSS	6 dB BW (15.247 a2)	Power (15.247 b)	PSD (15.247 d)
1	>500 kHz	13.6 dBm	1.4 dBm
2	>500 kHz	13.6 dBm	2.8 dBm
3	>500 kHz	13.7 dBm	4.8 dBm
4	>500 kHz	13.7 dBm	5.1 dBm

For an explanation of marker lines for 6 dB bandwidth measurements, see Figure 30.

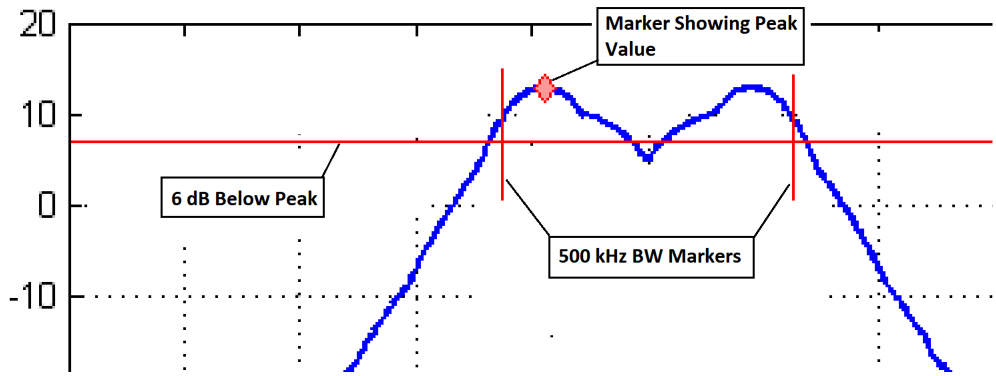

Figure 30. Explanation of 6 dB Bandwidth Figures

6.2.1 WB-DSSS 240 kbps, 2-GFSK, 195 kHz Deviation, 1x Spreading

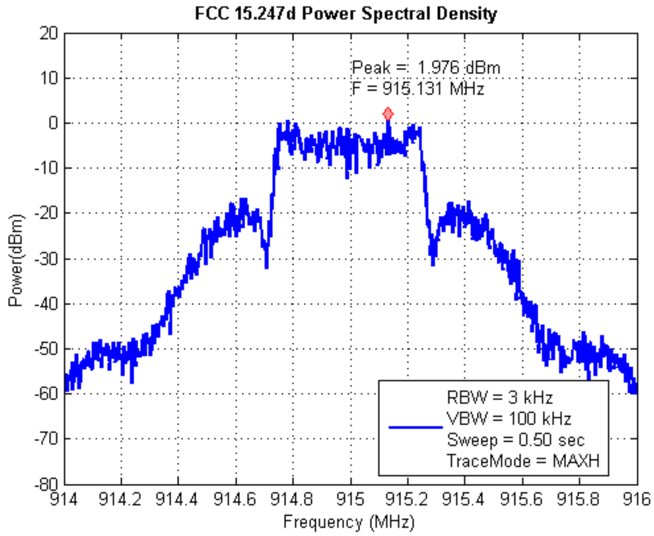

Figure 31. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

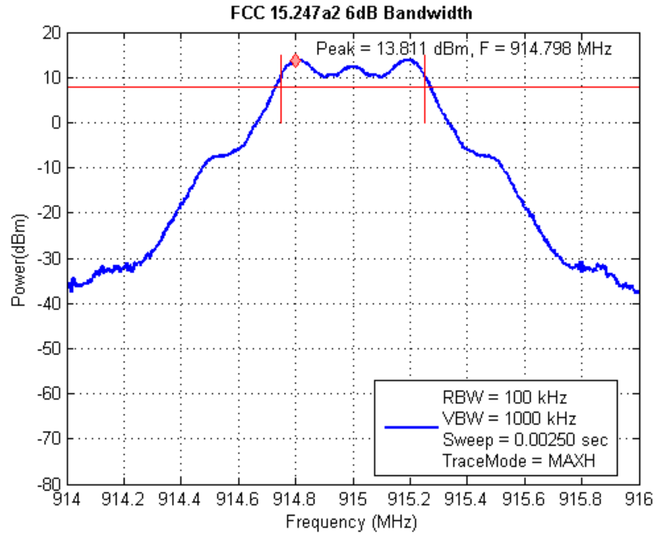

Figure 32. Transmit Spectrum 6 dB Occupied Bandwidth

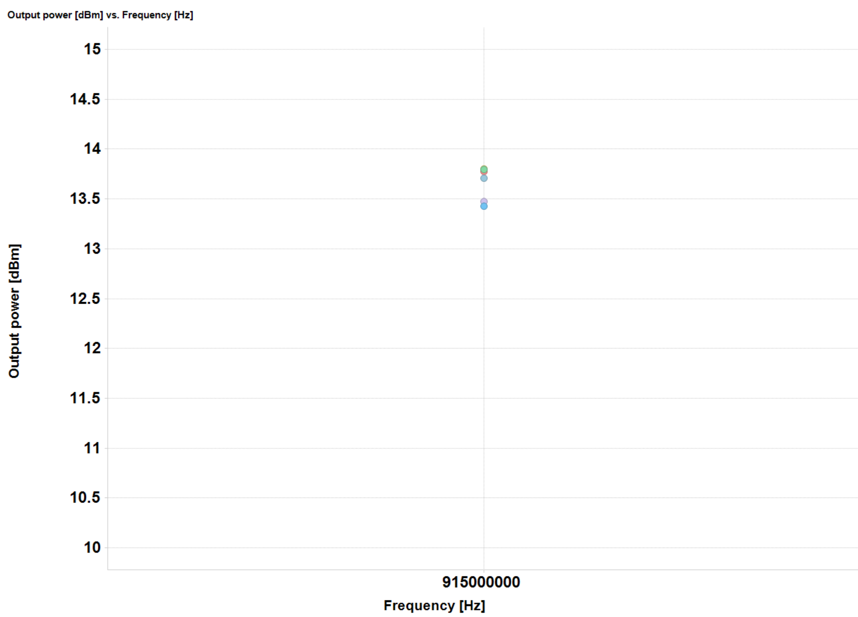

Figure 33. Max Output Power at 915 MHz

6.2.2 WB-DSSS 120 kbps, 2-GFSK, 195 kHz Deviation, 2x Spreading

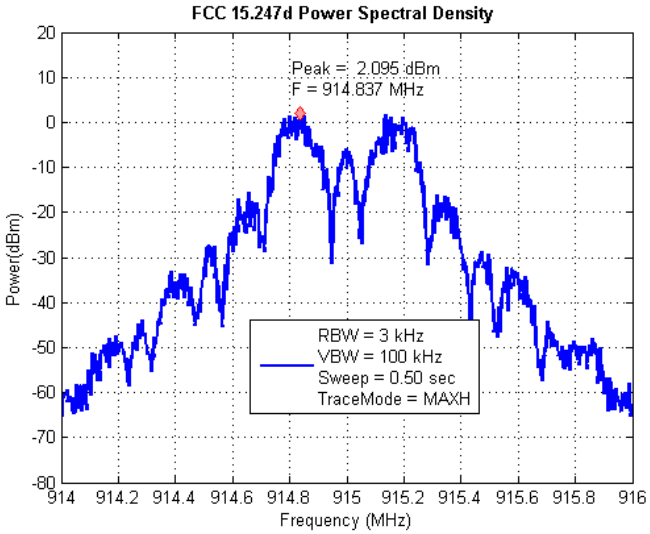

Figure 34. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

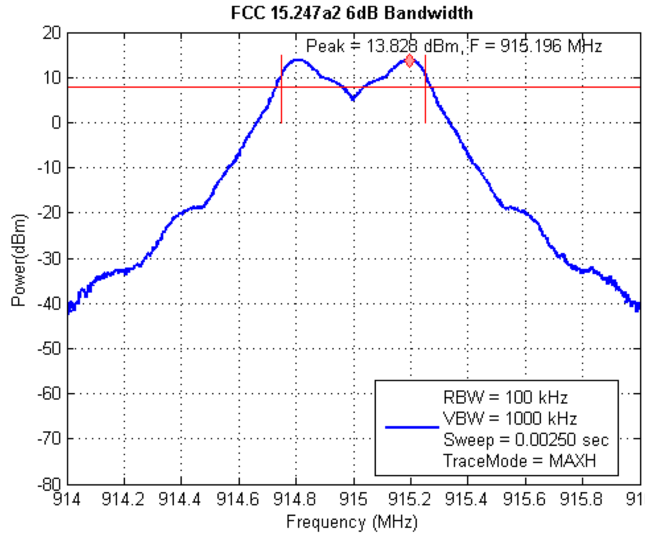

Figure 35. Transmit Spectrum 6 dB Occupied Bandwidth

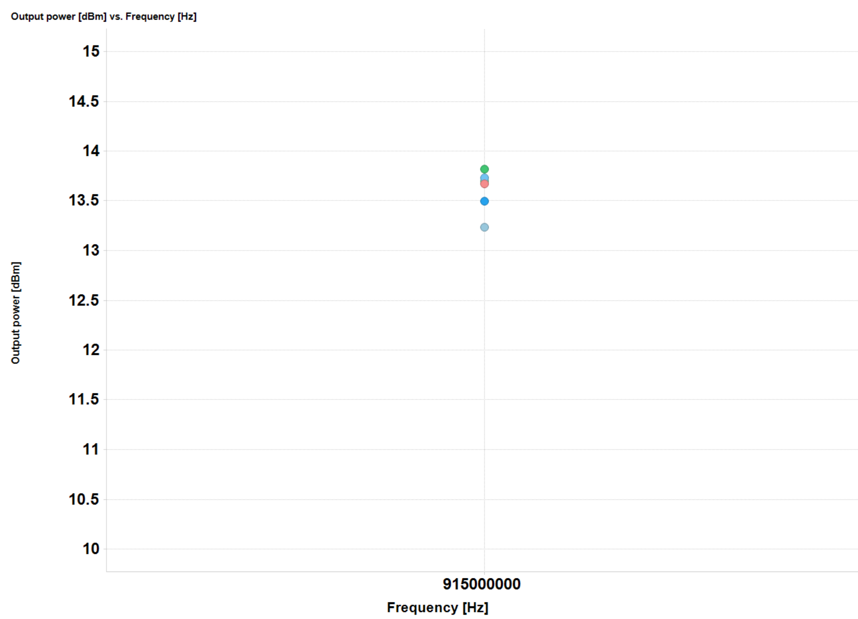

Figure 36. Max Output Power at 915 MHz

6.2.3 WB-DSSS 60kbps, 2-GFSK, 195 kHz Deviation, 4x Spreading

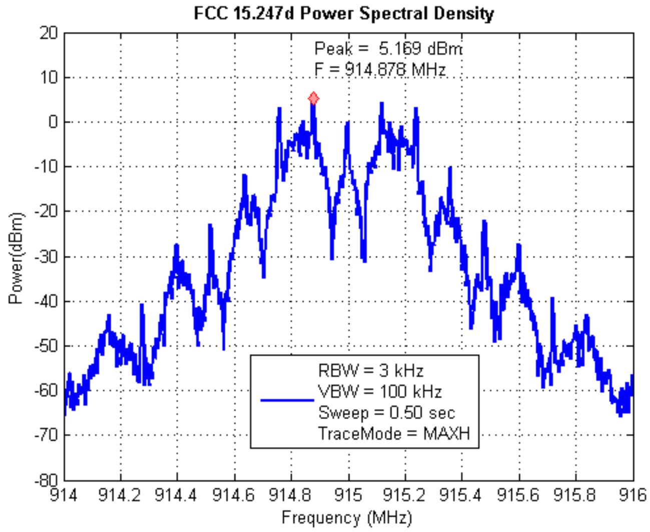

Figure 37. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

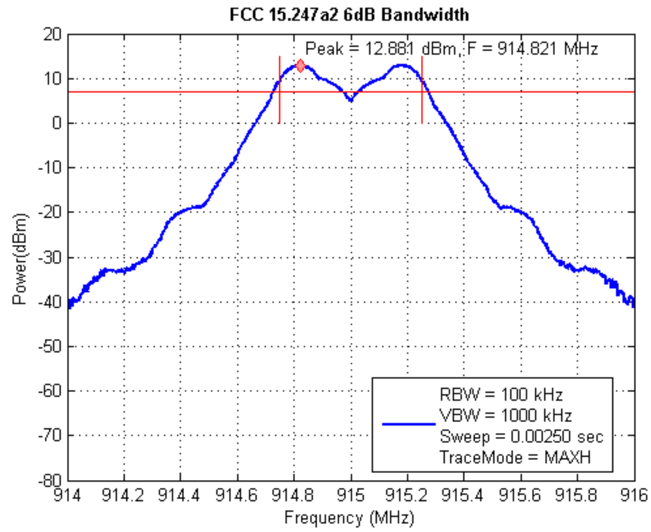

Figure 38. Transmit Spectrum 6dB Occupied Bandwidth

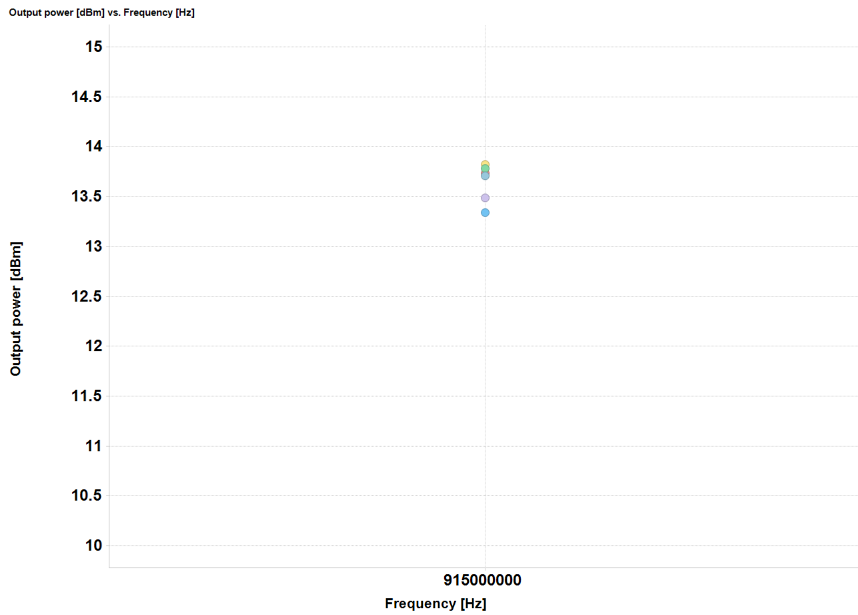

Figure 39. Max Output Power at 915 MHz

6.2.4 WB-DSSS 30 kbps, 2-GFSK, 195 kHz Deviation, 8x Spreading

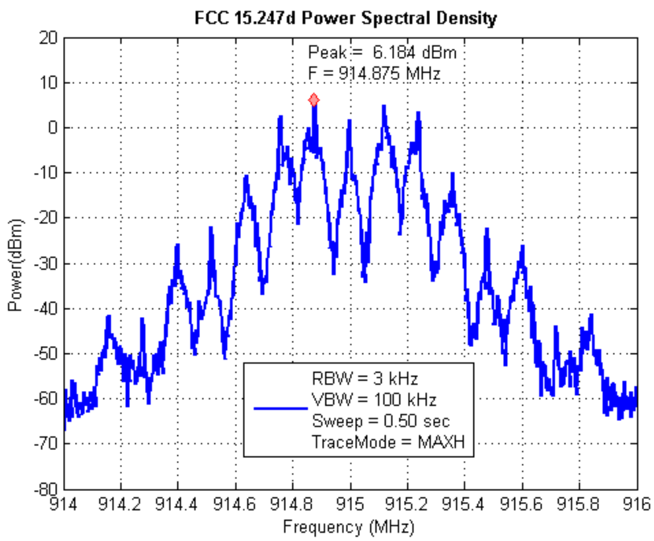

Figure 40. Transmit Spectrum PSD 8 dBm in any 3 kHz Bandwidth

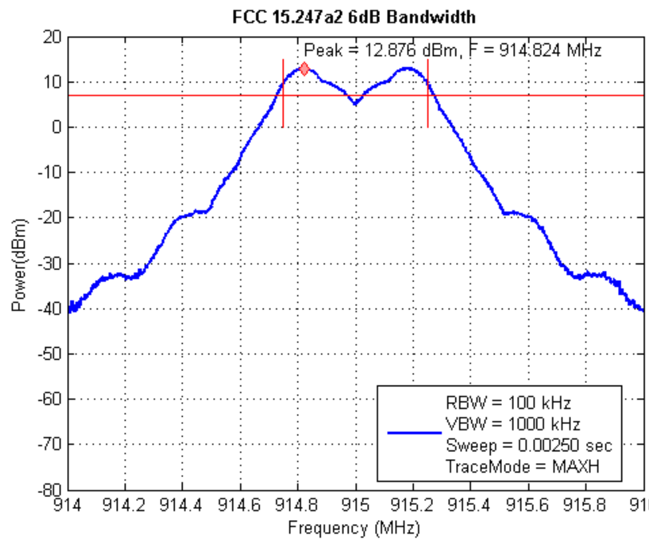

Figure 41. Transmit Spectrum 6 dB Occupied Bandwidth

Figure 42. Max Output Power at 915 MHz

7 References

1. Bernard Sklar. "Digital Communications – Fundamentals and Applications". 2nd Edition.
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3. Texas Instruments: *CC11xx Settings for FCC15.247 Solutions*
4. SmartRFTM Studio
5. SimpleLinkTM Sub-1 GHz CC1310 Evaluation Module Kit
6. SimpleLink Sub-1 GHz CC13x0 Software Development Kit

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