Application Report
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Watchdog Timer for mmwave Radar Sensors

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ABSTRACT

This application report describes a watchdog timer-based recovery for an application software cycle period, or loss of communication with the host processor or radar sensor. Some discussion of error signaling is included to ensure the radar sensor is reset for Sensed Error conditions.

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Trademarks

1 Introduction

The radar sensor-embedded Arm® processor executes the software communication, control, and measurement cycle. One way to mitigate a software stall in this cycle is to time the processor cycle, and update special hardware within the processor cycle. The special hardware is called a *watchdog timer*. If the watchdog timer is not updated, a restart of the Arm processor is performed. The watchdog timer can be internal to the radar sensor device, or external.

In some frequency modulated continuous wave (FMCW) applications, there is a radar sensor and a host processor. The radar sensor data, or computed values from the sensor data, are sent to the host processor. The host processor sends control messages, mmWave programming, and status requests. An additional timer can be used to ensure that there is not a loss of data or communication. In this application report, this feature is called a command-data communication timer.

For further discussion of the watchdog timer, see Introduction to Watchdog Timers. The internal watchdog timer for the radar sensor is described in the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page.

There are enhanced, window-time comparison watchdog timers which, instead of a too-long process cycle, also detect a too-short process cycle. However, these process cycles are not discussed in this application report.

NOTE: In specific applications, the nERROR_OUT output signal from the radar sensor is used for the error status. In specific applications, the WARMRESET output signal from the radar sensor is used to indicate that an internal reset of the radar sensor is occurring.

There are specific scenarios for a stand-alone radar sensor, host processor with a single radar sensor, and host processor with multiple radar sensors. The scenarios are described for the watchdog timer and Command-data communication timer.

NOTE: This is not a functional safety discussion, although the nERROR signal can be used for reading the functional safety status.

The radar sensor has several built-in processors, as follows:

- Master subsystem (MSS) – Controls and schedules functional software for the radar sensor, and can perform specific signal processing tasks
- Radar subsystem (BSS) – Controls the RF subsystem of the radar sensor
- DSP subsystem (DSS) – Performs signal processing functions on the radar sensor data (subsystem not present in all radar devices)

The MSS processor communicates through messages with the BSS and DSS. The MSS running the main software application updates the watchdog timer. In some software applications, the nERROR signal is also checked, to update the watchdog timer. This logic indicates that if the software cycle is too long or if an nERROR signal occurs, the reset recovery is performed.

NOTE: In some cases, hardware in parallel with software generates the nERROR output signal.

1.1 Internal Watchdog Timer Use With the Radar Sensor

Figure 1 shows a view of the radar sensor processes for reset (nRESET), running an application, and how through added software and hardware, the watchdog timer checks that the application code completes within a prescribed period, or resets the radar sensor processor. When the watchdog timer is armed (third row in Figure 1), the MSS software must retrigger the watchdog timer (fifth row in Figure 1) within a prescribed time. When the MSS processor cycle-time is too long (sixth row in Figure 1), the internal watchdog timer causes a Warm Reset that restarts the MSS processor in the radar sensor. Figure 4 shows the logic block diagram, discussed in Section 2.1.

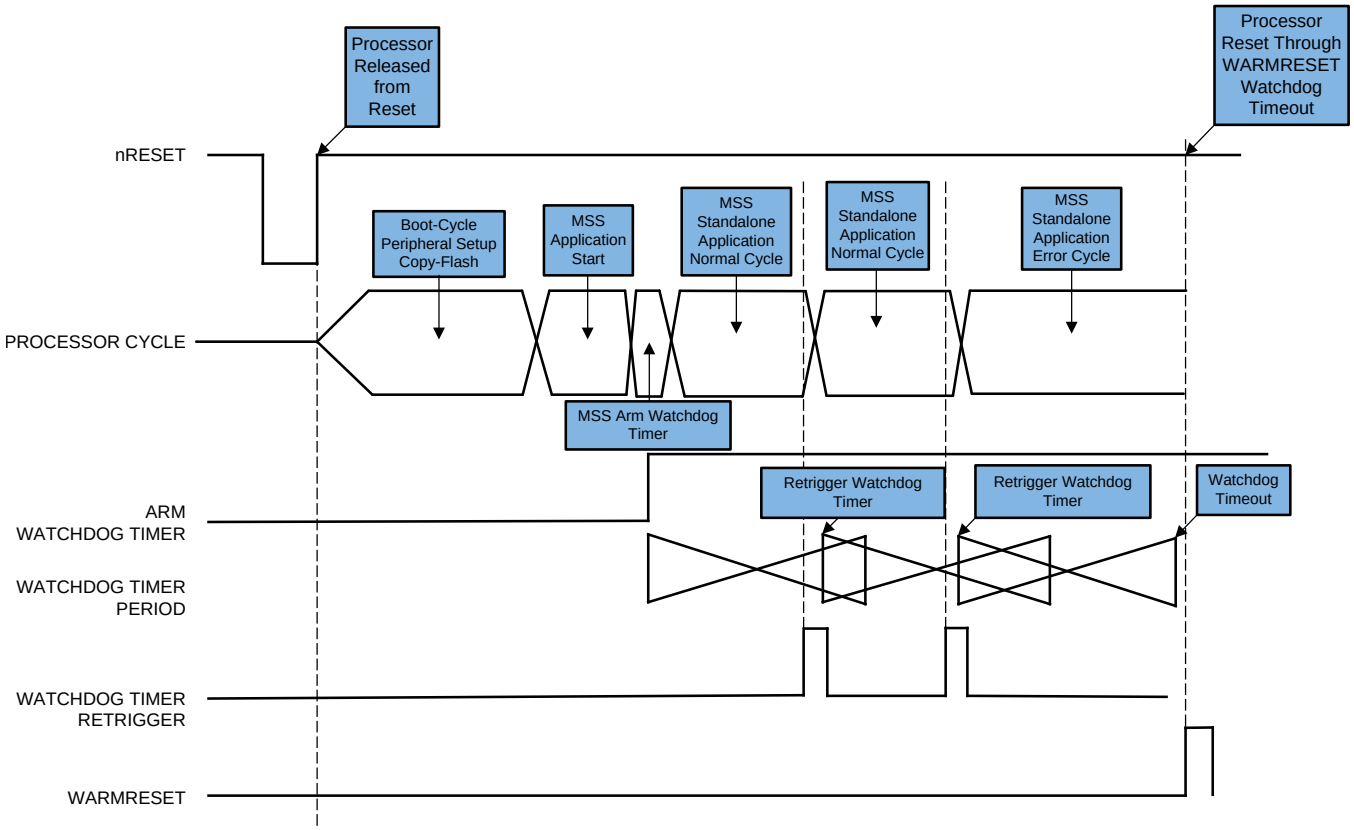

Figure 1. Radar Sensor Software and Internal Watchdog Timer Cycle

The Error Signaling Module (ESM) logic and nERROR signals are discussed in the *Safety* chapter of the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page.

For a discussion of the nERROR signals, see the *Error Signaling Module (ESM)* subsection in the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page.

In Figure 1, a radar sensor or host processor can check that the software cycle takes less than the time-out period of the internal watchdog timer. The WARMRESET signal from the radar sensor is an indication of an internal reset occurring.

In Figure 2, the nRESET external reset input triggers a restart of the MSS software. Like in Figure 1, the MSS processor of the radar sensor has a set of tasks to perform in a cycle. In that cycle is an update to change an external GPIO pin. Changing that GPIO pin value, within the expected value, indicates OK operation. If the GPIO pin does not retrigger the watchdog timer, then the external processor reset (nRESET) is activated.

Setting the expected watchdog timer period normally involves profiling the amount of time the radar sensor takes for the boot process and initial main process cycle. A margin is usually applied to this calculation.

1.2 External Watchdog Timer Use With the Radar Sensor

In some cases, the internal watchdog timer hardware of the radar sensor is not used; instead an external watchdog timer is used (see Section 2.2). If there is a host processor, the radar sensor nRESET signal is controlled by the host processor. The concept of the watchdog timer is the same. After arming the watchdog timer, if the timer is not updated within a prescribed period, the radar sensor nRESET is triggered, which restarts the MSS processor, shown in Figure 2.

Here also, setting the expected watchdog timer period normally involves profiling the amount of time the radar sensor takes for the boot process and initial main process cycle. A margin is usually applied to this calculation.

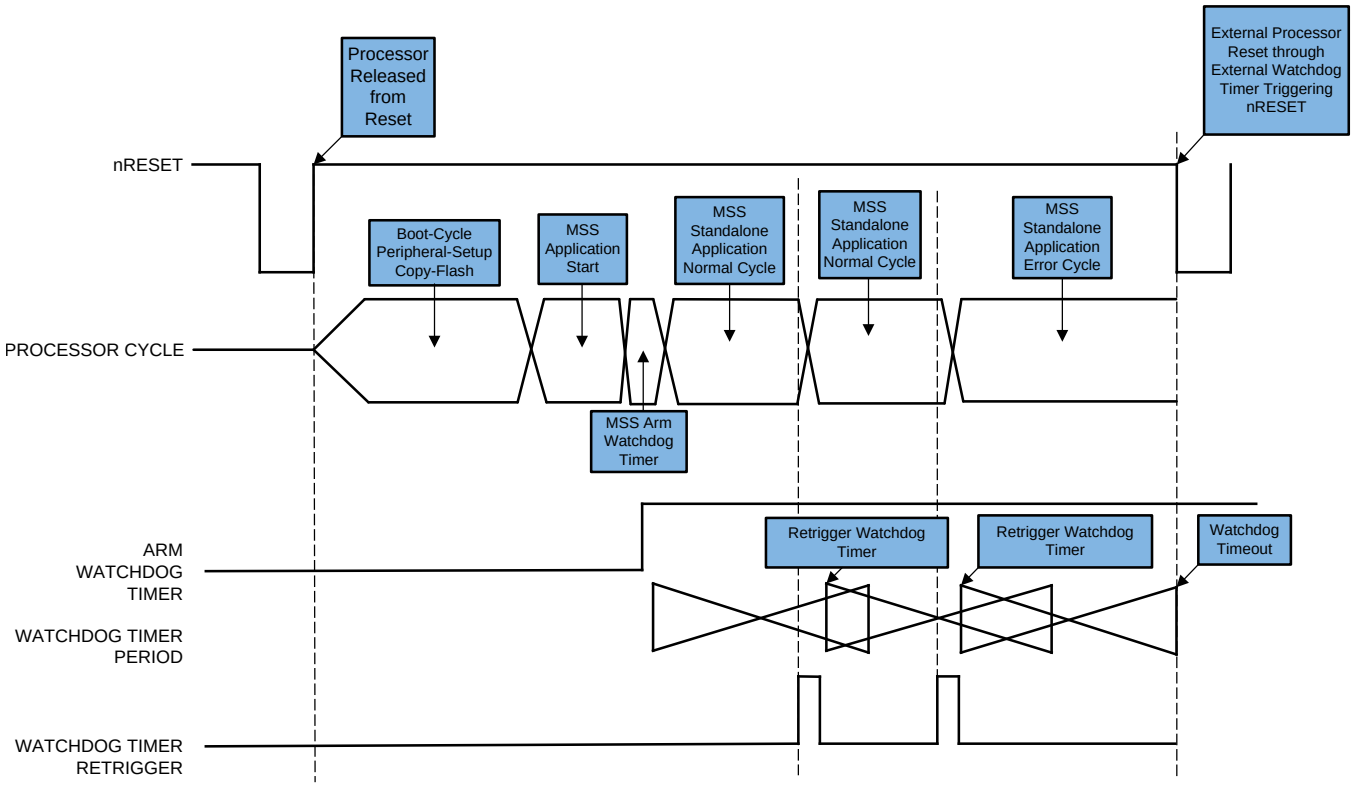

Figure 2. Radar Sensor With External Watchdog Timer

1.3 Control and Data Communication Timer

In some applications with an external host processor, users may want to have the host processor time the host processor-to-radar sensor command sequence, or a data output sequence. When using the SPI for the radar sensor, there is a 4-wire SPI and a host interrupt GPIO radar sensor output. The Host_Interrupt_GPIO output indicates that the radar sensor needs an SPI service (slave response to host processor SPI command, or other condition). In the high-speed LVDS or CSI-2 communication output, a Frame_Clock can be timed to check the high-speed data is being output.

As shown in Figure 3, the host processor can time the SPI command sent to the radar sensor host interrupt response. This is used to check if the SPI command communication is functioning. Additional error status indications in the SPI return status may need additional host processing.

NOTE: In certain applications of the host processor and radar sensor, the SPI can send radar sensor data as well as command or status information. This can be timed if desired.

When the radar sensor has been programmed with the mmWave API commands, the Sensor Start to LVDS data output can additionally be timed to check that the radar sensor high-speed data is output.

Loss of the SPI command or data may result in retransmission of a mmWave sequence, or a radar sensor reset.

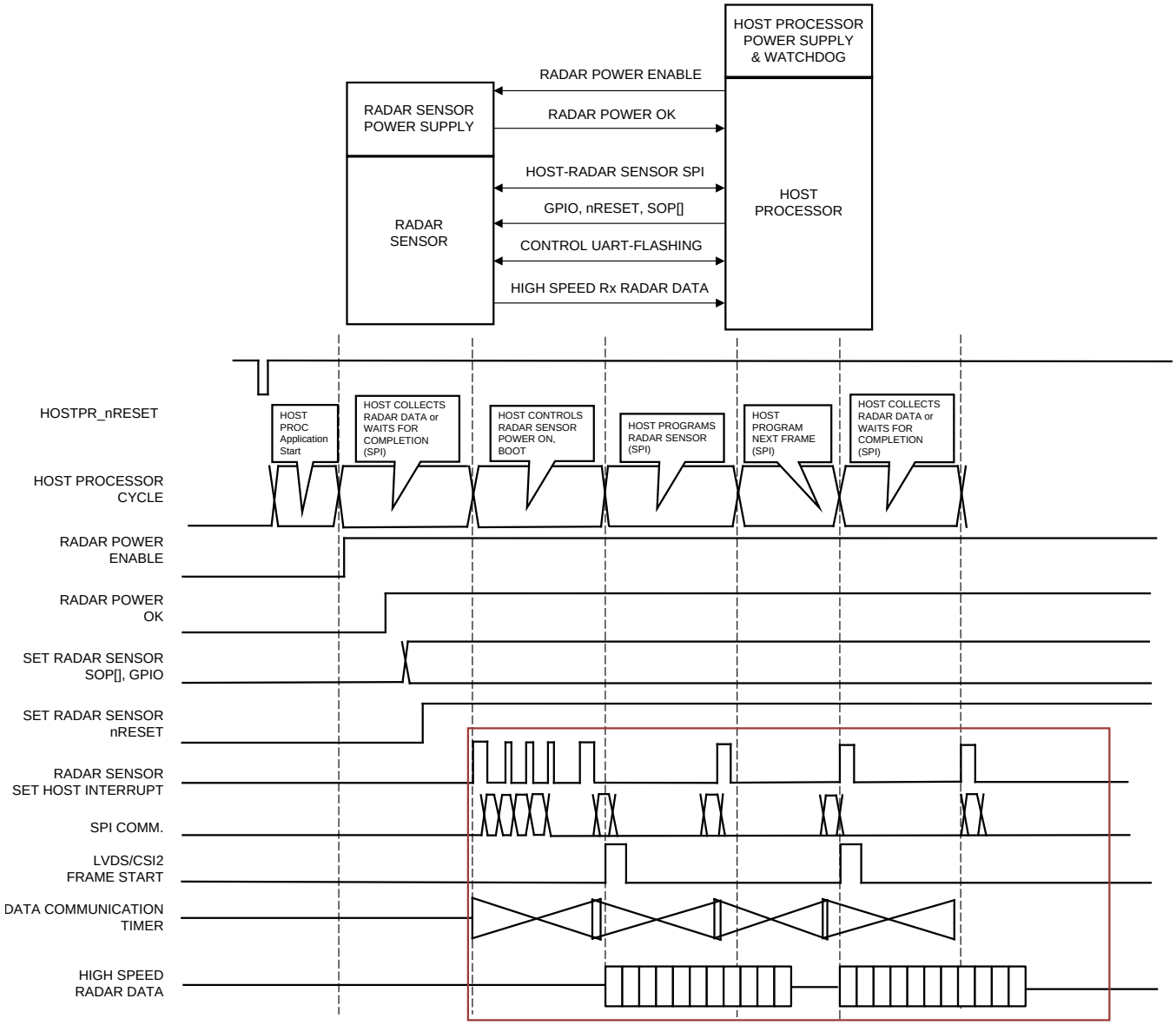

Figure 3. Host Processor Control and Data Communication Timer

2 Topology Description for Radar Sensors and Watchdog Timers

This section describes the different radar sensor and host processor configurations for the watchdog timer, and command-data communication timer implementations. Each of the following configurations has text, a block diagram (red rectangles to focus on reset, watchdog timer processing, and command and data communication timer processing). In addition, users can research specific mmwave application questions using the mmWave Sensors E2E Forum.

Four application scenarios are described, as follows:

- Stand-Alone Radar Sensor – Internal Watchdog Timer
- Stand-Alone Radar Sensor – External Watchdog Timer
- Host Processor and Radar Sensor – Host Processor Loss of Communication Error Reset of Radar Sensor
- Host Processor and Satellite Radar Sensors – Host Processor Loss of Communication Error Reset of Radar Sensor

NOTE: In this discussion, several TI devices for the supervisor + watchdog timer are listed. These devices are discussed in the Introduction to Watchdog Timers.

2.1 Stand-Alone Radar Sensor – Internal Watchdog Timer

Figure 4 shows a standard industrial sensor where no host processor is present; the sensor is always turned on. In this case, the watchdog timer is internal to the radar sensor. The MSS software updates the watchdog timer module, and hardware checks whether or not the watchdog timer is within range (updates in time).

When the 5-V power and PGOOD are OK, the nRESET signal is a logic 1, which allows the radar sensor processor to start.

In the normal cycle, the software updates the timer within a desired period and continues to the next processor main cycle. In the abnormal cycle, the processor does not update the timer, and the WARMRESET is triggered. This causes the radar sensor to perform an internal reset. The WARMRESET output signal is used to inform the external devices that a reset has occurred. The NERROROUT output signal can be used to inform the external devices that an error is detected.

When the software restarts, the WARMRESET signal is released.

NOTE: During software initialization, in the default condition the watchdog timer is not enabled. This must be evaluated in the radar sensor software.

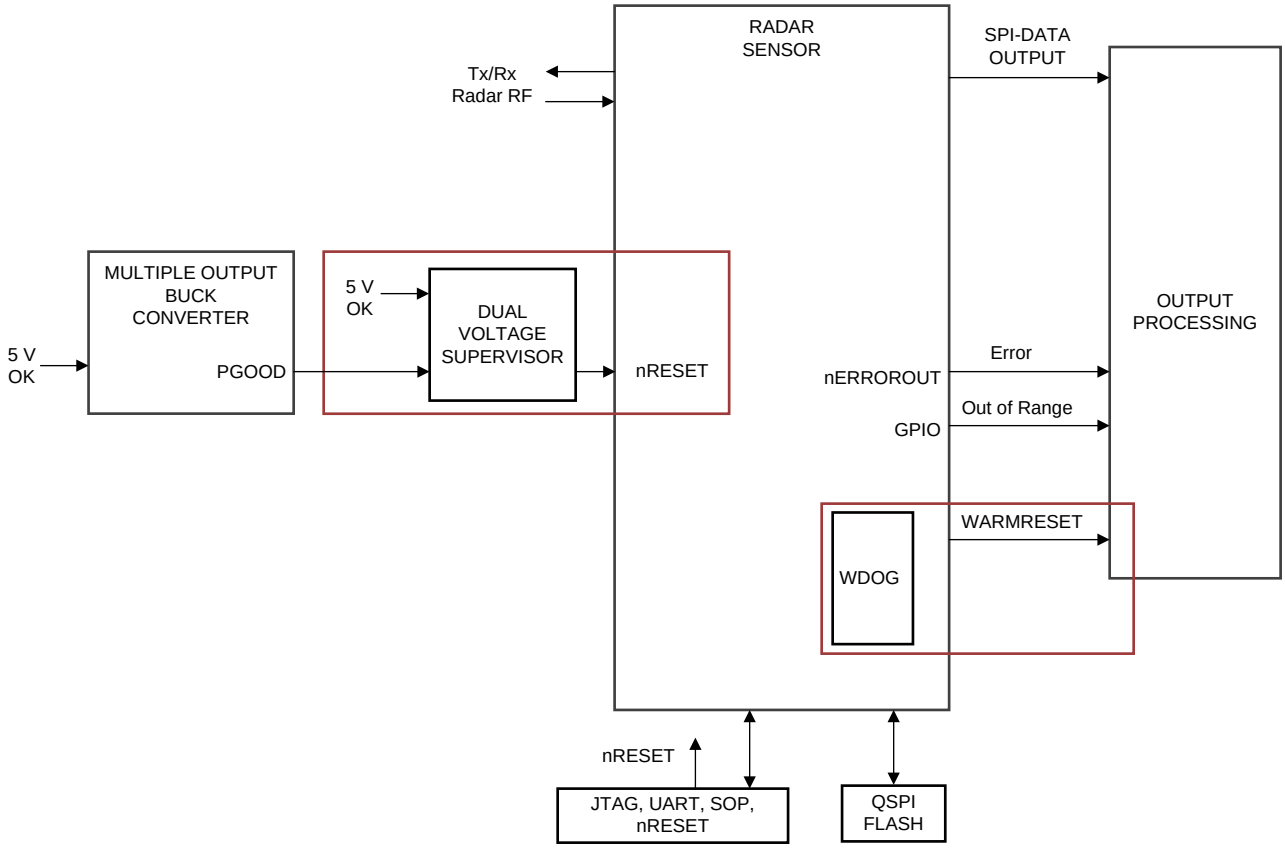

Figure 4. Stand-Alone Radar Sensor – Internal Watchdog Timer (WDOG)

2.2 Stand-Alone Radar Sensor – External Watchdog Timer

Figure 4 was modified to create Figure 5, which includes a GPIO that triggers an external watchdog timer. The output is modified in Figure 5, so that during the nRESET signal an out-of-range signal is generated. In this example, the radar sensor is always turned on.

NOTE: The WARMRESET signal is not used.

Different voltage supervisory and watchdog timer devices have voltage supervisory control and a retriggerable timer after reset.

When the 5-V power and PGOOD are OK and no watchdog reset is active, the nRESET signal is a logic 1, to allow the radar sensor processor to start.

If the process software is stuck, if the process cycle takes to long, or if the nRESET signal from the watchdog timer output causes a reset, then the output goes to the out-of-range condition.

NOTE: The watchdog timer update is completed before the time-out of the main software tasks. This triggers the GPIO output change to the watchdog input (WDI). In some applications, the nERROROUT condition is used to block the GPIO change, resulting in a watchdog reset for not completing the software in time, or if an nERROROUT condition occurs.

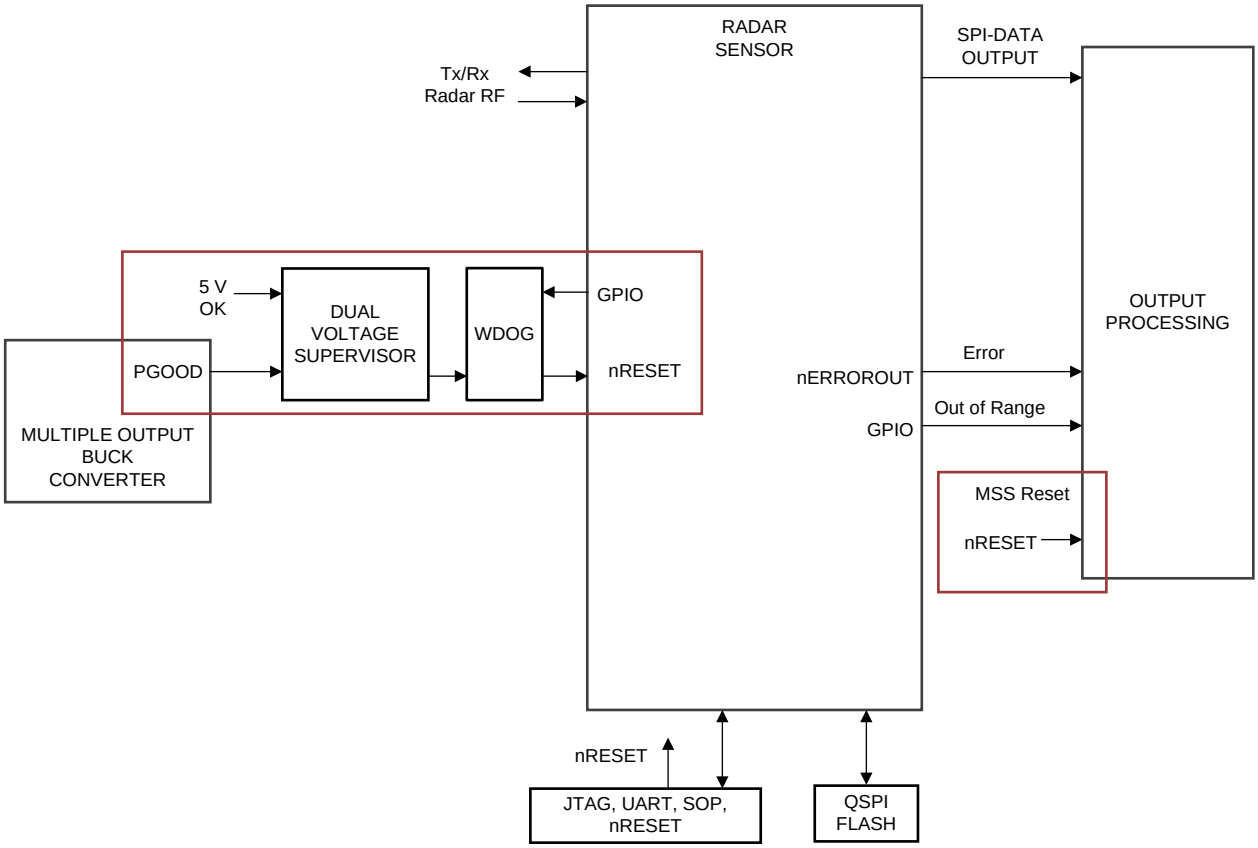

Figure 5. Stand-Alone Radar Sensor – External Watchdog Timer (WDOG)

2.3 Host Processor and Radar Sensor – Host Processor Loss of Communication Error Reset of Radar Sensor

In this section, both the radar sensor and a low-power host processor are used (see Figure 6). This diagram has some differences from Figure 4, in that the radar sensor is used for a short period of time. The host processor turns the radar sensor on and off. Because of this, the host processor is protected with a watchdog timer voltage supervisor; the radar sensor just has the voltage supervisor. The host processor controls the radar sensor PMIC enable and disable.

In this case, the host processor wakes up based on a timer. The host processor then enables the radar sensor PMIC power supply. After the radar PGOOD is received, the radar sensor outputs the mode control GPIO, then the nRESET signal is released. The radar sensor sends the GPIO interrupt to the host to signal boot completion. During this radar sensor wake up, measurement cycle, and data transfer, the host communication timer is running. If the radar sensor takes too long to complete the data transfer, the host reset occurs, which also resets the radar sensor.

During host initialization, its 3.3-V PMIC is routed through the watchdog timer to create the host nRESET signal. If the host does not complete the process cycle in time, or if the radar sensor does not complete the communication in time after retry, a host communication time-out triggers recovery software. An additional capability is that if the host has self monitoring, a detected failure can block the GPIO update to the host watchdog timer, which results in a host and radar sensor reset.

In Figure 6, the nERROROUT signal from the radar sensor is input as a GPIO/interrupt to the host, so that the SPI communication can request the radar sensor ESM status.

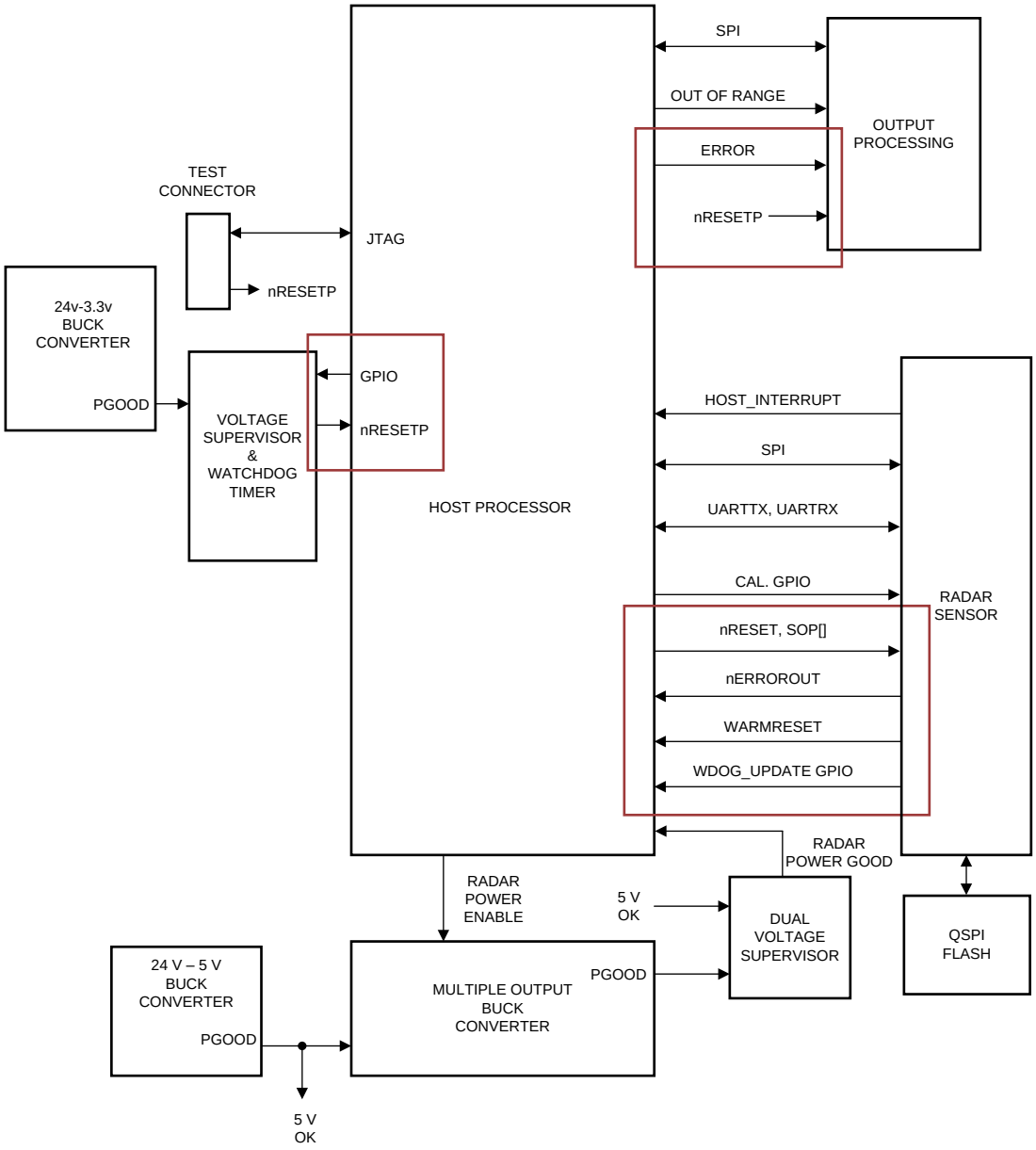

Figure 6. Host Processor and Radar Sensor – External Watchdog Timer for Host, Communication Timer for Radar Sensor

2.4 Host Processor and Satellite Radar Sensors – Host Processor Loss of Communication Error Reset of Radar Sensor

In this section a different topology is described, where multiple radar sensors are controlled from a common host processor. The same concepts of host-to-radar sensor communication and monitoring of error conditions are used.

In Figure 7, the primary signals for the radar sensor control and status from the host processor follow:

- 4-wire SPI – SPICK, SPI_CS, SPI_MISO, and SPI_MOSI: Control and status interface (may contain data)
- RadarSensor_Host Interrupt: Radar sensor to host interrupt GPIO
- RadarSensor_nRESET: Radar sensor reset
- RadarSensor_nERROROut: Error output status indication
- RadarSensor_WARMRESET: Reset output status indication
- RadarSensor_SOP signals: Each radar sensor has a BootMode. These signals indicate to the sensor whether the QSPI flash updates are performed or if the radar sensor is in functional mode.
- RadarSensor_UART_TxRx: QSPI flash mode uses these signals.

The host processor controls the radar sensor power sequencing based on two radar sensors per PMIC. The additional inter-integrated circuit (I^2C) port allows for power monitoring and customization of the PMIC-programmed OTP parameters.

- RadarSensorPMIC_Reset: PMIC reset (can be PMIC enable also)
- RadarSensorPMIC_PGood: Output power status from the PMIC
- RadarSensorPMIC_I2C: PMIC control and monitoring port

In Figure 7, the internal watchdog timer is used to time the radar sensor MSS processor completing its software cycle.

The host processor has an external watchdog timer and internal communication timers for each radar sensor. The host processor has four radar sensors and two radar PMICs in this example. The host processor starts the radar sensor power by releasing PMIC_Reset. The PMIC do their initialization, eventually asserting the PGood signal. When the PMICs have been programmed, and the PGOOD output is present, the SOP signals are asserted for the radar sensor for functional mode. After a short delay, the radar sensor nRESET signals are released.

The host processor starts a radar sensor boot completion cycle timer to check that the host interrupt from the radar sensor arrives within the expected time. At this point, each radar sensor loading MSS processor performs the boot loading, configuration, and start of the application. At the conclusion of loading, the radar sensor host interrupt is output when the host processor senses this signal. The WARMRESET and nERROROUT signals from each radar sensor are checked to ensure proper initialization.

In some applications, the radar sensors are preprogrammed, and then the host processor processes the LVDS outputs. In this case, the communication time-out timer for the host processor monitors each expected radar sensor message. If the host processor expects SPI data from the radar sensors, additional communications messages are checked. While the radar sensors are running, the local MSS processors communicate with the BSS and DSS (if present). The radar sensor MSS processor updates the internal watchdog timer, to keep the radar sensor running.

The WARMRESET signal is output from the radar sensor to indicate to the host processor that an external or internal reset is pending on the radar sensor. The nERROROUT signal is output from the radar sensor to the host processor, as an indication of an error condition. The host processor can communicate with the radar sensor over SPI to determine the error condition and recovery or reset needed.

The radar sensor can send high-speed radar receiver data over LVDS or CSI-2 data lines. The data lines are not discussed in this application description, see the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page. The radar sensors require clock and synchronization in satellite operation, which is not discussed in this application description either. The key difference between Section 2.3 and Section 2.4 is that the host processor has multiple radar sensors to control. The host processor and radar sensors each have a watchdog timer for the individual software cycle processes. In addition, the host processor manages the communication errors.

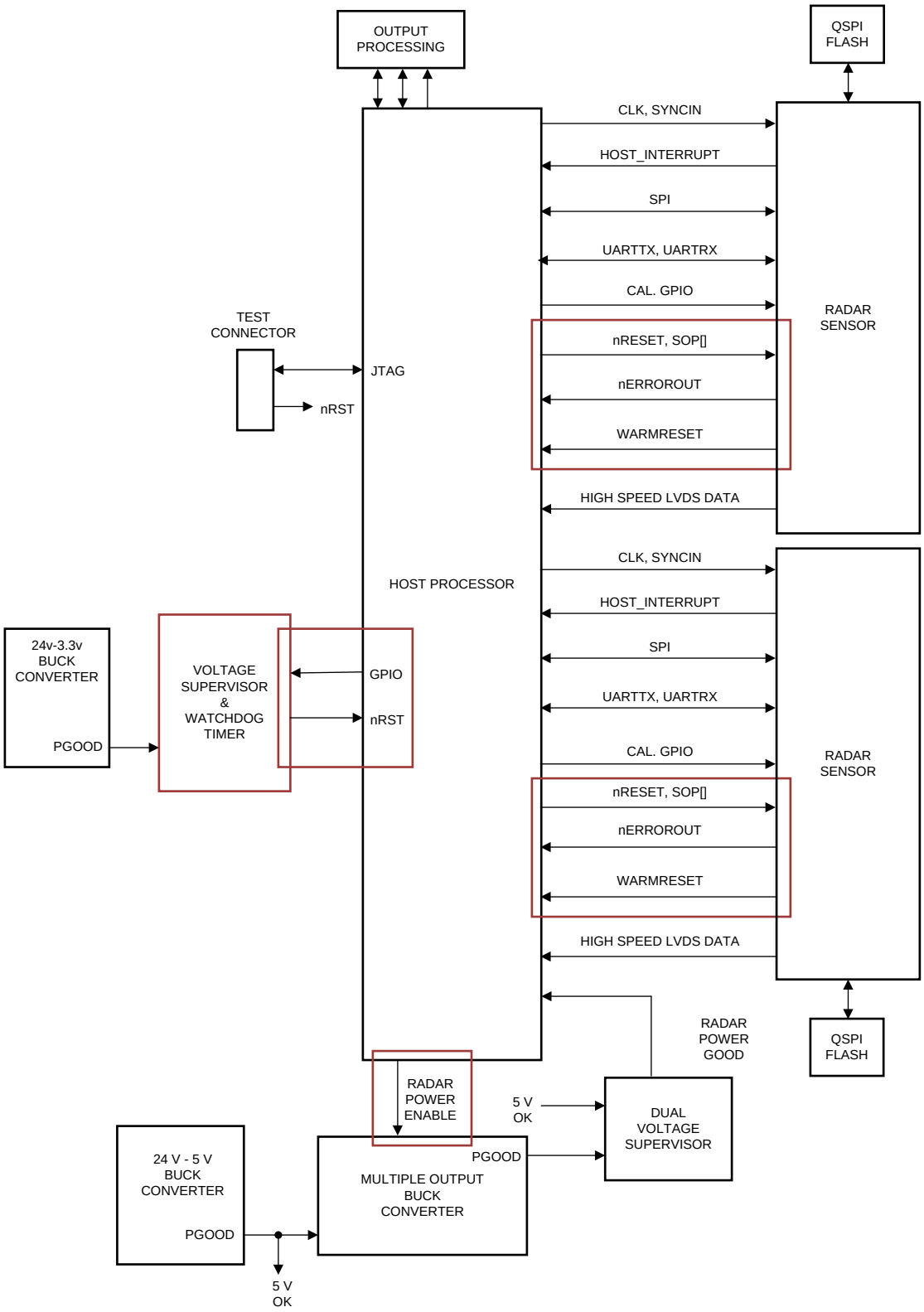

Figure 7. Host Processor and Satellite Radar Sensors – External Watchdog Timer for Host, Communication Timer for Radar Sensors, Internal Watchdog Timers for Radar Sensors

3 Details of nRESET, WARMRESET, nERROROUT Signals

This section discusses the hardware details for external reset, internal reset, and the ESM for the nERROROut signal.

3.1 Reset Signals

Minimum signal use:

- nRESET – External radar reset signal, power on reset, used to reset the device and latch the SOP mode for flashing, debugging or operation.

Other signals used:

- WARM_RESET – This signal is an indication of external reset or internal resets for the radar sensor.
- nERROR_OUT – This error signal is an output from the radar sensor to another device. It can be used for external monitoring or additional functions. It normally requires a pullup resistor.

3.1.1 External Radar Resets

- Reset input to the radar sensor – In the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page, see the *Reset* chapter. nRESET is the device RESET pin, active-low. In the *Reset Overview* figure, nRESET and WARM_RESET are shown.
- The WARM_RESET signal can be software configured as an external RESET input.

3.1.2 Internal Radar Resets

- In the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page, see the *Reset* chapter; several signals can be used as internal radar resets.
- DBGRSTN – Debug reset from the debug subsystem, used in emulator control of reset
- MSS_WD_RST – MSS_WDT(MSS_RTIB) watchdog timer reset of MSS_CCCB (16xx only) clock for timer error. In the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page, the RTI_RESETn time-out or MSS_CCCB counter error (if enabled) can cause an MSS_WD_RST. The MSS_CCCB counter compares the internal clock with the oscillator input for a clock reference error.

NOTE: The internal watchdog timer is part of MSS_RTIB (WDT/RTIB).

NOTE: WDRSTEN is the software enable for the watchdog timer. As a default, WDRSTEN disables the watchdog timer.

NOTE: The internal architecture generates an internal NMI or WARMRESET for a watchdog timer time-out. The NMI is used to force error logging, which then triggers a software reset. The *Real Time Interrupt (RTI) and RTI With Digital Watchdog Timer (WDT)* chapter in the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page discusses the real-time counter used for the watchdog timer.

- SOFTSYSRST – Software register reset that can trigger the WARMRESET function from a register write.

3.1.3 WARMRESET Output Indication of RESET

When enabled in the default RESET configuration, the WARMRESET output indicates that a RESET condition has occurred.

3.2 nERROR_OUT and nERROR_IN Error Signaling

The *Safety* chapter in the device-specific Technical Reference Manual (TRM) listed under Technical Documents on the mmwave product page discusses the ESM. There are several groupings of error conditions within the radar sensor, as follows:

- Low severity (generates an interrupt, may generate an nERROR_OUT)
- High severity (generates an interrupt, generates an nERROR_OUT)

The error conditions are a result of enhanced monitoring. Some may signal that a device reset is needed to recover from the error.

The nERROR_OUT signal needs a pullup resistor, and the error condition is a logic 0.

4 Summary

This application report reviews the industrial radar sensor use of the nRESET input, nERROROUT and WARMRESET output signals, and GPIO for the external watchdog timer update. The four application scenarios describe how a watchdog timer checks the Arm processor in the radar sensor for the completion of the software process cycle within a certain period of time. In cases where the radar sensor communicates over SPI with a host processor, there is an additional discussion of a communication time-out timer, to ensure that communication data is received within an expected period.

There are specific scenarios for a stand-alone radar sensor, host processor with single radar sensor, and host processor with multiple radar sensors.

5 References

1. American National Standards Institute, *IEC 61508 – Standards for Electronic Devices for Functional Safety*
2. Texas Instruments, *Overview of Texas Instruments Power Supervisory and Watchdog timer devices*
3. Texas Instruments, Introduction to Watchdog Timers

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to A Revision	Page
• Title was changed.	1
• Update was made in Section 1.	2
• Updates were made in Section 1.1.	3
• Update was made in Section 3.1.1.	13
• Updates were made in Section 3.1.2.	13
• Update was made in Section 3.2.	14
• Updates were made in Section 5.	14

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