TPS650860 PMIC User's Guide For I²C Configurable-Systems

This user's guide describes the default one-time programmable (OTP) settings for the TPS650860 orderable part number. The TPS650860 part-number specific settings are intended to demonstrate the range of factory-programmable settings for the TPS65086 family of devices available for custom spins, including voltage, sequencing, and GPO options for example. Additionally, the TPS650860 was designed to allow for I²C configuration of the volatile memories to generate the desired default voltages and power-up sequence using the I2C_RAIL_EN registers. The TPS650860 part-number specific settings were not chosen for use with any specific processor or system. Instead, new settings can be sent by a microprocessor to the power management IC (PMIC) device using I²C after the PMIC loads its default register values from the factory-programmed memory. These values are stored in the volatile memory registers. New factory-programmed versions of the TPS65086 device developed by Texas Instruments require sufficient business case and approval before implementation. For more information, contact a local TI sales representative.

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Trademarks

1 Introduction

This document is provided to define the part number specific settings for TPS650860 device. This document includes the power map, the default voltage settings, the power-up sequence, and the power-down sequence. Some guidance on connection with the system are also provided. This user's guide does not provide details about the power resources, external components, or functionality of the device. For such information, see the full specification in the device data sheet.

2 Device Versions

Table 1 lists the device versions described in this document.

Table 1. TPS650860 Orderable Part Numbers

Orderable Part Number	DEVICEID2 / DEVICEID1	Specific Package Quantity	Summary
TPS650860A0RSKR	0x6000	2000	Catalog
TPS650860A0RSKT	0x6000	250	Catalog

3 Power Map

The TPS650860 device is intended as a generic example of available features for the TPS65086xxx family of devices or to have the volatile memory configured by I^2C using a microcontroller to provide the desired voltages and enable timings. For this purpose, the LDOA1 regulator is enabled by default to power a microcontroller.

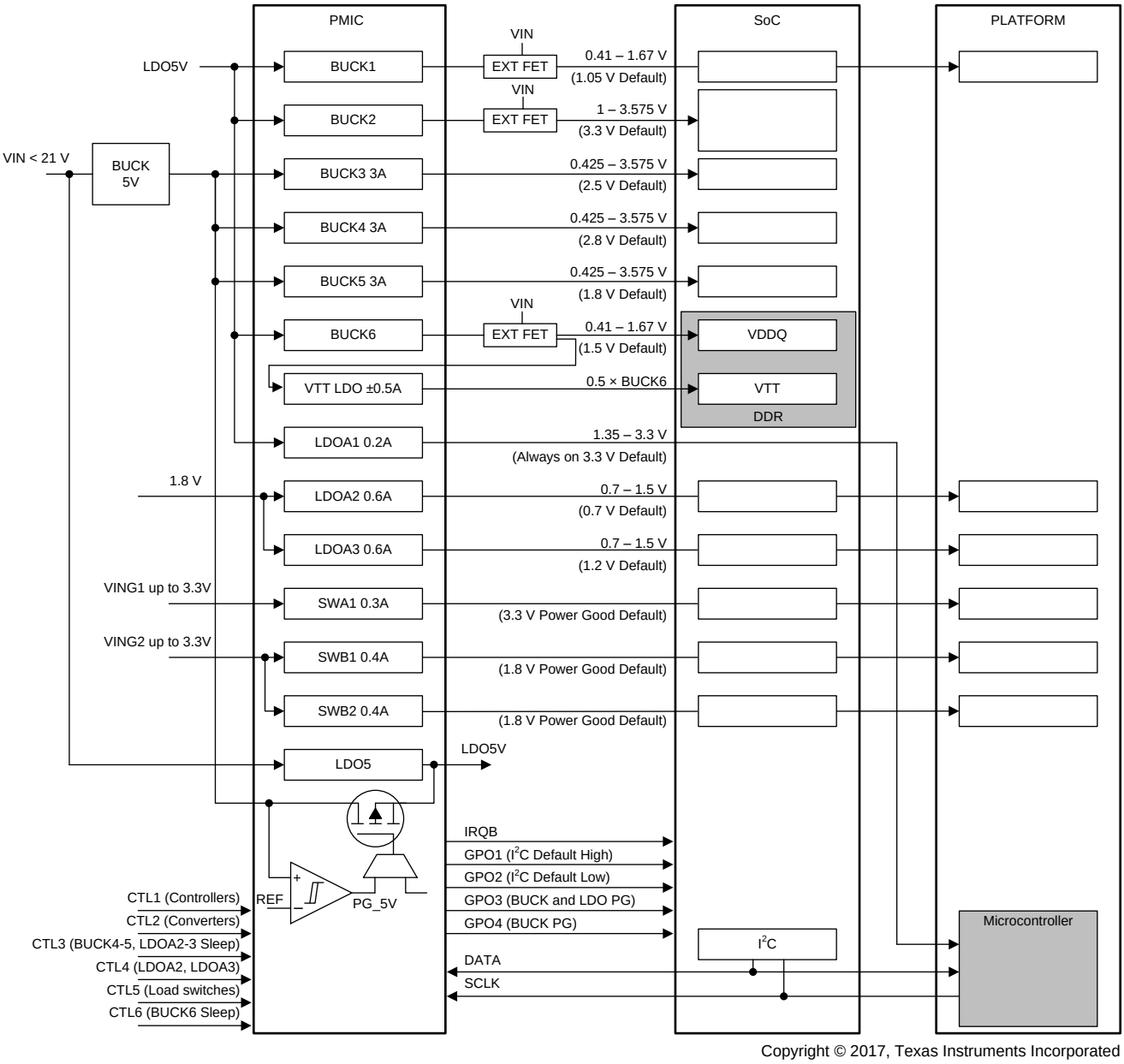

Figure 1. TPS650860 Typical Power Map

Table 2. CTL Pin Functionality

CTL Pin	Functionality	Description
CTL1	Controller Enable	The CTL1 pin is the pin-controlled enable for the BUCK1, BUCK2, and BUCK6 controllers. This pin should be connected to ground if using I^2C to set the voltage and enable or disable these rails.
CTL2	Converter Enable	The CTL2 pin is the pin-controlled enable for the BUCK3, BUCK4, and BUCK5. This pin should be connected to ground if using I^2C to set the voltage and enable or disable these rails.
CTL3	BUCK4-5, LDOA2-3 Sleep	When the CTL3 pin is pulled high, the BUCKx_VID registers are used for the BUCK4 and BUCK5 converters and LDOAx_SLP_VID bits are used for LDOA2 and LDOA3 regulators. When the CTL3 pin is pulled low, the BUCKx_SLP_VID registers are used for the BUCK4 and BUCK5 converters and LDOAx_VID bits are used for LDOA2 and LDOA3 regulators.

Table 2. CTL Pin Functionality (continued)

CTL Pin	Functionality	Description
CTL4	LDOA2_A3 Enable	The CTL4 pin is the pin-controlled enable for the LDOA2 and LDOA3 regulators. This pin should be connected to ground if using I^2C to set the voltage and enable or disable these rails. LDOA2 and LDOA3 will only be enabled by this pin if BUCK5 is enabled and BUCK5_PGOOD is 1b.
CTL5	Load Switches Enable	The CTL6 pin is the pin-controlled enable for the SWA1, SWB1, and SWB2 load switches. This pin should be connected to ground if using I^2C to enable or disable these rails. Load siwtches will only be enabled by this pin if BUCK5 is enabled and BUCK5_PGOOD is 1b.
CTL6	BUCK6 Sleep	When the CTL6 pin is pulled high, the BUCK6_VID register is for the BUCK6 controller. When the CTL6 pin is pulled low, the BUCK6_SLP_VID register is used for the BUCK6 controller.

4 Block Diagram

Figure 2 shows the labeled block diagram for the TPS650860 device.

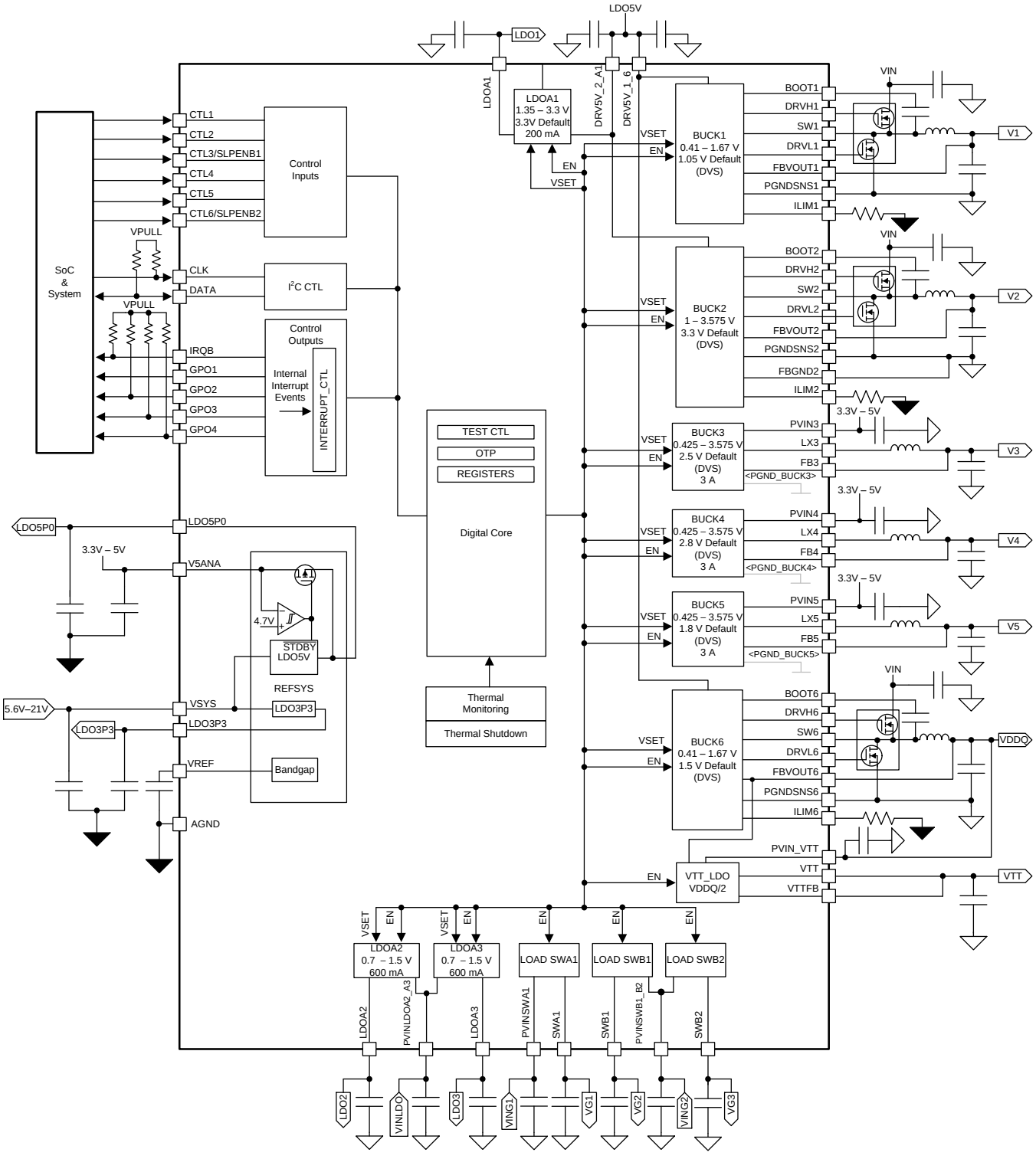

Figure 2. TPS650860 Example Block Diagram

5 Power-Up Sequence

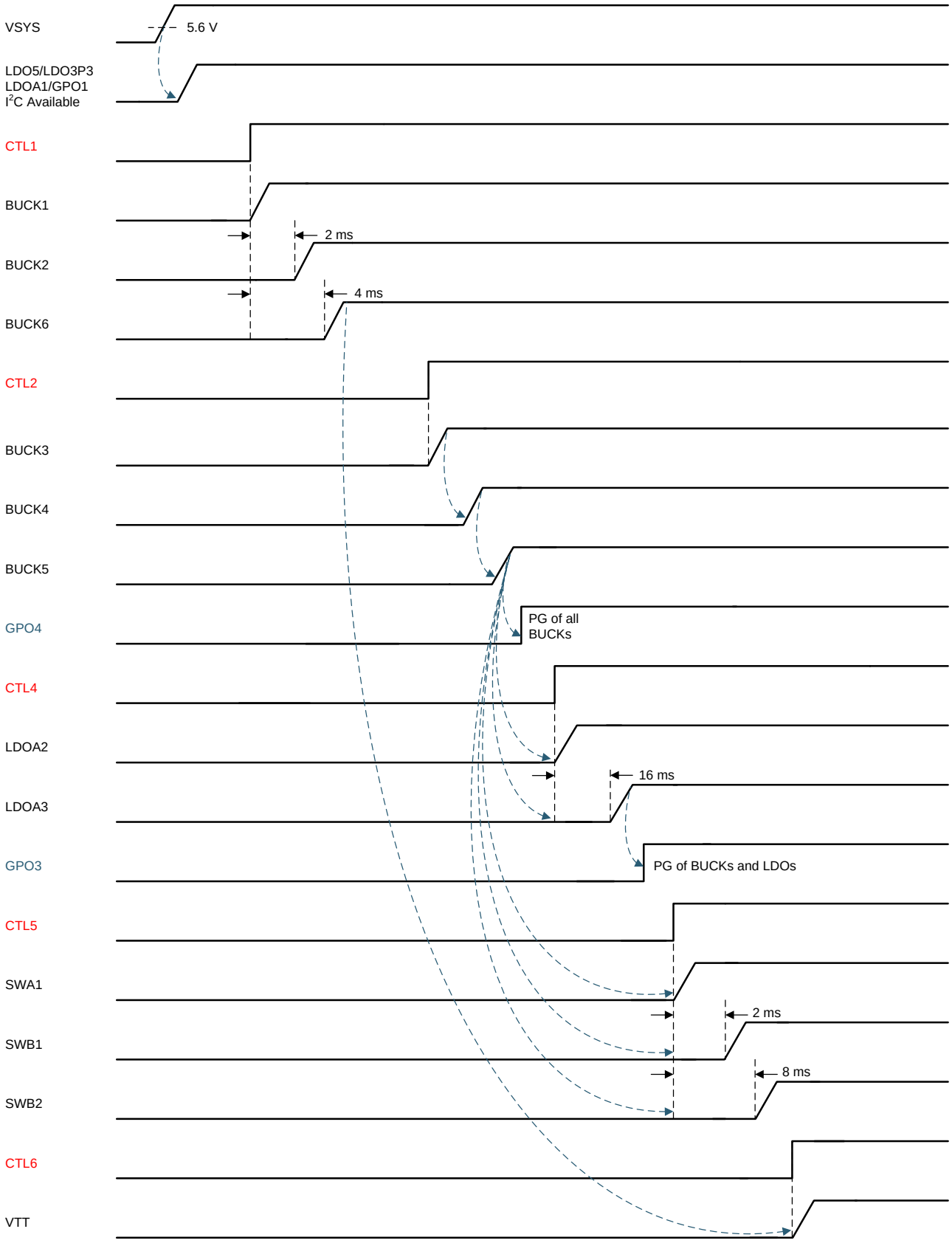

Figure 3. TPS650860 Power-Up Sequence

6 Power-Down Sequence

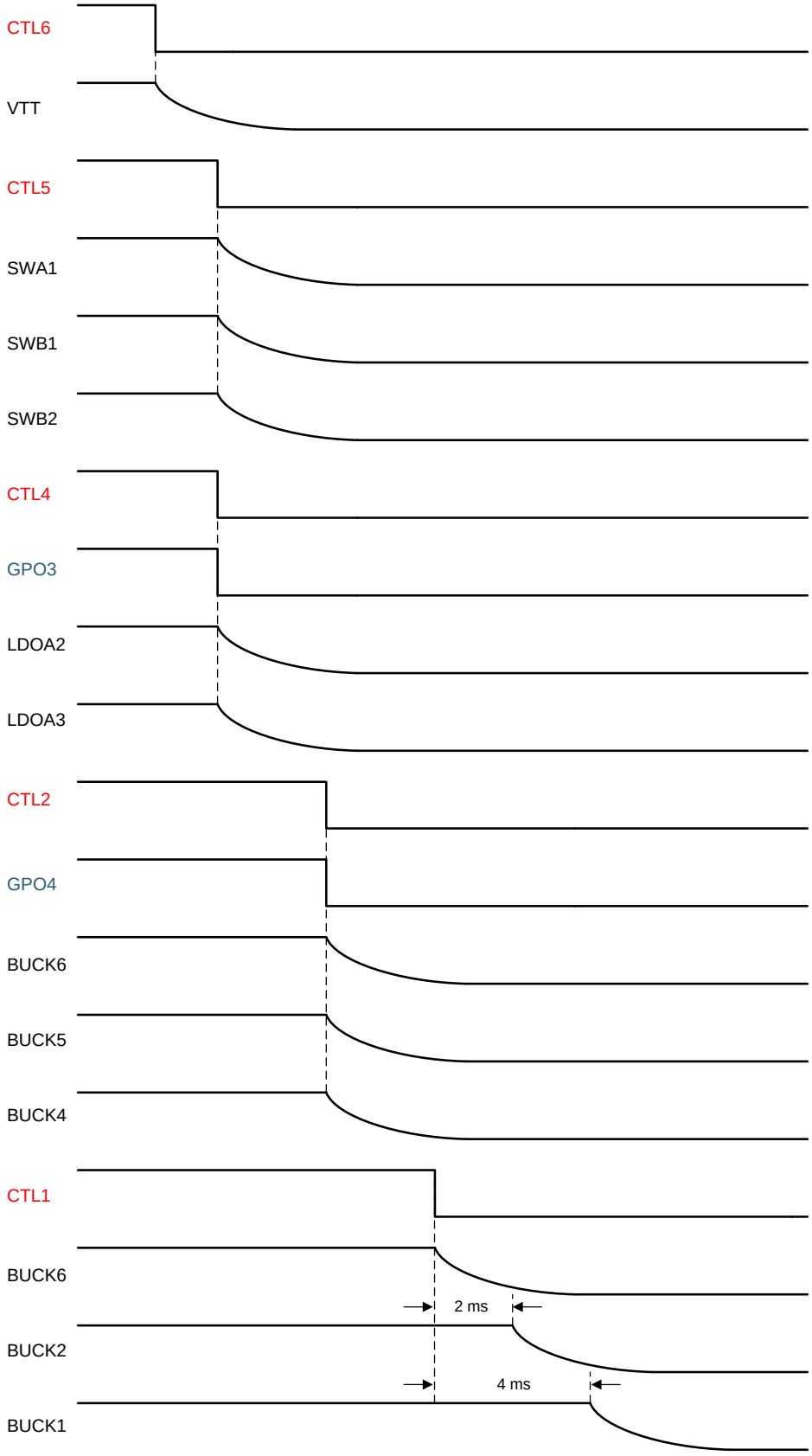

Figure 4. TPS650860 Power-Down Sequence

7 OTP Summary

For this OTP, LDOA1 is not used in sequence so all registers with LDOA1_SWB2 function as LDOA1. Additionally, SWB1 and SWB2 are not merged so all registers with SWB2_LDOA1 function as SWB2. All values that can be modified by I^2C after power on are shown in *italics*. For additional details (such as GPO power-good inputs), refer to the device register map.

Table 3. TPS650860 Settings Summary—Buck Regulators

Regulator	Default Voltage	Sleep Voltage	Step Size	SLP Pin	SLP_EN	Power fault Masked	Force PWM
BUCK1	*1.05 V*	*1.05 V*	10 mV	CTL3	*No*	*No*	*Auto*
BUCK2	*3.3 V*	*3.3 V*	25 mV	CTL3	*No*	*No*	*Auto*
BUCK3	*2.5 V*	*2.5 V*	25 mV	CTL3	*No*	*No*	*Auto*
BUCK4	*2.8 V*	*2.8 V*	25 mV	CTL3	*Yes*	*No*	*Auto*
BUCK5	*1.8 V*	*1.8 V*	25 mV	CTL3	*Yes*	*No*	*Auto*
BUCK6	*1.5 V*	*1.5 V*	10 mV	CTL6	*Yes*	*No*	*Auto*

Table 4. TPS650860 Settings Summary—General Purpose LDOs

Regulator	Default Voltage	Sleep Voltage	Always-On	SLP Pin	SLP_EN	Power Fault Masked
LDOA1	*3.3*	—	Yes	—	—	*Yes*
LDOA2	*0.7*	*0.7*	—	CTL3	*Yes*	*Yes*
LDOA3	*1.2*	*1.2*	—	CTL3	*Yes*	*No*

Table 5. TPS650860 Settings Summary—VTT LDO

Regulator	ILIM Setting	ENABLE Pin	Power Fault Masked
VTT LDO	0.95 A	CTL6	*No*

Table 6. TPS650860 Settings Summary—Load Switches

Regulator	Power-Good Voltage	SWB1_2 Merged	Power Fault Masked
SWA1	3.3 V	—	*Yes*
SWB1	1.8 V	No	*Yes*
SWB2	1.8 V	No	*Yes*

Table 7. TPS650860 Settings Summary—GPOs

GPO	Power Good (PG) or I^2C	State	Output Type
GPO1	I^2C	*High*	Push Pull
GPO2	I^2C	*Low*	Open Drain
GPO3	PG	—	Open Drain
GPO4	PG	—	Open drain

Table 8. TPS650860 Default Register Values

Address	Name	Default Value [7:0]
00h	DEVICEID1	8b01100000
01h	DEVICEID2	8b00000000
20h	BUCK1CTRL	8b10000010
21h	BUCK2CTRL	8b11101000
22h	BUCK3DECAY	8b10101000

Table 8. TPS650860 Default Register Values (continued)

Address	Name	Default Value [7:0]
23h	BUCK3VID	8b10101000
24h	BUCK3SLPCTRL	8b10101000
25h	BUCK4CTRL	8b00111101
26h	BUCK5CTRL	8b00111101
27h	BUCK6CTRL	8b00111101
28h	LDOA2CTRL	8b00111101
29h	LDOA3CTRL	8b00111101
40h	DISCHCTRL1	8b01010101
41h	DISCHCTRL2	8b01010101
42h	DISCHCTRL3	8b00010101
43h	PG_DELAY1	8b00000111
92h	BUCK1SLPCTRL	8b10000010
93h	BUCK2SLPCTRL	8b11101000
94h	BUCK4VID	8b11000000
95h	BUCK4SLPVID	8b11000000
96h	BUCK5VID	8b01110000
97h	BUCK5SLPVID	8b01110000
98h	BUCK6VID	8b11011100
99h	BUCK6SLPVID	8b11011100
9Ah	LDOA2VID	8b00000000
9Bh	LDOA3VID	8b10101010
9Ch	BUCK123CTRL	8b00000111
9Dh	PG_DELAY2	8b00010010
9Fh	SWVTT_DIS	8b11110000
A0h	I2C_RAIL_EN1	8b00000000
A1h	I2C_RAIL_EN2/GPOCTRL	8b00010000
A2h	PWR_FAULT_MASK1	8b11000000
A3h	PWR_FAULT_MASK2	8b00110110
A4h	GPO1PG_CTRL1	8b11111111
A5h	GPO1PG_CTRL2	8b11111111
A6h	GPO4PG_CTRL1	8b11000000
A7h	GPO4PG_CTRL2	8b11001111
A8h	GPO2PG_CTRL1	8b11011111
A9h	GPO2PG_CTRL2	8b11101111
AAh	GPO3PG_CTRL1	8b01000000
ABh	GPO3PG_CTRL2	8b10001110
ACh	MISCSYSPG	8b11111111
ADh	VTT_DISCH_CTRL	8b01001010
AEh	LDOA1_SWB2_CTRL	8b01011101

8 Application-Specific Information

The following sections describe additional information which may help in system-level design.

8.1 I²C Configuration

After the VSYS pin voltage of the PMIC device reaches 5.6 V and LDO5P0 output is stable, the PMIC device loads the default factory programmed values from the one-time programmable (OTP) memory into the volatile register memory. Many of these bits are user accessible and can be modified to provide the desired behavior. The following procedure provides a simple, general example configuration flow. This procedure assumes that all CTLx pins are connected to ground.

1. Write the desired voltages into VID bits.
   - With all CTLx pins low and no SLP_EN bits changed, the VID bits are:
     - BUCK1_VID
     - BUCK2_VID
     - BUCK3_VID
     - BUCK4_SLP_VID
     - BUCK5_SLP_VID
     - BUCK6_SLP_VID
     - LDOA2_SLP_VID
     - LDOA3_SLP_VID
   - SLP_VID values do not need to be used if BUCKx_SLP_EN and LDOAx_SLP_EN bits are first written to 0b.
   - Alternatively, both VID and SLP_VID values can be written for all regulators.
2. Write the desired GPO3PG_CTRLx and GPO4PG_CTRLx bits if they are used in the system.
3. Modify the I2C_RAIL_EN1 and I2C_RAIL_EN2 bits to enable the regulators in the required order for the application.
4. Set GPO1 low or GPO2 high using the GPO_LVL bits to signify that the sequence has been completed and connect this GPO back to the microprocessor to monitor.
5. If GPO1 or GPO2 value returns to default value after their polarity is changed by I²C, it would indicate part has experienced a shutdown condition and the configuration needs to be rewritten after the microcontroller checks the SHUTDNSRC register to identify the cause of the shutdown.

8.2 Limitations

Some settings are not accessible in the register map and cannot be changed without new factory programming. These settings include the following:

- Buck regulator VID step size cannot be changed. As a result, BUCK2 cannot be less than 1 V, BUCK1 cannot be more than 1.67 V, and BUCK6 cannot be more than 1.67 V.
- CTLx pin sequencing cannot be changed.
- Sleep pin assignment cannot be changed.
- LDOA1 can be disabled, but it will turn on again in the event of a shutdown.
- VTT current limit cannot be changed.
- Power good level of the load switches cannot be changed.
- GPOs being controlled by either GPO_LVL bits or PG bits cannot be changed. For GPOs factory programmed to be controlled by power good, the power good mask bits can be changed.
- GPO output type of push-pull or open drain cannot be changed.

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