TPS659105 User Guide For DaVinci Family of Processors

This user guide can be used as a reference for connectivity between the TPS659105 power-management integrated circuit (PMIC) and TI DaVinci™ processors, DM643x and DM644x.

Contents

List of Figures

List of Tables

1 Introduction

This user guide can be used as a reference for connectivity between the TPS659105 PMIC and TI DaVinci processors, DM643x and DM644x. This user guide does not provide details about the power resources or the functionality of the device. For such information, refer to the full specification document, *TPS65910 Data Manual*.

2 Platform Connection

Figure 1 and Figure 2 show the TPS659105 connections with the DM643x and DM644x processors, respectively.

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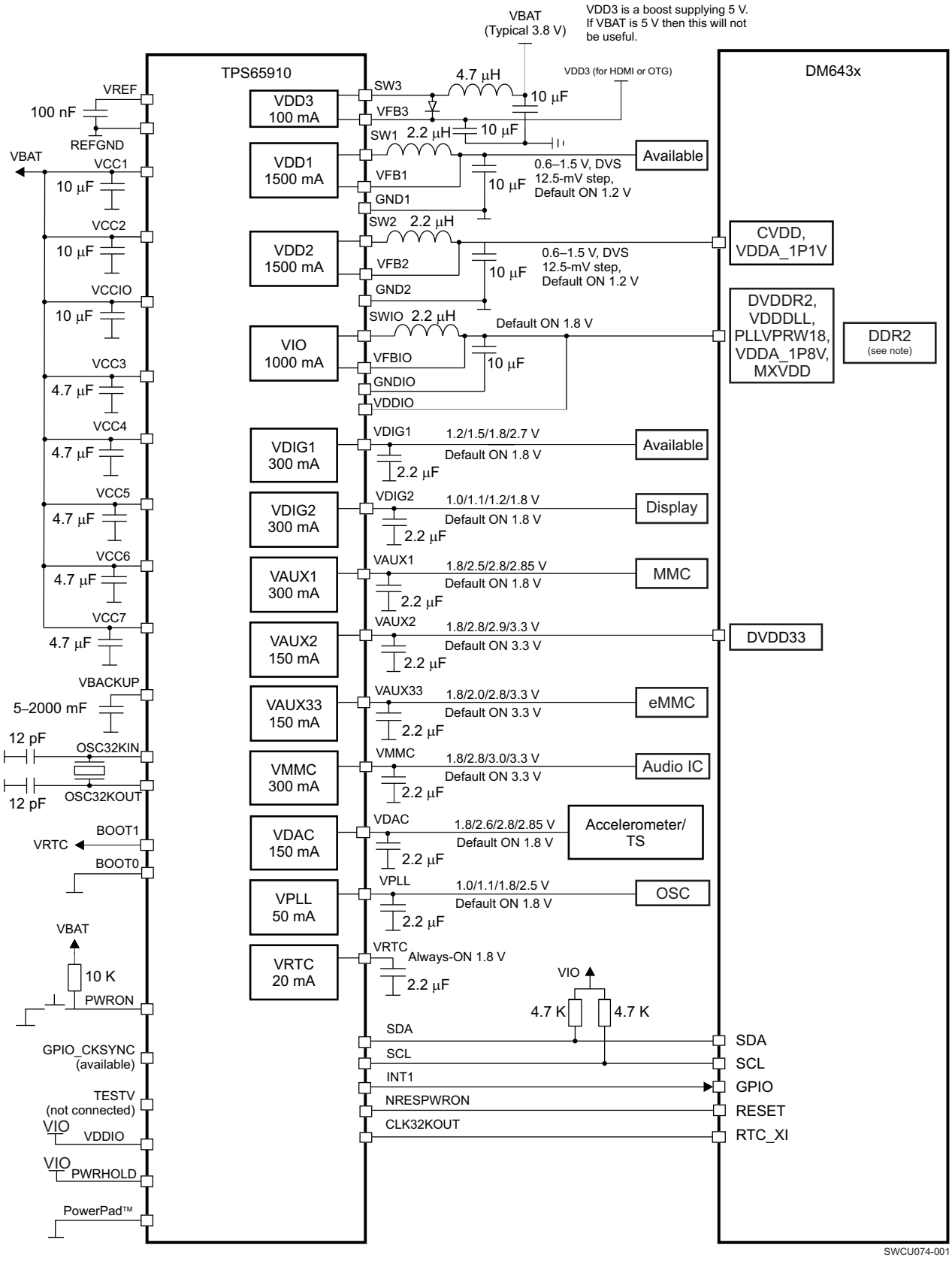

NOTE: DDR2 memory chip can be powered up with VIO domain.

Figure 1. DM643x Power Supply Connections With TPS659105

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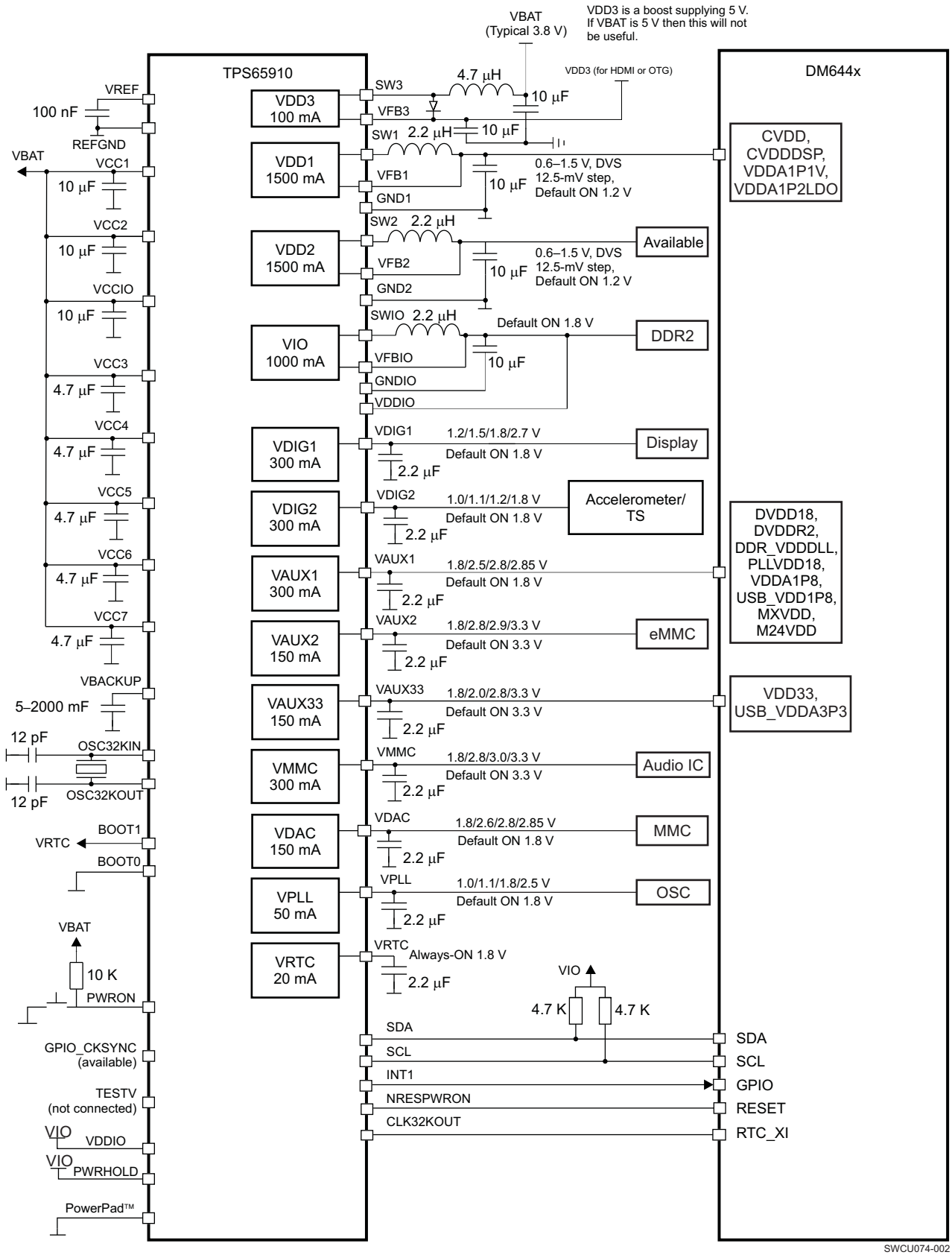

Figure 2. DM644x Power Supply Connections With TPS659105

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At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

The following sections show the power-up sequence requirement for the DM643x processors. To power on the system the user must press and release the PWRON switch (generating a negative pulse).

to correctly power on the device, the PWRHOLD signal must be high after the PWRON button is pressed. In this configuration, the PWRHOLD signal on the TPS659105 is connected to VIO as shown in the Figure 1 and Figure 2. The PWRHOLD signal transitions to high when VIO powers up.

3.1 Power-Up Sequence for DM643x Processors

The BOOT pads on the TPS659105 should be connected as follows:
BOOT0 = 0 and BOOT1 = 1.

Table 1. Power Rail Connections for DM643x

Power Domain	Pin Name	Imax (mA)	Voltage (V)	Sequence
Vcore	CVDD(1), VDDA_1P1V	1480	1.2	3
I/O	DVDD33	40	3.3	1
I/O	DVDDR2, DDR_VDDDL, PLLVPRW18, VDDA_1P8V, MXVDD	140	1.8	2

(1) 1.2 V CVDD for CPU frequencies > 400 MHz. 1.05 V CVDD is only supported on –6 devices running at SYSCLK1 ≤ 400 MHz.

3.2 Power-Up Sequence for DM644x Processors

Table 2. Power Rail Connections for DM644x

Power Domain	Pin Name	Imax (mA)	Voltage (V)	Sequence
Vcore	CVDD, VDDA_1P1V, VDDA1P2LDO, CVDDDSP	1700(1)	1.2	1
I/O	DVDD33, USB_VDDA3P3	25	3.3	2
I/O	DVDD18, DVDDR2, DDR_VDDDLL, PLLVDD18, VDDA1P8V, USB_VDD1P8, MXVDD, M24VDD	170	1.8	2

(1) For specific applications the current requirement is 1700 mA. TPS659105 can be used for applications with current requirement up to 1500 mA.

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3.3 Power-Up Sequence for TPS65910

To satisfy the power-up requirements for DaVinci processors, the TPS659105 powers up with the default sequence when in the EEPROM boot mode configuration (BOOT0 = 0 and BOOT1 = 1), see Table 3. The correct power-up sequence is configured in the EEPROM (factory programmable only).

Apart from the main power rails required for DaVinci processors, all other rails are also powered up at initial power up to support other system peripherals.

Figure 1 and Figure 2 show some typical examples for powering up other peripherals on the user platform.

Table 3 lists the power-up sequence for TPS659105.

Table 3. Power-Up Sequence TPS659105

TPS659105 Power Rail	Sequence Number	Delay (ms)
PWRON (1)	–	–
VDD1	1	2
VAUX2	2	2
VAUX33	2	0
VAUX1	2	0
VIO	3	2
VDD2	4	2
VPLL	5	2
VDIG1	5	0
VDIG2	5	0
VMMC	5	0
VDAC	5	0

(1) The PWRON signal is the start on event. All timings shown are with respect to the previous event.

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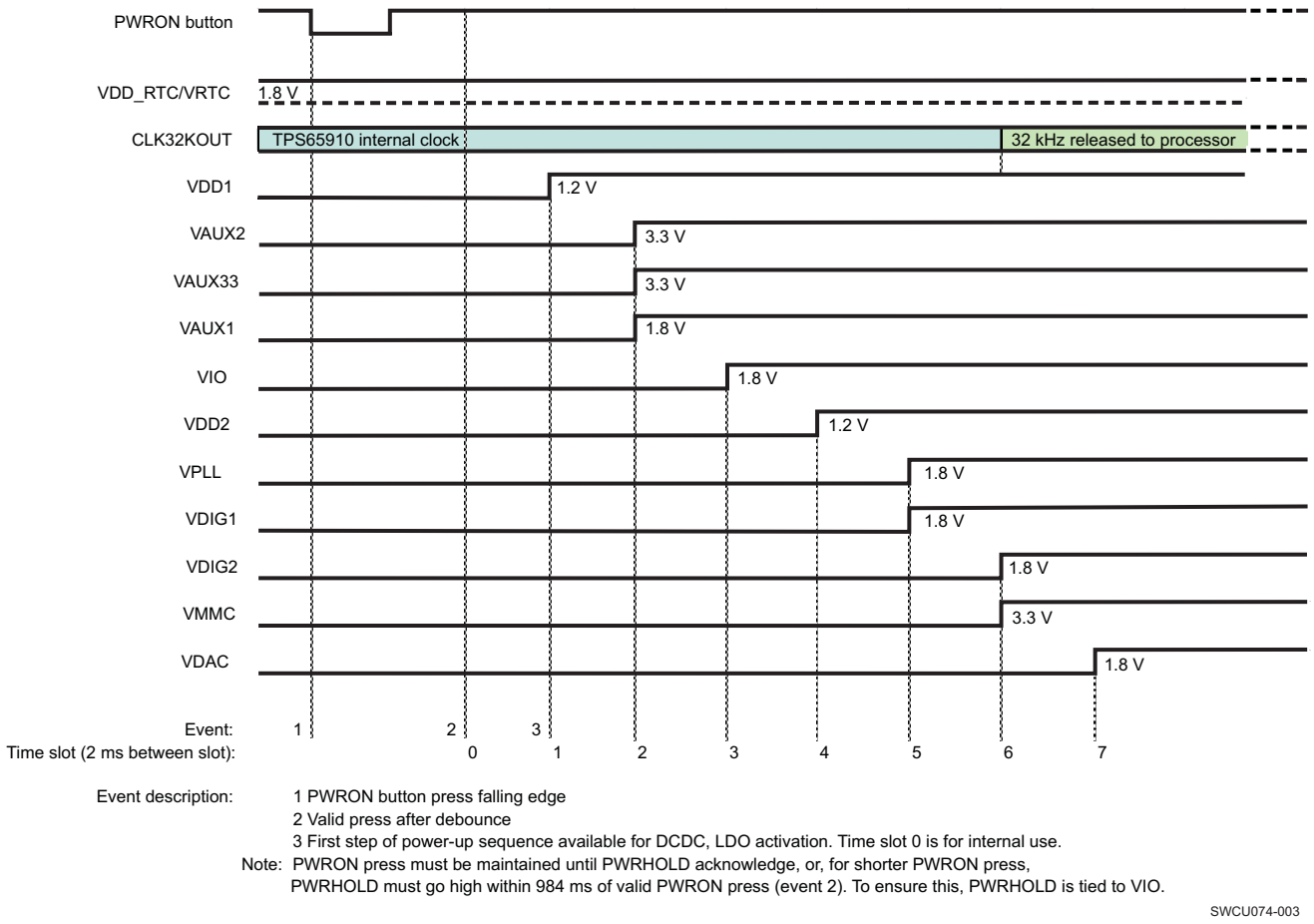

Figure 3. Power-Up Sequence Timing Diagram

Table 4 lists the EEPROM values for the TPS659105.

Table 4. EEPROM Configuration for TPS659105

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 Gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	1
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 Gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	4
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	3
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF (0)
VDIG1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
VDIG2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6

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Table 4. EEPROM Configuration for TPS659105 (continued)

Register	Bit	Description	Option Selected
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	7
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	2
VMMC_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	6
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	2
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	2
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up is reason required before switch-on.	0 = Automatic switch-on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

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4 Getting Started with TPS659105 and DM64xx

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

In the DEVCTRL2_REG register, program the SLEEPSIG_POL bit according to the GPIO or SYS_CLKREQ signal from the DM64xx. This can be set to active-low or active-high for SLEEP transitions. The software configuration allows specific power resources to enter the low-consumption state.

In the DEVCTRL_REG register, set the DEV_SLP bit to 1 to allow the SLEEP transition when requested. Update the GPIO0 configuration (GPIO0_REG) based on your needs.

4.1.2 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If the system has backup battery, set the BBCHEN bit to 1 in the BBCH_REG register to enable backup battery charging. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

4.1.4 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default, in sleep mode all resources maintain their output voltage but transient and load capability are reduced.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

4.2 Event Management Through Interrupts

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that a supply (VBAT) is connected (leaving the BACKUP or NO SUPPLY state) and the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state, then this acts as a wakeup event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 6 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds, the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. The software must take action to decrease the power consumption before automatic shutdown.

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4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shut down to prevent losing data. This interrupt is linked to VBAT but does not apply to a system where PMIC is connected to 5-V rails and not directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT indicates a GPIO interrupt event. It can be used to wake up the device from the SLEEP state. This can be an interrupt coming from any peripheral device or alike.

NOTE: This wakeup event is not valid for a transition from the OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

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