TPS659109 User Guide for i.MX51 and i.MX37 Processors

This user guide can be used as a reference for connectivity between the TPS659109 power-management integrated circuit (PMIC) and the Freescale i.MX51/37 processor.

Contents

List of Figures

List of Tables

1 Introduction

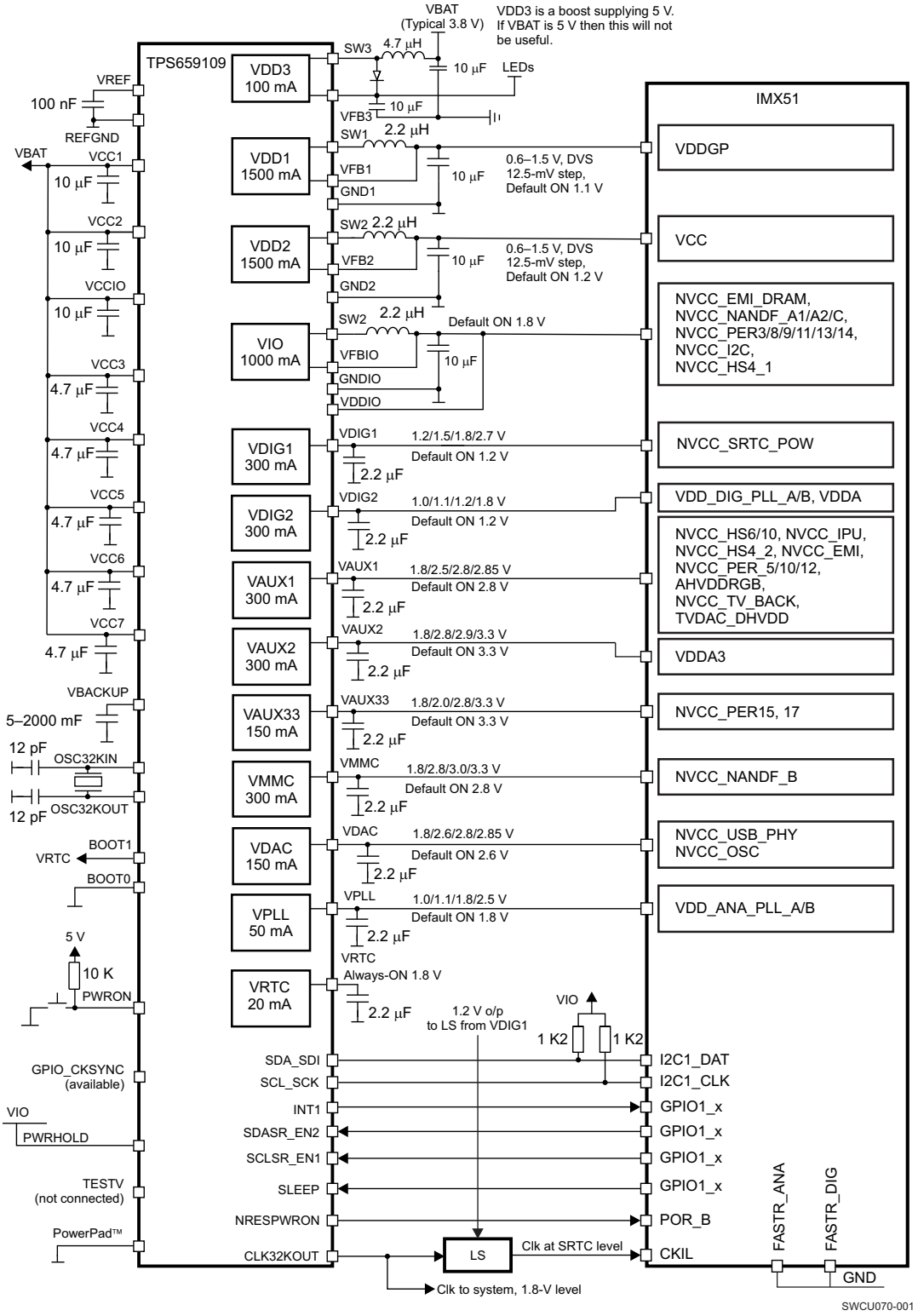
This user guide can be used as a reference for connectivity between the TPS659109 PMIC and the Freescale i.MX51/37 processor. This user guide does not provide details about the power resources or the functionality of the device. For such information, see the full specification document, *TPS65910 Data Manual*. For information about i.MX51/37 processors, refer to official information from Freescale.

NOTE: In this document, the basis for information regarding i.MX processors is from official Freescale documents. Reference is made wherever applicable.

2 Platform Connection

The platform connection in Figure 1 is based on the information in Freescale Application Note AN4053.

Figure 1 shows the TPS659109 connections with the i.MX51 processor.



NOTE:

1. VAUX33 will be powered ON in EEPROM to satisfy VDD3 boost output for LEDs. VDD3 can be enabled by software after initial power up.
2. According to document AN4051.pdf, VREG rail on i.MX51 should be left unconnected. User can disconnect this rail from external power source.

Figure 1. i.MX51 Power Supply Connections With TPS659109

At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

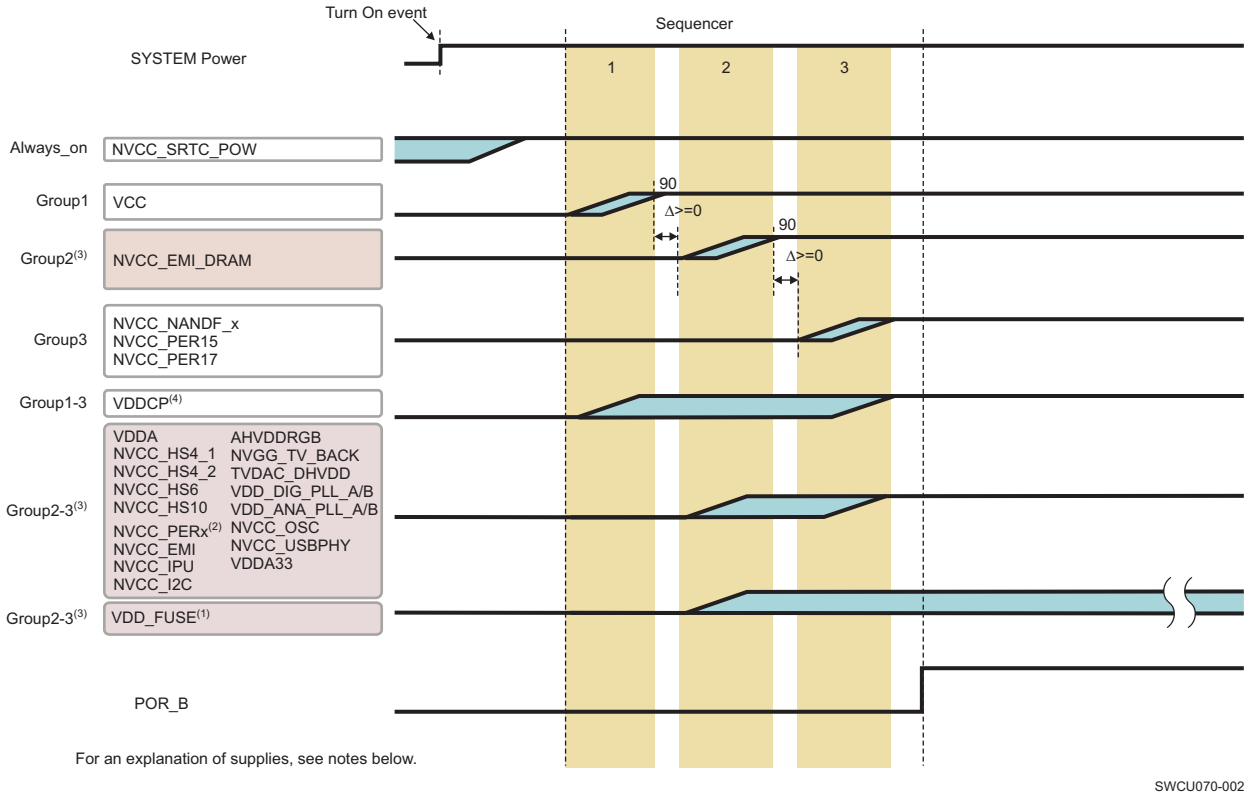
- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

To power on the system, the user must press and release the PWRON switch (generating a negative pulse) connected to the PWRON pad on the TPS659109.

Figure 2 shows the power-up sequence required by the i.MX51 processor (source: Freescale AN4053.pdf Application Note). This is satisfied by the power-up sequence of the TPS659109 when the BOOT pins are set as BOOT0 = 0 and BOOT1 = 1. The TPS659109 has a programmable EEPROM, which can be configured for the i.MX51 power-up sequence (factory programmable) as seen in Figure 2.

Table 1 shows the power domain mapping for the i.MX51 and TPS659109.



NOTE:

1. VDD_FUSE should only be powered when programming internal fuses.
2. NVCC_PERx NVCC_PER_3/5/8/9/10/11/12/13/14.
3. No power-up sequence depencies exist between the supplies shaded in grey in the diagram.
4. There is no requirement for VDDGP to be preceded by any power supply other than NVCC_SRTC_POW.

GENERAL NOTES:

1. Delay between stages can vary, depending on PMIC characteristics. It is up to the application board designer to ensure the power up of the next supply occurs only after the supplies in the previous stage have reached 90 pecent of their target voltage level.
2. Rise time within a group is flexible (that is, there is no special order).

Figure 2. Recommended Power-Up Sequence for i.MX51 (Source: Freescale ANA4053 Application Note)

Table 1. Power Domain Mapping

Atlas (MC13892) Power Supply[1]	i.MX51 Power Domain	TPS659109 Power Supply	Comments
SW1	VDDGP	VDD1	
SW2	VCC	VDD2	
SW3	VDDA VDD_DIG_PLL_A VDD_DIG_PLL_B	VDIG2	Absolute maximum current consumption on the three rails is 200 mA + 10 mA = 220 mA. For this reason VDIG2 LDO is capable of providing 300 mA, which is sufficient.
SW4	NVCC_EMI_DRAM NVCC_NANDF_A1/A2/B/C NVCC_PER3/8/9/11/13/14 NVCC_I2C NVCC_HS4_1	VIO	
SWBST	For LEDS	VDD3	SWBST in Atlas is not powered ON in the power-up sequence. VDD3 on TPS659109 is also not powered ON in the power up sequence.
VUSB	VDDA3	VAUX2	
VUSB2	NVCC_USBPHY NVCC_OSC	VDAC	
	NVCC_SRTC_POW	VDIG1	
VDIG	NVCC_PER15,17	VAUX33	VAUX33 powers up at 3.3 V and can be used for audio
VIOHI	NVCC_HS6/10 NVCC_IPU NVCC_HS4_2 NVCC_EMI NVCC_PER_5/10/12 AHVDDRGB NVCC_TV_BACK TVDAC_DHVDD	VAUX1	
VGEN2	NVCC_NANDF_B	VMMC	VMMC powers up at 3 V, it can be used to power NVCC_PER15 as per Freescale suggestions or can be used for MMC applications. In that case NVCC_PER15 can be connected to 2.8 V (VAUX1).
	VDD_ANA_PLL_A/B	VPLL	

(1) VREG is not included because it has to be kept floating (as per Freescale documentation).

3.1 TPS659109 Power-Up Sequence

Figure 3 shows the timing diagram for the for the TPS659109 power up.

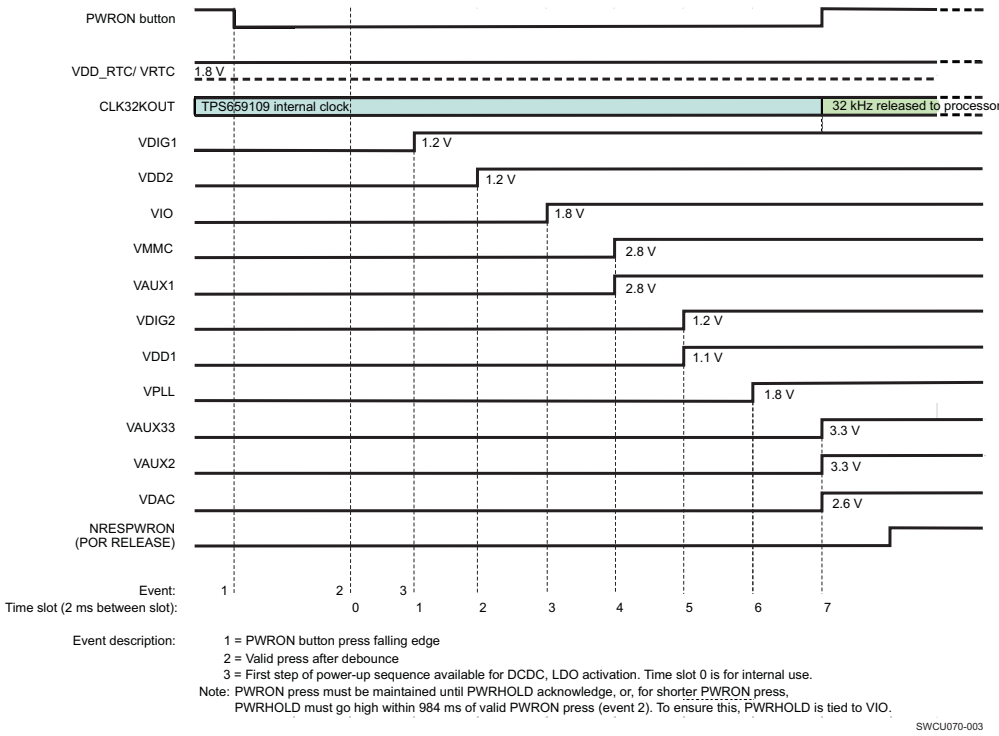


Figure 3. Power-Up Timing Diagram

Figure 4 shows the timing diagram for the power rails of MC13982.

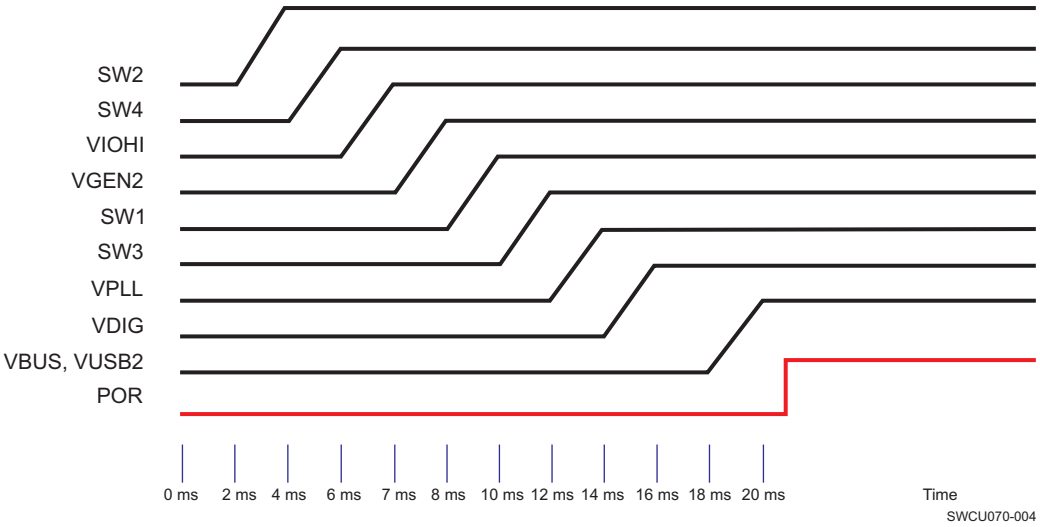


Figure 4. Timing Diagram of Power Rails for MC13982 (Source: Freescale AN4053.pdf Application Note)

Table 2 and Table 3 show the power rails connected to the switching regulator and the low-dropout regulator (LDO) from the Atlas. (Source: AN4053 Freescale Application Note)

Table 2. Power Rails Connected to the i.MX51

VSRTC	SW1	SW2	SW3	SW4	SWBST	VUSB
NVCC_SRTC_POW	VDDGP	VCC	VDDA	NVCC_EMI_DRAM	For LEDs	VDDA33
–	–	–	VDD_DIG_PLL_A	NVCC_NANDF_A1	–	–
–	–	–	VDD_DIG_PLL_B	NVCC_NANDF_A2	–	–
–	–	–	VREG	NVCC_NANDF_B	–	–
–	–	–	–	NVCC_NANDF_C	–	–
–	–	–	–	NVCC_EMI_DRAM	–	–
–	–	–	–	NVCC_PER3	–	–
–	–	–	–	NVCC_PER11	–	–
–	–	–	–	NVCC_PER14	–	–
–	–	–	–	NVCC_I2C	–	–
–	–	–	–	NVCC_HS4_1	–	–

Table 3. Power Rails Connected to the i.MX51

VUSB2	VPLL	VDIG	VIOHI	VGEN2
NVCC_USBPHY	VDD_ANA_PLL_B	For audio	NVCC_HS10	VDD_FUSE
NVCC_OSC	VDD_ANA_PLL_A	–	NVCC_HS6	NVCC_PER15
–	–	–	NVCC_HS4_2	–
–	–	–	NVCC_IPU	–
–	–	–	NVCC_PER5	–
–	–	–	NVCC_PER8	–
–	–	–	NVCC_PER9	–
–	–	–	NVCC_PER10	–
–	–	–	NVCC_PER12	–
–	–	–	NVCC_PER13	–

Table 4 shows the EEPROM values for the TPS659109.

Table 4. EEPROM Configuration for TPS659109

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.1 V
VDD1_REG	VGAIN_SEL	VDD1 Gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	5
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 Gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	3
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	0
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	1
VDIG2_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	5
VDAC_REG	SEL	LDO voltage selection	2.6 V
EEPROM		LDO time slot	7
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6
VAUX1_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	4
VMMC_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	4
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	7
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	7
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	0
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	0
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	0 (Cyrstal)
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	1
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	0
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up reason is required before switch on.	1
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

Table 5 describes the power-up sequence required for the i.MX51 and i.MX37 processor. The data is based on the power-up sequence for the i.MX37 and i.MX51 in Freescale Application Note AN3867.

Table 5. Typical Connections for Power-Up Sequence(1)

i.MX	37/51	37/51	37/51	37/51	35	27/31
PUMS1	**GND**	**Open**	**VCOREDIG**	**VCORE**	**GND**	**Open**
PUMS2	**Open**	**Open**	**Open**	**Open**	**GND**	**GND**
SW1(2)	0.775	1.050	1.050	0.775	1.200	1.200
SW2(2)	1.025	1.225	1.225	1.025	1.350	1.450
SW3(2)	1.200	1.200	1.200	1.200	1.800	1.800
SW4(2)	1.800	1.800	1.800	1.800	1.800	1.800
SWBST	Off	Off	Off	Off	5.000	5.000
VUSB	3.300(3)	3.300(3)	3.300(3)	3.300(3)	3.300(4)	3.300(4)
VUSB2	2.600	2.600	2.600	2.600	2.600	2.600
VPLL	1.800	1.800	1.800	1.800	1.500	1.500
VDIG	1.250	1.250	1.250	1.250	1.250	1.250
VIOHI	2.775	2.775	2.775	2.775	2.775	2.775
VGEN2	3.150	Off	3.150	Off	3.150	3.150

(1) Because the following supplies are not included in the matrix, they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO.
(2) The switchers SWx are activated in PWM pulse skipping mode, allowed when enabled by the startup sequencer.
(3) USB supply VUSB is enabled only if 5.0 V is present on UVBUS.
(4) SWBST = 5.0 V powers up and so does VUSB, regardless of 5.0 V present on UVBUS. By default, VUSB is supplied by SWBST.

Table 6 describes the PMUS2 connections required for the power-up sequence.

Table 6. PUMS2 Connections for Power-Up Sequence(1)(2)

Tap × 2.0 ms	PUMS2 = Open (i.MX37, i.MX51)	PUMS2 = GND (i.MX35, i.MX27)
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI
4	SW1	SWBST, VUSB(3)
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8		VDIG
9	VUSB(4), VUSB2	VUSB2

(1) Time slots may be included for blocks which are defined by the PUMS pins as disabled to allow for potential activation.
(2) Because the following supplies are not included in the matrix, they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO. SWBST is not included on the PUMS2=Open column.
(3) SWBST = 5.0 V powers up and so does VUSB, regardless of 5.0 V present on UVBUS. By default, VUSB is supplied by SWBST.
(4) USB supply VUSB is enabled only if 5.0 V is present on UVBUS.

4 Getting Started With TPS659109 (Basic Software Information)

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

Program DEVCTRL2_REG.SLEEPSIG_POL according to the GPIO or SYS_CLKREQ signal from the processor. This can be set to active-low or active-high for SLEEP transitions. The software configuration allows specific power resources to enter the low consumption state.

Set DEVCTRL_REG.DEV_SLP = 1 to allow the SLEEP transition when requested. Update the GPIO0 configuration (GPIO0_REG) based on your needs.

4.1.2 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If the system has a backup battery, set the BBCHEN bit to 1 in the BBCH_REG register, to enable backup battery charging. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

4.1.4 DCDC and Voltage Scaling Resource Configuration

If the SmartReflex™ interface is not used for voltage scaling (power saving) then these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2:

- VDDx_OP_REG.SEL = Roof voltage (ENx ball high)
- VDDx_SR_REG.SEL = Floor voltage (ENx ball low)

Assign control for DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set EN1_SMPS_ASS_REG. VDD1_EN1 = 1
- Set EN2_SMPS_ASS_REG. VDD2_EN2 = 1
- Set SLEEP_KEEP_RES_ON_REG. VDD2_KEEPON = 1 (allow low-power mode)
- Set SLEEP_KEEP_RES_ON_REG. VDD1_KEEPON = 1 (allow low-power mode)

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the sleep signal is used. By default, all resources go in SLEEP. In SLEEP state all resources maintain their output voltage but transient and load capability are reduced.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that a supply (VBAT) is connected (leaving the BACKUP or NO SUPPLY state) and the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

NT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 6 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds then the device interprets this as a power down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of die is reaching the limit. Software must take action to decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to prevent losing data. This interrupt is linked to VBAT but does not apply to a system where PMIC is connected to 5-V rails and not directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT is GPIO interrupt event that can be used to wake up the device from the SLEEP state. This can be an interrupt coming from any peripheral device or alike. This wake up event is not valid for a transition from the OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

Revision History

Changes from A Revision (June 2013) to B Revision	Page
• Updated VAUX2 to 300 mA	2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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