TPS659101 User's Guide for S5PV210 and S5PC110

This user guide describes how to integrate the TPS659101 power-management integrated circuit (PMIC) in a system with the S5PV210 and S5PC110 application processors. This user guide also describes the connectivity between the processor and the PMIC and also details the TPS659101 EEPROM bit configuration programmed to support power-up sequence requirements of the Samsung S5PV210 and S5PC110 processors.

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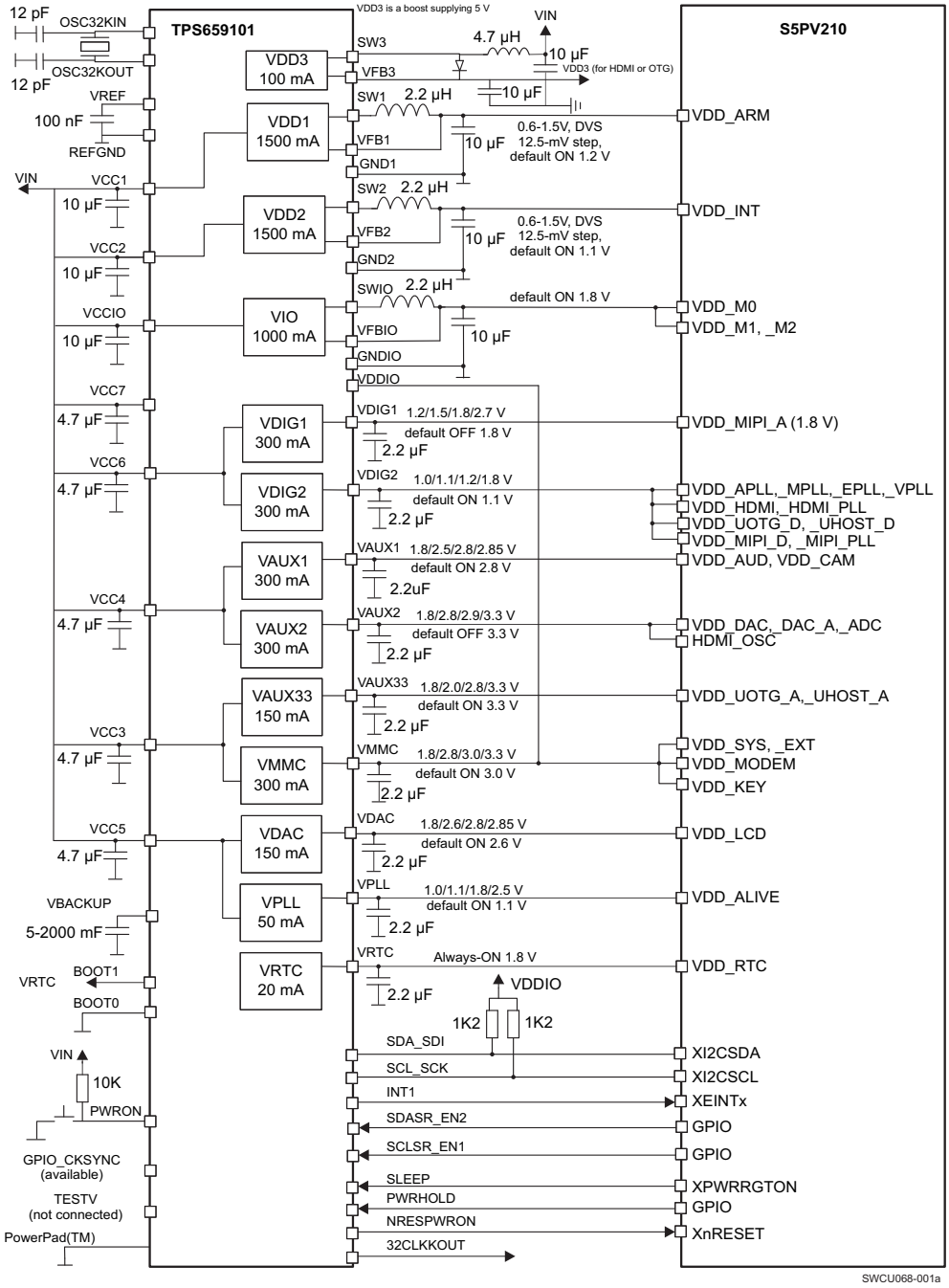
1 Introduction

This user guide describes how to integrate the TPS659101 PMIC in a system with the S5PV210 and S5PC110 application processors. This user guide also describes the connectivity between the processor and the PMIC and also details the TPS659101 EEPROM bit configuration programmed to support power-up sequence requirements of the Samsung S5PV210 and S5PC110 processors.

For details of the PMIC features and performance, see the full specification document, *TPS65910 Data Manual*.

2 Platform Connection Diagrams

Figure 1 shows the connections between the S5PV210/S5PC100 and the TPS659101.



(1) VIN can be connected to the battery (2.7–5.5 V) or to a preregulated supply (for example, 5 V in the netbook system).

(2) The voltage level of the TPS659101 I/O control signals (I2C, INT1, SLEEP, EN1/2, PWRHOLD, NRESPWRON) is defined by VDDIO input, which can be connected to 1.8–3.3 V.

(3) LDO connection for peripheral I/O is an example. Depending on system requirement, each peripheral I/O (CAM, LCD, AUD) can be connected to an LDO at the required level.

(4) For more details on SLEEP pin usage, see Section 4, Getting Started With TPS659101/Samsung Processor. The SLEEP input of the TPS659101 is an effective way to configure several DCDCs and LDOs to low-power mode or off with one signal to save power.

(5) SDASR_EN2 and SCLSR_EN1 can be used for dynamic control of VDD1 and VDD2 output voltage. For more details, see Section 4.1.4.

(6) When VDD3 boost is used, VAUX33 must be active and set to 2.8, 3, or 3.3-V level. Input for VDD3 is VCC7.

Figure 1. Block Diagram

3 Power-Up Sequence

Power-up sequence matching the S5PV210 and S5PC110 processors is programmed on the TPS659101 EEPROM. Figure 2 shows the power-up sequence.

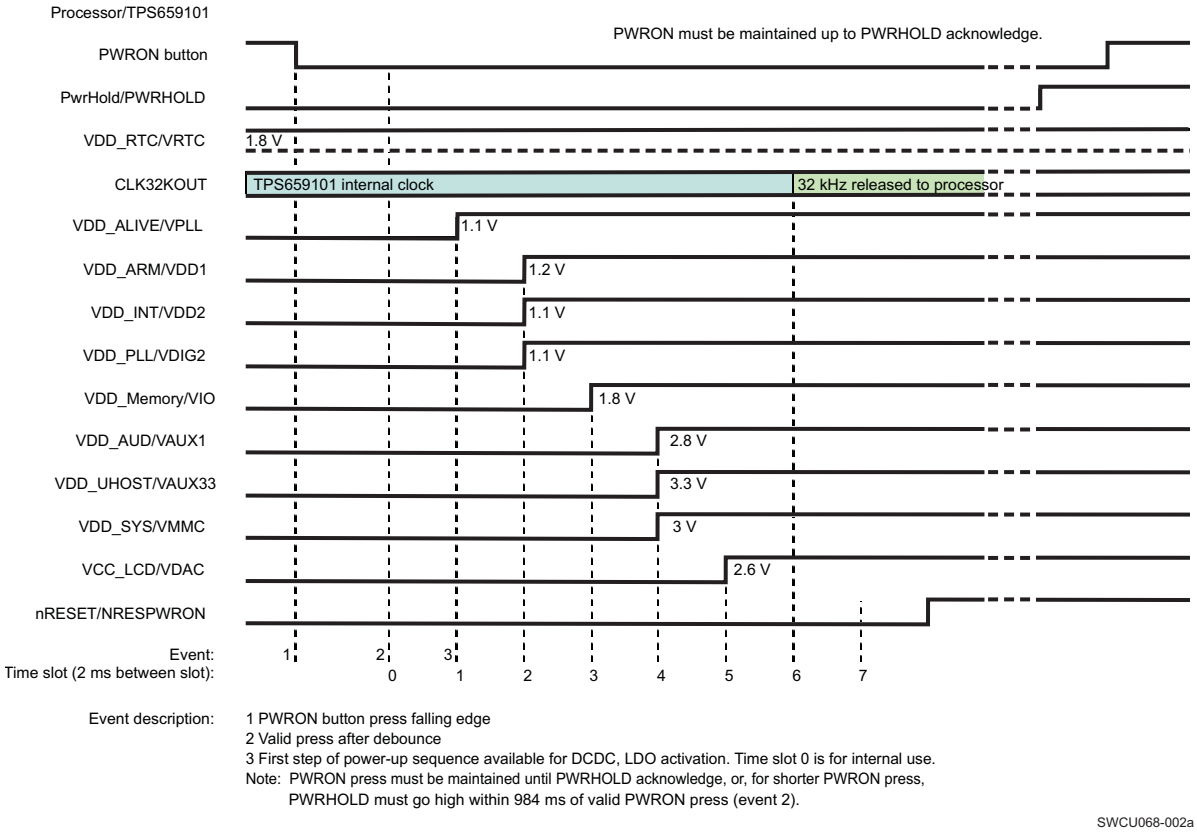


Figure 2. Power-Up Sequence Programmed on TPS659101 EEPROM

Table 1 shows the EEPROM configuration of the TPS659101, including power-up sequence and additional configurable bits.

Table 1. EEPROM Configuration of TPS659101

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	2
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.1 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	3
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VDIG2_REG	SEL	LDO voltage selection	1.1 V

Table 1. EEPROM Configuration of TPS659101 (continued)

Register	Bit	Description	Option Selected
EEPROM		LDO time slot	2
VDAC_REG	SEL	LDO voltage selection	2.6 V
EEPROM		LDO time slot	5
VPLL_REG	SEL	LDO voltage selection	1.1 V
EEPROM		LDO time slot	1
VAUX1_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	4
VMMC_REG	SEL	LDO voltage selection	3 V
EEPROM		LDO time slot	4
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	4
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	OFF
CLK32KOUT pin		CLK32KOUT time slot	6
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	Full-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	0
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up is reason required before switch on.	1 = Start-up reason required
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

4 Getting Started With TPS659101/Samsung Processor

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

In the DEVCTRL_REG register, set SR_CTL_I2C_SEL = 1 to use the SCLSR_EN1 and SDASR_EN2 pins for voltage scaling rather than the I^2C interface.

In the DEVCTRL_REG2 register, the SLEEPSIG_POL bit defines polarity for the SLEEP signal. to enable VDD1 and VDD2, use the default value (SLEEPSIG_POL = 0) when connected to XPWRRGTON of the processor.

In the DEVCTRL_REG register, set DEV_SLP = 1 to allow sleep transition when requested.

An update is not required in the DEVCTRL_REG2 register for the IT_POL bit; this is already programmed in the EEPROM.

GPIO0 is available for system use. If used, update the GPIO0 configuration (GPIO0_REG) and INT_MSK2_REG, based on the system requirements.

4.1.2 Define Wake Up/Interrupt Event (SLEEP or OFF)

In the INT_MSK_REG and INT_MSK2_REG registers, select which interrupts wake up the system. For the Samsung Netbook Platform, it is recommended to enable HotDie, PWRON_LP, and PWRON.

4.1.3 Backup Battery Configuration

If the system has backup battery, set BBCHEN = 1 in the BBCH_REG register to enable the backup battery charger. The maximum voltage to which backup battery is charged is set by the BBSEL[1:0] bits.

4.1.4 DCDC Maximum Current Capability

In the VDD1_REG and VDD2_REG registers, set ILMAX = 1 to increase the current limit from default 1 A to 1.5 A.

In the VIO_REG register, set the ILMAX bits based on the required current capablity, the default limit is 0.5 A.

4.1.5 DCDC Voltage Scaling

The DCDC output voltage can be controlled three ways.

- I^2C write to VDD1_OP_REG and VDD2_OP_REG to set the output voltage level with SEL[6:0] bits. The DCDCs can also be set to off (0 V).
- VDD1 and VDD2 can be enabled/disabled by using the SLEEP pin.
  By default, the SLEEP signal is active low.
  To disable VDD1 and VDD2 in sleep mode, in the SLEEP_SET_RES_OFF_REG register, set VDD1_SETOFF = 1 and VDD2_SETOFF = 1.

  These settings achieve the DCDC behavior described in Table 2:

Table 2. DCDC Behavior

SLEEP	VDD1	VDD2
0	Off	Off
1	On	On

By default, when returning to active mode, the DCDC output voltages return to the values set prior to the device entering sleep mode. To resume the values defined in the power-on sequence, set DEFAULT_VOLT = 1.

NOTE: To define how the SLEEP signal controls other LDOs and VIO (keep active/set off/set to low-power mode), see Section 4.1.6, *Sleep Configuration*.

- SCLSR_EN1 and SDASR_EN2 can be used for dynamic voltage control of the VDD1 and VDD2 DCDCs. EN1 and EN2 are mutually exclusive with the SLEEP signal; that is, if VDD1 and VDD2 are assigned to be controlled by EN1 and EN2, the SLEEP signal no longer controls these DCDCs.

  VDD1 is assigned to EN1 and VDD2 is assigned to EN2 with the following register settings:

  – In the EN1_SMPS_ASS_REG register, set VDD1_EN1 = 1.
  – In the EN2_SMPS_ASS_REG register, set VDD2_EN2 = 1.

  DCDC output voltage level switches between two levels based on ENx being low or high.

  DCDC output voltage levels are defined in the following registers:

  – In VDDx_OP_REG, the SEL[6:0] bits define roof voltage. Roof value is used when ENx ball = High.
  – In VDDx_SR_REG, the SEL[6:0] bits define floor voltage. Floor value is used when ENx ball = Low.

  During floor voltage operation (ENx input low), the operating mode of VDD1 and VDD2 is low-power PFM mode by default, which saves power but has limited transient capability.

  To maintain full transient performance:

  – In the SLEEP_KEEP_RES_ON_REG register, set VDD2_KEEPON = 1.
  – In the SLEEP_KEEP_RES_ON_REG register, set VDD1_KEEPON = 1.

4.1.6 Sleep Configuration

SLEEP input of TPS659101 is an effective way to configure several DCDCs and LDOs to low-power or off mode with one signal, minimizing system power consumption. By default, when the SLEEP signal is activated, all resources maintain their output voltage and load capability, but response to transients (load change) is reduced.

Resources that must keep full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set off in sleep to optimize power consumption must be indicated in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

For example, to keep VIO at full performance in sleep mode: In the SLEEP_KEEP_RES_ON_REG register, set VIO_KEEPON = 1.

For example, to set VAUX1 off in sleep mode: In the SLEEP_SET_LDO_OFF_REG register, set VAUX33_SETOFF = 1.

NOTE: No interrupt should be pending to allow transition to sleep mode.

Any DCDC or LDO assigned to EN1 or EN2 is not controlled by the SLEEP signal.

4.2 Event Management Through Interrupts

4.2.1 INT_STS_REG.VMBHI_IT

Indicates that supply has been inserted (leaving BACKUP or NO SUPPLY state), and the system must be initialized. (See Section 4.1, *First Initialization*.)

4.2.2 INT_STS_REG.PWRHOLD_IT

INT_STS_REG.PWRHOLD_IT indicates that an OFF-to-ACTIVE transition occurs through PWRON or any other allowed event. The processor gets the power supply back. Resets are released.

4.2.3 INT_STS_REG.PWRON_IT

NT_STS_REG.PWRON_IT indicates the PWRON button has been pressed. If the system was in the OFF or SLEEP state, it enters wakeup and resources are reinitialized.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. The user must decrease power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to prevent losing data. This interrupt is linked to VBAT but does not apply to a system where PMIC is connected to 5-V rails and not directly to VBAT.

4.2.6 INT_STS_REG.GPIO_X

INT_STS_REG.GPIO_X indicates that the GPIO event detection is linked to final platform use.

NOTE: An event is usable only for SLEEP wakeup and not OFF wakeup.

4.2.7 INT_STS_REG.RTC_XX

INT_STS_REG.RTC_XX is not commonly used in the Samsung processor.

Pin Mapping Between MX8698 and TPS659101

MX8698 Pin	TPS659101 Pin	Notes
BUCK1	VFB1	DCDC
IN1	VCC1	
LX1	SW1	
PGND1	GND1	
BUCK2	VFB2	DCDC
IN2	VCC2	
LX2	SW2	
PGND2	GND2	
BUCK3	VFBIO	DCDC
IN3	VCCIO	
LX3	SWIO	
PGND3	GNDIO	
LDO1	VRTC	
LDO2	VPLL	
LDO3	VDIG2	
LDO4	VDIG1	
LDO5	VAUX1	
LDO6	VDAC	
LDO7	VAUX2	
LDO8	VAUX33	
LDO9	VMMC	
IN4, IN6	VCC3, VCC4, VCC5, VCC6	LDO inputs. See Figure 1, *Block Diagram* in Section 2, *Platform Connection Diagrams*, for TPS659101.
IN5	VCC7	
VCC_COIN	VBACKUP	Backup battery
REFBP	VREF	Reference voltage
PWREN	SLEEP	
MR		Manual reset input not supported in TSP65910
SDA	SDA_SDI	
SCL	SCL_SCK	
PWRON	PWRON	See Figure 1,*Block Diagram* in Section 2, *Platform Connection Diagrams*, for TPS659101 connection
PWRHOLD	PWRHOLD	
SET1 (SET2)	SCLSR_EN1	TPS659101 can support two values; see Section 4.1.5, *DCDC Voltage Scaling*. Using EN1 is alternative for SLEEP pin.
SET3	SDASR_EN2	Using EN2 is alternative for SLEEP pin. See Section 4.1.5, *DCDC Voltage Scaling*.
JIGON		Not supported in TPS659101
SRAD		TPS659101 has single I^2C address, no selection pin
LBO		Low-Battery Detection in TPS659101 is through interrupt INT1 (VMBDCH_IT).

MX8698 Pin	TPS659101 Pin	Notes
ONO		PWRON signal indicated through INT1 in TPS659101
RSO	NRESPWRON	
AGND1, AGND2	PowerPad	TPS659101 analog ground pins connected to PowerPad

Revision History

Changes from A Revision (December 2010) to B Revision	Page
• Updated VAUX2 to 300 mA	2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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