Using the TPS65910 EVM, A Multichannel Power-management IC, 3 Buck, 1 Boost, and 8 LDOs

User's Guide

Literature Number: SWCU065F
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Introduction

1 Description

Device Description:

The TPS65910 device is an integrated power-management IC available in 48-QFN package and is dedicated to applications powered by one Li-Ion or Li-Ion polymer battery cell, 3-series Ni-MH cells, or a 5 V input, and which requires multiple power rails. The device provides three step-down converters, one step-up converter, and eight low dropout voltage regulators (LDOs) and is designed to support the specific power requirements of OMAP™ processors.

Two of the step-down converters provide power for dual processor cores and are controllable by a dedicated class-3 SmartReflex™ interface for optimum power savings. The third converter provides power for the I/Os and memory in the system. The device includes eight general-purpose LDOs providing a wide range of voltages and current capabilities. These LDOs can be controlled by the inter-integrated circuit (I^2C™) interface.

In addition to the power resources, the device contains an embedded power controller (EPC) to manage the power sequencing requirements of OMAP processor and a real-time clock (RTC).

EVM Kit Description:

The TPS65910 evaluation module (EVM) is a stand-alone module that demonstrates the functions of the integrated power management IC. It uses a USB-to-GPIO interface card (not included in the kit) to control the standard I^2C interfaces in the TPS65910 device. It includes Windows™-compatible software to interface with the device. The sofware is a simple graphical user interface (GUI) that simplifies registers access for the IC (software CD is not included in the kit, must be downloaded from product folder on ti.com).

EPROM Power-Up Sequence Description:

This user guide is common for all TPS65910x parts. The only difference in these parts is the EEPROM sequence for power-up. Each part has a unique EEPROM sequence to satisfy the attached application processor. For details of the EEPROM sequence please refer to the corresponding user guide in the “Application Notes” section on the TPS65910x folder page.

1.1 Applications

- Embedded application processor power
- Handheld/portable systems

1.2 Features

- An EPC
- Two efficient step-down DCDC converters for processor cores
- One efficient step-down DCDC converter for I/O power
- One efficient step-up 5-V DCDC converter
- SmartReflex-compliant dynamic voltage management for processor cores
- Eight LDO voltage regulators and one RTC LDO (internal purpose)
- One high-speed I^2C interface for general-purpose control command
- One high-speed I^2C interface for SmartReflex (SR) class-3 control command
- Two enable signals multiplexed with SR-I2C, configurable to control any supply state and processor cores supply voltage
- Thermal shutdown protection and hot-die detection
- An RTC resource with:
  - Oscillator for 32.768-kHz crystal or 32-kHz built-in RC oscillator
  - Complete calendar capability
  - Alarm capability
- One configurable general-purpose input/output (GPIO)
- DCDCs switching synchronization through internal or external 3-MHz clock
- Backup battery charger

2 TPS65910 EVM Power Capabilities

Table 1. TPS65910 EVM Resources Summary

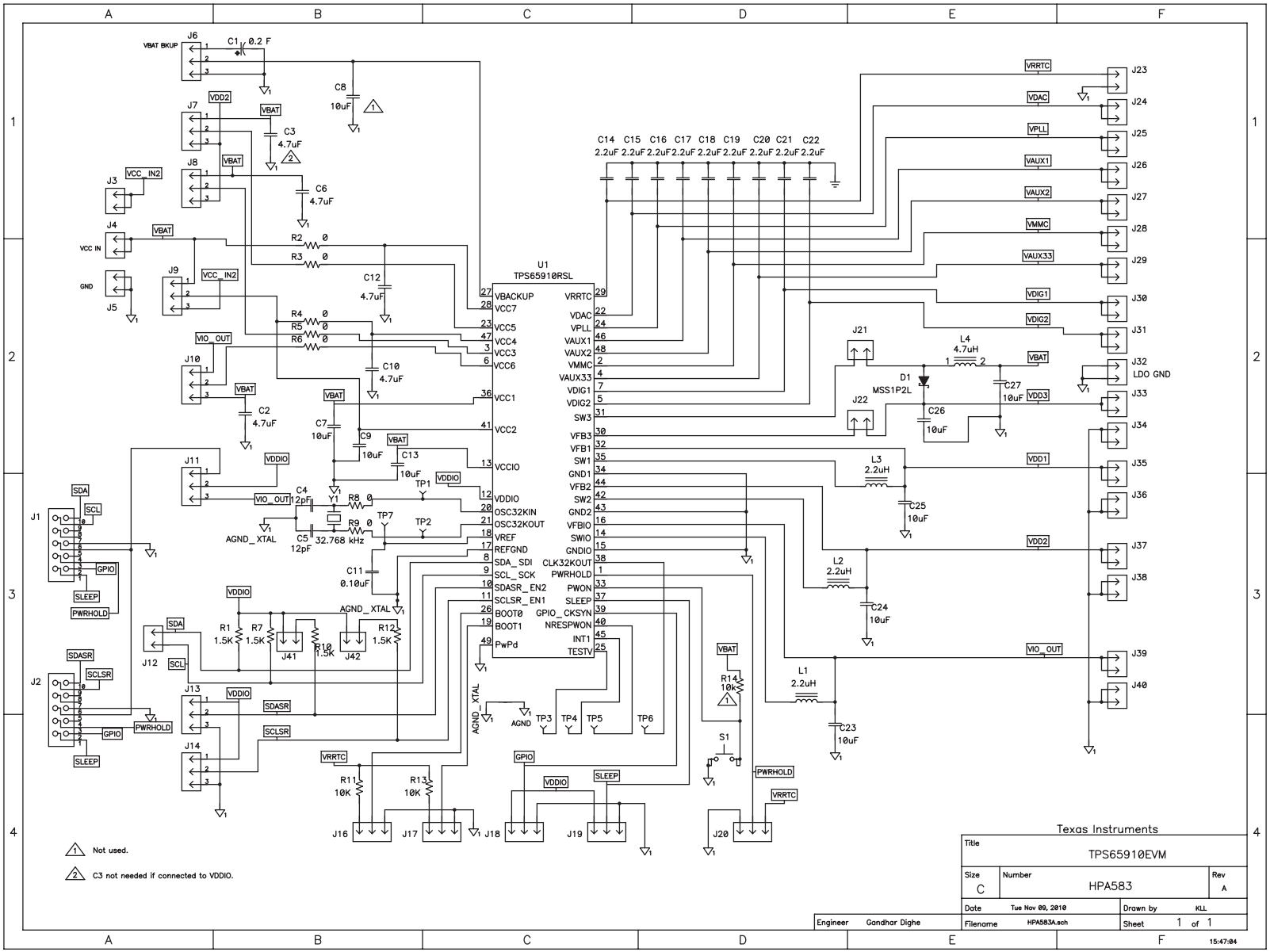
POWER RESOURCE	TYPE	VOLTAGE RANGE (V)	I_{max} (mA)
VIO	SMPS (buck)	1.5, 1.8, 2.5, 3.3	1000
VDD1	SMPS (buck)	0.6, 1.1, 1.5, 2.2, 3.2	1500
VDD2	SMPS (buck)	0.6, 1.1, 1.5, 2.2, 3.2	1500
VDD3	SMPS (boost)	5	100
VDIG1	LDO	1.2, 1.5, 1.8, 2.7	300
VDIG2	LDO	1.0, 1.1, 1.2, 1.8	300
VAUX33	LDO	1.8, 2.0, 2.8, 3.3	150
VMMC	LDO	1.8, 2.8, 3.0, 3.3	300
VAUX1	LDO	1.8, 2.5, 2.8, 2.85	300
VAUX2	LDO	1.8, 2.8, 2.9, 3.3	150
VDAC	LDO	1.8, 2.6, 2.8, 2.85	150
VPLL	LDO	1.0, 1.1, 1.8, 2.5	50

For detailed electrical characteristics of SMPS and LDO supplies, refer to the product data sheet.

3 Schematic

Figure 1 shows the TPS65910 EVM schematic.

Figure 1. TPS65910 EVM Schematic



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4 Connector and Test Point Descriptions

4.1 Connector Descriptions

4.1.1 Boot Pins

J16 and J17 are used to select the boot pin configuration for proper booting of the device. Table 2 shows the possible boot options.

Table 2. Boot Configuration

BOOT 0	BOOT 1	POWER UP OPTION
0	0	AM35xx
0	1	EEPROM boot mode
1	0	OMAP3x
1	1	Test mode only

4.1.2 Backup Battery

J6 is used for the backup battery connection. The user can connect a backup battery between J6-2 and J6-3 or alternatively can use the onboard 0.2 F, 3.3 V capacitor by shorting J6-1 and J6-2.

4.1.3 VBAT

VBAT (J4) is the main input source to the device. Table 3 lists the minimum and maximum levels that can be applied to these pins. Use J5 for ground.

Table 3. VBAT Minimum and Maximum Levels

VBAT	MIN (V)	TYP (V)	MAX (V)
	2.7	3.6	5.5

Ensure that the jumper settings for the jumpers listed in Table 4 are correct so the device is supplied by VBAT.

Table 4. VBAT Input Jumper Settings

JUMPER CONNECTION	DEVICE INPUT PIN	USE
J7 (1-2)	VCC5	Selects VBAT as power source
J8 (1-2)	VCC3	Selects VBAT as power source
J9 (1-2)	VCC2, VCC4	Selects VBAT as power source
J10 (2-3)	VCC6	Selects VBAT as power source

4.1.4 Default Jumper Settings for the Boost Converter

Table 5. Boost Converter Jumper Settings

JUMPER ID	LABEL	USE
J21	SW3	Short jumper to use boost converter
J22	VFB3	Short jumper to use boost converter

For correct functioning of VDD3, first VAUX33 must be enabled at 3.3V and then VDD3 should be enabled using the appropriate register settings.

4.1.5 I²C connector

TPS65910 has two slave I²C interfaces: one is a general-purpose interface to control the internal configuration registers, the second is dedicated to SmartReflex applications such as dynamic voltage frequency scaling (DVFS) or adaptive voltage scaling (AVS).

These interfaces support the standard slave mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps).

Table 6. I²C Connector

CONNECTOR NUMBER	PIN	DESCRIPTION
J1	9, 10	General purpose I²C interface for register configuration
J2	9,10	Dedicated I²C interface for SmartReflex

J1 and J2 also have GPIO, SLEEP, and PWRHOLD signals that can be controlled from the GUI and USB-to-GPIO interface.

The SmartReflex can be programmed as enable signals of one or several supplies when the device is on. A resource assigned to either SmartReflex signal (SDASR_EN2 or SCLSR_EN1) automatically disables the serial control interface.

Connectors J1 and J2 are used for the USB adapter. Table 7 lists the signal mapping to control the signals on the EVM. The GPIO field on the GUI can be toggled to drive the following signals on the EVM.

Table 7. GPIO Mapping For GUI

PIN NUMBER FOR J1 and J2	GPIO ON GUI	TPS65910x SINGAL
Pin 1	GPIO7	SLEEP
Pin 2	GPIO6	GPIO
Pin 3	GPIO5	PWRHOLD

4.1.6 3.3-V I/O for VDDIO

The USB-to-GPIO interface is on connectors J1 and J2. The USB-to-GPIO module generates 3.3 V, which is used as the I/O for the EVM. The following jumper configuration must be done for the I/O supply.

Table 8. Jumper for I/O Input Setting

JUMPER CONNECTION	DEVICE INPUT PIN	USE
J11 (1-2)	VDDIO	Connects J1-5 (or J2-5) to VDDIO for 3.3-V I/O input

4.1.7 Control Jumper Settings

TPS65910 has some control signals that can be configured using the on-board jumpers or by using the USB-to-GPIO connector.

Table 9. Control Signals

Jumper connection	Signal Name	Use
J18	GPIO	Jumper the three pin connector as required
J19	SLEEP	Jumper the three pin connector as required

Table 9. Control Signals (continued)

J20	PWRHOLD	If PWRHOLD is low then the device will not power-up. So, connect this to HI side of the jumper. See important description below.
J13	SDASR_EN2	Both these signals can be used to control the LDO and SMPS power supplies. Please refer details on programming the internal register to achieve this function.
J14	SCLSR_EN1	

If USB-to-GPIO connector is connected on J1 or J2 then the above signals can be controlled using the GPIO writes from the GUI. In this case the above jumpers should not be connected. Jumpers should be left open. In case of SLEEP and GPIO signals there will be contention for VDDIO supply. In case of PWRHOLD, the device will be damaged. This is because the PWRHOLD signal from USB-to-GPIO is at 3.3V. The HI side of J20 jumper is connected to VRRTC. If VRRTC is shorted to 3.3V then this will damage the device. When the adapter is connected all IOs should be at 3.3V, so ensure J11 is connected between VDDIO and 3.3V.

4.2 Test Point Descriptions

Table 10. Test Point Descriptions

Power Domain/Control	TP	Label	Use
VIO	J39	VIO_OUT	Monitor VIO output voltage
VDD1	J35	VDD1	Monitor VDD1 output voltage
VDD2	J37	VDD2	Monitor VDD2 output voltage
VDD3	J33	VDD3	Monitor VDD3 output voltage
VPLL	J25	VPLL	Monitor VPLL output voltage
VDAC	J24	VDAC	Monitor VDAC output voltage
VAUX1	J26	VAUX1	Monitor VAUX1 output voltage
VAUX2	J27	VAUX2	Monitor VAUX2 output voltage
VMMC	J28	VMMC	Monitor VMMC output voltage
VAUX33	J29	VAUX33	Monitor VAUX33 output voltage
VDIG1	J30	VDIG1	Monitor VDIG1 output voltage
VDIG2	J31	VDIG2	Monitor VDIG2 output voltage
VREF	J15	VREF	Monitor VREF output voltage
VRRTC	J23	VRRTC	Monitor VRRTC output voltage
PWRHOLD	J20-2	PWRHOLD	Monitor PWRHOLD level
PWON	S1	POWER ON	Power-on switch
SLEEP	J19-2	SLEEP	Control device status
GPIO/CKSYN	J18-2	GPIO/CKSYNC	GPIO test point
NRESPWRON	TP5	NRESPWON	Reset to processor
INT1	TP4	INT1	Interrupt to processor
CLK32KOUT	TP6	CLK32KOUT	32KHz to processor

Use J32 for all GND connections for measuring the LDO power supplies. J34, J36, J38, and J40 can be used for ground connections for measuring DCDC power supplies.

5 Test Set Up

5.1 Equipment

Recommended test equipments:

- Variable 6-V power supply capable of supplying 6 A current

- Voltmeter
- Oscilloscope
- Windows PC with a universal serial bus (USB) port
- USB-to-GPIO converter

6 GUI Information

The GUI accompanying this device is fairly simple. It runs on a Windows PC. Ensure that your machine supports Microsoft .NET Framework 3.5.

6.1 Installation Instructions:

To install the GUI follow these steps:

1. Download from site/Insert CD (based on how we package the GUI).
2. Create a new folder or unzip into any appropriate windows folder. If it is an exe, then select the location. The default is C:/xyz/.

6.2 Know the Files

GUI software consists of the following files:

- DLL
- EXE
- XML

The GUI can be opened by clicking the MS Installer, TPS65910.msi file. The .xml file is the main file that contains all the device registers. The registers in this file are categorized in blocks according to the functions. The .xml file also specifies the slave I^2C address for the device.

6.3 GUI Description

GUI windows are divided into the following sections:

6.3.1 Register Properties

The following blocks are on the GUI on the left-side pane under Register Properties:

- Time and Calendar Registers
- RTC Registers
- Back-up Registers
- DCDC Control Registers
- LDO Control Registers
- Device Control Registers
- Interrupts and GPIO Registers

Figure 2 shows a sample snapshot of the GUI.

Each block can be selected independently so that it appears on the main GUI window. Each register instance appears in a separate block. See Figure 3.

The user can write to the registers through the I^2C bus. Each bit in the 8-bit register can be written independently or the complete register can be written using an 8-bit hexadecimal value in the Value field. Individual bits can be toggled either by selecting the drop-down menu or by double-clicking the field.

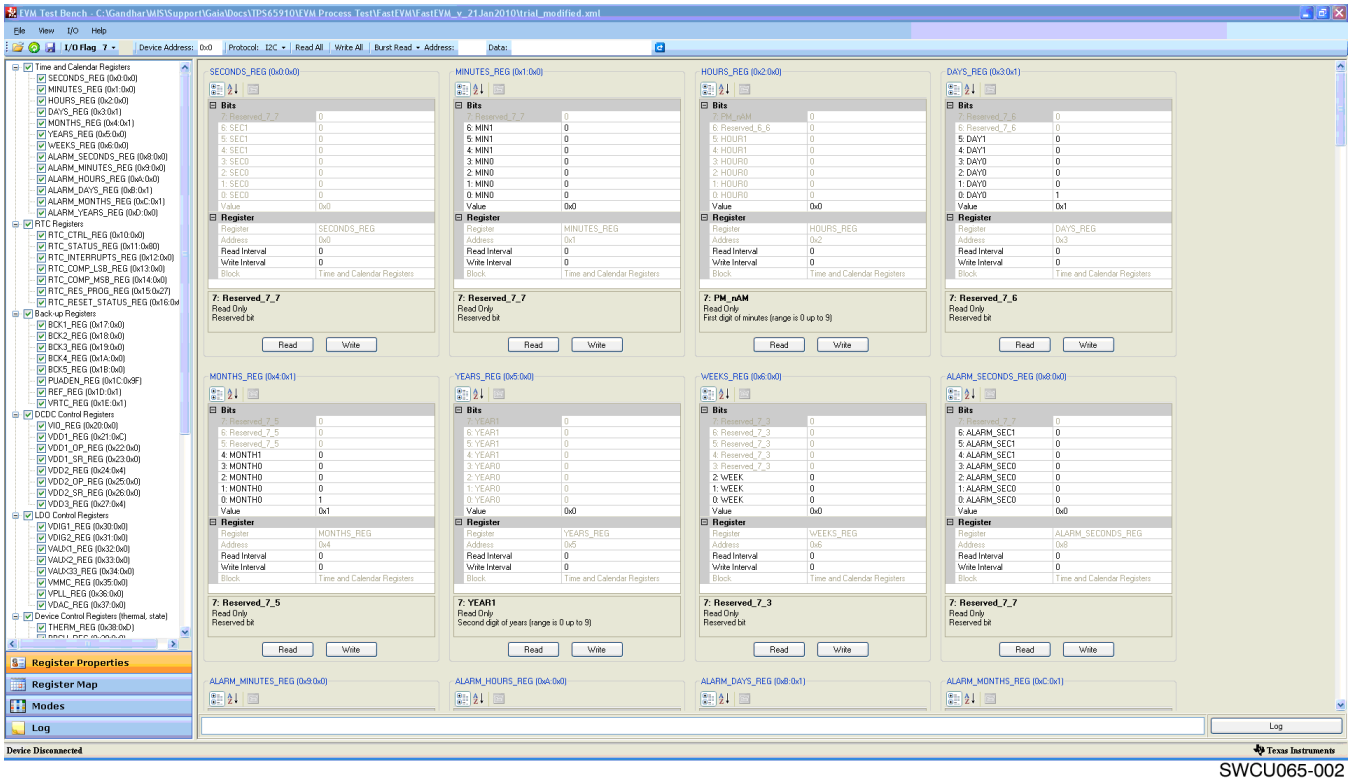

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Figure 2. GUI Snapshot – Register Properties

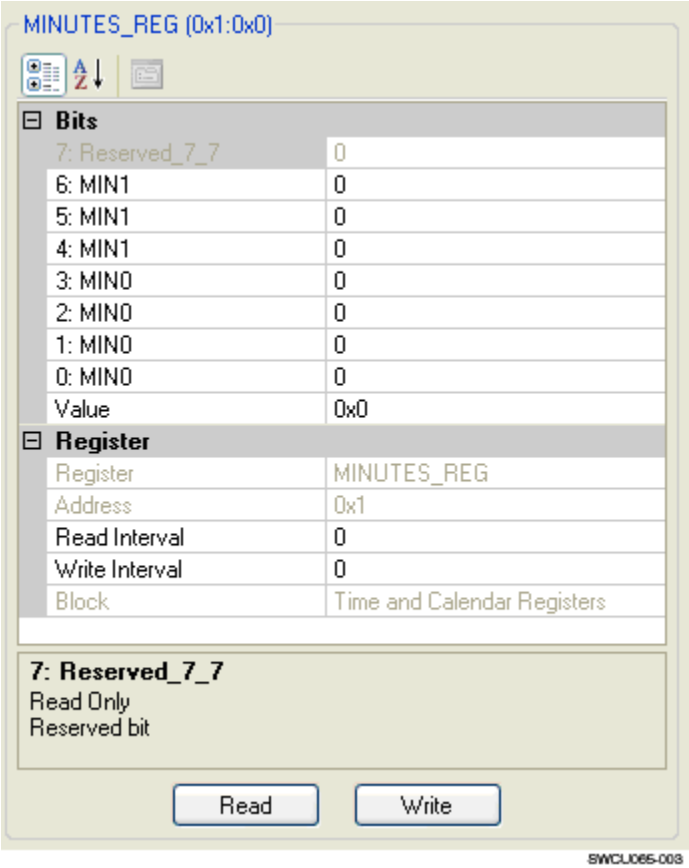

Figure 3. Single Register Instance

6.3.2 Register Map

Figure 4 shows the register map view. The Register Map tab provides an alternative way to access the device registers. Also in this view, the bits and complete words can be read or written through the I^2C bus.

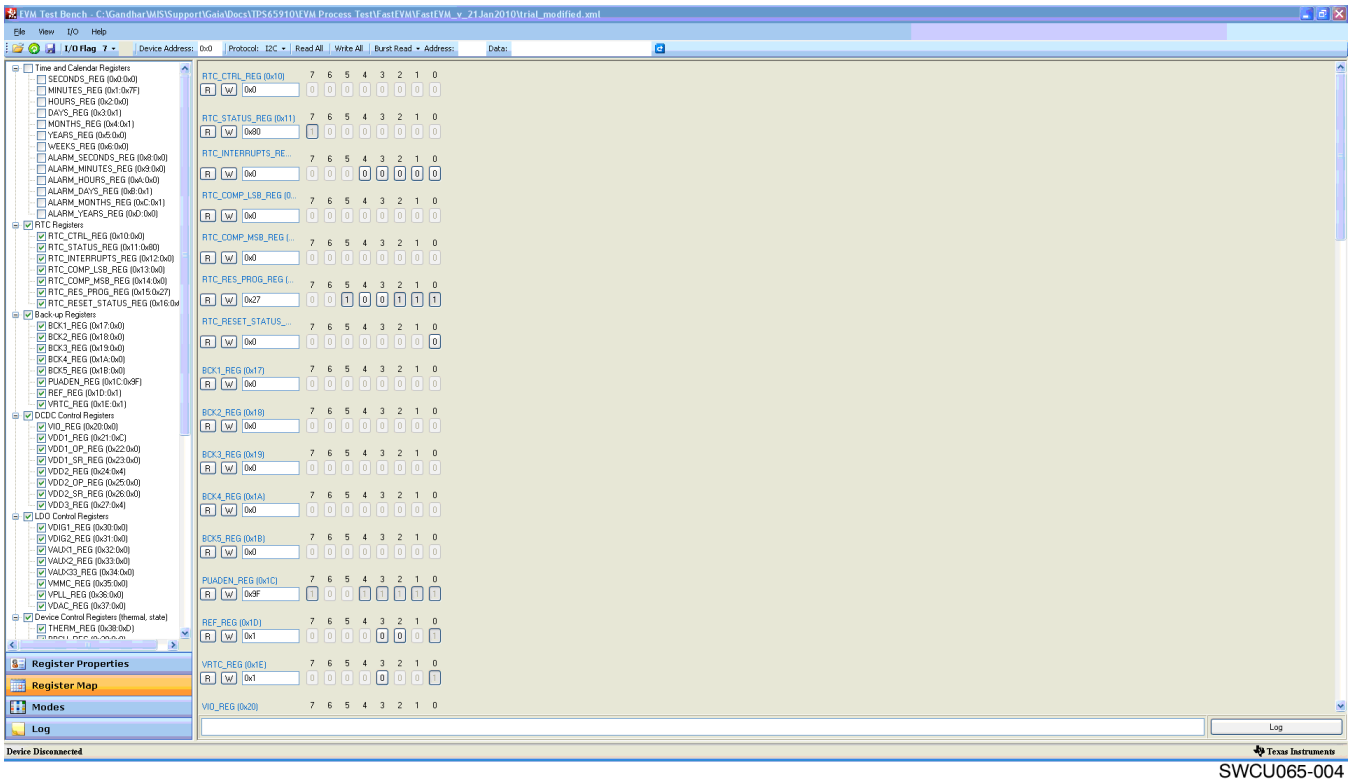

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Figure 4. Register Map View

6.3.3 Modes

This section is used for executing multiple register writes in a single step. For example, to configure the device in SLEEP state, multiple bits must be configured for SMPS and LDO supplies. An example is provided in the .xml file that comes with the GUI package.

Users can create their own sequences in the .xml file.

6.3.4 I/O writes

Three control signals for the TPS65910 (SLEEP, PWRHOLD and GPIO) can be altered using the GUI. To select these signals, the user can use the I/O Flag tab on the menu bar. For mapping of the I/O lines, refer to the TPS65910 schematic and datasheet for the GPIO-to-USB adapter at http://focus.ti.com/docs/toolsw/folders/print/usb-to-gpio.html.

7 EVM Assembly Drawings and Layout

The following figures show the design of the TPS65910 EVM printed circuit board. The EVM has been designed using a 4-layer, 2-ounce, 4-inch × 4-inch copper-clad circuit board with all components on the top side and all active traces to the top to let the user easily view, probe, and evaluate the TPS65910 IC.

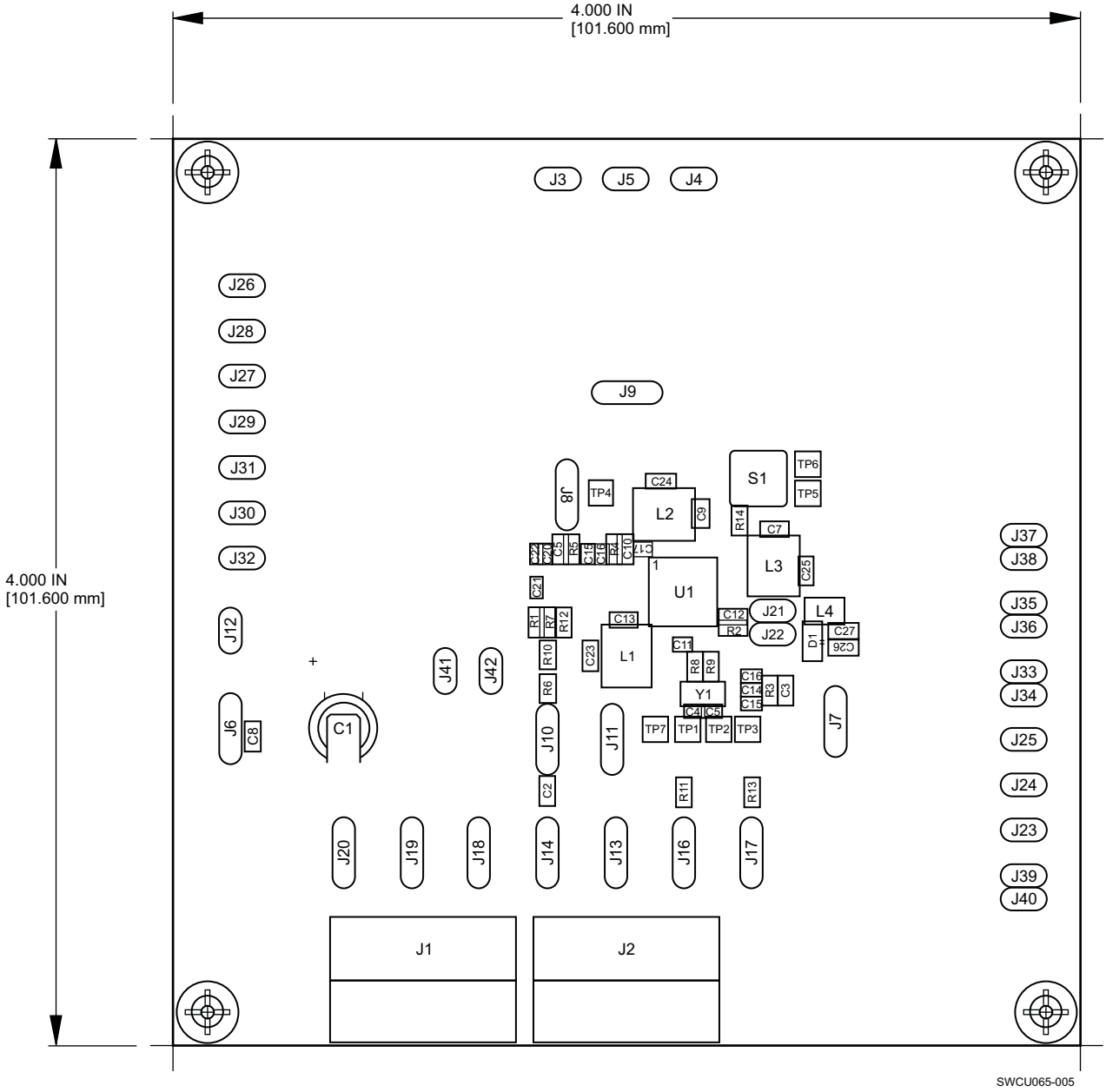

Figure 5. TPS65910 EVM Component Placement With Silkscreen Labels

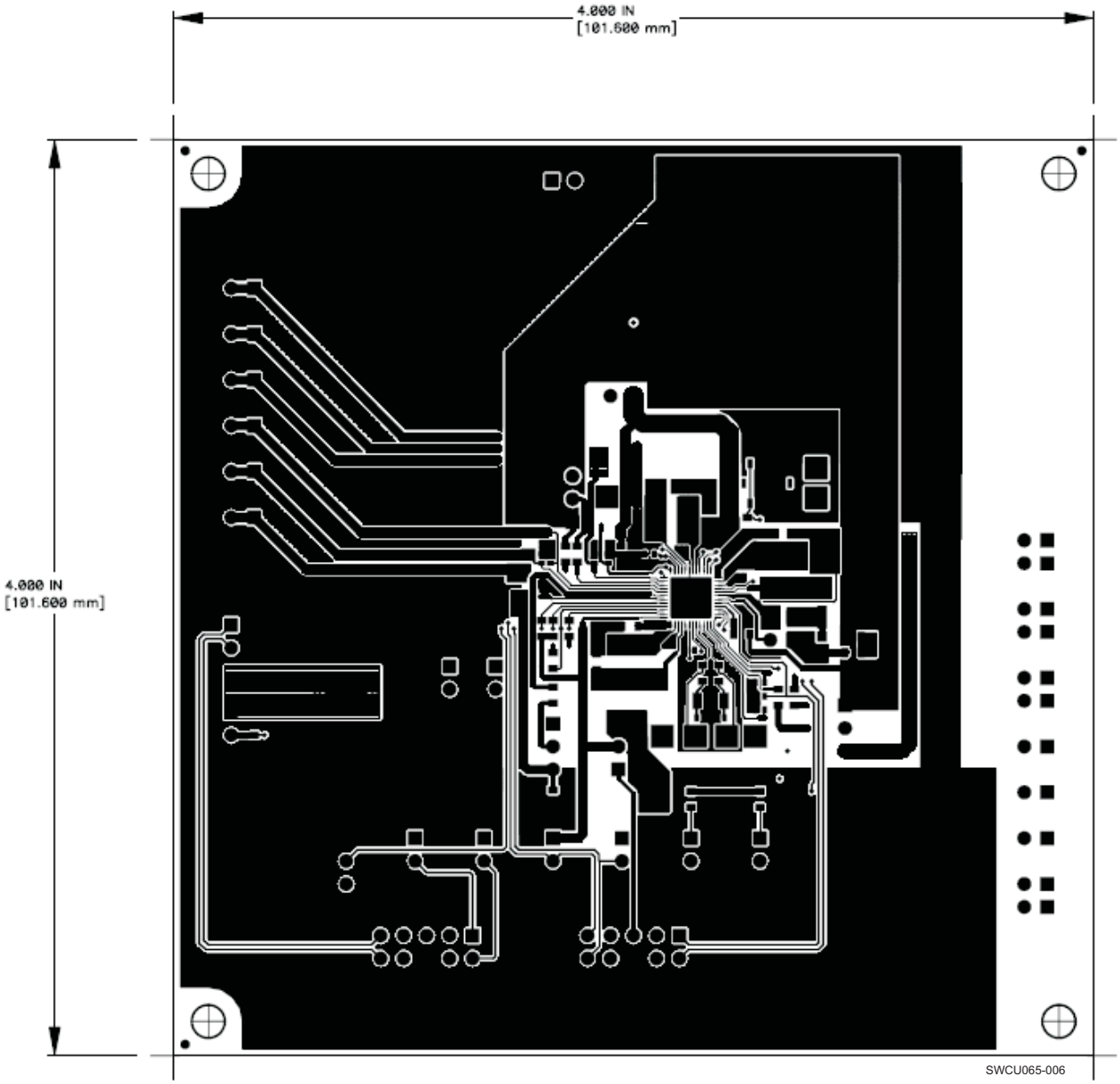

Figure 6. TPS65910 EVM Top Layer (L1)

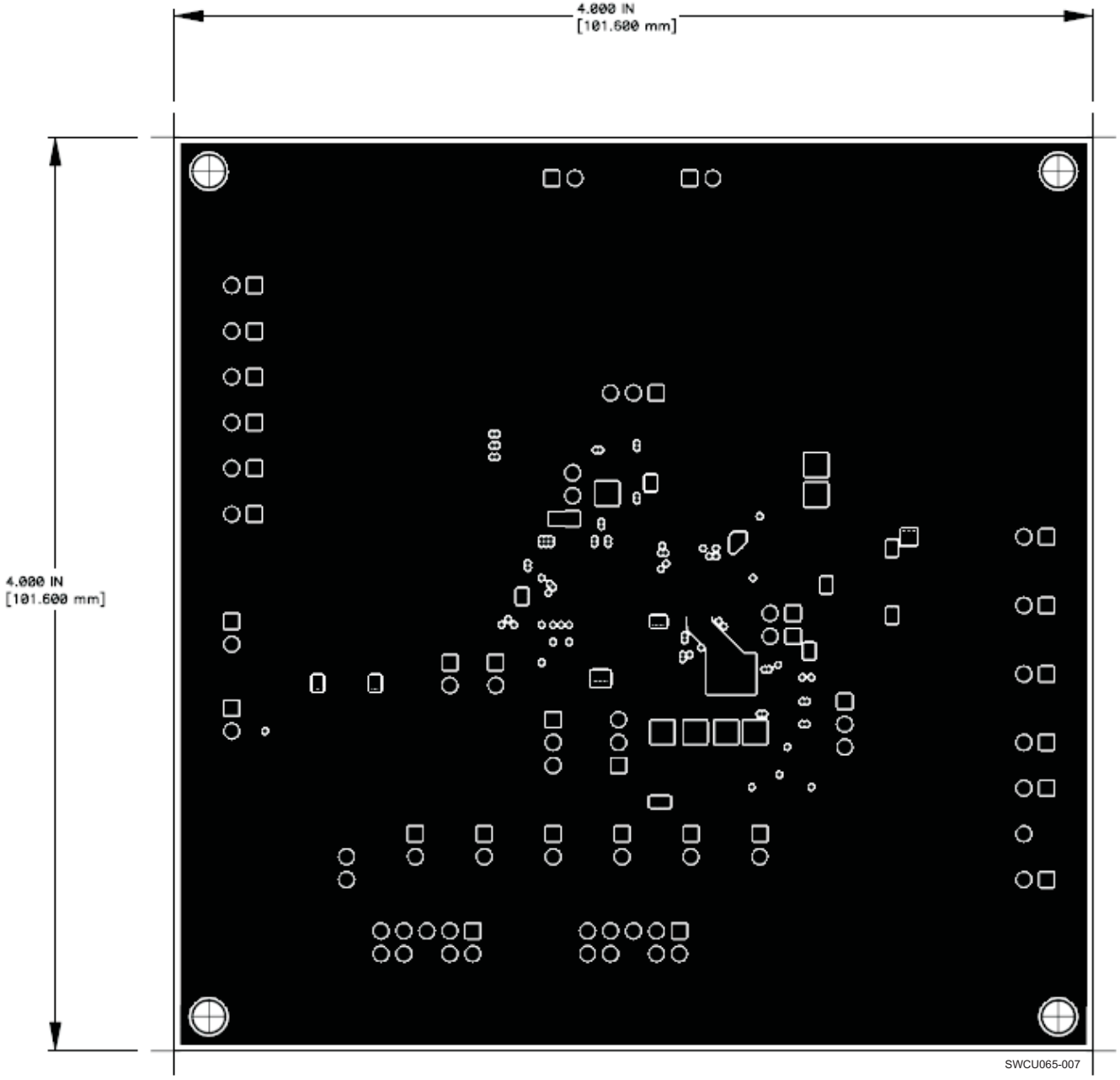

Figure 7. TPS65910 EVM Internal Layer (L2)

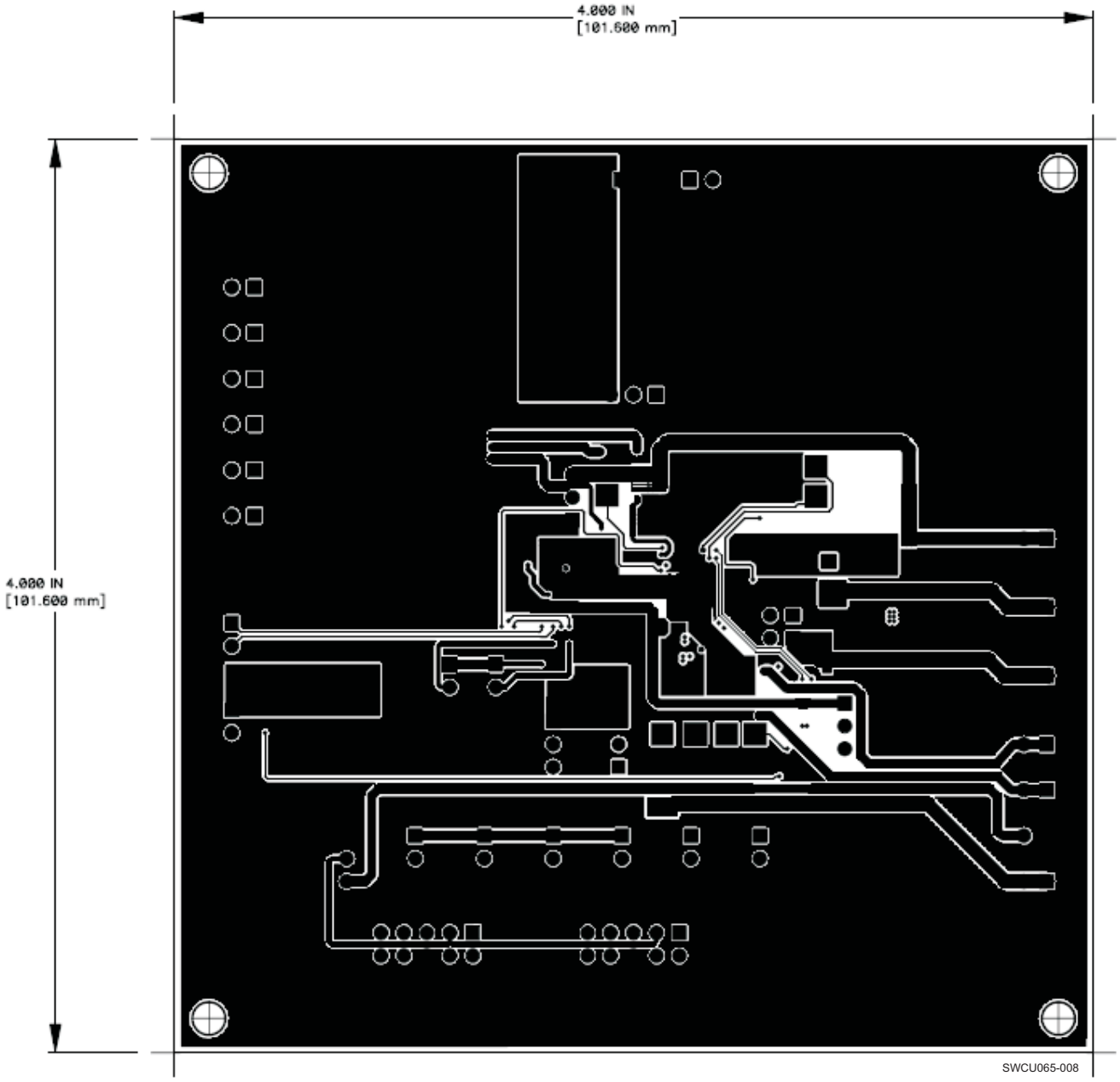

Figure 8. TPS65910 EVM Internal Layer (L3)

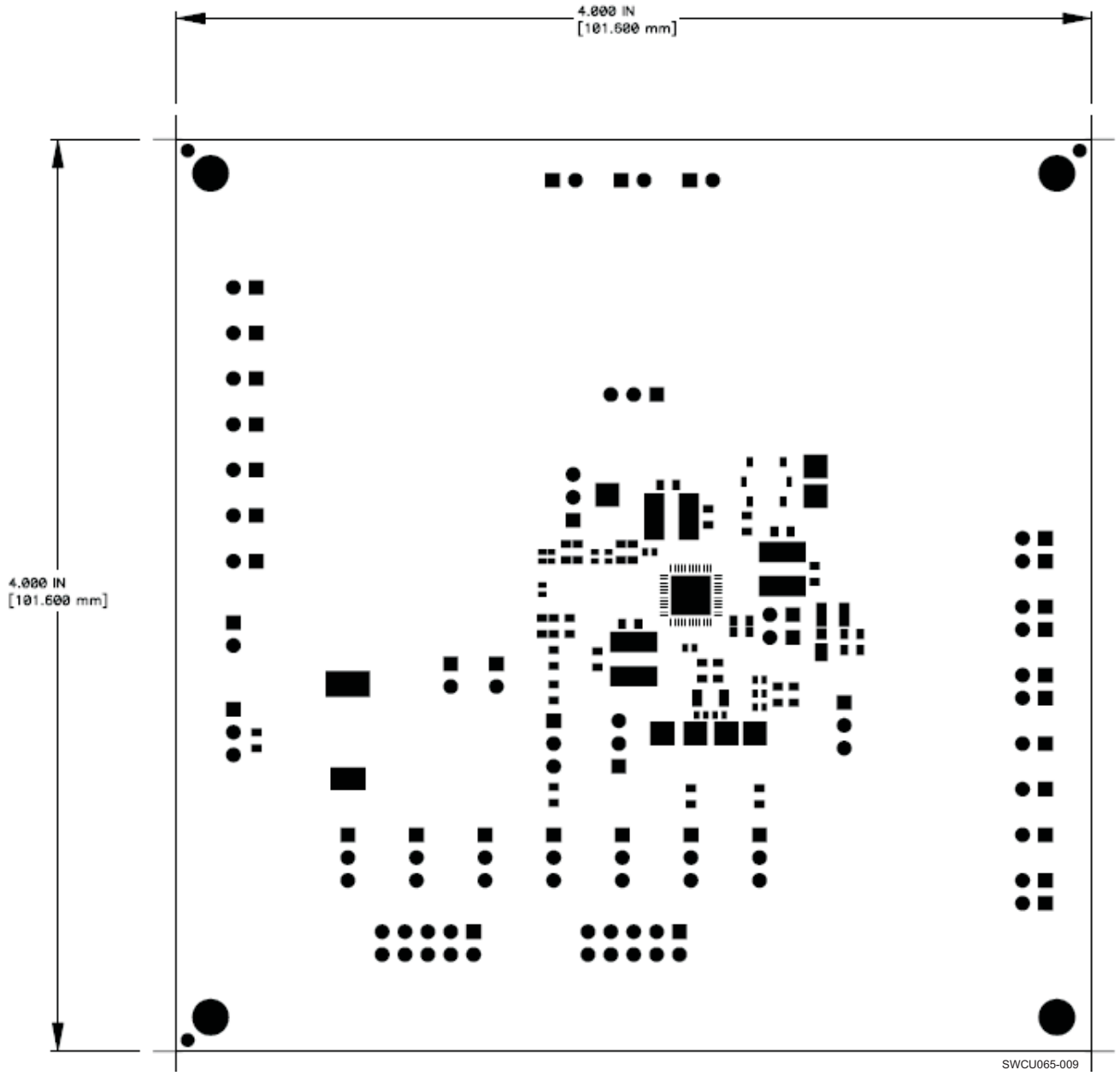

Figure 9. TPS65910 EVM Bottom Copper (L4)

8 List of Materials

Table 11 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 11. TPS65910 EVM Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	0.2 F	Capacitor, Electric Double Layer	AK	EECEN0F204AK	Panasonic
1	C11	0.10 µF	Capacitor, Ceramic, 10 V, X5R, 10%	0402	STD	{MFR}
9	C14, C15, C16, C17, C18, C19, C20, C21, C22	2.2 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0402	JMK105BJ225MV-F	Taiyo Yuden
5	C2, C3, C6, C10, C12	4.7 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0603	JMK107BJ475KA-T	Taiyo Yuden
2	C4, C5	12 pF	Capacitor, Ceramic, vvV, [temp], [tol]	0402	{Part Number}	{MFR}
9	C7, C8, C9, C13, C23, C24, C25, C26, C27	10 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0603	C0603C106M9PAC	Kemet
1	D1	MSS1P2L	Diode, Schottky, 20 V, 1 A	MicroSMP	MSS1P2L	Vishay
2	J1, J2	2510-5002UB	Connector, Male Right Angle 2x5 pin, 100 mil spacing, 4 Wall	0.100 inch x 2X5	2510-5002UB	3M
26	J3, J4, J5, J12, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42	PEC02SAAN	Header, Male 2-pin, 100 mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
13	J6, J7, J8, J9, J10, J11, J13, J14, J16, J17, J18, J19, J20	PEC03SAAN	Header, Male 3-pin, 100 mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
3	L1, L2, L3	2.2 µH	Inductor, SMT, 2.6 A, 58 mΩ	0.157 x 0.157 inch	VLCF5020T-2R2N2R6-3	TDK
1	L4	4.7 µH	Inductor, SMT Multi-layer, 1 A, 110 mΩ	2520 mm	MIPF2520D4R7S	FDK
					Alternate part:	
					LQM2HPN4R7MG0L	Murata
4	R1, R7, R10, R12	1.5 kΩ	Resistor, Chip, 1/16 W, 5%	0603	STD	STD
2	R11, R13	10 kΩ	Resistor, Chip, 1/16 W, 5%	0603	STD	STD
	R14	10 kΩ	Resistor, Chip, 1/16 W, 5%	0603	STD	STD
7	R2, R3, R4, R5, R6, R8, R9	0	Resistor, Chip, 1/16 W, 5%	0603	STD	STD
1	S1	EVQ-PLHA15	Switch, 1P1T, 50 mA, 12 V, 160 g	0.200 x 0.200 inch	EVQ-PLHA15	Panasonic
1	SH1		Short jumper			

Table 11. TPS65910 EVM Bill of Materials (continued)

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
7	TP1, TP2, TP3, TP4, TP5, TP6, TP7	PEC01SAAN	Through Hole, 0.040 Diameter		PEC01SAAN	Sullins
1	U1	TPS65910RSL	IC, Integrated Power Management	QFN	TPS65910RSL	TI
1	Y1	32.768 kHz	Crystal	1.50 x 3.20 mm	FC-135	Epson Toyocom

NOTE: These assemblies are ESD sensitive, ESD precautions must be observed.

These assemblies must be clean and free from flux and all contaminants. Use of contaminated flux is not acceptable.

These assemblies must comply with workmanship standards IPC-A-610 Class 2.

Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent manufacturer's components.

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