Technical White Paper

Reduce System Noise Using Parallel LDOs

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ABSTRACT

Low-dropout regulators (LDO) are required in many applications because, compared to switching converters, these regulators are inherently low noise and offer a simple solution with lower costs. Applications exist where even the lowest noise LDO cannot meet the desired noise specification, such as high-performance RF circuitry, laser current drivers, and so forth. Placing LDOs in parallel can potentially lower the noise even further when the correct parallel LDO architecture is chosen. This document provides a comprehensive analysis on the noise reduction of recent parallel LDOs using ballast resistors. The ballast resistor technique is compared against two other parallel LDO techniques, (1) using op-amps and an additional feedback loop to parallel the LDOs, and (2) using current mirrors formed from matched BJTs to parallel the LDOs.

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Trademarks

1 Introduction to Parallel LDOs Using Ballast Resistors

Parallel LDOs have become popular in recent years, with numerous LDOs in Texas Instruments' portfolio being paralleled in real world designs across many applications. Texas Instruments modernizes the design and analysis of parallel LDOs by using ballast resistors (see [1] and [2] in the References section). TI also developed a downloadable software tool to design the ballast resistor (R_B) for TI's LDOs against a set of user-defined system requirements (see [3] in the References section). Parallel LDOs offer numerous advantages over single LDOs, such as:

1. Increased load current
2. Improved PSRR for a given load current
3. Improved thermal spreading
4. Reduced headroom requirements (dropout)
5. Reduced volume over other converters: C_{OUT} typically drives the maximum system height
6. Reduced noise

For a comprehensive discussion on these advantages, see [1-3] in the References section. To date, no comprehensive white paper exists comparing and contrasting noise performance of the three common parallel LDO techniques. This white paper is intended to fill this gap and show the noise performance advantage of parallel LDOs using ballast resistors over the competing parallel LDO techniques.

2 Noise Analysis of Parallel LDOs Using Ballast Resistors

As described in reference [1], parallel LDOs using ballast resistors can be redrawn as shown in the schematic in Figure 2-1, and the V_{LOAD} formula is provided in equation 1.

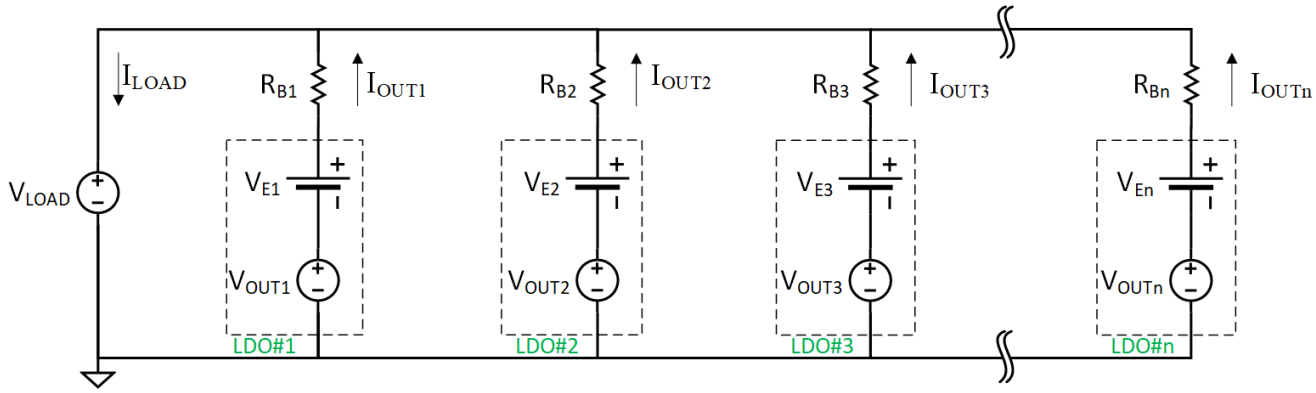

Figure 2-1. Equivalent Model for n Parallel LDOs Using Ballast Resistors

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{Bn}}} \quad (1)$$

Assume a parallel network in which no LDO regulates another LDO, and each feedback loop of the regulator operates independently of the others. Let Z_{OUTn} denote the output impedance of the n^{th} LDO in the parallel array. Since the noise analysis is performed under steady-state conditions, the load current I_{LOAD} contains no AC component; consequently, the load current is constant (for example, the frequency content is zero). Equation 1 can therefore be simplified by applying these assumptions.

1. Set $R_{Bn} = Z_{OUTn} + R_B$ = "R"
2. Replace V_{OUT1}, V_{OUT2},…, V_{OUTn} with noise source e_n
3. Set $V_{E1} = V_{E2} = \ldots = V_{En} = 0V$
4. Set $I_{LOAD} = 0$

Using these assumptions, rewrite equation 1 as equations 2 and 3.

$$e_{n,\ LOAD} = \frac{\sum_{n=1}^{n} \frac{e_n}{R}}{\sum_{n=1}^{n} \frac{1}{R}} = \frac{\sum_{n=1}^{n} e_n / R}{\frac{n}{R}} = \frac{\sum_{n=1}^{n} e_n}{n} = \sqrt{\sum_{n=1}^{n} \left(\frac{e_n}{n}\right)^2} \quad (2)$$

$$e_{n,\ LOAD} = \frac{e_n}{\sqrt{n}} \quad (3)$$

The output noise of the parallel LDOs is reduced by the square root of the number of LDOs in parallel. Fundamentally, these assumptions imply that all paralleled LDOs exhibit identical intrinsic noise (because the same LDO IC is used), operate at the same temperature, generate zero or negligible error-voltage, use the same ballast resistors with low tolerance (< 1%), and are closely matched in output impedance (Z_{OUT}).

3 LDO Output Impedance

Using the TPS7A57 as an example [2], the output impedance Z_{OUT} decreases with increasing load current (Figure 3-1). At very low frequencies, Z_{OUT} is dominated by the drain-source resistance (R_{DS}) of the internal pass MOSFET, the PCB trace impedance, and the internal bond wire impedance. In the mid-band region, the performance of the internal error amplifier becomes the dominant factor. At frequencies above the mid-band, the series impedance of the output capacitor, together with the PCB parasitics, dictates Z_{OUT}. To satisfy the condition that *R* falls out of equation 2, the output impedances of all parallel-connected LDOs must be identical.

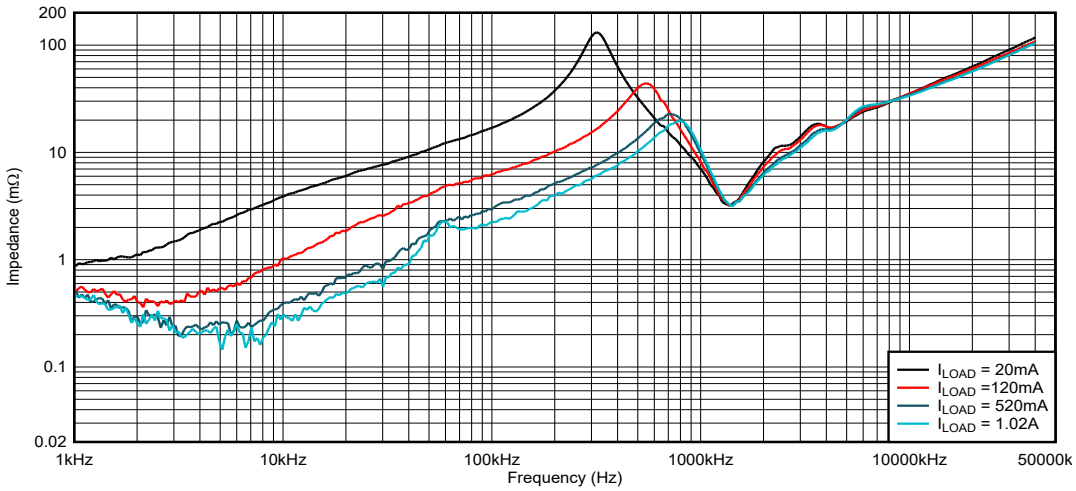

Figure 3-1. TPS7A57 Z_{OUT} Variation with Load Current

4 Strategies on Reducing the Noise of the Parallel LDO System

From sections 2 and 3, any variation between Z_{OUT} of the individual LDOs degrades the overall noise performance predicted by equation 3. The following design practices help equalize the effective resistance (“R”) seen at each output of the regulator in a parallel LDO architecture.

1. **Common input voltage** – Feed all regulators from the same input voltage source so that each device experiences the same junction temperature and input voltage.
2. **Matched output capacitors** – Use identical, tight-tolerance capacitors (both value and ESR) on every LDO to keep the capacitive component of Z_{OUT} consistent.
3. **Matched ballast resistors** – Select discrete ballast resistors with the same nominal value and low tolerance (≤ 1 %).
4. **Remote sensing** – Connect the remote-sense pin of the LDO directly to the V_{OUT} pad of the ballast resistor as a kelvin sense trace to eliminate lead-wire and trace resistance between V_{OUT} and R_B.
5. **PDN impedance matching** – Verify that the power-distribution network between each ballast resistor and the load, as well as the return path from the load to the RTN pin of the LDO, has matched impedance for every regulator.
6. **Common reference node** – Tie the reference pins of all LDOs together so that the pins share the same reference voltage.
7. **Prefer unity-gain architecture** – When possible, select an LDO that operates in unity-gain mode (no external feedback divider), eliminating one source of mismatch.
8. **Matched feedback network (if required)** – If the device does not support unity gain, use a feedback resistor network with identical, low-tolerance parts for each regulator to set the output voltage.

By applying these eight design practices, the output impedances of the parallel LDOs become closely matched, allowing the system to achieve the noise reduction indicated by equation 3.

5 Noise of Parallel LDOs Using Ballast Resistors

5.1 TPS7A57

Measurements were captured of parallel TPS7A57 LDOs using ballast resistors [3]. Each LDO in parallel has small variations in PCB impedance which affect the total ballast resistance between the LDOs [1]. This variation in ballast resistance causes each LDO to provide slightly different current to the load [1], causing the output impedance of each LDO to vary slightly from one another (see Figure 3-1).

To reduce the influence of the unequal PCB impedances, the ballast resistor value was increased from 2.5mΩ to 50mΩ. The resulting noise spectra are shown in Figure 5-1.

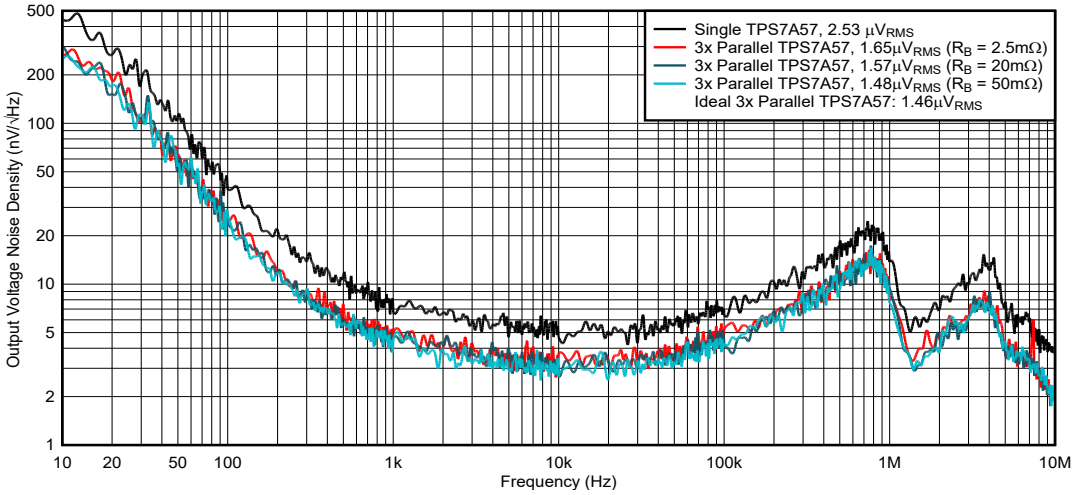

Figure 5-1. Noise Measurements of Parallel TPS7A57 LDOs

If noise is a critical parameter that must be absolutely minimized, a better approach than increasing R_B is to match the impedance of the PCB planes after each R_B of the LDOs. If a voltage drop across the ballast resistors is not critical (such as when configuring the parallel LDOs as a constant current source [4]), then a potential simpler approach is to use a large enough R_B (such as 50mΩ) to mitigate the effects of parasitic PCB impedance.

5.2 TPS7A94

The TPS7A94 LDO [5] currently provides an industry leading noise spectral density at just 0.46μV_{RMS} (10Hz–100kHz). While the TPS7A94 is rated for a 1A load current, the TPS7A96 is rated for a 2A load current [6]. Both of these LDOs are designed to be paralleled using ballast resistors. Paralleling these LDOs provide the lowest noise possible in linear regulator designs. Up to ten TPS7A94 LDOs are being paralleled in the industry to achieve ultra-low noise power rails. Noise analysis of parallel TPS7A94 LDOs (the conditions described in Section 2) is showcased in Figure 5-2.

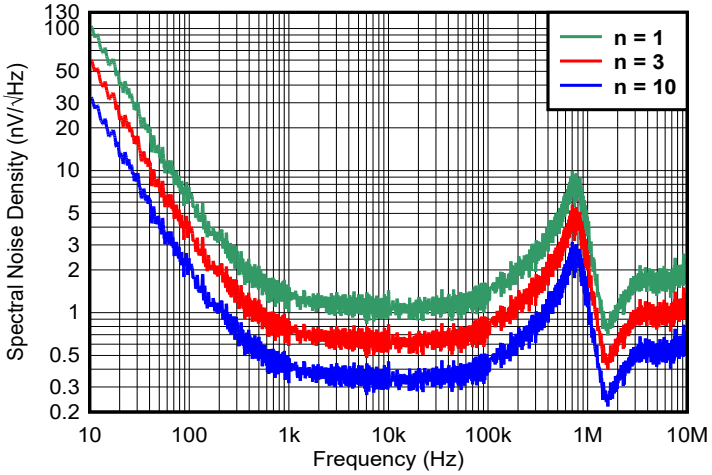

Figure 5-2. Parallel TPS7A94 Noise Performance

6 Noise Measurements of Alternative Parallel LDO Architectures

Other parallel LDO architectures configure one LDO as the primary and the remaining LDOs as the secondary. The primary LDO controls the secondary LDOs through an additional feedback loop. The LDOs do not operate independently from each other, unlike with the ballast resistor technique. For these architectures the preceding analysis is no longer valid and the system noise does not reduce by the √n. These external components can potentially result in an increase in noise, as the feedback loops are typically connected to the unfiltered feedback

pin. If the external components carry significant noise, then these components can potentially cause the parallel LDO system to become noisier as well.

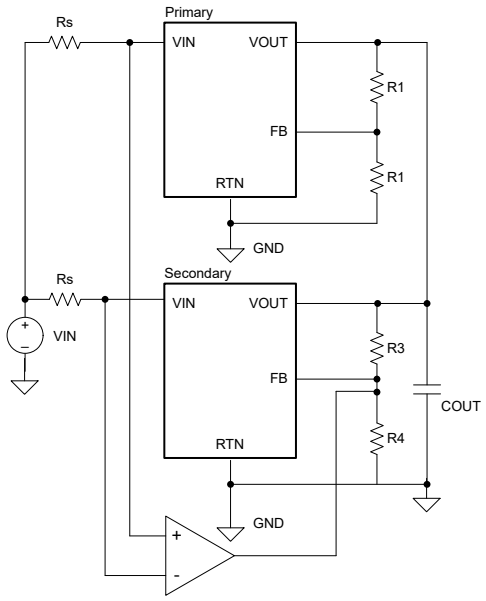

Figure 6-1. Parallel LDOs Using Op-Amps

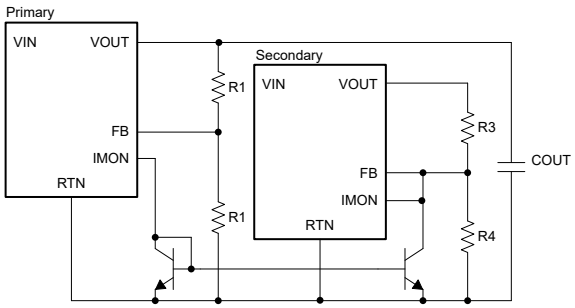

Figure 6-2. Parallel LDOs Using Current Mirrors

6.1 TPS7B7702-Q1

The TPS7B7702-Q1 [7] is a dual linear regulator with diagnostic features commonly used in standalone or in parallel applications. Ballast resistors can be used to parallel the TPS7B7702-Q1 (see Figure 6-1), and when using this architecture, the noise decreases with the √n (see Figure 6-2). See the reference design for test data covering the parallel operation using ballast resistors and op-amps [**10**]. Both channels inside the TPS7B7702-Q1 share the same V_{IN} pin, so a modified schematic to achieve similar paralleled LDOs is used in [**10**] (see Figure 6-3 below).

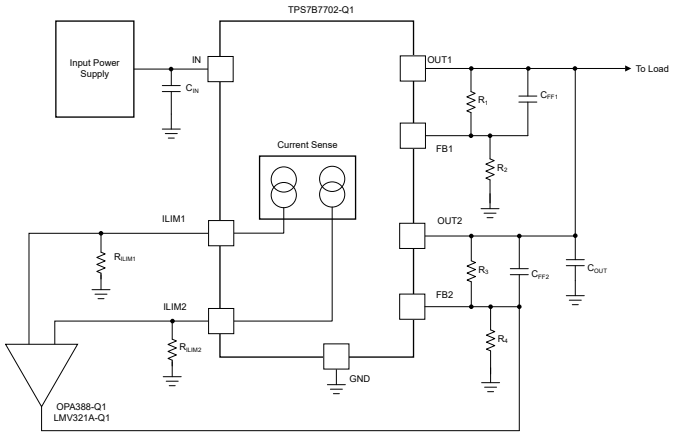

Figure 6-3. Parallel TPS7B7702-Q1 Using Op-Amps

The noise performance for three parallel LDO topologies was evaluated using the TPS7B7702-Q1 LDO:

1. **Op-amp-controlled architecture** – A single primary LDO channel drives up to three secondary LDO channels through external operational amplifiers.
2. **Current-mirror architecture** – Two TPS7B7702-Q1 channels are paralleled using a current-mirror network (see Figure 6-3).
3. **Ballast-resistor architecture** – Two TPS7B7702-Q1 channels are paralleled with discrete ballast resistors placed at each output of the regulator.

Noise was measured at the output of the parallel LDOs for each topology. The current-mirror and ballast-resistor configurations were tested with two parallel LDO channels; whereas, the op-amp-controlled architecture was evaluated with up to four parallel LDO channels (one primary, plus three secondaries).

All configurations produced output-noise levels equal to or higher than the noise of a single TPS7B7702-Q1, except for the ballast-resistor method. Only the ballast-resistor topology achieved a measurable reduction in noise, confirming the theoretical prediction presented earlier in this white paper (see Figure 6-4).

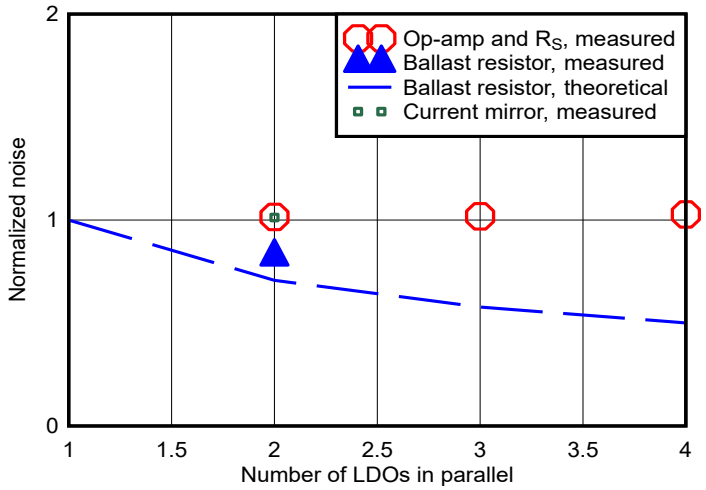

Figure 6-4. Only the Ballast Resistor Technique Offers Reduced System Noise

7 Conclusion

This document compares and contrasts the noise performance of three common parallel LDO techniques. For the first time, the technical foundation for noise reduction in parallel LDOs using ballast resistors is discussed while demonstrating that other techniques do not provide the same noise advantage. Designers can now architect the correct parallel LDO architectures to meet specific design requirements, including ultra low noise specifications, when no single LDO can meet the noise specification alone.

8 References

1. Texas Instruments, *Comprehensive Analysis and Universal Equations for Parallel LDOs Using Ballast Resistors*, white paper
2. Texas Instruments, *Parallel LDO Architecture Design Using Ballast Resistors*, white paper
3. Texas Instruments, Parallel Low-Dropout (LDO) Calculator, tool
4. Texas Instruments, *TPS7A57 5A, Low-VIN (0.7V), Low-Noise (2.1μV_{RMS}), High-Accuracy (1%), Ultra-Low Dropout (LDO) Voltage Regulator*, datasheet
5. Texas Instruments, *Scalable, High-Current, Low-Noise Parallel LDO Reference Design*, Design Guide
6. Texas Instruments, *Tips, Tricks and Advanced Applications of Linear Regulators*, Texas Instruments Power Supply Design Seminar SEM2600, 2024
7. Texas Instruments, *TPS7A94 1A, Ultra-Low Noise, Ultra-High PSRR, Low-Dropout Regulator*, datasheet
8. Texas Instruments, *TPS7A96 2A, Ultra-Low Noise, Ultra-High PSRR, RF Voltage Regulator*, datasheet
9. Texas Instruments, *TPS7B770x-Q1, Automotive, Single- and Dual-Channel Antenna LDO With Current Sense*, datasheet
10. Texas Instruments, *Scalable, high-current, parallel automotive reference design*, Design Guide

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