Enabling high voltage signal isolation quality and reliability

Texas Instruments

Tom Bonifield
Analog Technology Development
Texas Instruments

Circuit isolation, also known as galvanic isolation, prevents direct current (DC) and unwanted alternating current (AC) signals from passing from one area of a system to another area that needs to be protected.

Among its uses, isolation maintains signal integrity of the system by preventing high-frequency noise from propagating, protects sensitive circuitry from high-voltage surges and spikes, and provides safety for human operators. To ensure human safety, industrial standards require reinforced isolation — that is, twice the basic level of isolation needed for proper operation of the equipment.

Introduction

A newly developed manufacturing process from Texas Instruments (TI) provides reinforced signal isolation in a capacitive circuit that uses silicon-dioxide (SiO_2), the basic on-chip insulation, for a dielectric. The isolation circuit can thus be integrated on the same chip along with other circuitry. The process provides TI's second generation of capacitor-based integrated reinforced isolation technology for protective pass-through of high-voltage, high-frequency signaling. Products made with this process offer reliability, shock protection and reinforced isolation equivalent to two levels of basic isolation in a single package.

This technical brief discusses in detail TI's capacitor-based reinforced isolation for signaling. The brief offers extensive data from device characterization and testing to demonstrate that the process and related devices meet or exceed specifications for reinforced isolation and are, in fact, exceptional in their capabilities.

Achieving high voltage isolation

High voltage (HV) isolation is achieved using two thick SiO_2 capacitors in series – one on each side of the isolation barrier. SiO_2 is an excellent dielectric with the highest dielectric strength among materials commonly used for HV isolation components (**Table 1**). And, unlike polyimide and other polymer-based insulators, the reliability of an SiO_2-insulated capacitor does not degrade with exposure to ambient moisture.

Insulator Materials	Dielectric Strength
Air	~1 Vrms/µm
Epoxies	~20 Vrms/µm
Silica filled Mold Compounds	~100 Vrms/µm
Polyimide	~300 Vrms/µm
SiO_2	~500 Vrms/µm

***Table 1**. Common insulators used for HV isolation.*

The HV caps are manufactured in a high performance analog process and packaged in a multi-chip SOIC module. The wafer fab process is a multiple level metal process with the HV capacitor formed between metals as shown in **Figure 1**. This structure achieves the SiO_2 thickness needed for HV isolation simply by using standard interlevel dielectric layers. This multi-layered structure improves quality and reliability by reducing the dependence of the HV performance on any single layer.

Manufacturing of the HV caps uses the same processes and equipment that are used for high volume analog and CMOS production. The SiO_2 films are amorphous and homogeneous, and are deposited by plasma enhanced chemical vapor deposition. Each SiO_2 layer is planarized using chemical mechanical polishing. The final SiO_2 film thicknesses are measured and controlled during process. Using multiple layers reduces dielectric thickness variability for a well-controlled total capacitor dielectric thickness, which is verified by a wafer-level capacitance measurement prior to assembly.

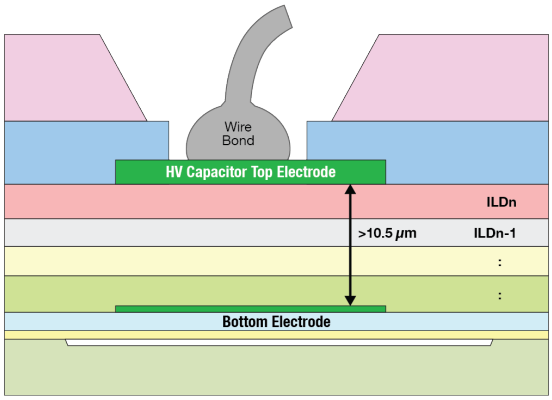

***Figure 1**. HV capacitor.*

A multi-chip module using this isolation capacitor technology is shown in **Figure 2**. Both the transmitter and receiver have isolation capacitors to double the high voltage capability compared to a single capacitor. A very thick multi-layer passivation layer protects the HV isolation die from possible breakdown in the mold compound surrounding the die.

Products using this configuration meet the industry standard requirements for reinforced isolation, including:

V_{IOTM} = 5.7 kVrms transient overvoltage

V_{IORM} = 2.0 kVrms 20 years reinforced iso working voltage

V_{IOSM} = 8 kV peak

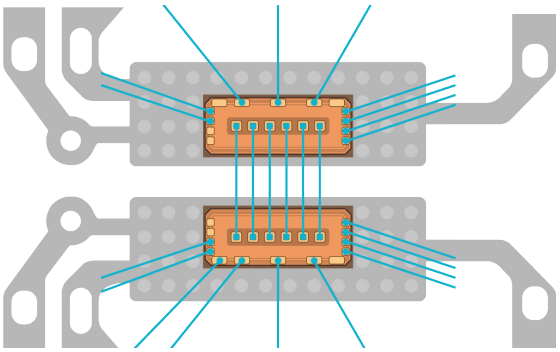

***Figure 2**. High voltage isolation multi-chip module with HV caps on transmitter and receiver connected in series.*

High voltage isolation testing

Multiple component-level as well as system- and end equipment-level standards govern and certify isolation products. Based on real world operating conditions, various voltage stress profiles are mandated for isolation products which quantify their HV isolation performance [Reference 1]. Some of these component-level parameters are working voltage (V_{IOWM}), maximum transient isolation voltage (V_{IOTM}), isolation withstand voltage (V_{ISO}), maximum repetitive peak voltage (V_{IORM}) and maximum surge isolation voltage (V_{IOSM}). These parameters and the tests used to verify these capabilities are listed in **Table 2**.

Parameter	HV Tests
V_{IOTM} , V_{ISO}	Method-B1 production screen, Ramp-to-Breakdown, Method-A, TDDB
V_{IORM} , V_{IOWM}	Method-B1 production screen, TDDB
V_{IOSM}	Surge, Surge breakpoint

***Table 2**. HV isolation tests.*

Routine high voltage production testing on every part follows Method-B1 as prescribed by IEC 60747-5-5. Method-B1 test conditions are shown in **Figure 3**. This test has two parts: an isolation test and a partial discharge test. The isolation test is a HV leakage test for 1 sec (t_{st1}) at a stress voltage $V_{ini,b}$ >/= 120% of V_{IOTM} or V_{ISO}. This part of the test screens out units with defective HV caps.

The second part of Method-B1 is a 1 second partial discharge test at "V_m" which is >/= 1.875x V_{IORM} for reinforced isolation. The partial discharge test screens out units with electrically active voids in the mold compound.

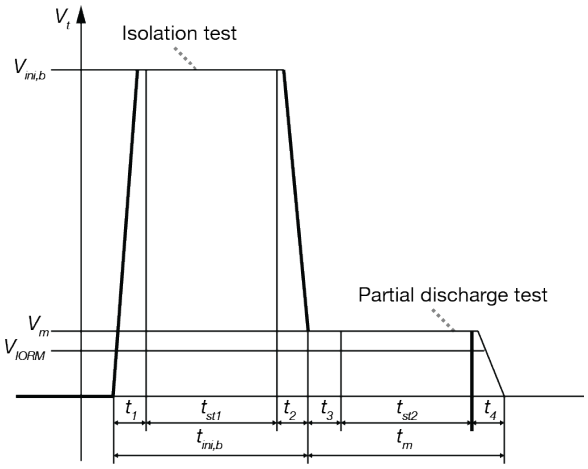

***Figure 3**. Method-B1 routine production test performed on all parts.*

RTB (Ramp-to-Breakdown) test is a destructive test performed on a sample basis as shown in **Figure 4**. These RTB data show a tight distribution of breakdown voltages with high margin to the Method-B1 leakage test at >/= 6.8 kVrms for 1 second.

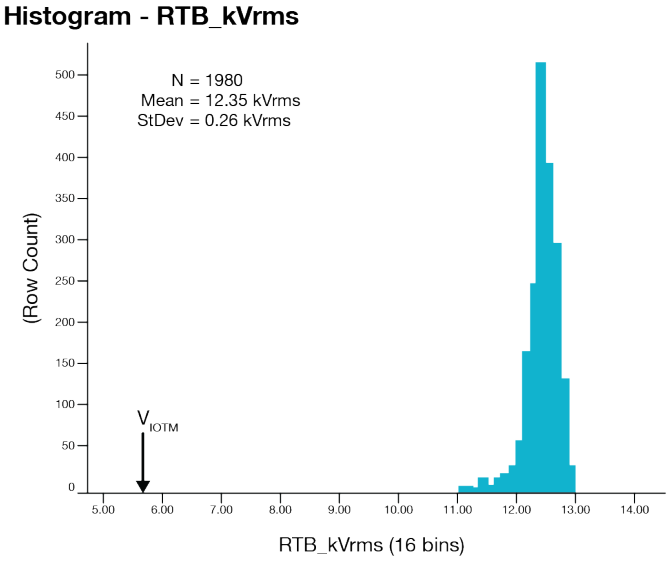

***Figure 4**. RTB voltage distribution, with1 kVrms/sec ramp rate.*

TDDB (Time Dependent Dielectric Breakdown) is the standard test method to verify the lifetime of any dielectric [References 2, 3, 4]. It is a key test of the high voltage isolation barrier. TDDB can be performed on final packaged product parts because the isolation insulator is directly accessible by testing between the two isolated voltage domains. TDDB is performed by stressing parts at a constant high AC or DC voltage for a long time until the insulator wears out and fails by electrical short. By testing TDDB at multiple voltages, the product lifetime at the working voltage is determined by extrapolation as shown in **Figure 5**.

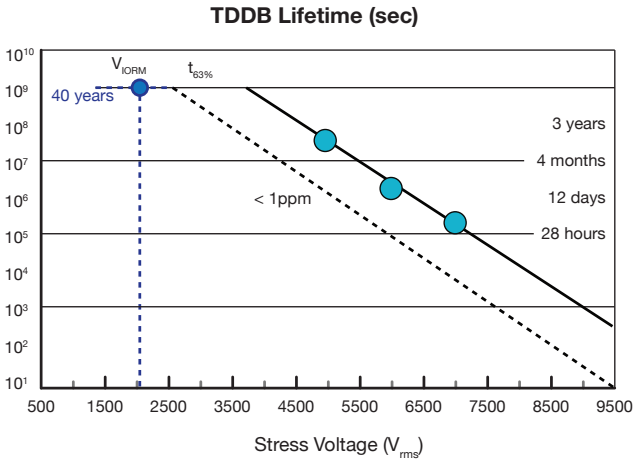

***Figure 5**. Time Dependent Dielectric Breakdown (TDDB). Circles are the time for 63% of units to break down. The dashed line represents 1ppm projections from the Weibull analyses.*

The breakdown times at each TDDB test voltage are analyzed by the Weibull method to determine an average fail time $t_{63\%}$ and extrapolation to 1 ppm failure probability. The TDDB breakdown times follow the commonly used model:

$$\text{Time-to-Fail} = A * \exp(-\gamma * E)$$

where γ is the field acceleration, E is the electric field, and A is the process and material dependent coefficient called the pre-factor.

Margins for establishing the lifetime of a reinforced isolation part using HV caps are covered in VDE884-11 spec. These include 20% margin in working voltage and 87.5% margin in lifetime; i.e., a 2 kVrms working

voltage with 20 year lifetime must demonstrate < 1ppm failure probability at 2.4 kVrms for 37.5 years. **Figure 5** demonstrates a good fit to the model and very high isolation barrier lifetimes for this technology at the maximum use condition or working voltage (V_{IORM}, V_{Iowm}) of 2.0 kVrms. TDDB testing is continuing at 4 kVrms with no fails after 23,000 hours so far.

Method-A test is prescribed by IEC to directly confirm V_{IOTM} on a sample basis. Method-A test includes a 60 sec leakage test at V_{IOTM}, which is 5.7 kVrms for this technology. TDDB is the best means to determine the quality of the actual distributions relative to the V_{IOTM} spec. **Figure 5** shows that the average time to breakdown at a TDDB voltage of 5.7 kVrms (V_{IOTM}) is 5 orders of magnitude higher than the 60 seconds required for Method-A testing.

Surge is an IEC sample test to check immunity to very high voltage, very short time events (such as lightning strikes). The surge pulse waveform is specified by IEC 61000-4-5, as shown in **Figure 6**. Reinforced isolation requires passing a surge test with a minimum of 50 pulses of 10 kV peak voltage.

Surge testing is performed periodically on production samples to verify they meet the requirement for reinforced isolation.

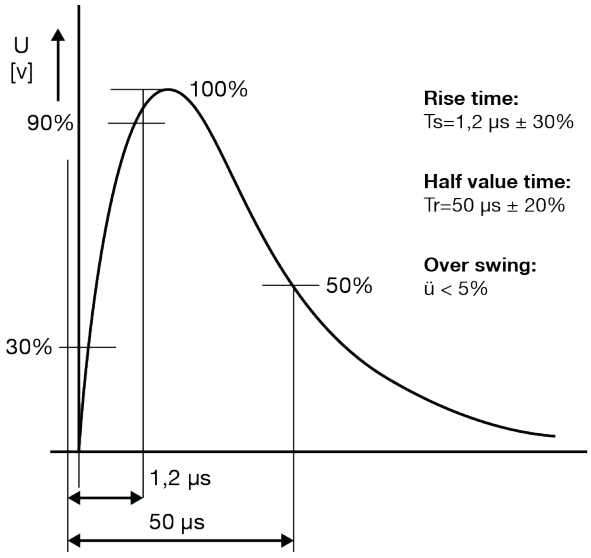

***Figure 6**. Surge test waveform.*

To assess the actual surge capability, the surge fail rate is measured as a function of the surge peak voltage. Many units are tested at each voltage. Two different surge test methods are assessed: "unipolar" where all pulses are of the same polarity, and "bipolar" where half of the pulses are one polarity and the other half are the opposite polarity. The actual surge breakpoint distributions are shown in **Figure 7**.

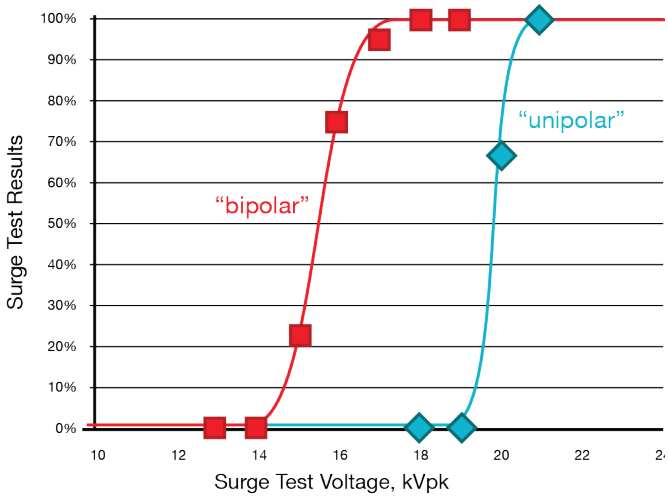

***Figure 7**. Surge breakpoint statistical assessment, by both "unipolar" and "bipolar" surge test methods .*

Both "unipolar" and "bipolar" surge breakpoints exceed the 10 kV surge requirement for reinforced isolation. The lower surge breakpoints for "bipolar" surge are a temporary hysteresis effect. The "unipolar" surge distribution is representative of single surge events.

Conclusion

TI's isolation family of products has high voltage capability that exceeds the requirements for reinforced isolation. The quality of HV isolation is demonstrated by substantial margins using statistical test methods. The reliability of the HV isolation process technology is proven to have high isolation margin by TDDB, which is the industry standard method of proving lifetime at use conditions.

For more information:

- View TI's isolation offerings
- Read the related white paper: Fully integrated signal and power isolation: Applications and benefits

References

[1] High-voltage reinforced isolation: Definitions and test methodologies: http://www.ti.com/lit/wp/slyy063/slyy063.pdf.

[2] J. W. McPherson, "Time dependent dielectric breakdown physics – Models revisited," in Microelectronics Reliability 52, 2012, p. 1753–1760.

[3] I. C. Chen, E. Holland, and C. A. Hu, "A quantitative physical model for time-dependent breakdown in SiO_2," in Proc. Int. Reliab. Phys. Symp., 1985, p. 24.

[4] J. W. McPherson, V. Reddy, K. Banerjee, and L. Huy, "Comparison of E and 1/E TDDB models for SiO_2 under long-term/low-field test conditions," in IEDM Tech. Dig., 1998, p. 171.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265