Technical Article

How to design a high-voltage DCM inverting charge pump converter

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A low-current, negative high-voltage is required to bias sensors in advanced driver assistance systems, ultrasonic transducers for sonar applications, and communications equipment. Flyback, Cuk, and inverting buck-boost converters are all possible solutions, but are penalized by bulky transformers (flyback and Cuk) or limited in their maximum negative voltage by the controller's input-voltage rating (inverting buck-boost). In this power tip, I'll detail the operation of a converter that pairs a single inductor with an inverting charge pump operating in discontinuous conduction mode (DCM). Paired with a ground referenced boost controller, a large negative output voltage can be generated at a lower system cost.

Figure 1 shows a simplified power-stage schematic. Note that this schematic is different from a traditional inverting buck-boost converter, which "floats" the controller between V_{IN} and $-V_{OUT}$. In that converter, the maximum $-V_{OUT}$ achievable is the maximum V_{CC} of the controller **minus** the maximum input voltage. This would make it nearly impossible to find a controller that can drive an N-channel field-effect transistor (FET) for an output voltage of −100V or more.

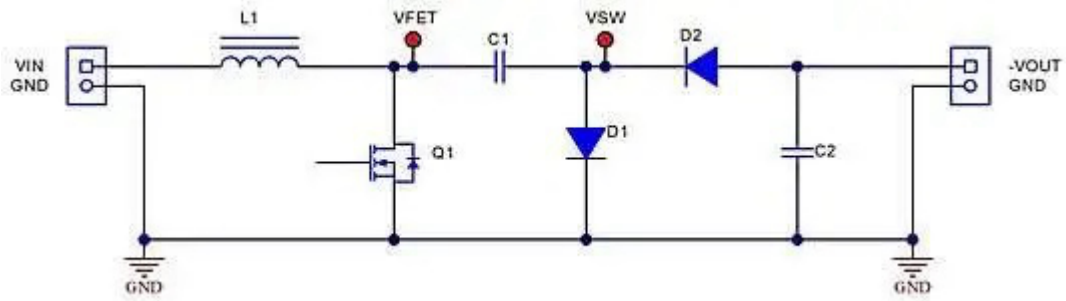

Figure 1. Simplified power stage of an inductor-driven inverting charge pump

The circuit's operation can be split into three intervals (Figure 2). In the first interval, the FET is on during duty cycle (d), which applies V_{IN} across the inductor, allowing current to ramp up from zero, storing energy. However, in the previous cycle, C1 (which maintains a voltage of approximately equal to V_{OUT}) has depleted its excess stored energy, reverse-biasing D1 and D2. This is why D1, D2, and C1 are not shown in this interval. C2 supplies all load current.

In the next interval, d', the FET turns off and the inductor current begins to discharge, causing its voltage polarity to reverse. This greatly increases the voltage present at node VFET, allowing C1 to recharge through D1. During this interval, current ramps downward until D1 turns off. However, due to the reverse-recovery characteristics of D1, current goes negative before it eventually turns off, at which point the inductor current slope changes and its voltage polarity reverses once again.

The third interval, d'', is when the energy transfer from C1 to C2 takes place. When D1 stops conducting, the inductor voltage is clamped to V_{IN} because the VFET node voltage is forced to ground by a current path through the FET's body diode. Current flows through D2 until the voltages across C1 and C2 equalize, but current through the FET's body diode continues until the inductor's current reaches zero. At this point, the voltage across the inductor collapses and resonates with circuit parasitics until the FET turns on again.

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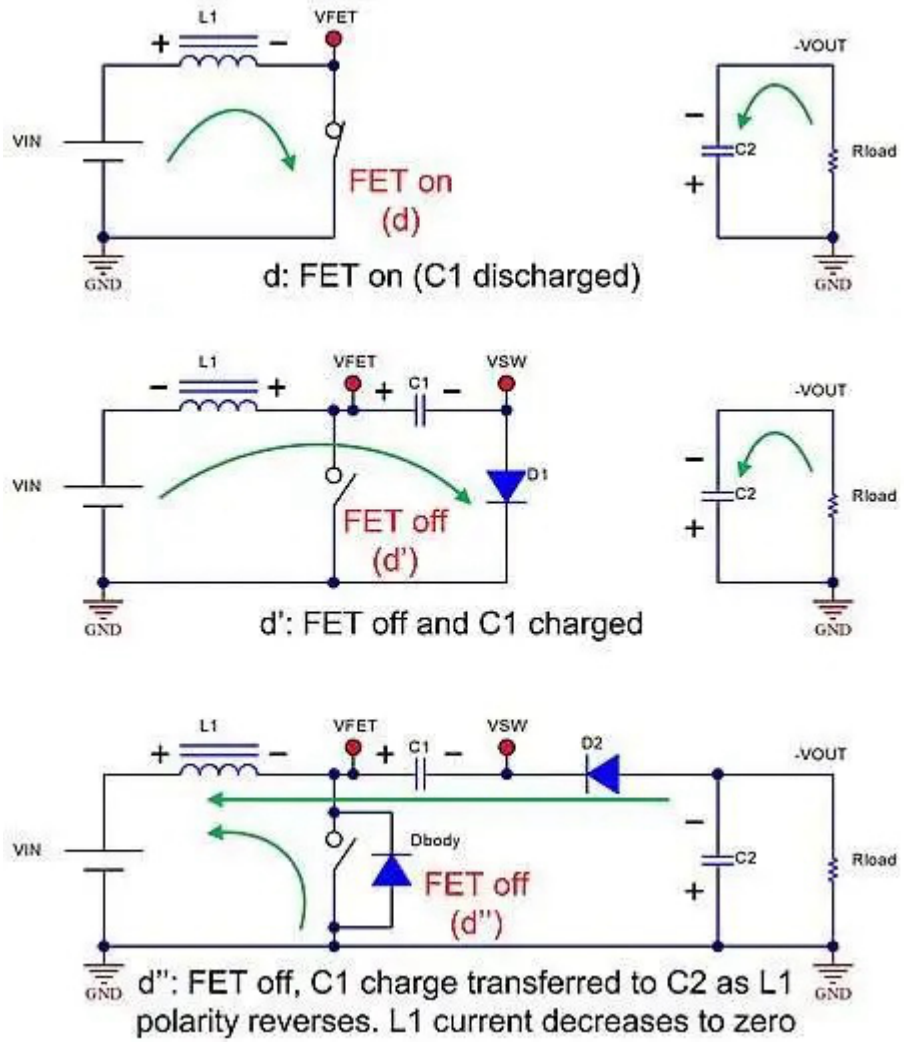

Figure 2. The three phases of DCM operation

Figure 3 details the key voltage and current waveforms. DCM operation allows for the smallest possible inductance, but with a higher peak current. Inductance for DCM operation is determined at the maximum duty cycle, minimum V_{IN} and full load. Carefully check the maximum duty cycle against the controller data sheet, but you can typically choose 60%-90%, or otherwise pulse skipping can occur. Larger inductances will push operation into continuous conduction mode (CCM), since the current will not return to zero before the next switching cycle. This results in using an inductor that may be larger than necessary and requires extra care to prevent subharmonic oscillation.

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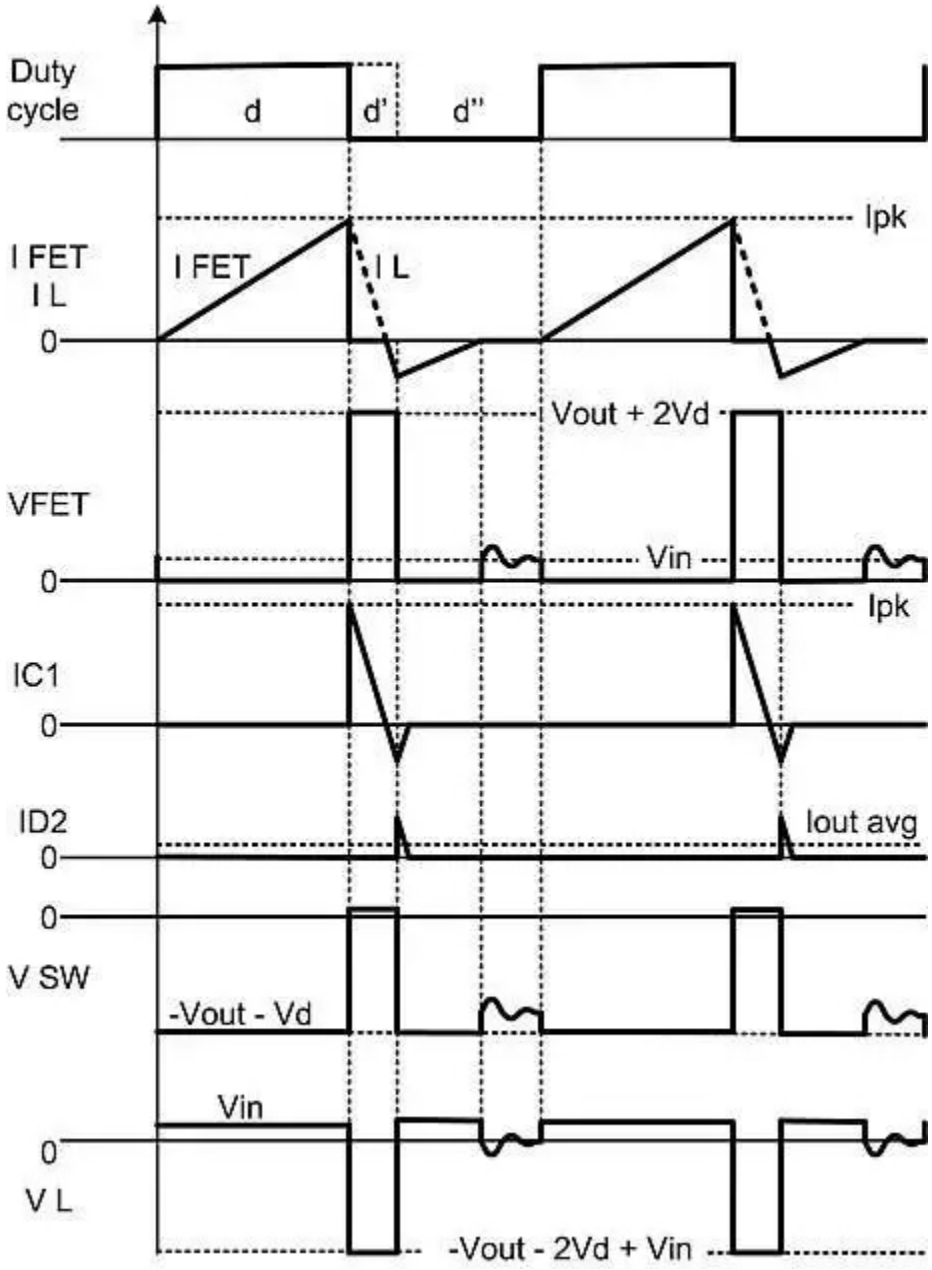

Figure 3. Key circuit waveforms in DCM

Design equations

For DCM operation, Equation 1 satisfies the relationship involving the inductor's stored energy:

$$\frac{1}{2} * L * i_{pk}^{2} * f_{sw} = \frac{\text{Vout}^{2}}{\text{Rload} * \eta} \quad (1)$$

where i_{pk} is the peak inductor current and η is the converter's efficiency. The peak inductor current is then equal to Equation 2:

$$i_{pk} = \sqrt{\frac{2 * \text{Vout}^{2}}{\text{Rload} * L * f_{sw} * \eta}} \quad (2)$$

From the following two equations, Equation 3 expresses the duty cycle (d) in terms of:

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$$V_L = L\frac{di}{dt} \text{and } d = dt * f_{sw}, \quad \text{then}, d = \frac{di * L * f_{sw}}{V_L} \tag{3}$$

Since V_{IN} is the voltage across the inductor when the FET is on and i_{pk} is the inductor current at the end of duty cycle d, substituting Equation 2 into Equation 3 yields Equations 4 and 5:

$$d = \frac{\text{Vout}}{\text{Vin}}\sqrt{\frac{2 * L * f_{\text{sw}}}{\text{Rload} * \eta}} \tag{4}$$

$$\text{or}, L = \frac{\text{Vin}^{\,2} * d^2 * \text{Rload} * \eta}{2 * \text{Vout}^{\,2} * f_{sw}} \tag{5}$$

The average load current is determined by the geometric relationship in Equations 6 and 7 during interval d':

$$\frac{\text{Vout}}{\text{Rload}} = \frac{l_{pk} + dr}{2} \tag{6}$$

$$\text{or}, d' = \frac{2 * \text{Vout}}{i_p * * \text{Rload}} \tag{7}$$

Substituting Equation 2 into Equation 7 provides Equation 8:

$$d' = \sqrt{\frac{2 + L \cdot f_{\text{sw}} \cdot \eta}{\text{Rload}}} \tag{8}$$

The remainder of the period is defined as d'', which is when the energy transfers into C2 and the remaining inductor current discharges to zero (Equation 9):

$$d'' = 1 - \text{d} - \text{d}' = 1 - \frac{\text{Vout}}{\text{Vin}}\sqrt{\frac{2 * L * f_{sw}}{\text{Rload} * \eta}} - \sqrt{\frac{2 * L * f_{sw} * \eta}{\text{Rload}}} \tag{9}$$

Figure 4 shows an example schematic implementing this converter with a voltage doubler, which allows the voltage stress of each power-stage component to be equal to one-half of the full output voltage. This provides a wider selection of components from which to choose. In this application, the inductance was calculated as if the output voltage was one-half, but at twice the load current.

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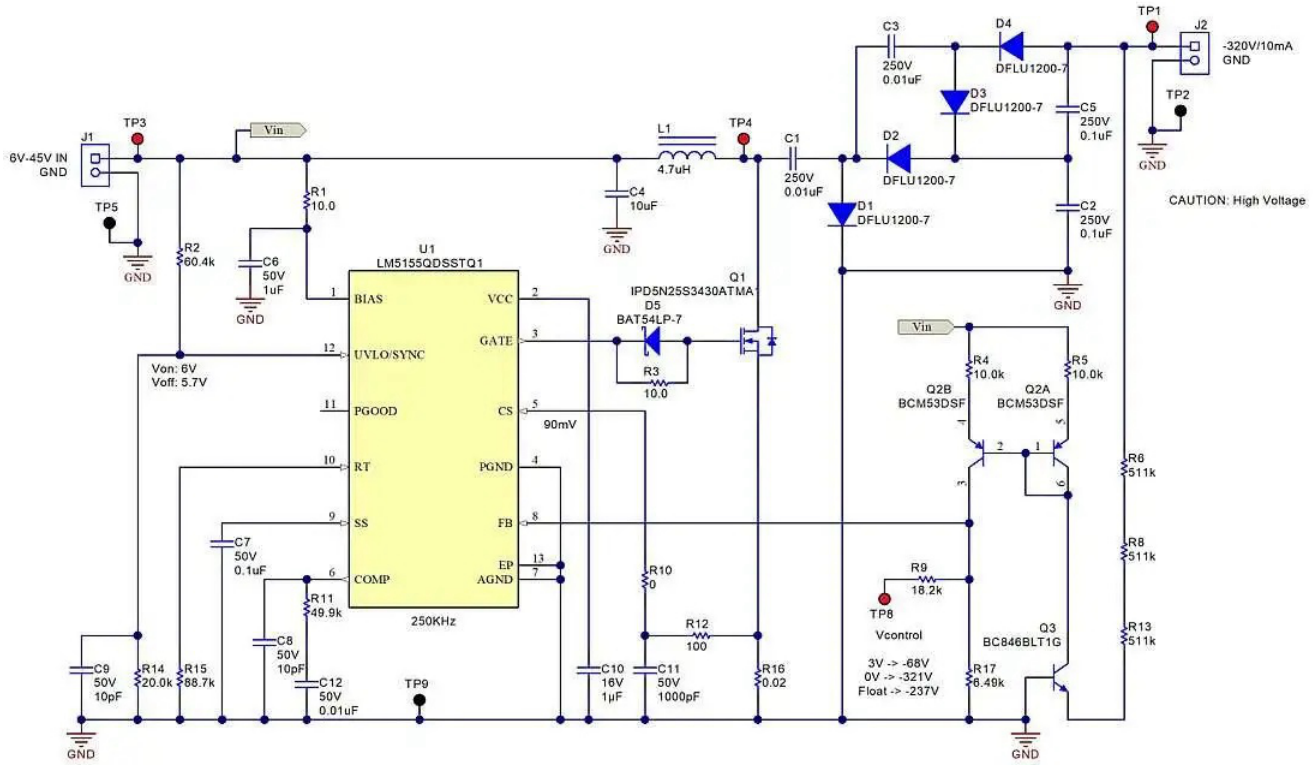

Figure 4. Inductor-driven inverting charge pump with voltage doubler and level-shifting current mirror schematic

This converter provides a small, single-inductor solution for generating a large negative voltage. Additionally, it allows the use of an inexpensive ground-referenced boost controller to drive an N-channel FET.

For more Power Tips, check out TI's Power Tips blog series on Power House.

Additional resources

- Power Tips: Increase your output voltage with a voltage multiplier, EETimes
- Using the TPS5430 as an Inverting Buck Boost Converter (Rev. A), TI Application Report

Related articles

- Charge-pump topology doubles voltage, breaks DC path
- Modded charge pump extracts power from digital signal
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