Technical Article

CLLLC vs. DAB for EV onboard chargers

Brent McDonald

In order to optimize power in electric vehicles (EVs), the onboard charger (OBC) must be highly efficient, light in weight, and small in size. A lighter EV also requires less power to move the vehicle, which increases overall efficiency.

The OBC needs to support an appropriate grid-to-vehicle (G2V) voltage and current battery-charging algorithm; as such, it functions as the power-conditioning interface between the power grid and the EV (Figure 1). In addition, it must be able to provide power from the vehicle-to-grid (V2G) so that the EV can supplement renewable energy sources that might have a fluctuating peak capacity.

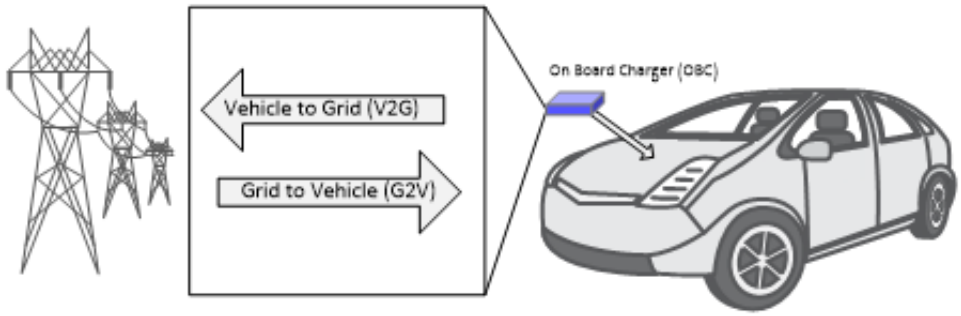

Figure 1. The OBC needs to support an appropriate G2V voltage and provide power from the V2G.

Facilitating the interface between the power grid and the high-voltage battery inside the EV requires an electromagnetic interference (EMI) filter, power factor correction (PFC) and an isolated DC/DC power stage. Figure 2 illustrates this architecture.

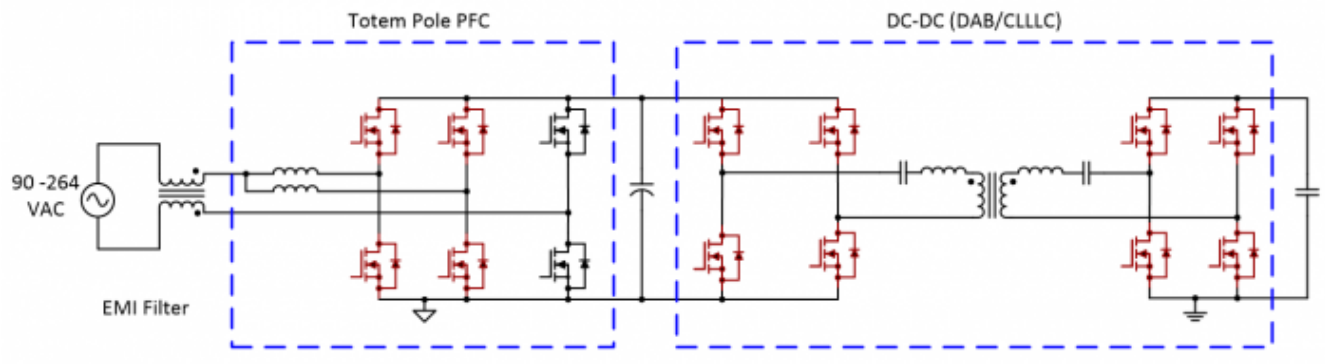

Figure 2. This simplified schematic shows how the OBC serves as the interface between the power grid and the battery.

The scope of this discussion is limited to the DC/DC stage. As of this writing, two popular choices for the DC/DC stage are the capacitor-inductor-inductor-inductor-capacitor (CLLLC) and the dual-active-bridge (DAB) topologies (figures 3 and 4). Both options can achieve a small solution size and provide the necessary G2V and V2G power demands.

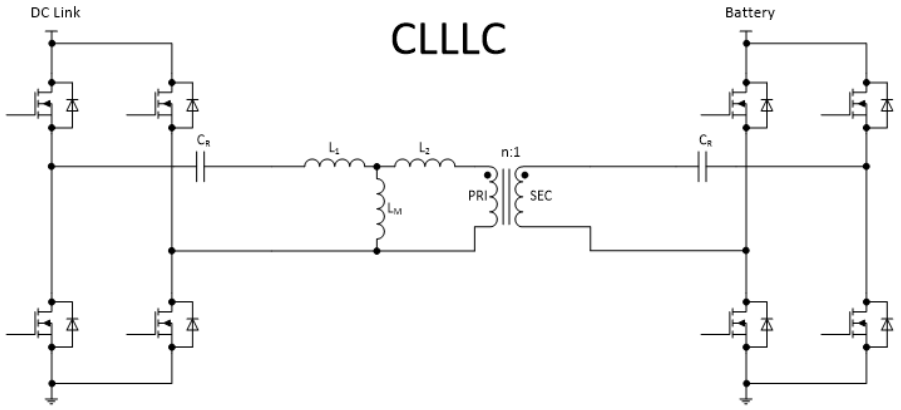

Figure 3. This schematic shows the basic topology of the CLLLC.

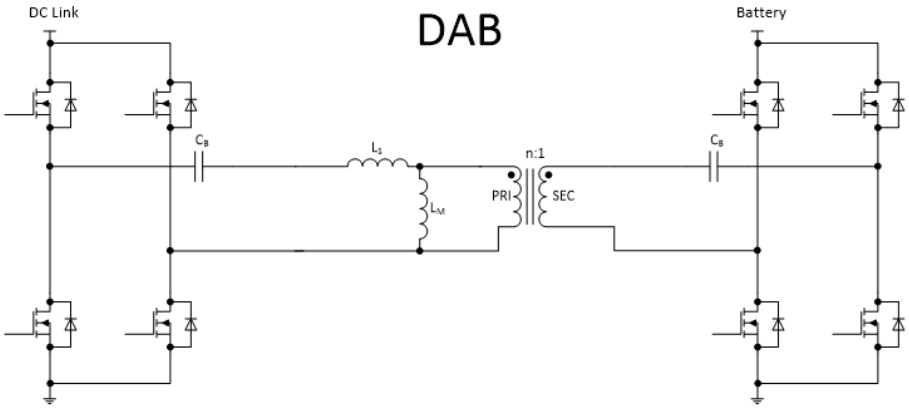

Figure 4. The DAB topology is shown in this schematic.

Maximize OBC performance and minimize its size

To understand how these two topology options can affect the size and performance of the OBC, let's further limit the scope to the battery-charging phase of operation, or G2V, considering how to minimize the charging time by providing the maximum battery power that the switches can tolerate. For example, consider a switch under the following operating conditions:

- P_{DISS} = 20 W
- ϑ_{JA} = 3°C/W
- T_A = 65°C

The switch will have a T_J = 125°C, according to Equation 1:

$$T_J = P_{DISS} \cdot \vartheta_{JA} + T_A \quad (1)$$

The switches in this design cannot tolerate a temperature above 125°C; therefore, this condition represents the highest power level that the OBC can provide to the battery without compromising the switch. The goal is to minimize the power dissipation in the switch and charge the battery as quickly as possible.

Two main factors drive the majority of power losses in the switches: root-mean-square (RMS) current and the switch's ability to maintain zero-voltage-switching (ZVS).

Given their low capacitance and fast turn on and turn off characteristics, Texas Instruments' GaN switches enable the converter to operate at a higher switching frequency than what would be possible with silicon. Higher-frequency operation directly affects the size of the reactive components and results in a smaller transformer, inductors, and capacitors. Let's start by establishing a baseline design for both the DAB and CLLLC, and then explore a circuit enhancement to extend the ZVS range of the converters.

Baseline DAB and CLLLC performance comparisons

Table 1 outlines the basic requirements for the OBC.

Table 1. OBC power requirements.

Description	Min	Typ	Max	Units
AC input voltage	90	220	264	V_{RMS}
AC input current			32	A_{RMS}
DC output voltage	250	400	450	V
DC output current (constant current mode)			20	A
DC output power (constant power mode): >210-V RMS input			6.6	kW

Creating a detailed design for both the DAB and CLLLC helps determine the most viable tank designs. The procedures for doing this are beyond the scope of this discussion; however, circuit simulation is best for adequately approximating the losses in the switches and verifying compliance with the overall functionality. I configured the simulator to run in batch mode over different power levels and input and output voltages and tested different DAB and CLLLC inductor, capacitor, and turns-ratio values. In each simulation run, I collected data on parameters such as VIN, VOUT, switch power, RMS current and switch ZVS conditions. Table 2 summarizes the two optimized topology designs.

Table 2. DAB and CLLLC optimized designs.

Topology	DAB	CLLLC
Tank	N_P/N_S = 1.1 L = 3.3 µH L_M = 20 µH	N_P/N_S = 1.1 $L_{R,1}$ = 2 µH $L_{R,2}$ = 2 µH L_M = 14 µH $C_{R,1}$ = 50 nF $C_{R,2}$ = 50 nF
Control	Triple phase-shift modulation	Frequency and phase-shift modulation
Variable DC link	400 V to 450 V	400 V to 450 V
f_s	500 kHz	300 kHz-800 kHz

Figure 5 illustrates the salient simulation results. While there are eight switches in each topology, the graphs plot only the switch with the highest power loss. For each switch, there are three plots. The first is the total losses in the switch. The second is the RMS current through that switch. The third plot, on the far right, shows the worst-case drain-to-source voltage that a given GaN switch experiences at turn on. This is a figure of merit of how much ZVS has been lost; the higher this voltage, the larger the losses will be in that switch. Thus, the switch's RMS current coupled with its ability to maintain ZVS represents the greatest portion of power losses in the device.

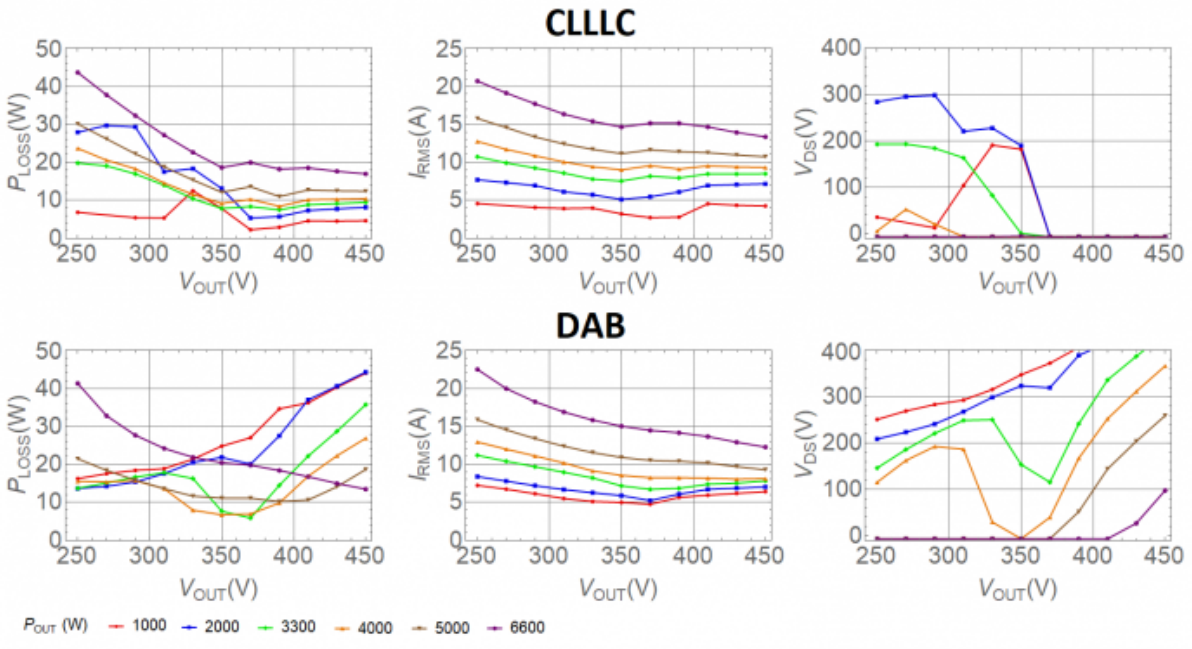

Figure 5. The simulation results show RMS and ZVS baseline conditions for both CLLLC and DAB.

Equipped with these facts and a careful examination of the data, it's clear that the CLLLC is able to maintain ZVS over a wider range of operation. Enhanced ZVS is therefore responsible for the lower power losses seen in the CLLLC switches. Having said that, at 6.6 kW of operation, the DAB has superior performance, which comes from good ZVS and reduced RMS current over most of the range. These observations suggest looking for a way to improve ZVS without adversely impacting the RMS current.

Improving ZVS with commutation inductors

Figure 6 and Figure 7 show the same CLLLC and DAB circuits as figures 3 and 4 with extra inductors (highlighted in yellow) added to the topologies to provide the additional current required to maintain ZVS over a wider range of operation. For now, consider a case when these extra inductors are operational all the time.

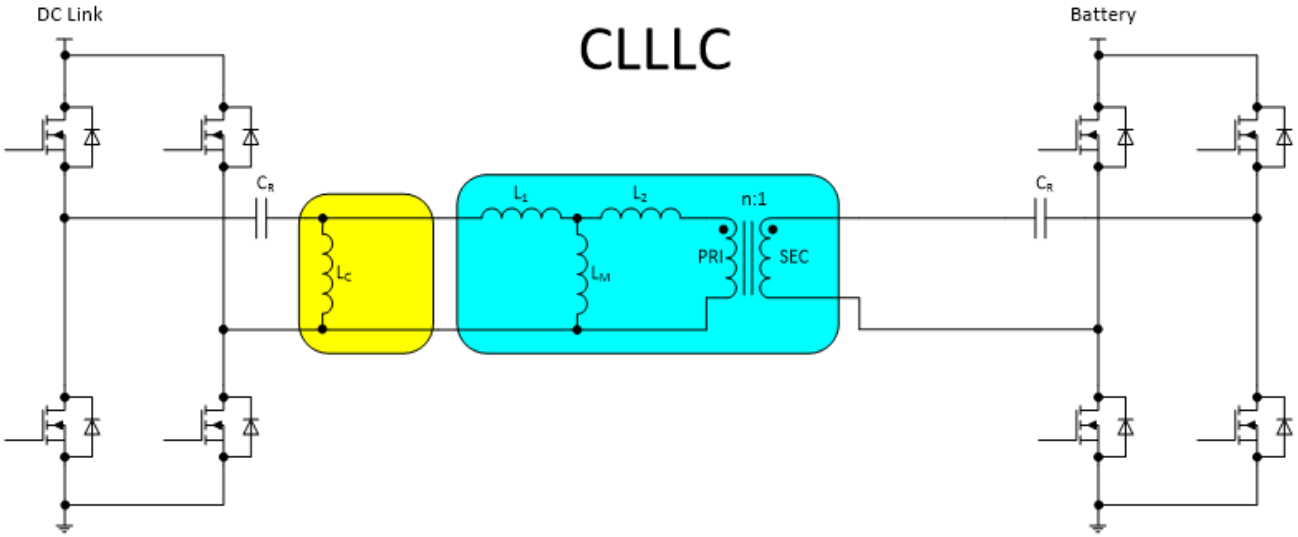

Figure 6. This schematic shows the CLLLC with a commutation inductor.

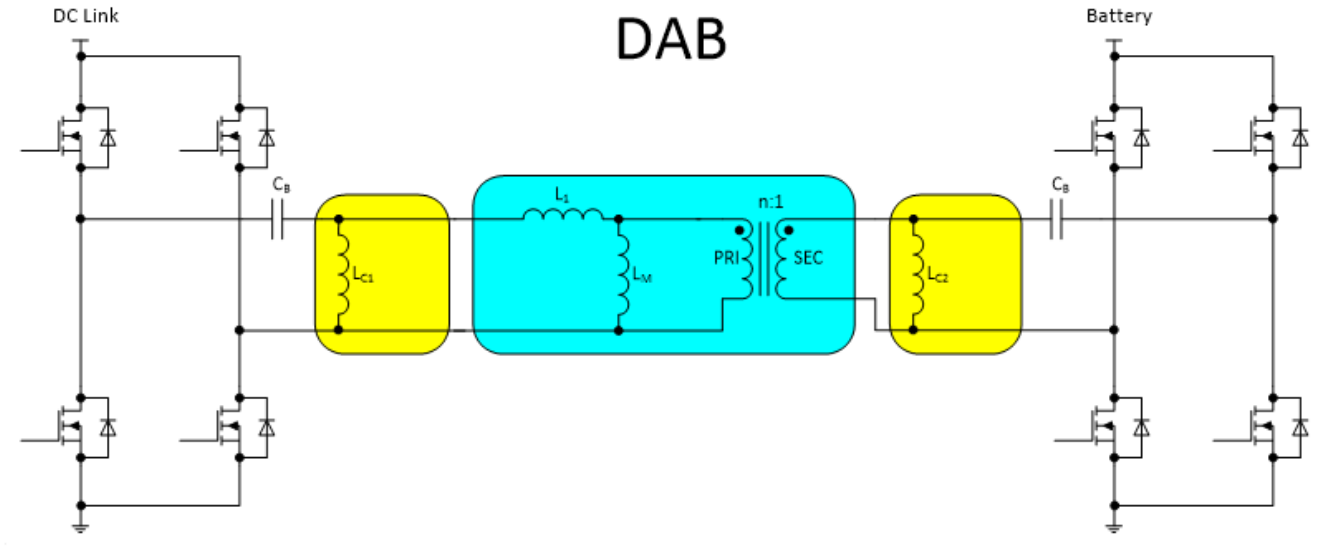

Figure 7. This schematic shows the DAB with commutation inductors.

Table 3 lists the values for the new inductors, and repeats the other tank parameters for convenience.

Table 3. DAB and CLLLC designs with commutation inductor (L_C) values

Topology	DAB	CLLLC
Tank	N_P/N_S = 1.1 L = 3.3 µH L_M = 20 µH **L_C = 20 µH**	N_P/N_S = 1.1 $L_{R,1}$ = 2 µH $L_{R,2}$ = 2 µH L_M = 14 µH $C_{R,1}$ = 50 nF $C_{R,2}$ = 50 nF **L_C = 50 µH**

Figure 8 shows the results after repeating the simulations in Figure 5.

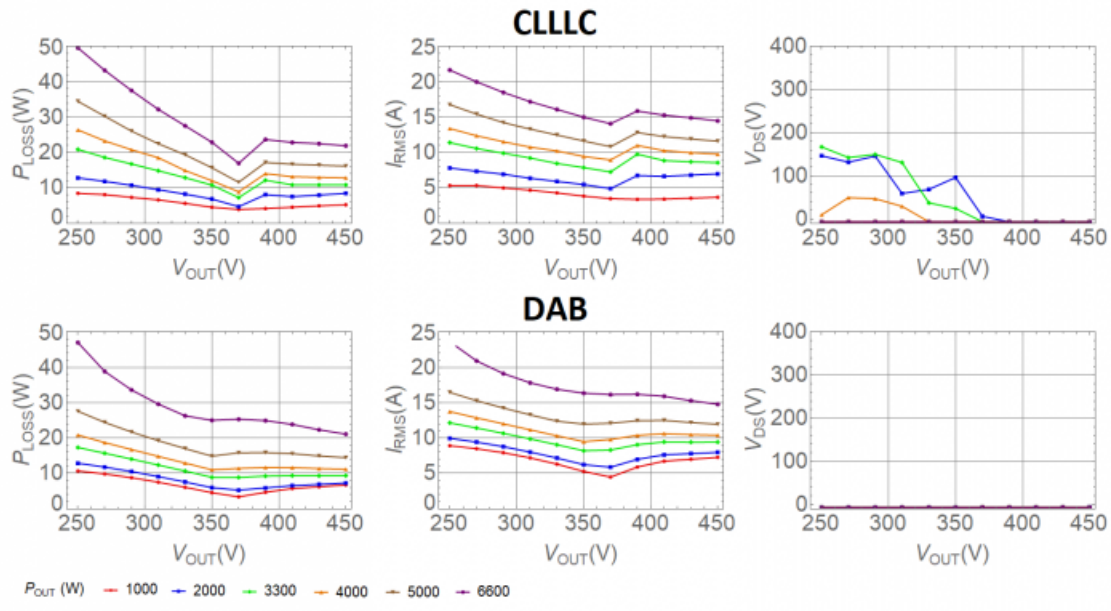

Figure 8. The RMS and ZVS results for each circuit show the impact of L_C.

In this case, notice that the DAB is able to achieve full ZVS over the entire range of operating conditions. This is clearly illustrated by the fact that the V_{DS} of the GaN switch is always at 0V at turn on. The CLLLC, while not achieving full ZVS, is able to achieve significantly improved ZVS. Also notice, however, that the ZVS improvement comes at a significant expense to the RMS currents in both topologies. Looking at the power losses alone, it appears that the DAB converter has the advantage over most of the range.

Before going too far, go back and compare Figure 8 to Figure 5, and you'll notice that under some conditions the commutation inductor actually makes the losses worse. This begs the question – is it possible to create a hybrid approach where you can achieve the lowest of the losses shown in Figure 5 and Figure 8?

Minimizing total losses: have your cake and eat it too

The addition of a commutation inductor creates a broader range of operating conditions where the converter maintains ZVS. This is of tremendous benefit when the converter can't maintain ZVS. The problem with a commutation inductor is that it only improves the losses when ZVS would otherwise be lost. If the converter is already in ZVS, the commutation inductor hurts operation by increasing the current, which results in more ohmic loss in the switches.

This thought process leads to the testing of a hybrid approach where the commutation inductors are left off at the heavier loads and turned on at lighter loads. Figure 9 shows the results after repeating the simulations with this approach, which enables the design to harness each topology's lower RMS currents and natural ZVS ability at heavy loads.

I was careful to add only enough commutation inductance and operation time to fit within the thermal envelope of the switches, in order to prevent unneeded RMS current to the switches or an unnecessary solution size. Note that the DAB converter does not achieve full ZVS over the operating range. The ZVS conditions are much improved, but only as much as they are needed to stay within in the 20-W switch target previously discussed.

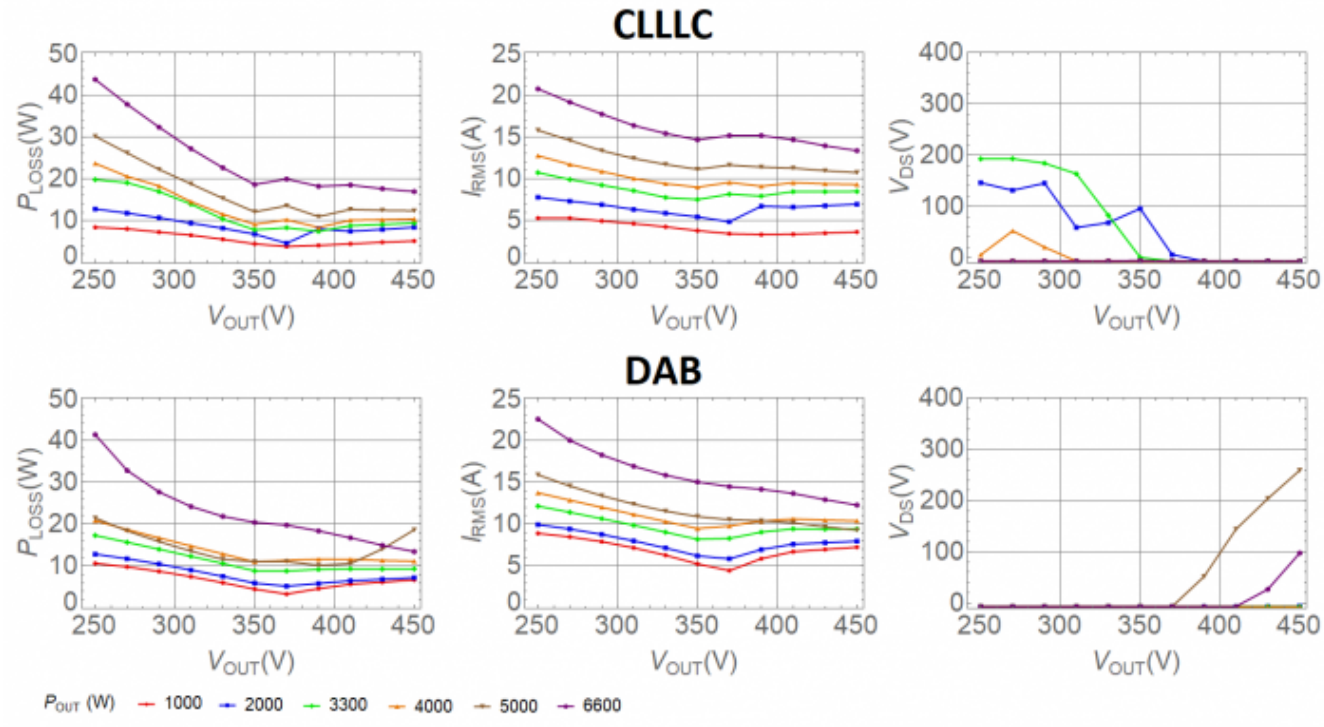

Figure 9. These are RMS and ZVS results using a hybrid approach.

In order to better visualize the trade-offs, Figure 10 summarizes the power losses for each case. You can see that the DAB converter has a clear advantage in terms of power losses in the switch.

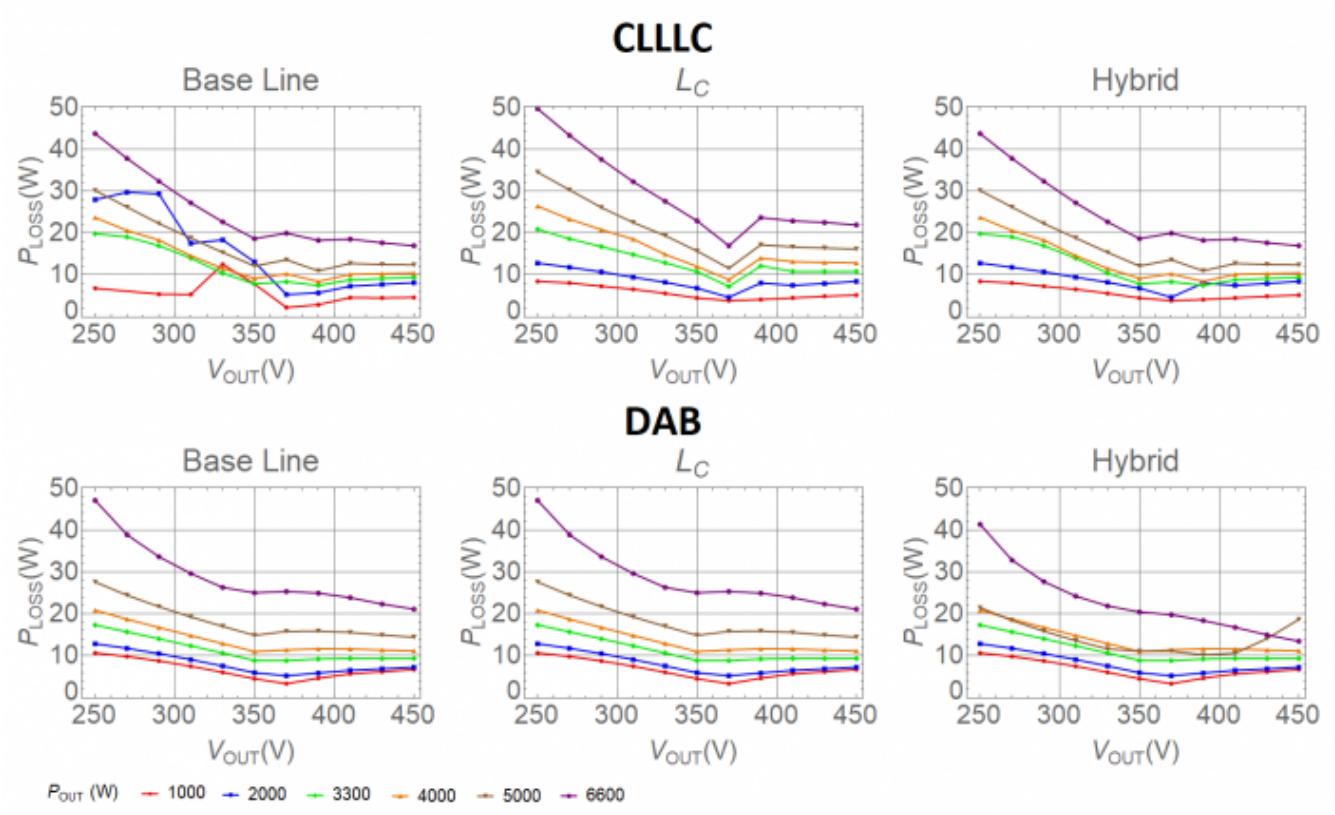

Figure 10. This summary of the power losses for each case helps visualize the trade-offs.

To better illustrate the performance capabilities between these two converters, Figure 11 reformats and plots the data shown in Figure 10. The graph shows the maximum power that each converter can supply, assuming that the switch cannot safely dissipate more than 20 W of power. Remember, 20 W represents the largest loss the switch can tolerate and still keep the junction temperature below 125°C.

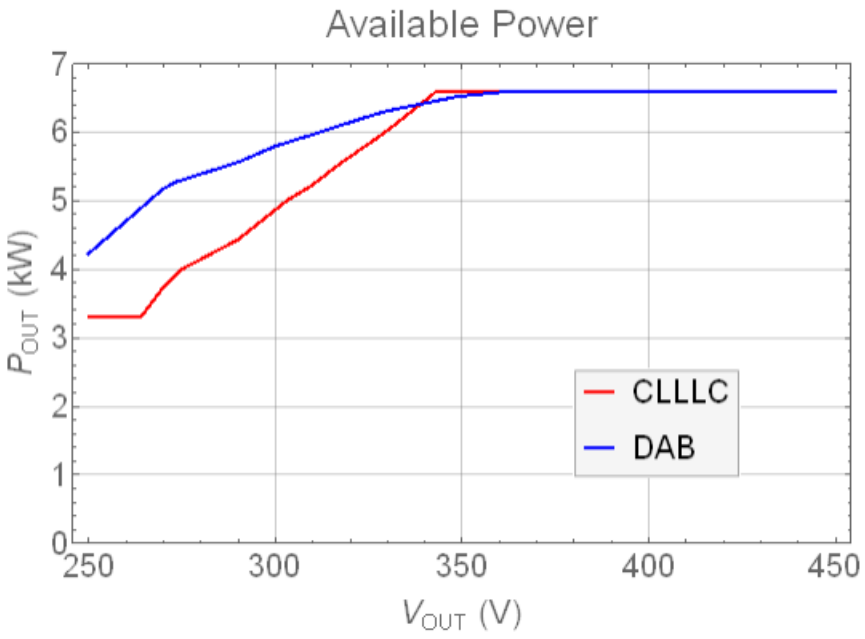

Figure 11. This plot shows the maximum power that each converter can supply.

Is CLLLC or DAB better?

As evidenced by the fact that the blue line is above the red in Figure 11, the DAB converter can provide more power over the entire range than the CLLLC. This makes it tempting to assume that the DAB is the clear winner. However, remember that minimal size and weight are central requirements of an OBC. The DAB converter needs two extra inductors, but the CLLLC only needs one. In my opinion, that gives the win to the CLLLC.

Like most things in engineering, what's best is almost always a matter of trade-offs against the requirements. It's pretty rare that big advantages come for free, and in this case it's no different. To me, the CLLLC edges out the DAB because it appears to have a clear size advantage.

References

1. de Oliveira, E.F., and P. Zacharias, "Comprehensive Mode Analysis and Optimal Design Methodology of a Bidirectional CLLC Resonant Converter for E-Vehicles Applications," 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Sept. 3-5, 2019, pp. 1-10.
2. Krismer, F., and J.W. Kolar, "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," IEEE Transactions on Industrial Electronics 59, no. 7 (July 2012): pp. 2745-2760.
3. Texas Instruments. n.d., "Gallium nitride (GaN): pushing performance beyond silicon," Accessed Oct. 19, 2020.

Related articles

- Electric vehicle charging: How technology and smart engineering will make our electric future possible
- Power transfer for wireless charging in electric vehicles
- GaN enables efficient, cost-effective 800V EV traction inverters
- Portable charging solutions offer roadside assistance for EVs
- Power Tips #75: USB Power Delivery for automotive systems
- Power Tips #92: High-frequency resonant converter design considerations

Previously published on EDN.com.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265