Technical Article

Differential Pairs: What You Really Need to Know

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The demand for speed is ever increasing, and transmission rates are doubling every few years. This trend is seen in many modern communications systems such as PCIe in computing, SAS and SATA in storage, and Gigabit Ethernet in cloud computing. This information revolution presents huge challenges in delivering data through transmission media, which continue to rely on copper wires and serial bit-stream transfers with a symbol rate >25Gbps and a throughput rate >100Gbps in a data link.

These serial data transmission designs use differential signaling to deliver data through a pair of copper wires called a differential pair. The complementary signals in the A-wire and B-wire are high-speed pulses of equal amplitude but opposite in phase. Many circuit technologies are used in differential signaling: low-voltage differential signaling (LVDS), current mode logic (CML) and positive emitter-current logic (PECL) are a few examples.

Delivering a Perfect Serial Bit-stream

The serial bit-stream is a pair of differential signals propagated through a differential pair. As shown in Figure 1, the differential signals are expected to arrive at the same time so that they retain the properties of a differential signal (with equal amplitude, opposite in phase) at the receiving end. A receiver is used to restore the signal fidelity, then sample and recover the data correctly, achieving error-free data transfer.

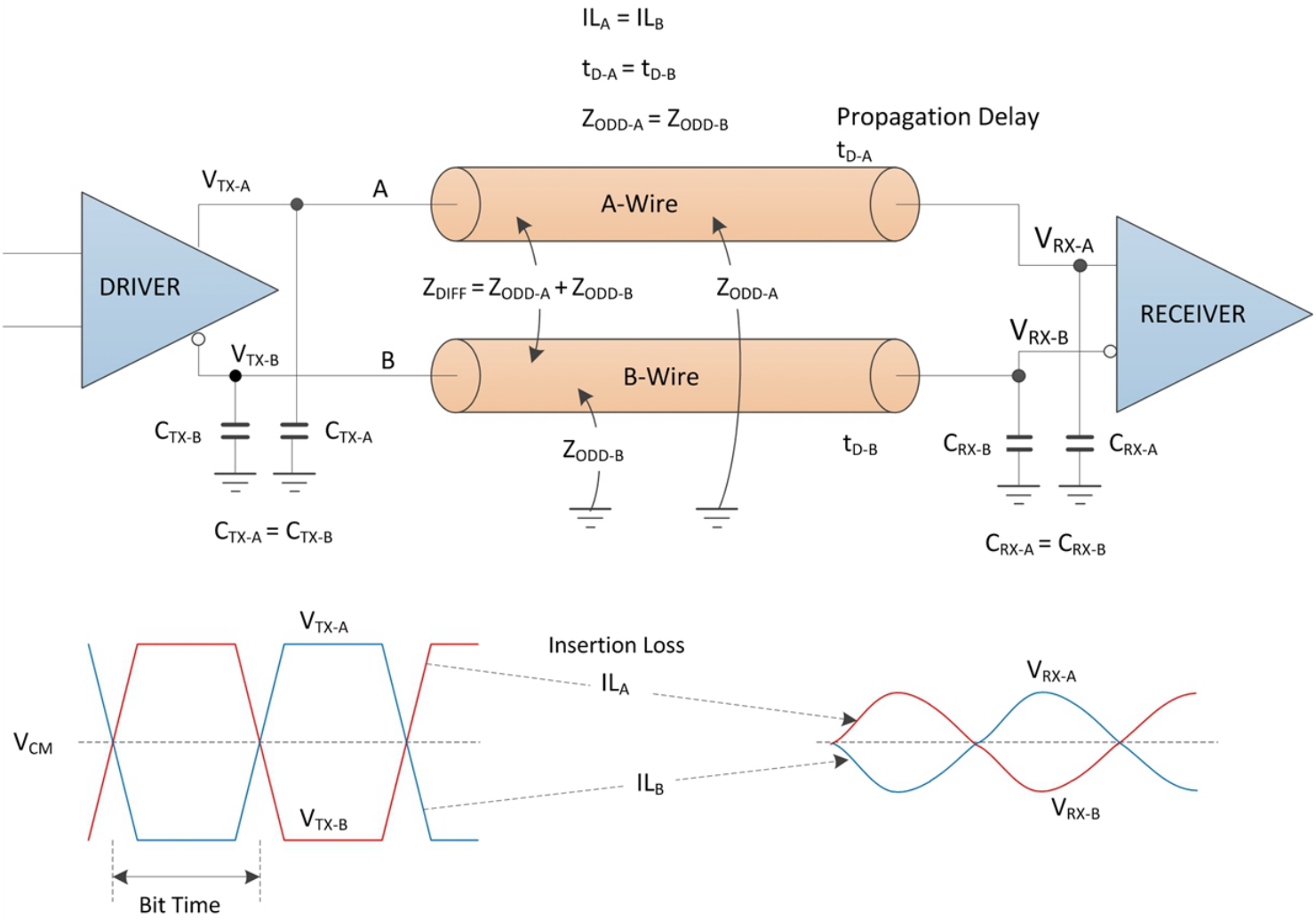

Figure 1. Electrical Properties for a Perfect Differential Pair

Requirements for a Differential Pair

Implementing a well-designed differential pair is a key factor in successful data transmissions at high speeds. Depending on the application, the differential pair can be a pair of printed circuit board (PCB) traces, a pair of twisted-pair copper wires or a pair of parallel wires sharing a dielectric and shielding (usually called twin-axial cable). In this series, I'll discuss the characteristics of differential pairs, as well as the design challenges and solutions for high-speed data transmission.

For this first installment, let's examine the main requirements for a differential pair:

- Both the A-wire and B-wire need to maintain fairly constant and equal characteristic impedance, commonly called odd-mode impedance, when both wires are excited differentially.
- The differential signals should arrive at the destination while preserving the differential signal's properties: approximately equal amplitude and opposite in phase.
  - The insertion loss of each wire should be approximately equal.
  - The propagation delay of each wire should be approximately equal.

In summary, we are looking for equal and fairly constant odd-mode impedance, minimizing the impedance fluctuation along the length of the differential pair from its source to destination. We are looking for delay matching and insertion loss matching between the A- and B-wires. In addition, we need to make sure the insertion loss is not excessive so that the receiver can recover the data correctly.

To satisfy the above requirements, the A- and B-wires should maintain a high degree of symmetry in their physical layout. The transmitter and receiver should also be highly symmetric in their A- and B-wire circuitry so that they present equal electrical loadings to the A- and B-wires.

Designing Differential Pairs to Minimize Distortion

In an ideal world, differential pairs are perfectly symmetrical, have unlimited bandwidth and offer complete isolation from adjacent signals. In the real world, differential signals propagate through integrated circuit (IC) packages, external components, different PCB structures, connectors and cabling subsystems. Implementing a perfectly symmetrical differential pair is a big challenge. In future posts, I'll discuss differential pair design trade-offs and mitigation techniques to minimize distortions to transmitted signals.

Texas Instruments has a rich portfolio of high-speed signal-conditioning ICs, such as retimers and redrivers. They ease the challenge in mitigating imperfections and high insertion loss from all styles of differential pairs, enabling reliable data communication and extending transmission distance for modern systems.

Find out more about TI's LVDS/MLVDS/ECL/CML and signal-conditioning redrivers and retimers. I hope you'll read the rest of my series on differential pairs.

Additional Resources

- Read more about differential signaling with the LVDS owner's manual.
- Check out TI's 40GbE/10GbE QSFP+ signal conditioner reference design.
- Learn about TI's PCIe Gen-3 cards with DS80PCI810 linear redriver reference design.
- Read about TI's WEBENCH® Interface Designer

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